# Le79238

## Octal Subscriber Line Audio-Processing Circuit
## Next Generation Carrier Chipset (NGCC)
Data Sheet

Document ID#: 081193 Version 17 June 2012

## Applications

- Cost-effective voice solution for long or short loops providing POTS, IVD and integrated test capabilities:
  - IVD, DLC, CO
  - Voice-enabled DSLAM
  - PBX/KTS
  - MDU, MSAP, MSAN

## Features

- Optimized for Next Generation Broadband xDSL and triple play applications
- Eliminates CO transients that could cause CRC errors
- Best-in-class testing, GR-844 equivalent with Next Generation VoiceEdge™ Control Processor (NGVCP)
- Wideband 16 kHz sampling mode capability (on product code F and later revisions)
- Ideal for high density, medium and large line count applications
- API-compatible with VE790 Series designs
- High performance digital signal processor provides programmable control of all major line card functions
  - A-law/µ-law and linear codec/filter
  - Transmit and receive gain, Two-wire AC impedance, Transhybrid balance, Equalization
  - DC loop feeding
  - Loop supervision
  - Internal ringing generation and ring-trip detection
  - Metering generation and shaping (12 kHz and 16 kHz)
- Enhanced line control and line-test support
  - DTMF and Modem Tone Detection
  - GR-909 plus extensive line and self test capabilities
  - Tone generation (DTMF, FSK, and arbitrary tone)

### Ordering Information

| | | | |
|---|---|---|---|
| Le792388TVC | 176-Pin LQFP (Green)[1] | Tray[3] |
| Le792388VQC | 164-Pin LGA (Green)[1] | Tray[3] |
| ZL792388GDG | 196-Pin BGA (RoHS-5)[2] | Tray |
| ZL792388GDF | 196-Pin BGA (RoHS-5)[2] | Tape and Reel |
| ZL792388GDG2 | 196-Pin BGA (Green)[1] | Tray |
| ZL792388GDF2 | 196-Pin BGA (Green)[1] | Tape and Reel |

1. *The green package meets RoHS Directive 2002/95/EC of the European Council to minimize the environmental impact of electrical equipment.*
2. *The RoHS-5 package is compliant with the requirements of the European Union's Restriction on Use of Hazardous Substances ("RoHS") Directive, 2002/95/EC, with the following Exemption: Lead (Pb) in the solder terminations used in the product.*
3. *For a tape and reel packing system, add a "T" suffix.*

- Standard PCM and MPI digital interfaces
- General purpose I/O pins, can be used as relay drivers

## Features with Le79124 NGVCP

- 72 channel call aggregation
- GR-844 equivalent line testing

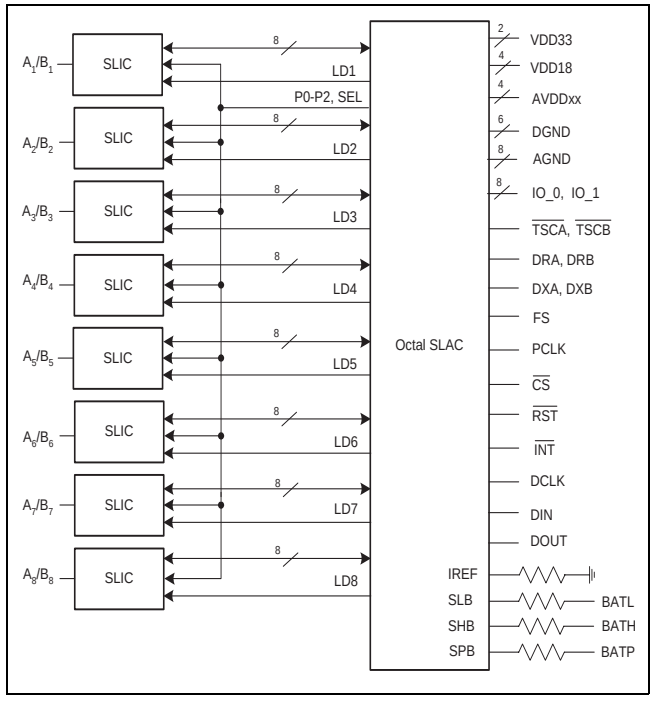


**Figure 1 - Block Diagram**

## Related Literature

- 126583 NGCC Hardware Design Guide
- 128623 NGCC Designer's Guide
- 081555 Le79271 NGSLIC Device Data Sheet
- 138884 Le79272 Dual NGSLIC Device Data Sheet
- 136868 ZL79258 External Ringing NGSLAC Device Data Sheet
- 081567 Le79124 NGVCP Device Data Sheet
- 133514 Le79234 NGVCP Device Data Sheet
- 127671 Le79124-SW NGVCP Software Package
- 133545 Le79234-SW NGVCP Software Package
- 135486 LE71SK7920-SW Ve792 Software Package
- 127063 VoicePath™ Profile Wizard User's Guide
- VoicePath™ API-II Reference Guide

## Description

The Le79238 Next Generation Octal Subscriber Line Audio-processing Circuit (SLAC), in combination with the Le79271 SLIC, implements a DSL friendly, high density 8-channel universal telephone line interface with wideband capability. This enables the design of a low cost, high performance, fully software programmable line interface with worldwide applicability. All AC, DC, and signaling parameters are programmable via a microprocessor interface. The Le79238 has an integrated test tool box which can be used standalone or with an NGVCP to resolve faults to the line or line circuit.

## Change Summary

Below are the changes from the March 2012 version to June 2012 version.

| Page | Section | Description |
|---|---|---|
| 8, 9 | 1.0 | Enhanced product description. |
| 26 | 7.1, No. 11 & No. 12 | Reduced power dissipation values. Test and use condition values provided. |
| 27 | 7.2, No. 4 | Expanded idle channel noise test description. |

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## 1.0 Product Description

The Next Generation Carrier Chipset integrates all the functions of eight voice subscriber lines. Eight Le79271 SLIC devices and one Le79238 Octal SLAC device make up the chipset.

- The Le79271 SLIC device is a high voltage, bipolar IC that drives the subscriber line and senses line conditions.
- The Le79238 SLAC device is a low voltage CMOS IC that provides conversion and DSP functions for eight channels and senses line conditions.

The SLIC device is built with a high voltage bipolar technology to provide the power necessary to drive a wide variety of subscriber lines. It can be programmed by the SLAC device to operate in eight different modes that control power consumption and signaling. The SLIC design is based on a voltage feed, current sense architecture.

The SLAC device processes information regarding line voltage and loop current from the SLIC device. The SLIC device senses the A and B lead currents, computes the metallic loop current and feeds it in analog form to the SLAC device. The SLAC device also senses A and B lead voltages and monitors battery voltage levels.

- The output signals supplied by the SLAC device to the SLIC device are:
- A lead (DCA) and B lead (DCB) DC voltages for DC feed or internal ringing.
- AC transmission and 12 or 16 kHz metering signals (on the RCVN, RCVP pins).

The SLAC device controls the SLIC device mode via the SLIC control bus P0-P2, SEL and the load signal LD.

- The SLAC device contains high-performance circuits that provide A/D and D/A conversion for voice (codec/filter), DC-feed control, ringing, and supervision signals. The SLAC device contains a DSP core that handles signaling, DC-feed, supervision and line diagnostics for all eight channels. The DSP core also interfaces to a standard PCM/MPI backplane. These functions involve converting an analog voice signal into digital PCM samples and converting digital PCM samples back into an analog signal. During conversion, digital filters are used to band-limit the voice signals. The PCM codes can be:
- 8-bit companded A-law with 8 kHz sampling
- 8-bit companded µ-law with 8 kHz sampling
- 16-bit linear two's-complement with 8 kHz sampling
- 16-bit linear two's-complement with 16 kHz sampling (wideband mode)

The SLAC device provides a complete software configurable solution to the BORSCHT functions as well as complete programmable control over subscriber line DC-feed characteristics, such as current limit and feed resistance. In addition, the SLAC device provides extensive loop supervision capability including off-hook, ring-trip and ground-key detection. Detection thresholds for these functions are programmable. A programmable debounce timer is available that eliminates false detection due to contact bounce.

User-programmable filters include receive and transmit gain and bandwidth, transhybrid balance, two-wire termination impedance, and frequency attenuation (equalization) of the receive and transmit signals. All programmable digital filter coefficients can be calculated using WinSLAC™ software. This PC software allows the designer to enter a description of system requirements, WinSLAC™ then computes the necessary coefficients and plots the predicted system results.

The main functions that can be observed and/or controlled through the SLAC device backplane interface are:

- Narrowband 3.4 kHz or wideband 7.0 kHz codec modes
- DC-feed characteristics
- Ground-key detection
- Off-hook detection
- DTMF tone detection
- Modem tone detection
- Metering signal
- DC voltages on A and B leads
- Subscriber line voltage and currents
- Ring-trip detection
- Abrupt and smooth reversal
- Subscriber line impedance matching
- Ringing signal generation
- Sophisticated line and circuit tests

These functions are all handled in a manner to limit voice service transients. Minimizing disturbances caused by the CO line circuit helps to eliminate cyclic redundancy check (CRC) errors in IVD systems.

For subscriber line diagnostics, AC and DC line conditions can be monitored using built in test tools. DTMF and modem tone detection functions are also built-in. Measured parameters can be compared to programmed threshold levels to set a pass/fail bit. Both longitudinal and metallic resistance and capacitance can be measured, which allows leakage resistance, line capacitance, and telephones to be identified.

The Le79124 Next Generation Voice Control Processor (VCP) provides integrated test software routines to perform comprehensive line diagnostics. Self-test and line-test capabilities can resolve faults to the line or line circuit. In addition, the VCP device provides aggregated codec/filter and call control.

The SLAC device requires two power supplies. Low power consumption is achieved by use of a separate +1.8 VDC supply for the DSP core and the DSP Core Power Reduction firmware algorithm. The analog and digital I/O circuitry is powered from a +3.3 VDC supply.

Figure 2 presents an overview of the NGCC system. Refer to the *Next Generation Carrier Chipset Hardware Design Guide (Document ID 126583)* for detailed Application Circuits and Parts Lists for various applications.

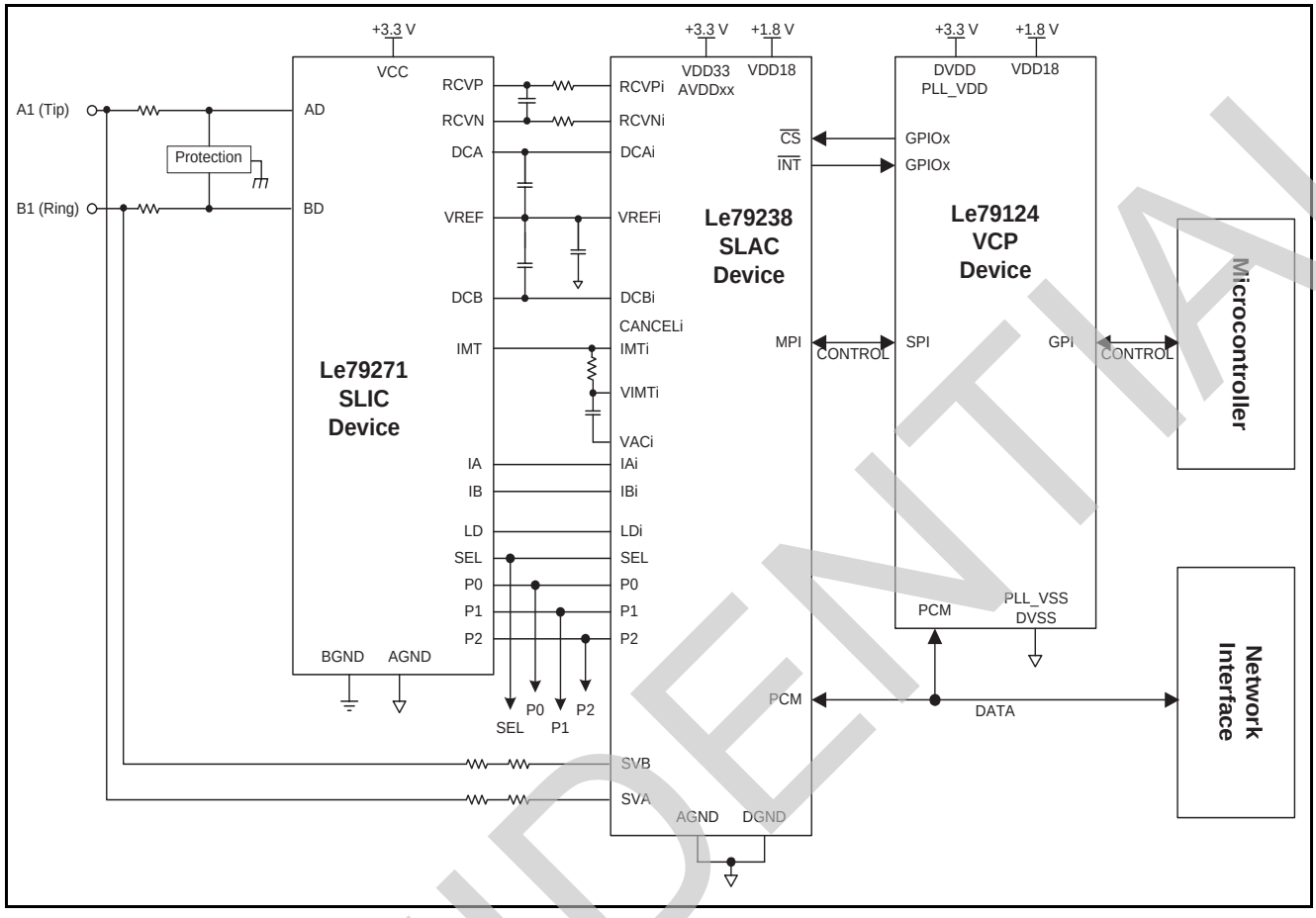



**Figure 2 - NGCC System with Le79124 VCP Device**

## 1.1 Wideband Codec Mode

The Le79238 device can be operated in a wideband mode to provide better voice quality. Wideband mode is intended to be used with a packet based processor with an adaptive echo canceller algorithm.

When wideband mode is selected, the nominal voice bandwidth is doubled to 7000 Hz. The wideband mode can be selected on a per channel basis. In this mode, internal clocks are doubled, increasing the sampling rates of the internal digital filters. Narrowband and wideband modes require their own unique set of coefficients. Therefore if switching between PCM operating modes on a given channel, the coefficients must be reprogrammed.

In wideband mode the PCM interface transmits and receives two evenly spaced sets of 16-bit timeslots in each frame. The user selects one timeslot during the first 62.5 µS of the frame. The first set of 16-bits will transmit or receive starting in this timeslot. The timeslot for the second set of 16-bits is generated automatically and placed 125/2 µS from the first timeslot.

Note: Wideband mode is supported by Product Code F and later revisions.

## 1.2 Le79238 Device Internal Block Diagram

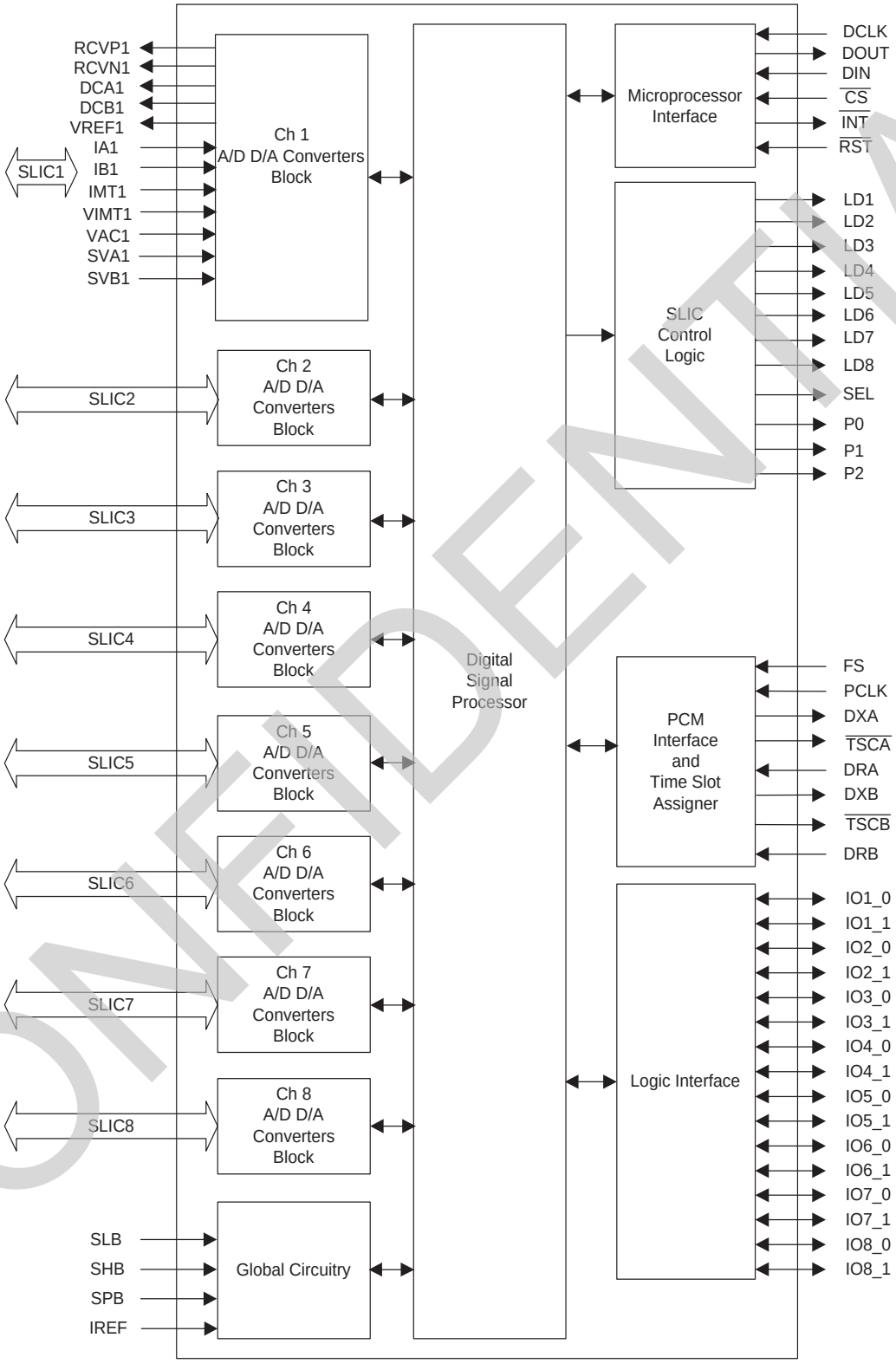
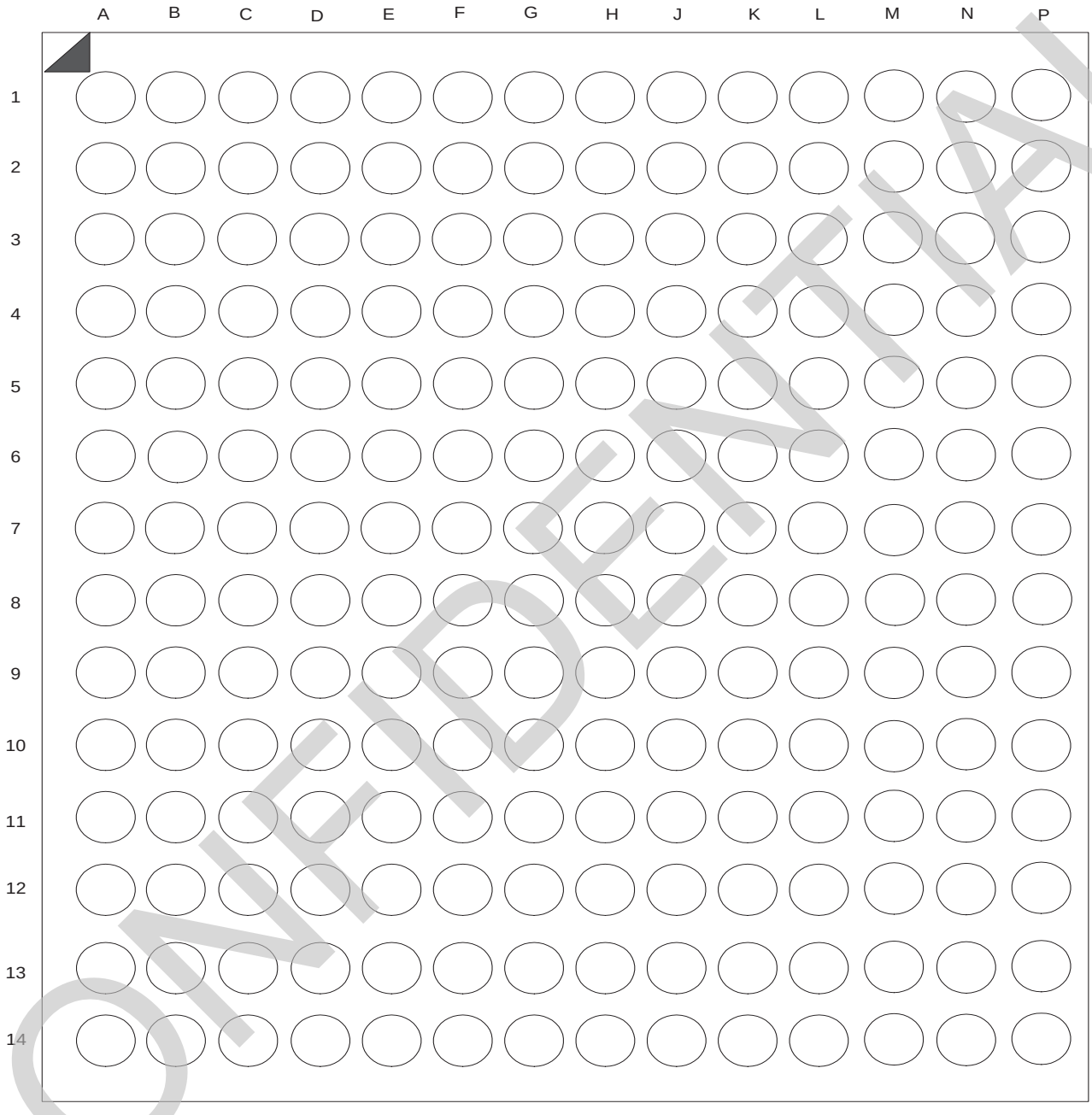



**Figure 3 - Internal Block Diagram**

### 1.3 Features of the NGCC

- Performs all battery feed, ringing, signaling, hybrid and test (BORSCHT) functions
- Controlled state changes to eliminate transients that could cause CRC errors
- Two or three chip solution supports high density, multi-channel architecture
- Supports two negative batteries and one positive battery
- Single hardware design meets multiple country requirements through software programming of:
  - Ringing waveform and frequency
  - DC loop-feed characteristics and current-limit
  - Loop-supervision detection thresholds
  - Off-hook debounce circuit
  - Ground-key and ring-trip filters
  - Off-hook detect de-bounce interval
  - Two-wire AC impedance
  - Transhybrid balance impedance
  - Transmit and receive gains
  - Equalization
  - Digital I/O pins
  - A-law/µ-law and linear selection
- Supports wideband 7.0 kHz codec mode
- Supports internal ringing with DC bias
  - Programmed ringing cadence
  - Self-contained ringing generation and control
  - Integrated ring-trip filter and software enabled manual or automatic ring-trip mode
- Supports external ringing (with ZL79258 SLAC)
- Supports metering generation with envelope shaping
  - Programmable metering cadencing
- Smooth polarity reversal
- Supports both loop-start and ground-start signaling
- SPI and PCM interfaces
- Exceeds LSSGR and CCITT central office requirements
- On-hook transmission
- Power/service denial mode
- Line-feed characteristics independent of battery voltage
- Low idle-power per line
- Compatible with inexpensive protection networks
- Monitors two-wire interface voltages and currents for subscriber line diagnostics
- Can monitor and/or drive A and B lead independently
- Automatic CID and Signaling and FSK and DTMF modes
- Tone generation
  - Howler
  - Call Progress
  - DTMF
- Modem support
- DTMF tone detection
- Dial Pulse and Flash detection
- Power-cross, fault, and foreign voltage detection
- Integrated line-test and self-test features
  - GR-909 and GR-844 equivalent
  - Built-in voice path test modes
  - 15 kHz noise filter

## 2.0 Connection Diagrams




**BOTTOM VIEW**

**Figure 4 - 196-Pin BGA Diagram**

| BGA Pin# | Pin Name | BGA Pin# | Pin Name | BGA Pin# | Pin Name | BGA Pin# | Pin Name | BGA Pin# | Pin Name |
|---|---|---|---|---|---|---|---|---|---|
| A1 | VAC1 | D1 | CANCEL2 | G1 | VAC2 | K1 | VIMT3 | N1 | IMT4 |
| A2 | VIMT1 | D2 | SVB2 | G2 | DCA2 | K2 | DCB3 | N2 | SVA4 |
| A3 | IMT1 | D3 | VREF1 | G3 | VREF2 | K3 | VREF3 | N3 | VREF4 |
| A4 | CANCEL1 | D4 | RSVD_B1 | G4 | IA2 | K4 | RSVD_B3 | N4 | IA4 |
| A5 | VDD18_4A | D5 | AVDD12A | G5 | AGND2 | K5 | AVDD34A | N5 | DGND_2A |
| A6 | $\overline{\text{TSCB}}$ | D6 | DEBUG_ CLK | G6 | IO1_1 | K6 | DGND_2 | N6 | LD3 |
| A7 | DRA | D7 | $\overline{\text{TSCA}}$ | G7 | IO2_0 | K7 | IO4_0 | N7 | P2 |
| A8 | PCLK | D8 | DCLK | G8 | IO8_1 | K8 | IO5_0 | N8 | SEL |
| A9 | DIN | D9 | $\overline{\text{RST}}$ | G9 | IO7_1 | K9 | DGND_3 | N9 | LD6 |
| A10 | VDD18_3 | D10 | AVDD78A | G10 | SLB | K10 | AVDD56 | N10 | DGND_4 |
| A11 | DCB8 | D11 | RSVD_B8 | G11 | IB7 | K11 | RSVD_B6 | N11 | IB5 |
| A12 | DCA8 | D12 | RCVN8 | G12 | RCVN7 | K12 | RCVN6 | N12 | RCVN5 |
| A13 | VAC8 | D13 | DCA7 | G13 | SVB7 | K13 | SVA6 | N13 | SVB5 |
| A14 | VIMT8 | D14 | VAC7 | G14 | CANCEL7 | K14 | IMT6 | N14 | DCA5 |
| B1 | DCA1 | E1 | IMT2 | H1 | CANCEL3 | L1 | VAC3 | P1 | VIMT4 |
| B2 | SVB1 | E2 | SVA2 | H2 | SVB3 | L2 | DCA3 | P2 | VAC4 |
| B3 | RCVN1 | E3 | RCVN2 | H3 | RCVN3 | L3 | RCVN4 | P3 | DCA4 |
| B4 | IB1 | E4 | RSVD_B2 | H4 | IB3 | L4 | RSVD_B4 | P4 | DCB4 |
| B5 | VDD18_4 | E5 | AVDD12 | H5 | AGND2A | L5 | AGND3 | P5 | VDD18_1 |
| B6 | DRB | E6 | VDD33_2 | H6 | IO2_1 | L6 | AGND4 | P6 | LD2 |
| B7 | DXA | E7 | DGND_6 | H7 | IO4_1 | L7 | VDD33_1 | P7 | LD4 |
| B8 | FS | E8 | IO8_0 | H8 | IO5_1 | L8 | RSVD_O | P8 | LD5 |
| B9 | DOUT | E9 | AGND8 | H9 | IO6_1 | L9 | AGND5 | P9 | LD7 |
| B10 | DGND_5 | E10 | AVDD78 | H10 | SPB | L10 | AVDD56A | P10 | VDD18_2 |
| B11 | IB8 | E11 | RSVD_B7 | H11 | IA6 | L11 | RSVD_B5 | P11 | CANCEL5 |
| B12 | VREF8 | E12 | VREF7 | H12 | VREF6 | L12 | VREF5 | P12 | IMT5 |
| B13 | SVA8 | E13 | DCB7 | H13 | DCA6 | L13 | SVB6 | P13 | VIMT5 |
| B14 | IMT8 | E14 | VIMT7 | H14 | VAC6 | L14 | CANCEL6 | P14 | VAC5 |

**Table 1 - 196-Pin BGA Pin Numbers and Pin Names**

| BGA Pin# | Pin Name | BGA Pin# | Pin Name | BGA Pin# | Pin Name | BGA Pin# | Pin Name | BGA Pin# | Pin Name |
|---|---|---|---|---|---|---|---|---|---|
| C1 | DCB1 | F1 | VIMT2 | J1 | IMT3 | M1 | CANCEL4 | | |
| C2 | SVA1 | F2 | DCB2 | J2 | SVA3 | M2 | SVB4 | | |
| C3 | RCVP1 | F3 | RCVP2 | J3 | RCVP3 | M3 | RCVP4 | | |
| C4 | IA1 | F4 | IB2 | J4 | IA3 | M4 | IB4 | | |
| C5 | DGND_1 | F5 | IREF | J5 | AVDD34 | M5 | AGND4A | | |
| C6 | DEBUG_ IO | F6 | AGND1 | J6 | IO3_1 | M6 | LD1 | | |
| C7 | DXB | F7 | IO1_0 | J7 | IO3_0 | M7 | P1 | | |
| C8 | $\overline{CS}$ | F8 | IO7_0 | J8 | IO6_0 | M8 | P0 | | |
| C9 | $\overline{INT}$ | F9 | AGND7 | J9 | AGND6 | M9 | LD8 | | |
| C10 | AGND8A | F10 | RSVD_C | J10 | SHB | M10 | AGND5A | | |
| C11 | IA8 | F11 | IA7 | J11 | IB6 | M11 | IA5 | | |
| C12 | RCVP8 | F12 | RCVP7 | J12 | RCVP6 | M12 | RCVP5 | | |
| C13 | SVB8 | F13 | SVA7 | J13 | DCB6 | M13 | SVA5 | | |
| C14 | CANCEL8 | F14 | IMT7 | J14 | VIMT6 | M14 | DCB5 | | |

**Table 1 - 196-Pin BGA Pin Numbers and Pin Names**

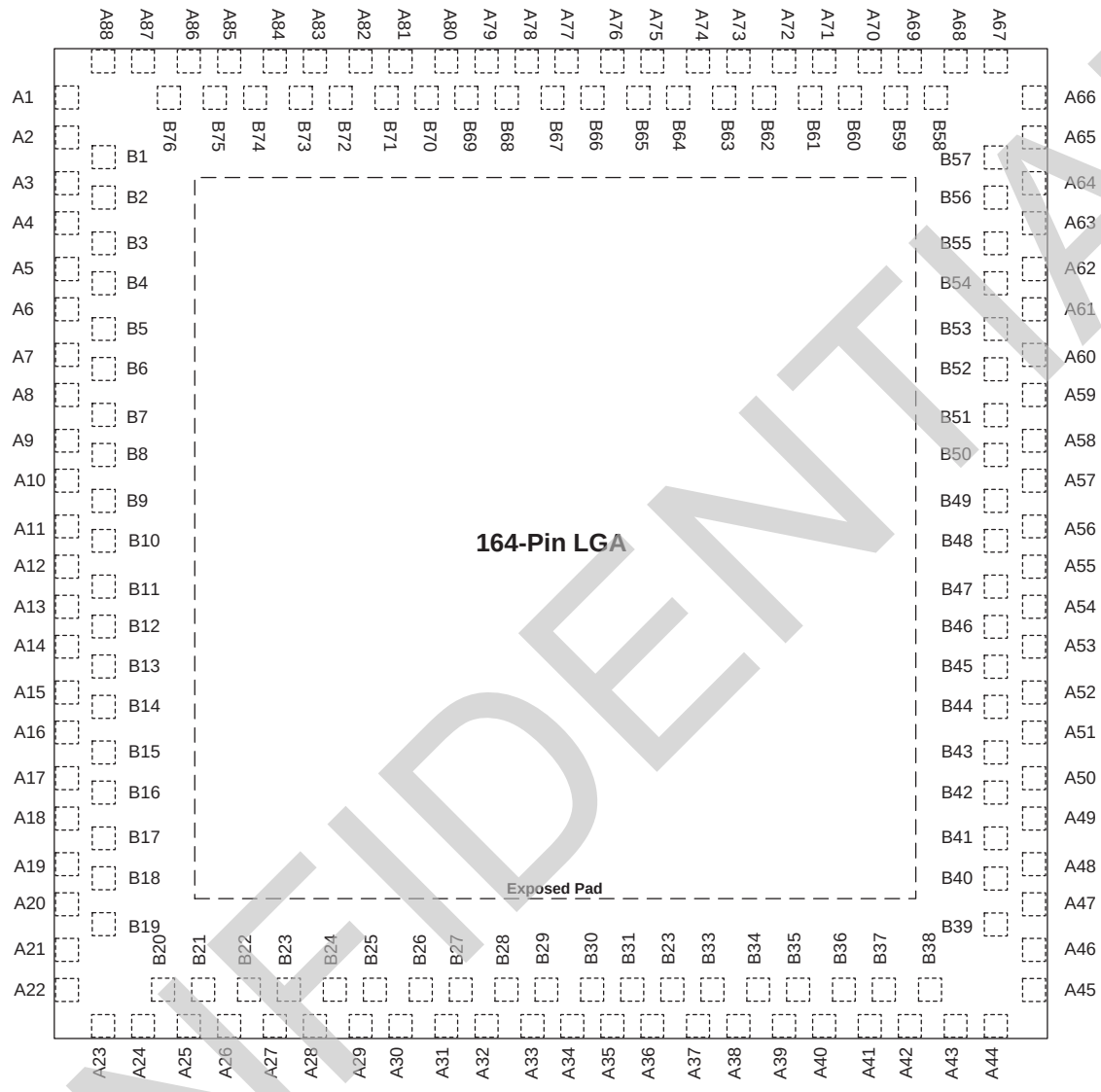



**Figure 5 - 164-Pin Land Grid Array (LGA) Diagram**

| LGA Pin# | Pin Name | LGA Pin# | Pin Name | LGA Pin# | Pin Name | LGA Pin# | Pin Name | LGA Pin# | Pin Name |
|---|---|---|---|---|---|---|---|---|---|
| A1 | RCVN1 | A34 | SEL | A67 | CANCEL8 | B11 | SVB3 | B44 | VREF6 |
| A2 | IO1_1 | A35 | LD6 | A68 | IA8 | B12 | VIMT3 | B45 | RCVP6 |
| A3 | SVA2 | A36 | LD8 | A69 | VREF8 | B13 | CANCEL3 | B46 | IO6_0 |
| A4 | IB2 | A37 | SVA5 | A70 | RCVN8 | B14 | DCA3 | B47 | SPB |
| A5 | VAC2 | A38 | IB5 | A71 | IO8_1 | B15 | DCB3 | B48 | SVA7 |
| A6 | CANCEL2 | A39 | VAC5 | A72 | IO8_0 | B16 | RCVN3 | B49 | IB7 |
| A7 | IA2 | A40 | IMT5 | A73 | $\overline{INT}$ | B17 | IO3_1 | B50 | VAC7 |
| A8 | DCA2 | A41 | DCA5 | A74 | DOUT | B18 | SVA4 | B51 | IMT7 |
| A9 | DCB2 | A42 | VREF5 | A75 | DCLK | B19 | IB4 | B52 | DCA7 |
| A10 | RCVP2 | A43 | RCVN5 | A76 | VDD33_2 | B20 | VAC4 | B53 | AVDD78 |
| A11 | IO2_0 | A44 | IO5_1 | A77 | PCLK | B21 | IMT4 | B54 | RCVP7 |
| A12 | SVA3 | A45 | IO5_0 | A78 | DXA | B22 | VREF4 | B55 | IO7_0 |
| A13 | IB3 | A46 | SVB6 | A79 | DXB | B23 | RCVN4 | B56 | SVB8 |
| A14 | VAC3 | A47 | VIMT6 | A80 | $\overline{TSCB}$ | B24 | IO4_1 | B57 | VIMT8 |
| A15 | IMT3 | A48 | AVDD56 | A81 | DEBUG_IO | B25 | VDD18_1 | B58 | IMT8 |
| A16 | IA3 | A49 | IMT6 | A82 | SVA1 | B26 | LD2 | B59 | DCA8 |
| A17 | VREF3 | A50 | DCA6 | A83 | IB1 | B27 | LD4 | B60 | DCB8 |
| A18 | AVDD34 | A51 | DCB6 | A84 | VAC1 | B28 | P0 | B61 | RCVP8 |
| A19 | RCVP3 | A52 | RCVN6 | A85 | CANCEL1 | B29 | P2 | B62 | $\overline{RST}$ |
| A20 | IO3_0 | A53 | IO6_1 | A86 | IA1 | B30 | LD5 | B63 | VDD18_3 |
| A21 | SVB4 | A54 | SHB | A87 | VREF1 | B31 | LD7 | B64 | DIN |
| A22 | VIMT4 | A55 | SLB | A88 | NC | B32 | VDD18_2 | B65 | $\overline{CS}$ |
| A23 | NC | A56 | SVB7 | | | B33 | SVB5 | B66 | FS |
| A24 | CANCEL4 | A57 | VIMT7 | B1 | RCVP1 | B34 | VIMT5 | B67 | DRA |
| A25 | IA4 | A58 | CANCEL7 | B2 | IO1_0 | B35 | CANCEL5 | B68 | VDD18_4 |
| A26 | DCA4 | A59 | IA7 | B3 | SVB2 | B36 | IA5 | B69 | $\overline{TSCA}$ |
| A27 | DCB4 | A60 | VREF7 | B4 | VIMT2 | B37 | DCB5 | B70 | DRB |
| A28 | RCVP4 | A61 | DCB7 | B5 | AVDD12 | B38 | RCVP5 | B71 | DEBUG_ CLK |
| A29 | IO4_0 | A62 | RCVN7 | B6 | IMT2 | B39 | SVA6 | B72 | SVB1 |
| A30 | LD1 | A63 | IO7_1 | B7 | VREF2 | B40 | IB6 | B73 | VIMT1 |
| A31 | LD3 | A64 | SVA8 | B8 | RCVN2 | B41 | VAC6 | B74 | IMT1 |
| A32 | VDD33_1 | A65 | IB8 | B9 | IO2_1 | B42 | CANCEL6 | B75 | DCA1 |
| A33 | P1 | A66 | VAC8 | B10 | IREF | B43 | IA6 | B76 | DCB1 |
| The Exposed Pad is the AGND and DGND connection. Connect to a PCB ground plane using a thermal pad and a grid of thermal vias. Refer to the Hardware Design Guide for use and considerations. | | | | | | | | | |

**Table 2 - 164-Pin LGA Pin Numbers and Pin Names**

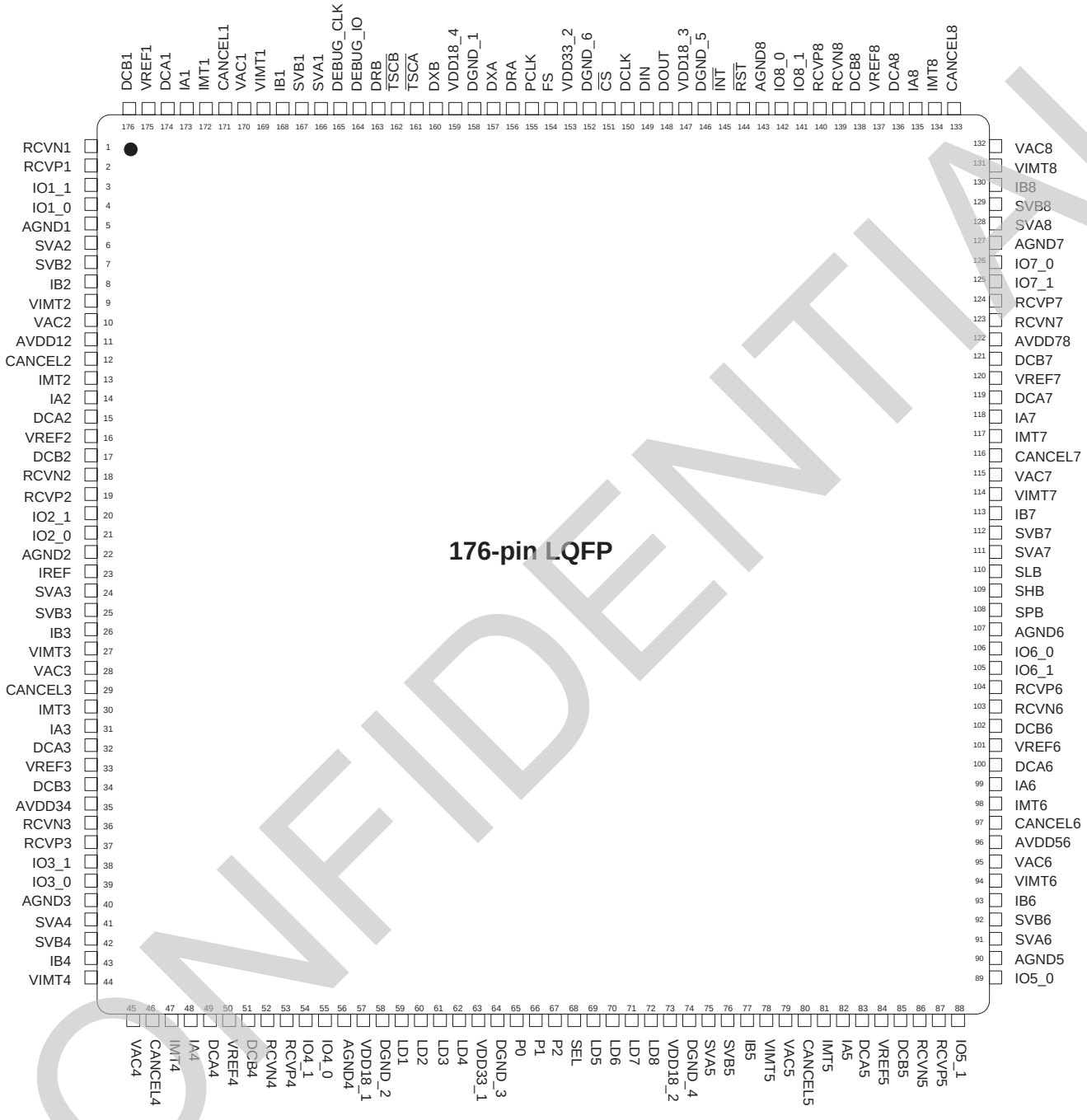



**Figure 6 - 176-Pin LQFP Diagram**

## 3.0 Pin Descriptions

| Pin Name | LQFP Pin # | LGA Pin # | BGA Pin # | Type | Description |
|---|---|---|---|---|---|
| AGND[1:8] | 5, 22, 40, 56, 90, 107, 127, 143 | EPAD | F6, G5, L5, L6, L9, J9, F9, E9 | Ground | Analog ground. Separate analog and digital grounds are provided to allow noise isolation, however the grounds must be connected together on the circuit board. |
| AGND2A, AGND4A, AGND5A, AGND8A | — | — | H5, M5, M10, C10 | | |
| AVDD12, AVDD34, AVDD56 AVDD78 | 11, 35, 96, 122 | B5, A18, A48, B53 | E5, J5, K10, E10 | Supply | +3.3 VDC analog power supply inputs. For best performance, all of the AVDD and VDD33 power supply pins should be connected together at the device. Four decoupling capacitors should be used. Place a decoupling capacitor near AVDD12, AVDD34, AVDD56, and AVDD78. AVDD12A, AVDD34A, AVDD56A, and AVDD78A do not require their own decoupling capacitors. |
| AVDD12A, AVDD34A, AVDD56A AVDD78A | — | — | D5, K5, L10, D10 | | |
| CANCEL[1:8] | 171, 12, 29, 46, 80, 97, 116, 133 | A85, A6, B13, A24, B35, B42, A58, A67 | A4, D1, H1, M1, P11, L14, G14, C14 | Output | Metering cancellation output. If metering is used, connect a capacitor from this pin to the respective channel's IMT pin. If metering is not used, let this pin float. |
| $\overline{CS}$ | 151 | B65 | C8 | Input | MPI interface chip select. A logic low placed on this pin enables serial data transmission into DIN or out of the DOUT port. |
| DCA[1:8] | 174, 15, 32, 49, 83, 100, 119, 136 | B75, A8, B14, A26, A41, A50, B52, B59 | B1, G2, L2, P3, N14, H13, D13, A12 | Output | DC feed and low-frequency voltage control of the SLIC device's A lead amplifiers. |
| DCB[1:8] | 176, 17, 34, 51, 85, 102, 121, 138 | B76, A9, B15, A27, B37, A51, A61, B60 | C1, F2, K2, P4, M14, J13, E13, A11 | Output | DC feed and low-frequency voltage control of the SLIC device's B lead amplifiers. |
| DCLK | 150 | A75 | D8 | Input | MPI interface data clock. Provides data control for MPI interface control. |
| DEBUG_CLK | 165 | B71 | D6 | Input | DEBUG Clock. This node needs to be tied to VDD33 through a 0 Ω resistor. |
| DEBUG_IO | 164 | A81 | C6 | Input/ Output | DEBUG input output. This node needs to be tied to DGND through a 0 Ω resistor. |
| DGND_[1:6] | 158, 58, 64, 74, 146, 152 | EPAD | C5, K6, K9, N10, B10, E7 | Ground | Digital ground. Separate analog and digital grounds are provided to allow noise isolation, however the grounds must be connected together on the circuit board. |
| DGND_2A | — | — | N5 | | |
| DIN | 149 | B64 | A9 | Input | MPI interface control data input. Control data is serially written into the Le79238 device via the DIN pin with the MSB first. DIN can be tied to DOUT for a single bi-directional interface. The data clock (DCLK) determines the data rate. |

| Pin Name | LQFP Pin # | LGA Pin # | BGA Pin # | Type | Description |
|---|---|---|---|---|---|
| DOUT | 148 | A74 | B9 | Output | MPI interface control data output. Control data is serially read out of the Le79238 device via the DOUT pin with the MSB first. DOUT can be tied to DIN for a single bi-directional interface. The data clock (DCLK) determines the data rate. DOUT is high impedance except when data is being transmitted from the Le79238 device under control of $\overline{CS}$. |
| DRA, DRB | 156, 163 | B67, B70 | A7, B6 | Input | PCM highway data receive ports. The receive PCM data is input serially through the DRA or DRB ports. Data is always received with the most significant bit first. For compressed signals, 1 byte of data is received every 125 µs at the PCLK rate. In the Linear mode, 2 consecutive bytes of data for each channel are received every 125 µs at the PCLK rate. In Wideband mode, the frame sync stays at 8 kHz, the Le79238 operates internally at 16 kHz and outputs data twice per frame in evenly spaced timeslots. If an input is not used, tie to DGND. |
| DXA, DXB | 157, 160 | A78, A79 | B7, C7 | Output | PCM highway data transmit ports. The transmit PCM data is transmitted serially through the DXA or DXB ports. Data is always transmitted most significant bit first. The output is available every 125 µs and the data is shifted out in 8-bit (16-bit in Linear mode) bursts at the PCLK rate. In Wideband mode, the frame sync stays at 8 kHz, the Le79238 operates internally at 16 kHz and outputs data twice per frame in evenly spaced timeslots. DXA and DXB are high impedance between bursts and while the device is in the inactive mode. If an output is not used, let the pin float. |
| FS | 154 | B66 | B8 | Input | PCM highway frame sync. PCM operation is selected by the presence of an 8 kHz frame sync signal on this pin in conjunction with the PCM clock on the PCLK pin. This 8 kHz pulse identifies the beginning of a frame. The Le79238 device references individual timeslots with respect to this input, which must be synchronized to PCLK. |
| IA[1:8] | 173, 14, 31, 48, 82, 99, 118, 135 | A86, A7, A16, A25, B36, B43, A59, A68 | C4, G4, J4, N4, M11, H11, F11, C11 | Input | Input current is proportional to current in SLIC's A lead. |
| IB[1:8] | 168, 8, 26, 43, 77, 93, 113, 130 | A83, A4, A13, B19, A38, B40, B49, A65 | B4, F4, H4, M4, N11, J11, G11, B11 | Input | Input current is proportional to current in SLIC's B lead. |
| IMT[1:8] | 172, 13, 30, 47, 81, 98, 117, 134 | B74, B6, A15, B21, A40, A49, B51, B58 | A3, E1, J1, N1, P12, K14, F14, B14 | Input | Input current is proportional to the differential current in the SLIC's AD and BD leads. AGND on this node indicates a SLIC thermal overload condition. |
| $\overline{INT}$ | 145 | A73 | C9 | Output | Interrupt. When a subscriber line requires service, this pin goes to a logic 0 to interrupt a high level processor. Logic drive is selectable between open drain and TTL-compatible outputs. |
| IO[1:8]_0 | 4, 21, 39, 55, 89, 106, 126, 142 | B2, A11, A20, A29, A45, B46, B55, A72 | F7, G7, J7, K7, K8, J8, F8, E8 | Input/ Output | General purpose logic input/output and relay driver port. These pins can be programmed as an input or an output. These pins can be programmed as an open drain 50 mA relay driver. Unused pins should either be tied to AGND through a 10 KΩ resistor or programmed as low outputs. |

| Pin Name | LQFP Pin # | LGA Pin # | BGA Pin # | Type | Description |
|---|---|---|---|---|---|
| IO[1:8]_1 | 3, 20, 38, 54, 88, 105, 125, 141 | A2, B9, B17, B24, A44, A53, A63, A71 | G6, H6, J6, H7, H8, H9, G9, G8 | Input/ Output | General purpose logic input/output. These pins can be programmed as an input or an output. Unused pins should either be tied to AGND through a 10 KΩ resistor or programmed as low outputs. |
| IREF | 23 | B10 | F5 | Input | External resistor ($R_{REF}$) connected between this pin and analog ground generates an accurate, on-chip reference current for the A/D's and D/A's on the Le79238 device. |
| LD[1:8] | 59, 60, 61, 62, 69, 70, 71, 72 | A30, B26, A31, B27, B30, A35, B31, A36 | M6, P6, N6, P7, P8, N9, P9, M9 | Output | Logic output that controls data transfer into the SLIC device. When LD is Low, the data on outputs P0–P2 is transferred to the respective data latches as directed by the SEL pin. When LD is High, the data is locked in the latches. |
| NC | — | A23, A88 | — | | No connect. This pin is not internally connected. |
| PCLK | 155 | A77 | A8 | Input | PCM highway clock. A valid PCLK is required for overall device operation. PCLK determines the rate at which PCM data is serially shifted into or out of the PCM ports. The minimum clock frequency for linear/companded data is 1.536 MHz. |
| P[0:2] | 65, 66, 67 | B28, A33, B29 | M8, M7, N7 | Output | P-bus. Controls the operating modes of the SLIC and LCAS devices connected to the Le79238 device. |
| $\overline{RST}$ | 144 | B62 | D9 | Input | Hardware reset. This pin should be driven by a logic signal (0V and +3.3 V) or else an external RC circuit (capacitor between $\overline{RST}$ and DGND, resistor between $\overline{RST}$ and VDD33) should be used to apply a low signal for enough time to guarantee that all supplies are valid before the reset is de-asserted. |
| RCVN[1:8] | 1, 18, 36, 52, 86, 103, 123, 139 | A1, B8, B16, B23, A43, A52, A62, A70 | B3, E3, H3, L3, N12, K12, G12, D12 | Output | Receive signal output (Inverting). Voice and metering control voltage signals for SLIC amplifiers. |
| RCVP[1:8] | 2, 19, 37, 53, 87, 104, 124, 140 | B1, A10, A19, A28, B38, B45, B54, B61 | C3, F3, J3, M3, M12, J12, F12, C12 | Output | Receive signal output (Noninverting). Voice and metering control voltage signals for SLIC amplifiers. |
| RSVD_B[1:8], RSVD_C, RSVD_O | — | — | D4, E4, K4, L4, L11, K11, E11, D11, F10, L8 | Reserved | Reserved. These pins are internally connected. Pins must be left floating. |
| SEL | 68 | A34 | N8 | Output | Logic output that selects data outputs P0–P2 to either control the SLIC's operating modes or the SLIC's switch states. |
| SHB, SLB, SPB | 109, 110, 108 | A54, A55, B47 | J10, G10, H10 | Input | Battery sense leads. Resistors that sense the high, low, and positive battery voltages connect here. If only one negative battery is used, connect both negative battery resistors to the same supply or leave SLB unconnected. If the positive battery is not used, connect the SPB resistor to AGND or leave the pin unconnected. These pins are current inputs into pins whose voltage is held at VREF, do not short these pins together. |
| SVA[1:8] | 166, 6, 24, 41, 75, 91, 111, 128 | A82, A3, A12, B18, A37, B39, B48, A64 | C2, E2, J2, N2, M13, K13, F13, B13 | Input | Senses the voltages on A lead through external sense resistors. |

| Pin Name | LQFP Pin # | LGA Pin # | BGA Pin # | Type | Description |
|---|---|---|---|---|---|
| SVB[1:8] | 167, 7, 25, 42, 76, 92, 112, 129 | B72, B3, B11, A21, B33, A46, A56, B56 | B2, D2, H2, M2, N13, L13, G13, C13 | Input | Senses the voltages on B lead through external sense resistors. |
| $\overline{\text{TSCA}}$, $\overline{\text{TSCB}}$ | 161, 162 | B69, A80 | D7, A6 | Output | PCM highway backplane driver enables. $\overline{\text{TSCA}}$ or $\overline{\text{TSCB}}$ are active low when PCM data is output on the DXA or DXB pins, respectively. The outputs are open-drain and are normally inactive (high impedance). Pull-up loads should be connected to VDD33. If output not used, let the pin float. |
| VAC[1:8] | 170, 10, 28, 45, 79, 95, 115, 132 | A84, A5, A14, B20, A39, B41, B50, A66 | A1, G1, L1, P2, P14, H14, D14, A13 | Input | Voice (AC only) signal proportional to the IMT current of the SLIC. |
| VDD18_[1:4] | 57, 73, 147, 159 | B25, B32, B63, B68 | P5, P10, A10, B5 | Supply | +1.8 VDC digital power supply inputs. Place a decoupling capacitor near VDD18_1, VDD18_2, VDD18_3, and VDD18_4. VDD18_4A does not require its own decoupling capacitor. A bulk decoupling capacitor is also advised. |
| VDD18_4A | — | — | A5 | | |
| VDD33_[1:2] | 63, 153 | A32, A76 | L7, E6 | Supply | +3.3 VDC digital power supply inputs. For best performance, all of the VDD33 and AVDD power supply pins should be connected together at the device. A decoupling capacitor should be used on each pin. |
| VIMT[1:8] | 169, 9, 27, 44, 78, 94, 114, 131 | B73, B4, B12, A22, B34, A47, A57, B57 | A2, F1, K1, P1, P13, J14, E14, A14 | Input | Signal proportional to the IMT current of the SLIC. |
| VREF[1:8] | 175, 16, 33, 50, 84, 101, 120, 137 | A87, B7, A17, B22, A42, B44, A60, A69 | D3, G3, K3, N3, L12, H12, E12, B12 | Output | This pin provides a +1.5 V, single-ended reference to the respective SLIC. This pin requires an external capacitor to AGND, whether the output is used or not. |

## 4.0 Absolute Maximum Ratings

Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability.

| | |
|---|---|
| Storage Temperature | $-55^{o}C \leq T_A \leq +125^{o}C$ |
| Ambient Temperature, under Bias | $-40^{o}C \leq T_A \leq +85^{o}C$ |
| Ambient relative humidity (non condensing) | 5% to 95% |
| VDD33 with respect to AGND or DGND | –0.4 V to +4.0 V |
| VDD18 with respect to AGND or DGND | –0.4 V to +1.98 V |
| AVDD with respect to AGND or DGND | –0.4 V to +4.0 V |
| AVDD with respect to VDD33 | ±0.4 V |
| IMT, VIMT, VAC, IA, IB with respect to AGND or DGND | –0.4 V to (AVDD + 0.4 V) |
| IO [1:8]_0 current | 75 mA |
| AGND | DGND ±0.4 V |
| Latch up immunity (any pin) | ±100 mA |
| Any other pin with respect to DGND | –0.4 V to (VDD33 + 0.5 V) |
| ESD Immunity (Human Body Model) | JESD22 Class 1C compliant |

### 4.1 Green Package Assembly

The green package devices are assembled with enhanced, environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. Refer to IPC/JEDEC J-Std-020 for recommended peak soldering temperature and solder reflow temperature profile.

The package referred to as a Land Grid Array (LGA) in this document uses a Cu Alloy Leadframe as the substrate and its construction is such that it would be classified as a QFN per JEDEC Standard JESD30. Refer to the Hardware Design Guide for PCB mounting of the LGA.

# 5.0 Operating Ranges

Microsemi guarantees the performance of this device over commercial (0º to 70ºC) and industrial (–40º to 85ºC) temperature ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling. These characterization and test procedures comply with the Telcordia GR-357-CORE Generic Requirements for Assuring the Reliability of Components Used in Telecommunications Equipment.

## 5.1 Environmental Ranges

| | |
|---|---|
| Ambient Temperature | –40 to +85ºC |
| Ambient Relative Humidity | 15 to 85% |

## 5.2 Electrical Ranges

| | | |
|---|---|---|
| Analog Supply AVDD | +3.3 V ±5%, VDD33 ±50 mV | |
| Digital Supply VDD33 | +3.3 V ±5% | Refer to “Reset at Power-Up” on page 35 for supply and reset sequencing. |
| Digital Supply VDD18 | +1.8 V ±5% | |
| DGND | 0 V | |
| AGND | DGND ±10 mV | |

# 6.0 Programming of the SLAC Parameters

The line circuit parameters are stored in a Device Profile file. The Device Profile files are generated by Microsemi’s application support programs WinSLAC™ and Profile Wizard. The Device Profile file is loaded into the Le79238 SLAC through the API-II software interface.

The Device Profile file consists of a System-Device Profile and a number of optional parameter profiles. If the NGVCP is used, profiles for cadencing and Caller ID are added. The following optional files pertain to parameters that are programmable in the SLAC:

## 6.1 AC Parameters

- Input impedance $Z_D$
- 2-4W Hybrid balance impedance $Z_L$
- Test termination impedance $Z_T$
- Transmit Relative Level and frequency response equalization
- Receive Relative Level and frequency response equalization
- A-law, µ-law, 16-bit linear, or wideband PCM encoding

### 6.2 DC Parameters

- Loop current limit value
- Feed resistance before current limit
- Metallic voltage at transition between current limit and resistive feed
- Anti-saturation headroom voltage
- Abrupt or smooth reversal
- Off-hook detection threshold
- GND start threshold
- DC fault detection threshold
- AC fault detection threshold

### 6.3 Ringing Parameters

- A lead DC voltage $V_{DCA}$ during internal ringing
- B lead DC voltage $V_{DCB}$ during internal ringing
- Balanced or unbalanced internal ringing
- Amplitude of internal ringing
- Frequency of internal ringing
- Wave shape of internal ringing
- Short loop ring trip threshold
- Long loop ring trip threshold

### 6.4 Tone and Metering Signal Parameters

- Frequency
- Amplitude

For a complete description of parameters, consult the *WinSLAC™ Software User's Guide (Document ID 080779)* and the *Profile Wizard User's Guide (Document ID 127063)*.

# 7.0 Electrical Characteristics

## 7.1 AC/DC Specifications

Typical values are for TA = 25ºC and nominal supply voltage. Minimum and maximum values are over the temperature and supply voltage ranges as shown in “Operating Ranges” on page 23, except as noted. PCLK and FS are present and valid.

Refer to the *Next Generation Carrier Chipset Hardware Design Guide (Document ID 126583)* for sensitive nodes that have trace capacitance restrictions.

| No. | Item | Condition | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| 1 | Input Low Voltage ($V_{IL}$)<br>Digital inputs and IO[1:8]_[0:1] programmed as an input | | –0.50 | — | 0.80 | V | |
| 2 | Input High Voltage ($V_{IH}$)<br>Digital inputs and IO[1:8]_[0:1] programmed as an input | | 2.0 | — | VDD33 + 0.5 | V | |
| 3 | Input Leakage Current, IO[1:8]_[0:1] | 0 to VDD33 | –10 | — | +10 | µA | |
| | All other digital inputs | | –120 | — | +180 | | |
| 4 | Input hysteresis<br>PCLK, FS, DRA, DRB, DCLK, DIN and IO[1:8]_[0:1] programmed as an input | | 0.15 | — | 0.30 | V | 2 |
| 5 | Output Low Voltage ($V_{OL}$)<br>DXA, DXB, DOUT, IO[1:8]_[0:1], $\overline{INT}$, $\overline{TSCA}$, $\overline{TSCB}$ | Iol = 10 mA | — | — | 0.4 | V | |
| | IO[1:8]_0 when programmed as relay driver | Iol = 50 mA | — | — | 0.7 | | |
| | P[0:2], LD, SEL | Iol = 3 mA | — | — | 0.4 | | |
| 6 | Output High Voltage ($V_{OH}$)<br>All digital outputs except $\overline{INT}$ in open drain mode and $\overline{TSCA}$, $\overline{TSCB}$ | Ioh = 400 µA | VDD33 – 0.4 | — | — | V | |
| 7 | Input Leakage Current<br>IMT | | –1 | — | 1 | µA | |
| 8 | Full scale voltage levels, input or output DCA, DCB | | — | VREF±1.2 | — | V | |
| | RCVP, RCVN | Normal gain | | VREF±0.6 | | | |
| | | High gain | | VREF±1.2 | | | |
| | CANCEL | Normal gain | | VREF±0.6 | | | |
| | | High gain | | VREF±1.2 | | | |
| | VIMT | | | See Note | | | 3 |
| | VAC | | | See Note | | | 4 |
| 9 | Output voltage, VREF[1:8] | Load current = 0 to 0.8 mA, Source or Sink | 1.47 | 1.50 | 1.53 | V | |

**Table 3 - AC/DC Specifications**

| No. | Item | Condition | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| 10 | Battery read A/D relative error | % of input voltage | –3% | — | +3% | | 2, 7 |
| | Battery read A/D absolute error | | –0.5 | — | +0.5 | V | |
| 11 | +3.3 V Supply Power Dissipation, Nonoperational, Power per channel | Active state | — | 80 | 110 | mW | 8 |
| | | Standby state | — | 27 | 40 | | |
| | +1.8 V Supply Power Dissipation, Nonoperational, Power per channel | Active state | — | 43 | 60 | | |
| | | Standby state | — | 14 | 22 | | |
| 12 | +3.3 V Supply Power Dissipation, Operational, Power per channel | Active state | — | 72 | — | mW | 9, 10 |
| | | Standby state | — | 29 | — | | |
| | | Disabled state | — | 5 | — | | |
| | +1.8 V Supply Power Dissipation, Operational, Mean power per channel | Active state | — | 36 | — | | |
| | | Standby state | — | 22 | — | | |
| | | Disabled state | — | 18 | — | | |

**Table 3 - AC/DC Specifications**

## 7.2 Transmission Specifications

Transmission specifications are tested with the X-filter, R-filter, GX, and GR set to a gain of 1, the Z-filter, B-filter, AISN, and DISN set to a gain of 0, the VDAC gain set to 0 dB, the DRX gain set to 5/8, and the VAC gain set to 15. The receive path 0 dB output level is defined as 0.18472 Vrms per pin on RCVP-RCVN (0.36944 Vrms differential) and the transmit path 0 dB input level is defined as 0.032839 Vrms on the VAC pin. Supplies are as specified in “Electrical Ranges” on page 23. PCLK and FS are present and valid.

| No. | Item | Condition | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| 1 | Insertion Loss A-D, D-A | input: 1014 Hz, 0 dBm0 GR = GX = 0 dB; AISN, R, X, B and Z disabled | –0.25 | 0 | +0.25 | dB | 7 |
| | A-D + D-A | Temperature = 25°C | –0.15 | 0 | +0.15 | | |
| | | Variation over temperature | –0.1 | 0 | +0.1 | | |
| 2 | Level set error (Error between setting and actual value) | A-D, D-A | –0.1 | 0 | 0.1 | dB | 7 |
| 3 | DR to DX gain in full digital loopback mode | DR Input: 1014 Hz, –10 dBm0 GR=GX=0 dB; AISN, R, X, B and Z filters default | –0.3 | 0 | +0.3 | dB | 7 |

**Table 4 - Transmission Specifications**

| No. | Item | Condition | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| 4 | Idle Channel Noise Psophometric Weighted (A-law) | A-D (DX output) | — | — | –69 | dBm0p | 5, 10 |
| | | D-A (RCVN, RCVP output) | — | — | –78 | | |
| | C Message weighted (µ-law) | A-D (DX output) | — | — | +19 | dBrnC0 | |
| | | D-A (RCVN, RCVP output) | — | — | +12 | | |
| | 15 kHz flat (Wideband linear mode) | A-A (VAC input any channel, RCVN, RCVP output any other channel, DX tied to DR) | — | 16 | — | dBrn0 | 1 |
| 5 | PSRR Image frequency (VDDxx) A-D | Input: 4.8 to 7.8 kHz, 200 mVp-p | 37 | — | — | dB | 1 |
| | D-A | Measure at: 8000 Hz – Input frequency | 37 | — | — | | |
| 6 | End-to-end absolute group delay | 1014 Hz, –10 dBm0; B=Z=0; X=R=1 | — | — | 725 | µS | 2, 6 |
| 7 | Crosstalk TX to RX same channel RX to TX | 300 Hz to 3400 Hz, 0 dBm0 | — | — | –75 | dBm0 | 2 |
| | | | — | — | –75 | | |
| 8 | Crosstalk TX or RX to TX other channel TX or RX to RX | 1014 Hz, 0 dBm0 | — | — | –75 | | |
| | | | — | — | –75 | | |

**Table 4 - Transmission Specifications**

Note 1: Not tested or partially tested in production. This parameter is guaranteed by characterization or correlation to other tests.

Note 2: Guaranteed by design.

Note 3: VIMT has an analog range of VREF ±1.2 V, although only VREF ±1.0 V is used by the A/D input.

Note 4: Full scale voltage level for VAC is VREF ± (1.0 V / VAC Gain).

Note 5: The specification holds for any setting of GX gain from 0 to 12 dB or GR from 0 to –12 dB when tested with a transmission level point of 0 dBr.

Note 6: The end-to-end group delay is the absolute group delay at the echo path with the B-filter turned off. Refer to the Next Generation Carrier Chipset Designer's Guide for more information. See Figure 9 for Group Delay Distortion versus frequency.

Note 7: Requires that the calibration command be performed to achieve this performance.

Note 8: Firmware and DC feed not operational.

Note 9: Firmware and DC feed operational, batteries applied.

Note 10: DSP Core Power Reduction enabled.

## 7.3 Transmit and Receive Paths

In this section, the transmit path is defined as the analog input to the Le79238 device (VAC) to the PCM voice output. The receive path is defined as the PCM voice input to the Le79238 analog output (RCVN, RCVP). All limits defined in this section are tested with B = 0, Z = 0 and X = R = GR = GX = 1, unless otherwise specified. These transmission characteristics are valid for 0 to 70º C.

## 7.4 Attenuation Distortion

The attenuation of the signal in either path is nominally independent of the frequency. The deviations from nominal attenuation will stay within the limits shown in Figure 7 and Figure 8 for narrowband operation and within the limits shown in Table 5 for wideband operation when the calibration command is performed and equalized coefficients are used.

The reference signal level is –10 dBm0. The minimum transmit attenuation at 60 Hz is 24 dB.

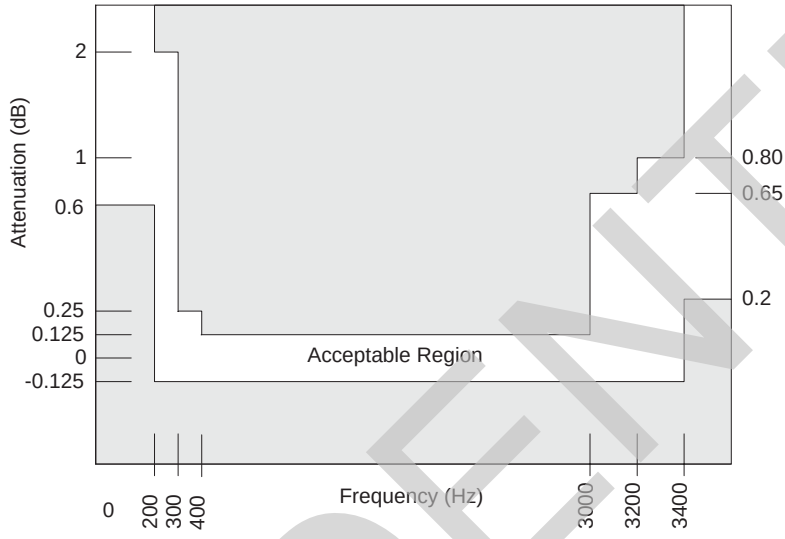



**Figure 7 - Narrowband Transmit Path Attenuation vs. Frequency**

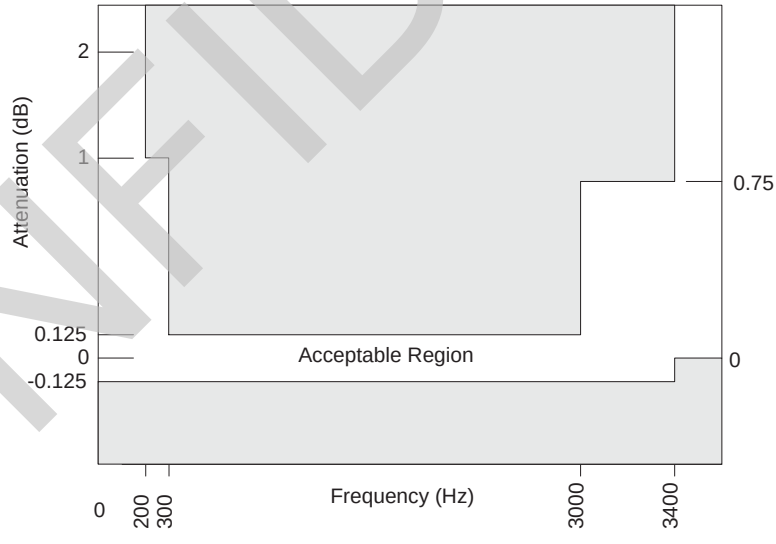



**Figure 8 - Narrowband Receive Path Attenuation vs. Frequency**

| No. | Item | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| 1 | Transmit Path Loss | Relative to 1020 Hz: | | | | dB |
| | | 50 Hz | +20 | — | — | |
| | | 60 Hz | +20 | — | — | |
| | | 200 Hz | 0 | — | +3.0 | |
| | | 300 Hz | –0.25 | — | +0.5 | |
| | | 500 Hz | –0.25 | — | +0.3 | |
| | | 4800 Hz | –0.25 | — | +0.3 | |
| | | 6000 Hz | –0.25 | — | +0.5 | |
| | | 6400 Hz | –0.25 | — | +0.75 | |
| | | 6800 Hz | 0 | — | +1.0 | |
| | | 8000 Hz | +14 | — | — | |
| | | 9200 Hz | +32 | — | — | |
| 2 | Receive Path Loss | Relative to 1020 Hz: | | | | dB |
| | | 50 Hz | 0 | — | — | |
| | | 60 Hz | 0 | — | — | |
| | | 200 Hz | 0 | — | +2.0 | |
| | | 300 Hz | –0.25 | — | +0.5 | |
| | | 600 Hz | –0.25 | — | +0.3 | |
| | | 4800 Hz | –0.25 | — | +0.3 | |
| | | 6000 Hz | –0.25 | — | +0.5 | |
| | | 6400 Hz | –0.25 | — | +0.75 | |
| | | 6800 Hz | 0 | — | +1.0 | |
| | | 8000 Hz | +14 | — | — | |
| | | 9200 Hz | +28 | — | — | |
| | | 12000 Hz | +28 | — | — | |

**Table 5 - Wideband Attenuation vs. Frequency**

*Note:*
*Not tested or partially tested in production. These parameters are guaranteed by characterization or correlation to other tests.*

### 7.5 Group Delay Distortion

For either transmission path, the group delay distortion is within the limits shown in Figure 9. The minimum value of the group delay is taken as the reference. The signal level is –10 dBm0.

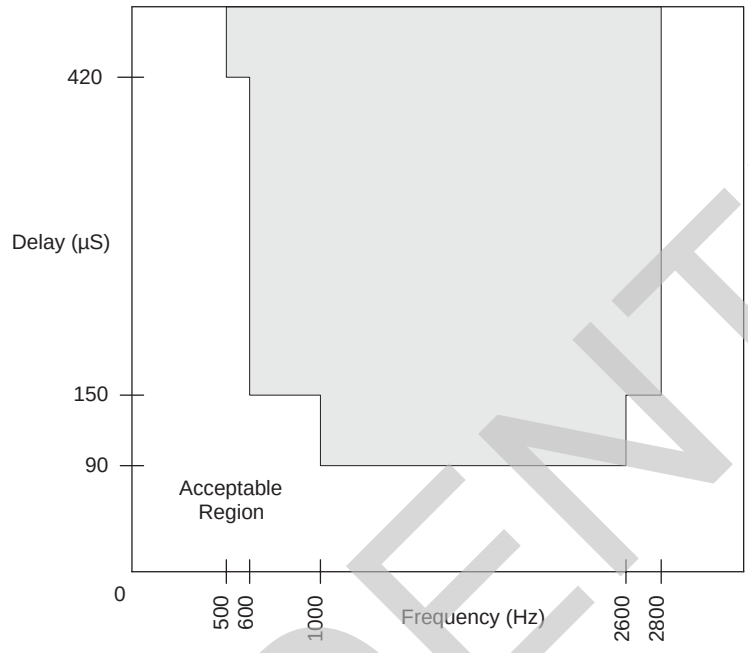



**Figure 9 - Group Delay Distortion**

### 7.6 Single Frequency Distortion

The output signal level, at any single frequency in the range of 300 to 3400 Hz, other than that due to an applied 0 dBm0 sine wave signal with frequency f in the same frequency range, is less than –46 dBm0. With f swept between 0 Hz to 300 Hz and 3.4 kHz to 12 kHz, any generated output signals other than f are less than –28 dBm0. This specification is valid for either transmission path.

## 7.7 Gain Linearity

The gain deviation relative to the gain at –10 dBm0 is within the limits shown in Figure 10 (A-law) and Figure 11 (µ-law) for either transmission path when the input is a sine wave signal of 1014 Hz.

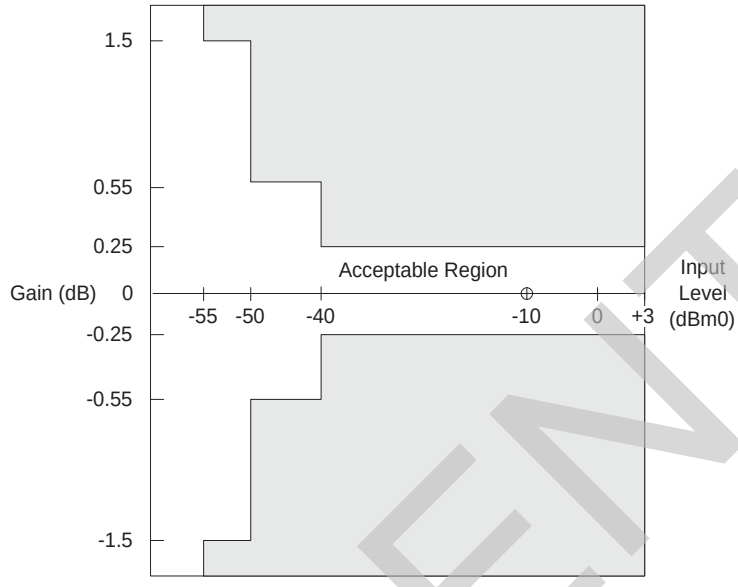



**Figure 10 - A-law Gain Linearity with Tone Input (Both Paths)**

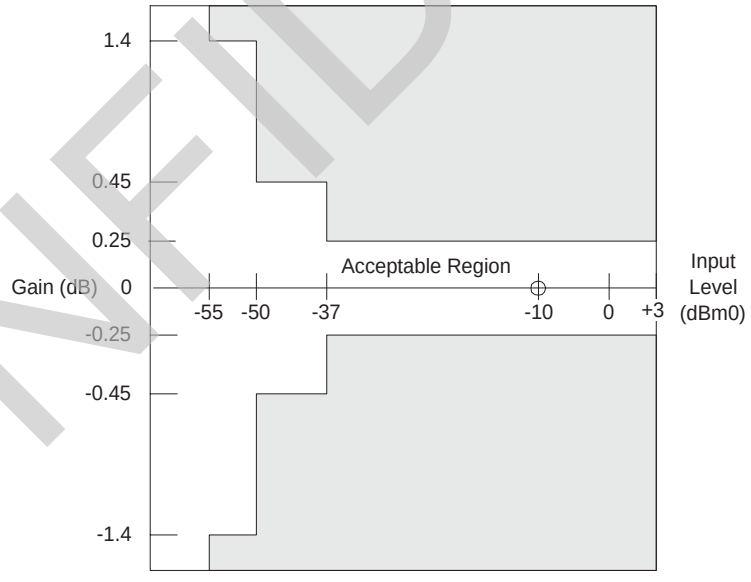



**Figure 11 - µ-law Gain Linearity with Tone Input (Both Paths)**

## 7.8 Total Distortion Including Quantizing Distortion

The signal to total distortion ratio will exceed the limits shown in Figure 12 for either path when the input signal is a sine wave signal of frequency 1014 Hz.

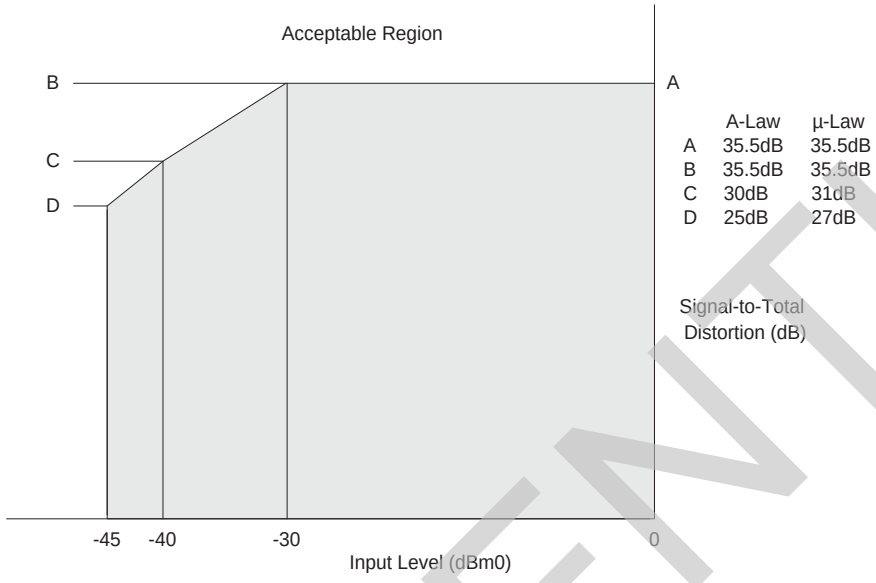



**Figure 12 - Total Distortion with Tone Input, Both Paths**

## 7.9 Overload Compression

Figure 13 shows the acceptable region of operation for input signal levels above the reference input power (0 dBm0). The conditions for this figure are:

(1) With GX in the range of +1 dB < GX ≤ +12 dB as set by WinSLAC™; (2) GR in the range of –12 dB ≤ GR < –1 dB as set by WinSLAC™; (3) Digital voice output connected to digital voice input; and (4) measurement analog to analog.

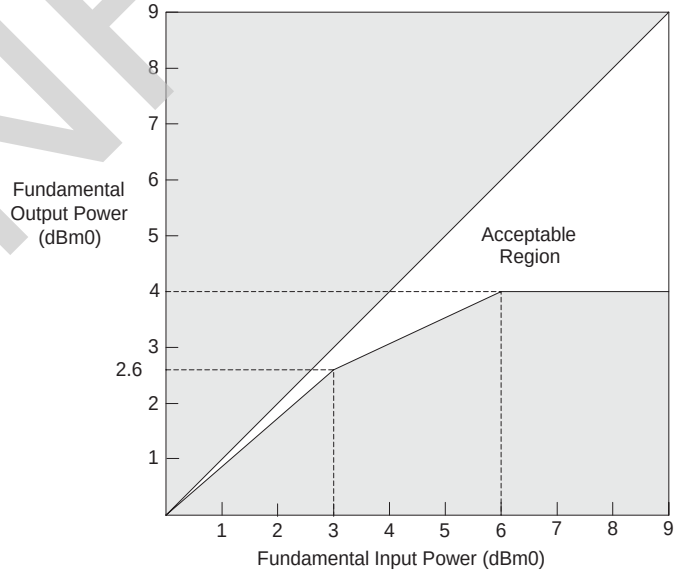



**Figure 13 - A/A Overload Compression**

## 7.10 Discrimination Against Out-of-Band Input Signals

When an out-of-band sine wave signal with frequency and level A is applied to the analog input, there may be frequency components below 4 kHz at the digital output which are caused by the out-of-band signal. These components are at least the specified dB level below the level of a signal at the same output originating from a 1014 Hz sine wave signal with a level of A dBm0 also applied to the analog input. The specifications for narrowband mode are shown below.

| Frequency of Out-of-Band Signal | Amplitude of Out-of-Band Signal | Level below A |
|---|---|---|
| 16.6 Hz < f < 45 Hz | –25 dBm0 < A ≤ 0 dBm0 | 18 dB |
| 45 Hz < f < 65 Hz | –25 dBm0 < A ≤ 0 dBm0 | 25 dB |
| 65 Hz < f < 100 Hz | –25 dBm0 < A ≤ 0 dBm0 | 10 dB |
| 3400 Hz < f < 4600 Hz | –25 dBm0 < A ≤ 0 dBm0 | see Figure 14 |
| 4600 Hz < f < 100 kHz | –25 dBm0 < A ≤ 0 dBm0 | 32 dB |

**Table 6 - Minimum Specifications for Out-of-Band Input Signals**

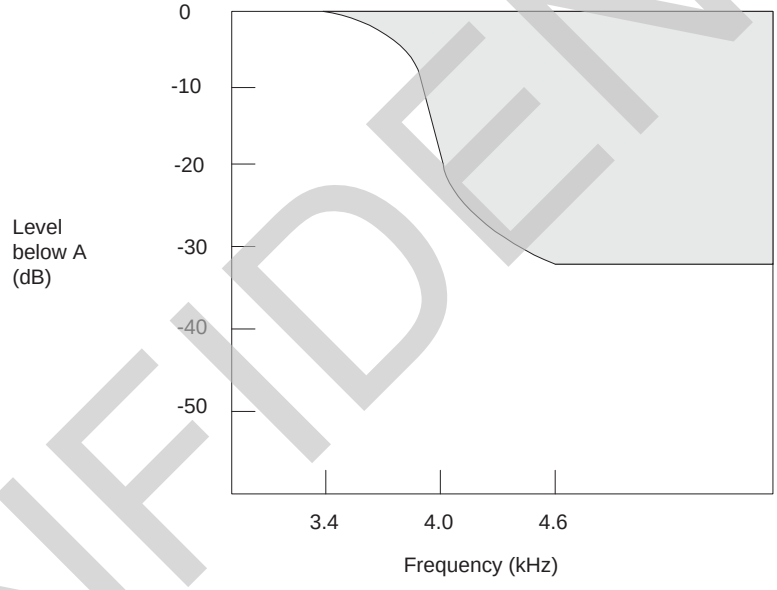



**Figure 14 - Discrimination Against Out-of-Band Signals**

***Note:***

*The attenuation of the waveform below amplitude A between 3400 Hz and 4000 Hz is given by the formula:*

$$\text{Attenuation} = \left[14 - 14\sin\left(\frac{\pi(4000 - f)}{1200}\right)\right] \text{dB}$$

*The attenuation of the waveform below amplitude A between 4000 Hz and 4600 Hz is given by the formula:*

$$\text{Attenuation} = \left[14 - 18\sin\left(\frac{\pi(4000 - f)}{1200}\right)\right] \text{dB}$$

## 7.11 Spurious Out-of-Band Signals at the Analog Output

With PCM code words representing a sine wave signal in the range of 300 Hz to 3400 Hz at a level of 0 dBm0 applied to the digital input, the level of the spurious out-of-band signals at the analog output for narrowband mode is less than the limits shown below.

| Frequency | Level |
|---|---|
| 4.6 kHz to 40 kHz | –32 dBm0 |
| 40 kHz to 240 kHz | –46 dBm0 |
| 240 kHz to 1 MHz | –36 dBm0 |

**Table 7 - Limits for Spurious Out-of-Band Signals**

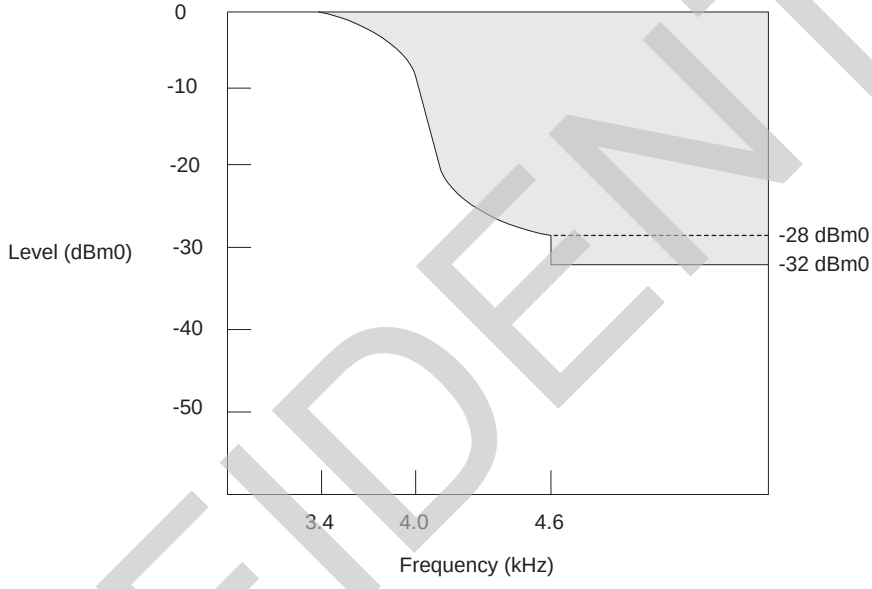



**Figure 15 - Spurious Out-of-Band Signals**

***Note:***

*The amplitude of the spurious out-of-band signals between 3400 Hz and 4600 Hz is given by the formula:*

$$\text{Level} = \left[ -14 - 14\sin\left(\frac{\pi(f-4000)}{1200}\right)\right] \text{dBm0}$$

## 8.0 Reset at Power-Up

This section discusses the handling of the reset signal at power-up. Two power-up sequences are presented.

If VDD33 and VDD18 power supplies are powered up separately, refer to Figure 16. For this sequence, VDD33 is powered up shortly before VDD18 is powered up (period D). Reset can be held high or low at power-up; PCLK can be running or turned off initially. After VDD18 is powered up and stabilized, a short reset (B) needs to be asserted (within period A). When reset is de-asserted, PCLK must be running and main device initialization functions can now proceed.

If VDD33 and VDD18 power supplies are powered up at the same time, refer to Figure 16. For this sequence, reset must be held low at power-up; PCLK can be running or turned off initially. After the supplies have stabilized, reset needs to be de-asserted (within period A). At this point PCLK must be running and main device initialization functions can now proceed.

*Note: If the intent for either power-up sequence is to hold the line card in reset, apply the initial short reset, de-assert, then wait period C before re-asserting reset. Reset can then be held indefinitely, with or without PCLK operational.*

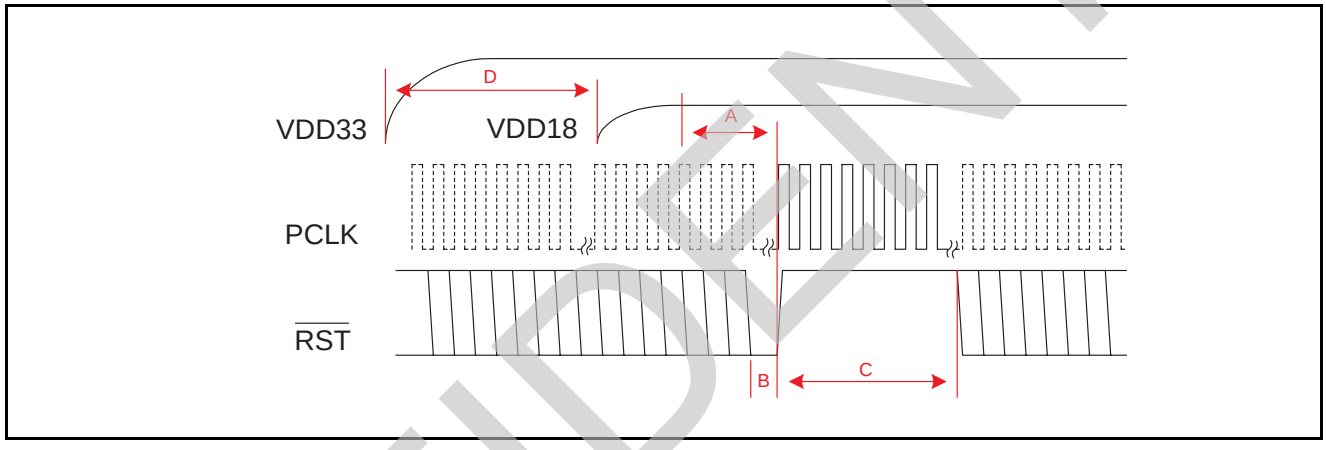



**Figure 16 - Reset Sequence when VDD33 and VDD18 are Powered Up Separately**

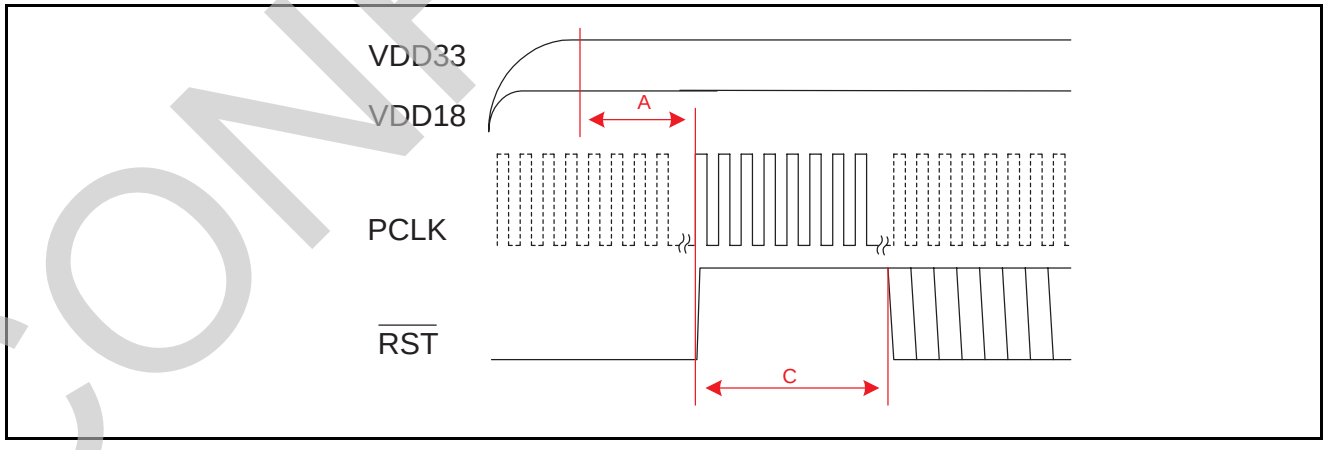



**Figure 17. Reset Sequence when VDD33 and VDD18 are Powered Up Together**

*Note: A valid reset should be applied as soon as possible after power-up.*

| No. | Parameter | Min. | Typ | Max | Unit |
|---|---|---|---|---|---|
| A | Time after power supplies are stable until reset is de-asserted | 300 | — | See note | µS |
| B | Reset pulse width | 1 | — | See note | |
| C | Time after reset is de-asserted until reset can be re-asserted. (Only applies to initial power-up sequence.) | 1000 | — | — | |
| D | Delay between VDD33 and VDD18 power-up | 500 | — | See note | |

**Table 8 - Recommended Reset Sequence Timing**

## 9.0 Host Bus Control Interface (HBI) Overview

The Host Bus Interface provides a means for exchanging control, configuration and status information with an external processor. This is accomplished by allowing the host to access regions of the DSP memory, and selected hardware registers. Essentially, the host peeks and pokes internal memory to exchange data.

This interface is implemented through a combination of hardware and firmware. The design is layered as shown in Figure 18. Hardware provides a generic means for transporting data between the host and internal memory. The interpretation of the data is provided by firmware running on the DSP. This layered architecture allows the definition of the application level interface to change by modifying the DSP firmware.

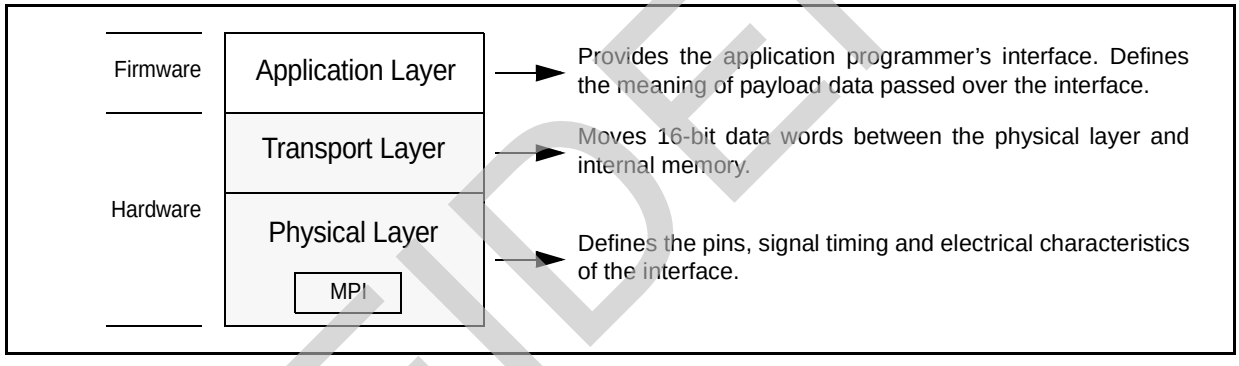



**Figure 18 - Host Bus Interface Layers**

The transport layer moves 16-bit data words between the physical interface and internal DSP memory or hardware registers on an internal bus. It defines the structure of a transport frame, which consists of a 16-bit command word followed by 0 or more 16-bit payload data words. It also defines the interface address model, and provides mapping between interface and internal addresses.

The application layer defines the programmer's interface, and is almost entirely implemented in firmware. The exception is a handful of configuration registers implemented in hardware. This layer defines the meaning of the payload data delivered by the transport layer. Because it is implemented in firmware, the definition of the programmer's interface can change by providing new software.

The physical layer provides the functionality needed to electrically interface with a network processor. The Microprocessor Interface (MPI) implements a common, industry standard 3-wire or 4-wire synchronous serial slave interface included with many DSPs and microcontrollers.

### 9.1 Transport Layer

The primary responsibility of the transport layer is to move 16-bit data words between the physical interface and locations on an internal bus, which includes DSP memory. Data is organized into transport frames, which consist of a 16-bit command word followed by 0 or more data words. The command word provides address and length

information to the transport hardware. In a sense, this hardware provides an internal DMA-like function, moving data over the internal bus under host control.

### 9.1.1 Interface Addressing

The transport command word provides address information to the interface hardware.

The host interface address model is based on a paged memory scheme, as shown in Figure 19. The command design permits up to 257 pages, with up to 128 offset-addressable 16-bit wide register locations. Therefore, an interface address is composed of an 8-bit page number and a 7-bit register offset. Pages are selected by using a command to write the page register. All data access commands operate on the selected page. One exception is the direct page, which can be accessed at any time without changing the page register.

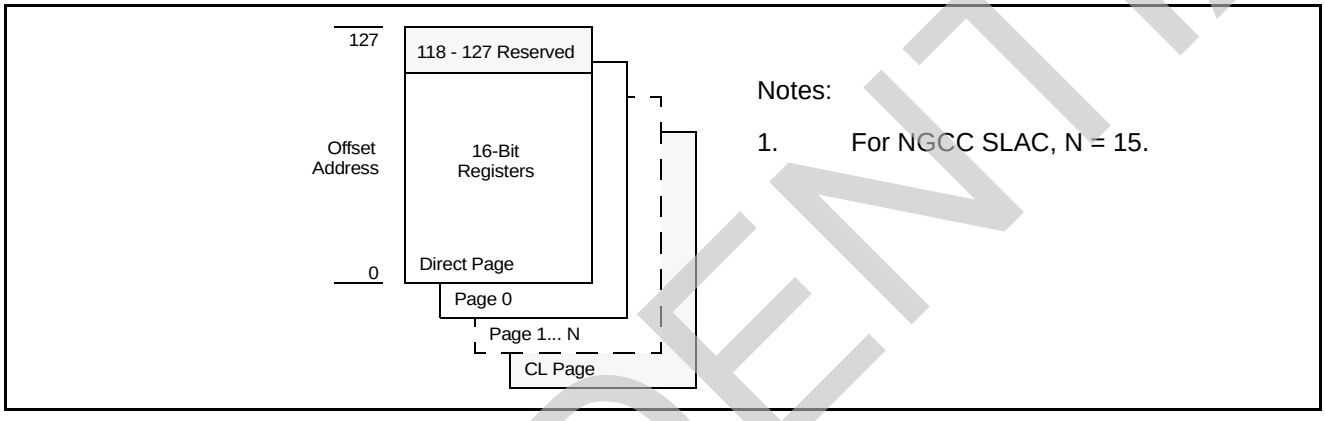



**Figure 19 - Host Bus Interface Address Mode**

### 9.1.2 Command Structure

All transport frames start with a 16-bit command word followed by 0 or more 16-bit data words.

| Transport Command | Command Bit Position | | | | | | | | Number of 16-bit Data Words |
|---|---|---|---|---|---|---|---|---|---|
| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | |
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Paged Offset Access | 0 | Offset Address (0 - 127) | | | | | | | Length + 1 |
| | r/w[1] | Length (0 - 127) | | | | | | | |
| Direct Page Offset Access | 1 | Offset Address[b] (0 - 118) | | | | | | | Length + 1 |
| | r/w | 0 | 0 | 0 | Length[b] (0 - 15) | | | | |
| Start Mailbox Access | 1 | 1 | 1 | 1 | 1 | 0 | 0 | r/w | Length + 1 |
| | Length (0 - 255) | | | | | | | | |
| Continue Mailbox Access | 1 | 1 | 1 | 1 | 1 | 0 | 1 | r/w | Length + 1 |
| | Length (0 - 255) | | | | | | | | |
| Reserved | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| | Reserved | | | | | | | | |

**Table 9 - Host Bus Interface Transport Commands**

| Transport Command | Command Bit Position | | | | | | | | Number of 16-bit Data Words |
|---|---|---|---|---|---|---|---|---|---|
| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | |
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| Configure Interfaces | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| | Interface Option Bits | | | | | | | | |
| Select Page | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| | 0 | 0 | 0 | 0 | Page Number (0 - 15) | | | | |
| Select CL Page | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| Reserved | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| NOP | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |

**Table 9 - Host Bus Interface Transport Commands**

1. Read / Write select bit. 0 = Read. 1 = Write.
b. Addresses 120-127 on the Direct Page are reserved.

### 9.1.3 Paged Offset Access

This command accesses one or more contiguous 16-bit registers on the currently selected page; it must be preceded by a page selection command. The 7-bit offset specifies the starting address on the page. The command is followed by (Length + 1) 16-bit data words. The 7-bit Length field allows accessing between 1 and 128 locations with a single transport frame. For nonzero Lengths, the address automatically increments, and consecutive locations are accessed.

### 9.1.4 Direct Page Offset Access

Direct Offset Access is the same as Paged Offset Access, except that the direct page is the target. By using this command, the direct page can be accessed at any time without modifying the page register. The 4-bit Length field allows accessing between 1 and 16 locations on a single transport frame. For nonzero Lengths, the address automatically increments, and consecutive locations are accessed.

### 9.1.5 Start Mailbox Access

This command accesses a contiguous stream of 16-bit data words starting from offset 0 on the currently selected page. The command is followed by (Length + 1) 16-bit data words. The 8-bit Length field allows accessing between 1 and 256 locations (i.e., up to 512 bytes) with a single transport frame. Access always begins from offset 0, and the address automatically increments.

### 9.1.6 Continue Mailbox Access

Continue Mailbox Access is the same as Start Mailbox Access, except that access starts from where the last mailbox access left off. By using this command, packets of arbitrary length can be supported. Note that Offset Access commands can be executed between multiple Mailbox Access commands. This gives the host the freedom to split data transfers into smaller sizes if desired.

### 9.1.7 Configure Interfaces

This global command is used to configure various physical interface options. It is a write only global command and is followed by 0 data words.

**Interface Configuration Register (Configure)**

| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Data Byte | HBI WAKE | RSVD | RSVD | INT DRIVE | RSVD | RSVD | RSVD | RSVD |

INT_DRIVE: $\overline{\text{INT}}$ pin drive mode.
0: open drain (default).
1: TTL.

HBI_WAKE: Assert Wake to the DSP. This bit will be cleared by hardware on the first HBI clock after the DSP has responded.
0: No Wake event is present from HBI (default)
1: HBI is forcing a wake event to the DSP and clocks.

*Note: RSVD pins need to be written as zero.*

### 9.1.8 Select Page

This command selects the active interface page. It is a write only command and is followed by 0 data words. The 4-bit page field allows up to 16 selectable pages per SLAC to be defined.

### 9.1.9 Select CL Page

This command selects the special CL (Code Load) page. It is a write only command and is followed by 0 data words.

### 9.1.10 NOP

A command is reserved to serve as a NOP. Note that all commands, except for the Offset Access commands, are implemented by reserving an address from the direct page.

### 9.1.11 Associated Registers

The following registers are used by the HBI – CL Page Base Address Register (special type of base address register used for code loading) and Mailbox Flag Register.

#### 9.1.11.1 CL Page Base Address Register

*Address:* *Direct Page Offset 06 (High) and 07 (Low)*

*Power Up Default:* *0000 0000h*

This special base address register is used for code loading.

| | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|---|
| Data Byte | 0 | 0 | BASE_ADDR[29:24] | | | | | |

| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Data Byte | BASE_ADDR[23:16] | | | | | | | |

**Table 10 - CL Page Base Address High Register (User)**

| | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|---|
| Data Byte | BASE_ADDR[15:8] | | | | | | | |

| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Data Byte | RSVD | | | | | | | |

**Table 11 - CL Page Base Address Low Register (User)**

### 9.1.11.2 CL Page CRC

*Address:* *Direct Page Offset 04 (High) and 05 (Low)*

*Power Up Default:* *0000 0000h*

This special register is used to check code load integrity. This a writable and readable register. The booting sequence should always write a predetermined seed into this register before loading the memory. Each write through the CL page is fed into a CRC generator to create a unique code in this register. At the end of the booting sequence, the user software should check for the expected value in this register.

| | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|---|
| Data Byte | SEED[31:24] | | | | | | | |

| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Data Byte | SEED[23:16] | | | | | | | |

**Table 12 - CL Page CRC High Register (User)**

| | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|---|
| Data Byte | SEED[15:8] | | | | | | | |

| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Data Byte | SEED[7:0] | | | | | | | |

**Table 13 - CL Page CRC Low Register (User)**

SEED[31:0]: Current CRC value of data written to the CL page.

#### 9.1.11.3 Mailbox Flag Register

*Address:* *Direct Page Offset 03*

*Power Up Default:* *0000 0000h*

This register is used to communicate the handshaking control flags between the DSP and the host. There is one flag for each mailbox in the system.

| | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 |
|---|---|---|---|---|---|---|---|---|
| Data Byte | MBOX_FLAG[15:8] | | | | | | | |

| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Data Byte | MBOX_FLAG[7:0] | | | | | | | |

**Table 14 - Mailbox Flag Register (User and DSP, located in DSPIO)**

MBOX_FLAG[15:0]: Mailbox flags. These bits will be allocated for downstream or upstream handshaking in order to determine whether the host or the DSP owns a particular mailbox at any given point in time.

### 9.2 Code Loading

The NGCC SLAC device will always come up in boot mode during a power-on reset or when the reset pin of the chip is de-asserted. The DSP will hold off program execution until the on-chip CM location 0 has been written by the host via the MPI interface. The enabling or disabling of the boot operation during a hardware reset command is controlled by the boot sequence register bit in the Hardware Reset register. If the boot sequence is disabled when the hardware reset command is issued, the DSP immediately starts program execution from address 0 without any boot operation.

The CL page base address register resides in the direct page and is accessible by the host. When the host writes the upper 24-bits of the destination address to the CL page base address register and the lower 7-bits of the address to the offset address field of the paged offset command, the host can write up to 128 words of code/data into destination bus addresses with the paged offset commands. The formula to compute the AMBA bus address for paged offset access commands with the CL page is:

AMBA address = base_addr * 256 + offset_ address * 2

#### 9.2.1 Code Load Integrity

Code integrity is guaranteed by CRC hardware which resides in this block. The CL Page CRC High and Low registers are writable and readable registers. Any boot sequence should start with writing a seed into these registers. Each subsequent write through the CL page will appropriately alter the value held in that register. It is modified by both the address and the data of the write access. After all memory is loaded the user should read the new value in the CL Page CRC register and compare it with the expected value. Any discrepancy indicates that the code should be rebooted.

### 9.2.2 Host Boot Procedure

The sequence to perform the boot procedure through the MPI interface is outlined below.

1. Power-On Reset, hardware pin reset, or a hardware reset command with boot sequence enabled will put the DSP into boot mode.
2. Initialize the CL Page CRC register with the desired seed.
3. Select the CL Page on an individual SLAC or to ALL SLAC devices.
4. Write the higher 24-bits of the destination bus address into the CL page base address registers, and the lower 7-bits of the address into the offset address field of the paged offset access command. Use the paged offset access command to write a block of code into DSP memory. Each access command can write up to 128 16-bit words of data.
5. Repeat step 4 for the next block of code into another block of DSP memory space.
6. After all the program codes are loaded, repeat steps 4-5 for PM data memory and DM data memory.
7. Check the CL Page CRC register to verify proper code load. If a loading error is present then repeat starting at step 2.
8. When all DSP memories are loaded, issue a paged offset access command to CM address 0 in order to trigger the DSP to start program execution.

### 9.2.3 Partial Code Load Procedure

After the boot procedure, the DSP will execute instructions continuously. If the system wants to load a new codec program, it requires a pre-defined mechanism between firmware and the host software so that the DSP would not execute from the same code memory space that the host is trying to download with new program code. There will be a performance hit on the DSP, as each CM memory write steals one cycle from the DSP operation. Since a complete code load could take as long as 10 to 20 ms, the host can not wait that long to process any interrupt. Thus, the partial code load needs to partition the code load into manageable blocks in order to allow the system to service an interrupt. The sequence to perform partial code loading is outlined below.

1. Trigger the handshake between the DSP firmware and the host software to exchange information and ensure the destination CM code memory is not being used by the DSP firmware. This mechanism is pre-defined by firmware without any hardware assistance.
2. Initialize the CL Page CRC with the desired seed.
3. Select the CL Page register on an individual SLAC or on ALL SLAC devices.
4. Write the higher 24-bits of the destined bus address into full access base register, and the lower 7-bit of the address into the offset address field of the paged offset access command. Use the paged offset access command to write a block of code into DSP memory. Each access command can write up to 128 16-bit words of data.
5. Repeat step 4 for the next block of code with size up to 128 16-bit words. Fill codes into different blocks of DSP memory space.
6. Finish loading the program code in the present block, then allow interrupts to be serviced by the host. At the end of interrupt service routine or if no interrupt exists, go back to step 4 to load a new block of program code until all the blocks are loaded.
7. Check the CL Page CRC registers to verify proper code load. If a loading error is present then repeat starting at step 2.
8. After all the program codes are loaded, trigger another predefined handshake between the DSP firmware and the host software to indicate the end of partial code loading.

## 9.3 Application Layer

The application layer defines the programmer's interface and is almost entirely implemented in firmware. The exception is a handful of configuration registers implemented in hardware. This layer defines the meaning of the payload data delivered by the transport layer. Because it is implemented in firmware, the definition of the host programmer's interface can change by providing a new ROM firmware image. The NG-SLAC programmer's model is depicted in Figure 20.

The programmer's model dedicates HBI pages 0 through 7 for channel specific registers, page 8 for the Command Mailbox, and page 9 for the Response Mailbox. These register locations are all implemented in DSP memory.

The direct page contains a small number of registers implemented by the hardware blocks on the AMBA bus. The remainder of direct page registers are dedicated to global (not specific to a channel) registers, and are implemented in DSP memory by the firmware.

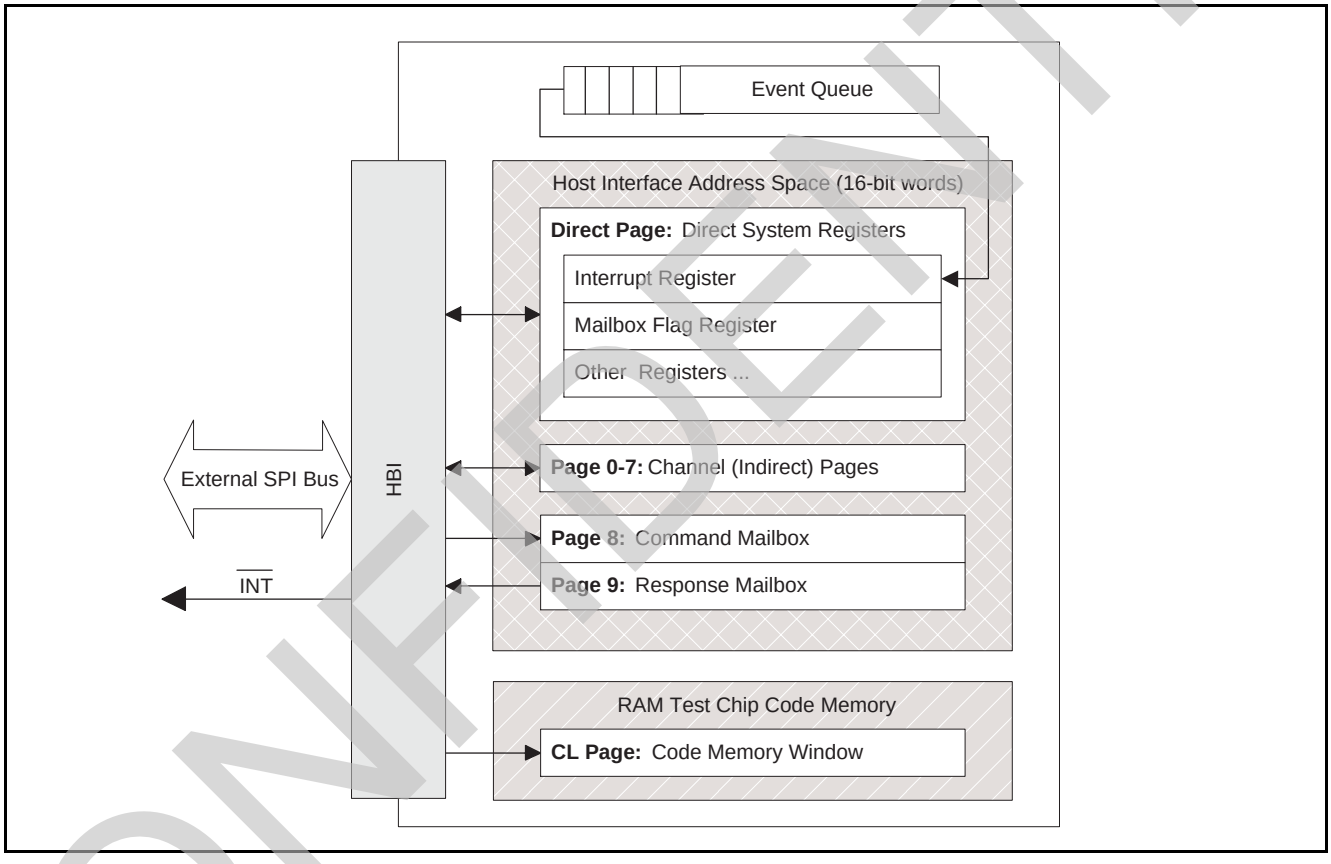



**Figure 20 - NGCC SLAC Programmer's Mode**

## 9.4 Physical Layer

### 9.4.1 Microprocessor Interface (MPI)

The microprocessor Interface is an external interface of the NGCC SLAC device used by the external host to communicate with the device. The MPI interface is compatible with the SPI interface used by general DSPs, so that those chips can interface with the NGCC SLAC device without any glue logic.

#### 9.4.1.1 MPI External Pins Connection

The MPI is a 3-wire or 4-wire synchronized serial interface used in many DSPs and micro controllers. The data is transferred bidirectionally from master to slave and from slave to master. The master provides clock SCK to synchronize the data transfer, and the signals SIMO and SOMI are for the data bit stream. SPI master can be a 3-wire or 4-wire SPI master, depending on if the master drives the $\overline{SS}$ signal. If the master is a 3-wire SPI master, the master does not drive $\overline{SS}$. Otherwise, the 4-wire SPI master pulls $\overline{SS}$ Low when transferring data. If the master is a 3-wire SPI master, the $\overline{SS}$ pin at the slave can be tied Low in the single master/slave pair or connected to the GPIO output of the master in the multiple slaves system.

| Signal Name (SLAC MPI Pin Name) | Type | Description |
|---|---|---|
| SCK (DCLK) | I | SPI clock |
| SIMO (DIN) | I | SPI slave input/master output |
| SOMI (DOUT) | O | SPI slave output/master input |
| $\overline{SS}$ ($\overline{CS}$) | I | SPI Slave select low |

**Table 15 - SPI Signals**

The NGCC SLAC device will be the SPI slave, and the external host will be the SPI master. Signal SIMO will connect to the DIN pin and signal SOMI will connect to the DOUT pin of the NGCC SLAC device. NGCC SLAC devices sample the input signal DIN on the rising edge of the clock and change the output signal DOUT on the falling edge of the clock.

Figure 21 shows the SPI interface system with a 4-wire SPI master. TI DSPs and Motorola 68HC12s have a 4-wire SPI master. For example, TI TMS320F28x chips can set the chip as the master (SPICTL[2]=1), 8-bit (SPICCR[3:0]=7) transfer with clock polarity (SPICCR[6]=1 falling), clock phase (CPICTL[3]=0 no delay) or with SPICCR[6]=0 (rising), CPICTL[3]=1 (delay) to connect to the NGCC SLAC device. Figure 22 shows the SPI interface system with a 3-wire SPI master. Most Motorola DSP/controllers, except 68HC12 and ADI DSP, have 3-wire SPI masters. For example, Motorola 68HC05Cx SPCR register can set the Clock Phase (CPHA=0) with the clock polarity (CPOL=0) or CPHA=1 with CPOL=1 to interface with the NGCC SLAC device. One of the GPIO pins is needed to drive the $\overline{SS}$ pin of the NGCC SLAC device. As the NGCC SLAC device supports command framing on the $\overline{SS}$ pin, the GPIO pin of the master connecting to the $\overline{SS}$ pin of the slave is required, as shown in Figure 22.

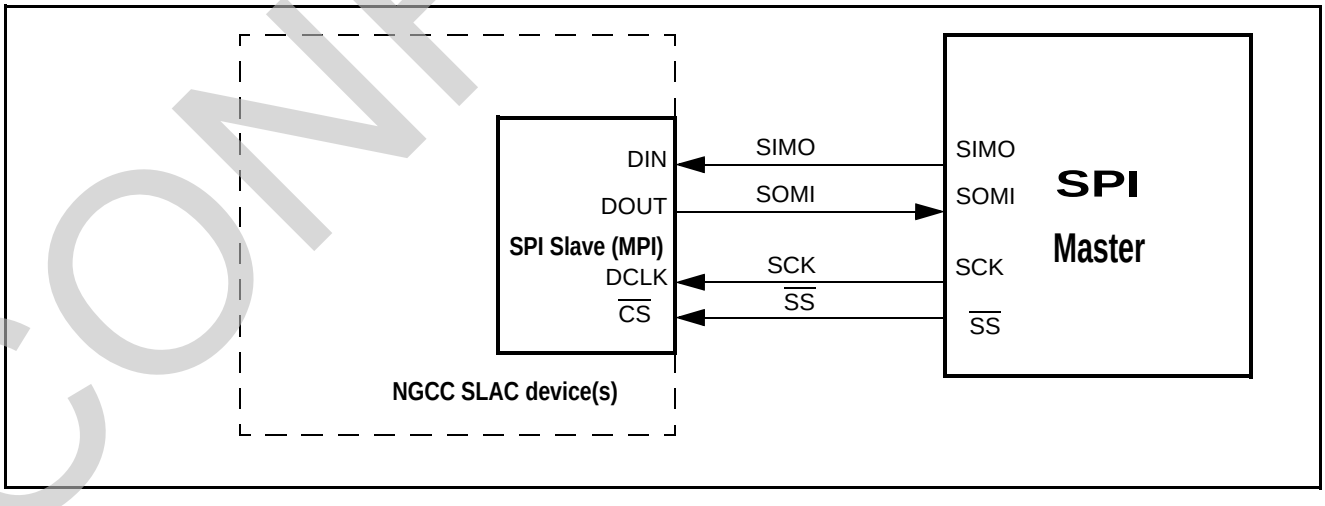



**Figure 21 - 4-wire Master-Slave Connections**

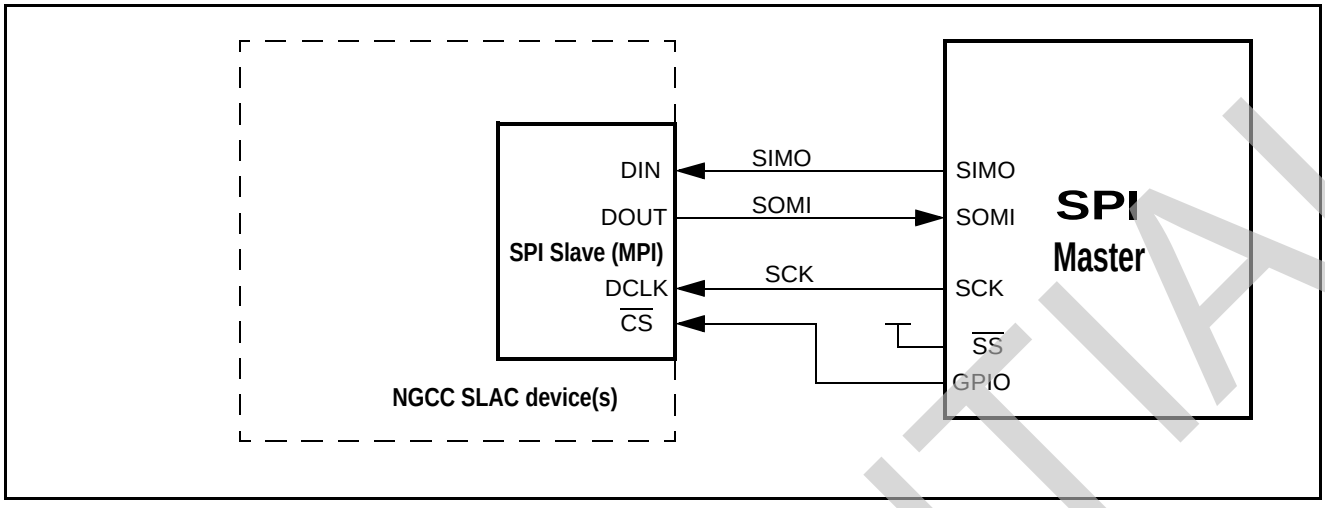



**Figure 22 - 3-wire Master-Slave Connections**

### 9.4.1.2 MPI Features

In order to connect to different SPI masters, the MPI of the NGCC SLAC device has the following designs:

- Separate input and output pins.
- No daisy chain support.
- No read latency: no latency between the read command word and the first data word.
- $\overline{CS}$ pin supports byte/word framing, and command framing mode, as shown in Figure 23. The SPI slave state machine will reset if $\overline{CS}$ returns to High when the number of active DCLK pulses is not equal to 8 or 16. If there is no clock, $\overline{CS}$ has to be Low for more than 125 ns to be recognized to reset SPI slave state machine. In command framing mode, the transition of $\overline{CS}$ to High means the command has ended. This event resets the SPI slave state machine, and the next falling edge of $\overline{CS}$ starts a new command.

Figure 23 shows three kinds of framing modes based on the behavior of $\overline{CS}$. In byte/word framing mode, $\overline{CS}$ is Low for 8/16 SCK clocks. For a two-word command, $\overline{CS}$ needs to toggle 4/2 times to complete the command transfer. In command framing mode, $\overline{CS}$ is Low for the whole duration of the command transfer. When the command is finished, $\overline{CS}$ will go back to High. If $\overline{CS}$ Low lasts shorter than the expected command length, the command is aborted and the SPI slave state machine resets. However if the user pulls $\overline{CS}$ Low longer than the expected command length, the extra words will start a new command sequence. In both byte/word framing mode and command framing mode, DCLK can be free-running or absent when $\overline{CS}$ is inactive High.

Every time $\overline{CS}$ returns to High and the number of active DCLK pulses is not equal to 8 or 16, the SPI slave state machine will reset. The next $\overline{CS}$ Low starts a new command sequence. In command framing mode, the transition back to High means the end of the command. If $\overline{CS}$ Low lasts less than 16 SCK clock cycles, no command byte is processed. If $\overline{CS}$ Low lasts more than 16 clock cycles, each 16-clock cycles triggers the SPI slave to process the word until $\overline{CS}$ returns back to High. The SPI slave will not reset state machine when $\overline{CS}$ Low lasts exactly 8 or 16 SCK clock cycles to support byte/word framing mode. In byte/word framing mode, the user has to be aware of the command length, as there is no indication of command boundary.

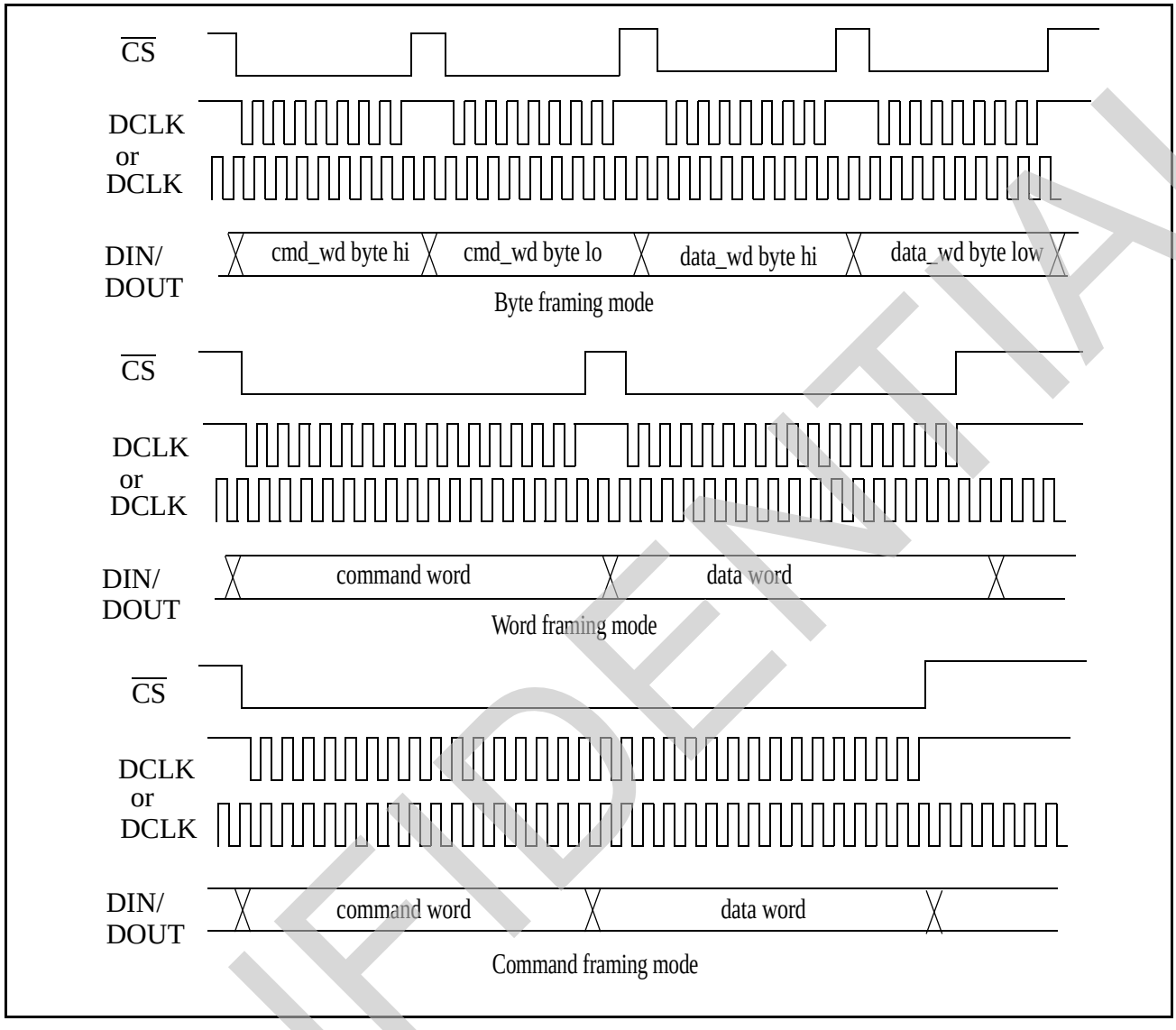



**Figure 23 - $\overline{CS}$ Framing Modes**

The timing requirements for read and write accesses are shown in the following timing diagrams. The single data word read and write command is shown in Figure 24 and Figure 25.

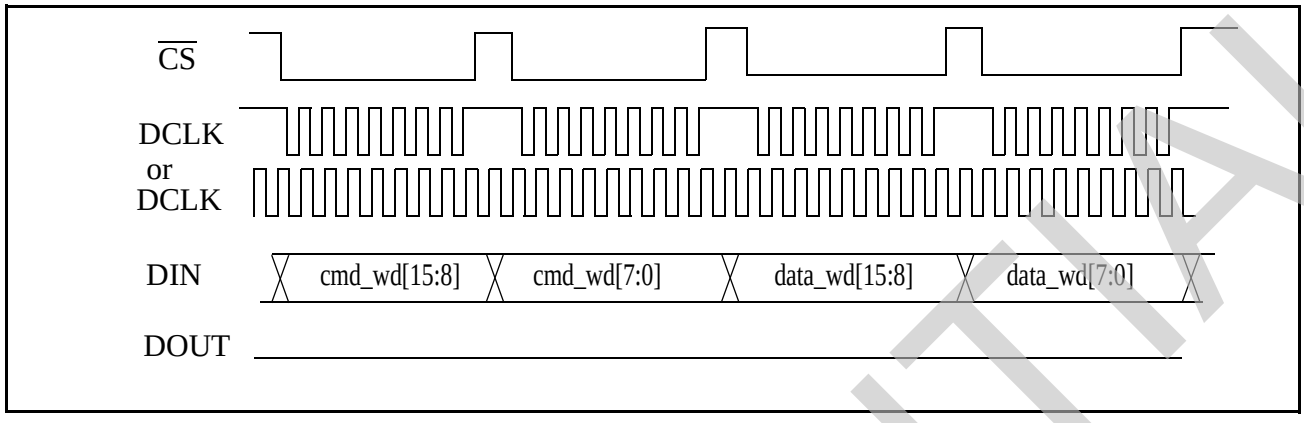



**Figure 24 - One Data Word Write in Byte Framing Mode**

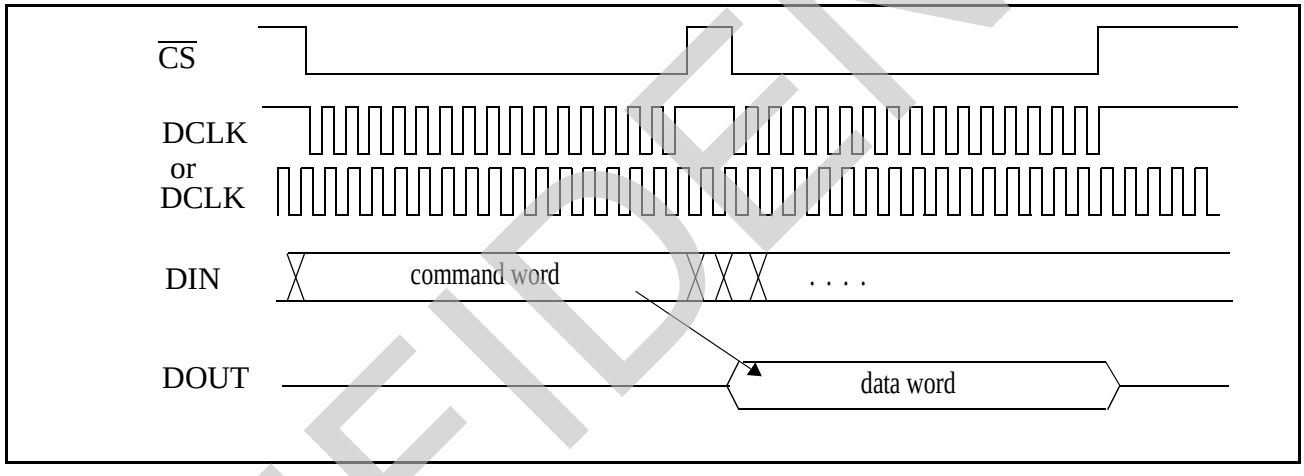



**Figure 25 - One Data Word Read in Word Framing Mode**

### 9.4.1.3 MPI Timing Specifications

Min and max values are valid for all digital outputs with a 150 pF load. Pictorial definitions for these parameters can be found in Figure 26 and Figure 27.

| Timing Diagram No. | Symbol | Parameter | Min | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| 1 | $t_{DCY}$ | Data clock period | 122 | — | — | | |
| 2 | $t_{DCH}$ | Data clock HIGH pulse width | 30 | — | — | | 1 |
| 3 | $t_{DCL}$ | Data clock LOW pulse width | 48 | — | — | | 1 |
| 4 | $t_{DCR}$ | Rise time of clock | — | — | 25 | | |
| 5 | $t_{DCF}$ | Fall time of clock | — | — | 25 | | |
| 6 | $t_{ICSS}$ | Chip select setup time, Input mode | 30 | — | $t_{DCY}$–10 | | |
| 7 | $t_{ICSH}$ | Chip select hold time, Input mode | 0 | — | $t_{DCY}$–20 | | |
| 8 | $t_{ICSL}$ | Chip select pulse width, Input mode | — | $8t_{DCY}$ | — | | |
| 9 | $t_{ICSO}$ | Chip select off time, Input mode | $t_{DCY}$ | — | — | | 1 |
| 10 | $t_{IDS}$ | Input data setup time | 25 | — | $t_{DCY}$–10 | ns | |
| 11 | $t_{IDH}$ | Input data hold time | 30 | — | $t_{DCY}$–10 | | |
| 13 | $t_{OCSS}$ | Chip select setup time, Output mode | 30 | — | $t_{DCY}$–10 | | |
| 14 | $t_{OCSH}$ | Chip select hold time, Output mode | 0 | — | $t_{DCH}$–20 | | |
| 15 | $t_{OCSL}$ | Chip select pulse width, Output mode | — | $8t_{DCY}$ | — | | |
| 16 | $t_{OCSO}$ | Chip select off time, Output Mode | $t_{DCY}$ | — | — | | 1 |
| 17 | $t_{ODD}$ | Output data turn on delay | — | — | 35 | | 2 |
| 18 | $t_{ODH}$ | Output data hold time | 3 | — | — | | |
| 19 | $t_{ODOF}$ | Output data turn off delay | 0 | — | 35 | | |
| 20 | $t_{ODC}$ | Output data valid | 3 | — | 35 | | |

**Table 16 - MPI Specifications**

Note 1: DCLK may be stopped in the High or Low state indefinitely without loss of information.

Note 2: The first data bit is enabled on the falling edge of $\overline{CS}$ or on the falling edge of DCLK, whichever occurs last.

#### 9.4.1.4 Timing Diagrams

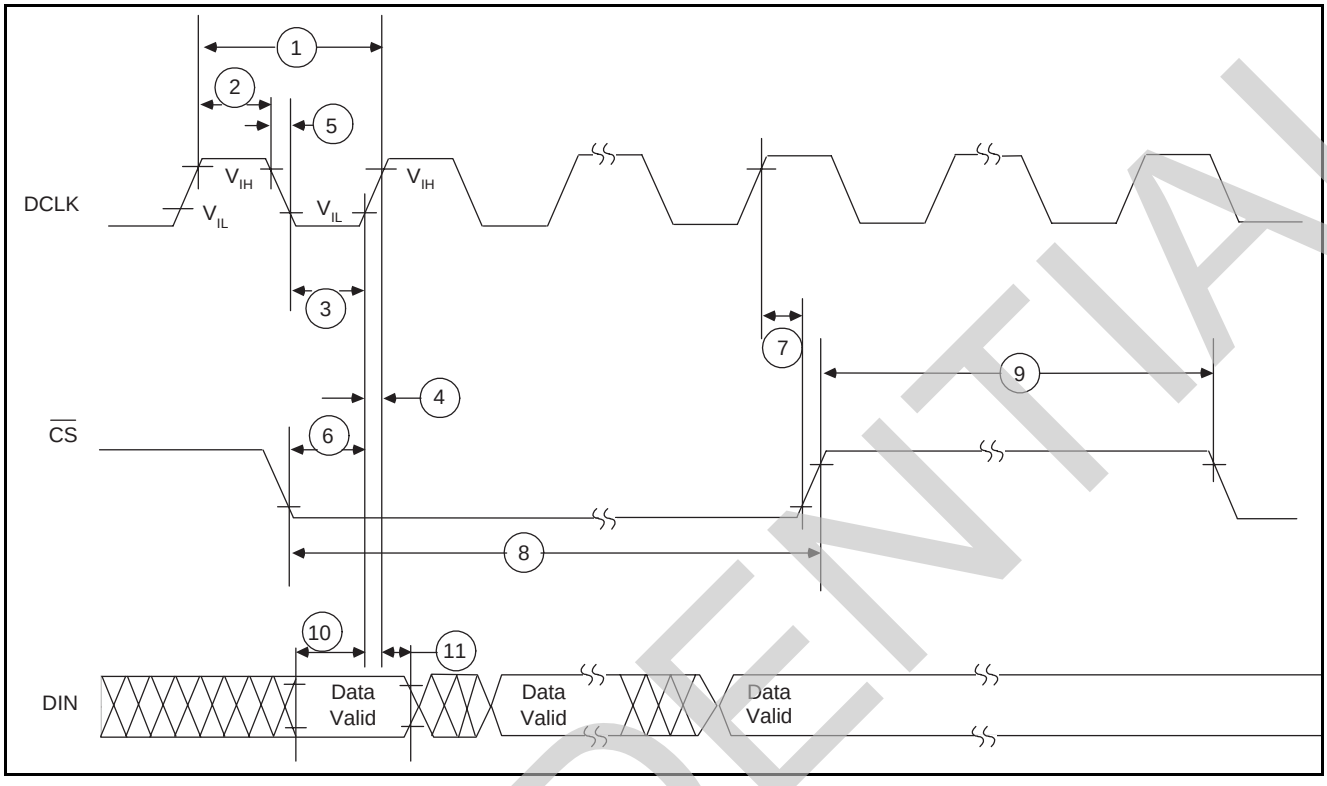



**Figure 26 - Microprocessor Interface (Input Mode)**

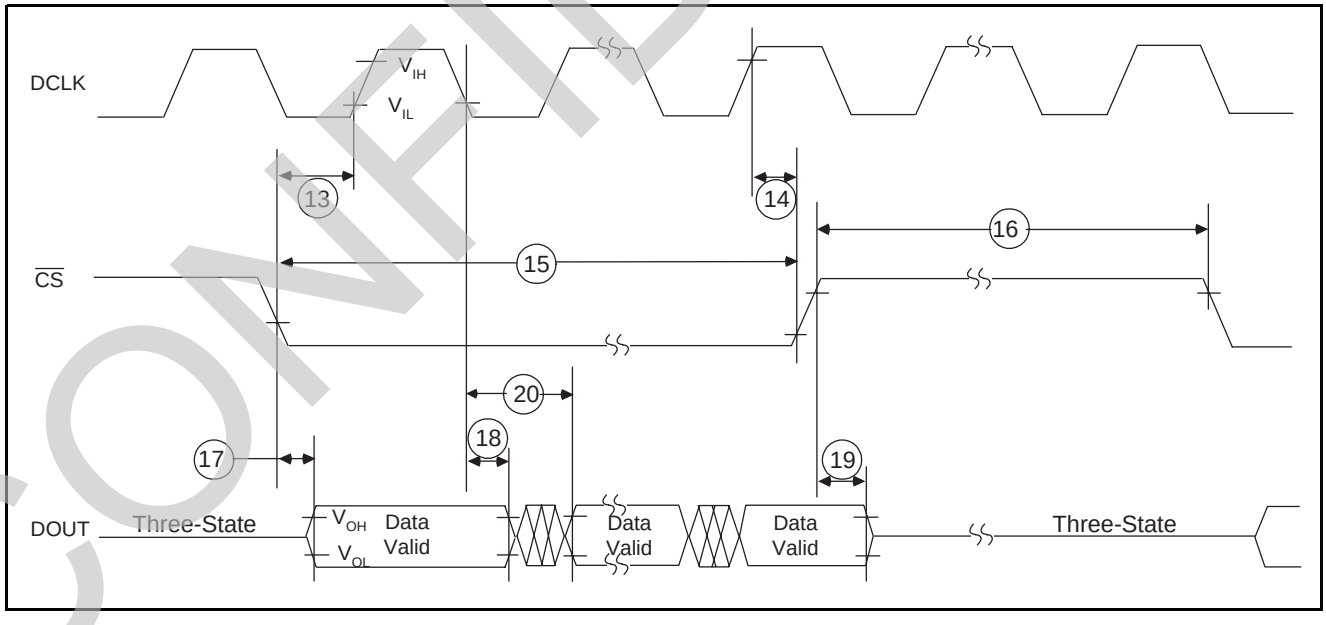



**Figure 27 - Microprocessor Interface (Output Mode)**

## 10.0 PCM Highway

PCM interface features:

- The PCM interface supports two transmit and receive PCM highways (A & B) using shared PCLK and FS timing references.
- The following PCLK (or highway) rates are supported for narrowband or wideband modes: 1.536 MHz, 2.048 MHz, 3.072 MHz, 4.096 MHz, 6.144 MHz, and 8.192 MHz (default). For narrowband mode, the following PCLK rates are also supported: 1.544 MHz, 3.088 MHz, and 6.176 MHz. A valid PCLK is required for overall device operation. These clock frequencies mean that 24 to 128 timeslots of 8 bits per highway are possible in one frame of data. The timeslots are user programmable but are common for both highway channels. The transmit data can be sent out either highway A or highway B or both highways simultaneously (which is programmable on a per channel basis).
- An 8-kHz frame sync signal indicating the beginning of a transmit/receive frame shall be supplied by the system and all timeslots shall be referenced to it.
- The PCM interface can transmit/receive 8-bit compressed (A-law/µ-law) or 16-bit linear data with 8 kHz sampling (narrowband), or 16-bit linear data with 16 kHz sampling (wideband). Each time slot can carry one A-law or µ-law PCM voice channel. Two timeslots are required to carry 16-bit linear data. In wideband mode, two evenly spaced sets of 16-bit timeslots are exchanged in each frame. The user programs the first timeslot and the second set is generated automatically and placed 125/2 µS from the first timeslot (all wideband supported PCLK frequencies exhibit an even number of timeslots). When programming transmit and receive timeslots for wideband mode, the programmed timeslot must occur during the first 62.5 µS of the frame.
- Data can be transmitted on the positive or negative edge of PCLK. Receive data is always evaluated on the negative edge of PCLK.
- To avoid timing and clock skew problems, the PCM interface has a clock slot feature that allows the transmit and receive data to be independently offset from the zero timeslot defined in relation to the frame sync signal applied. The clock slot permits 0-7 PCLK cycles of delay from the position defined by the applied frame synchronization signal.

| Pin Name | Type | Reset | Description |
|---|---|---|---|
| DXA | O | Z | Primary downstream serial data output |
| DXB | O | Z | Secondary downstream serial data output |
| $\overline{\text{TSCA}}$ | O | Z | Primary timeslot control signal (active low - open drain) |
| $\overline{\text{TSCB}}$ | O | Z | Secondary timeslot control signal (active low - open drain) |
| DRA | I | | Primary upstream serial data input |
| DRB | I | | Secondary upstream serial data input |
| PCLK | I | | 1.536 MHz - 8.192 MHz PCM Interface clock |
| FS | I | | 8-kHz frame sync |

**Table 17 - PCM Interface Pins**

### 10.1 PCM Transmit Interface

The PCM transmit interface controls the transmission of data onto the PCM highway through the output port selection circuitry and the time and clock slot control block. The timeslot control signals ($\overline{\text{TSCA}}$/$\overline{\text{TSCB}}$) go low whenever PCM data is transmitted on the DXA/DXB pin. These signals can be used for arbitration when there are multiple devices connected to the PCM bus. The data can be transmitted on either edge of PCLK. The clock edge at which the data is transmitted is selected by the XE bit in the PCM Configuration Register. The data is transmitted with the most significant bit first.

The Frame Sync (FS) pulse identifies timeslot 0 of the transmit frame and all timeslots are referenced to it.

### 10.2 PCM Receive Interface

The PCM Receive interface logic controls the reception of the data bytes from the PCM highway. Each timeslot is associated with one 8-bit data byte. The data is received with the most significant bit first. The received data coming on the DR pin is latched at the falling edge of PCLK.

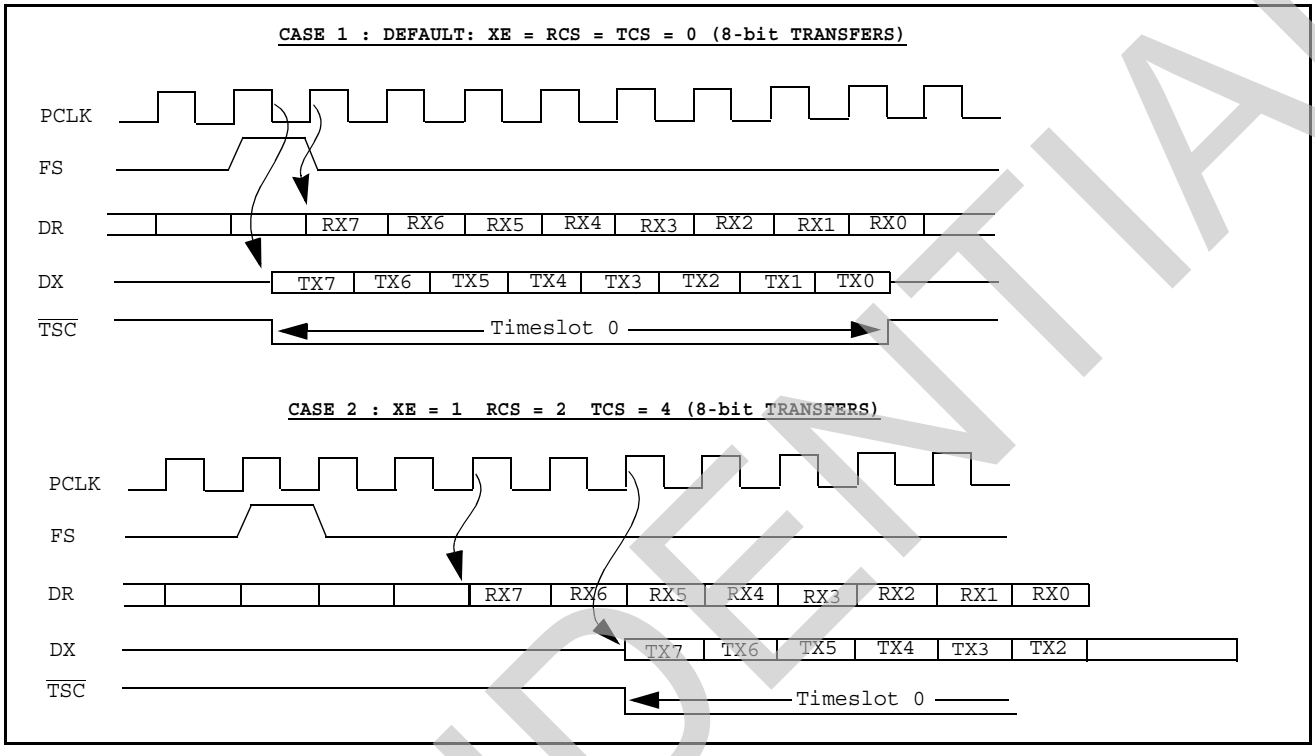



**Figure 28 - PCM Highway 8-bit Transfers**

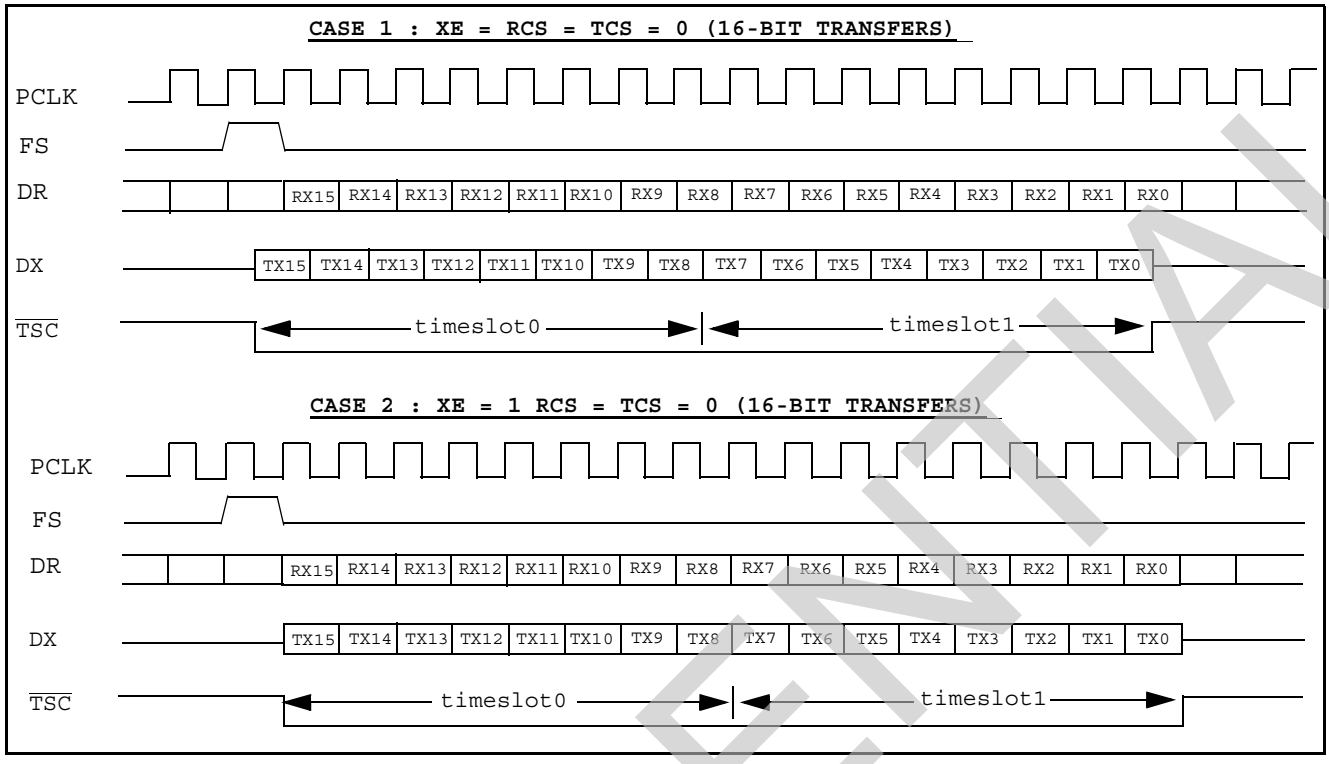



**Figure 29 - PCM Highway 16-bit Transfers**

## 10.3 PCM Interface Timing

Min and max values are valid for all digital outputs with a 150 pF load. Pictorial definitions for these parameters can be found in Figure 30 and Figure 31. PCLK accuracy = ± 100 PPM.

| Timing Diagram No. | Symbol | Parameter | Min. | Typ | Max | Unit | Note |
|---|---|---|---|---|---|---|---|
| 22 | $t_{PCY}$ | PCM clock period | 122 | — | 651 | ns | 1 |
| 23 | $t_{PCH}$ | PCM clock HIGH pulse width | 48 | — | — | | |
| 24 | $t_{PCL}$ | PCM clock LOW pulse width | 48 | — | — | | |
| 25 | $t_{PCF}$ | Fall time of clock | — | — | 8 | | |
| 26 | $t_{PCR}$ | Rise time of clock | — | — | 8 | | |
| 27 | $t_{FSS}$ | FS setup time | 30 | — | $t_{PCY}$–30 | | |
| 28 | $t_{FSH}$ | FS hold time | 50 | — | 125000-3$t_{PCY}$--30 | | |
| 29 | $t_{TSD}$ | Delay to $\overline{TSCX}$ valid | 5 | — | 25 | | 2 |
| 30 | $t_{TSO}$ | Delay to $\overline{TSCX}$ off | 0 | — | 10 | | 3 |
| 31 | $t_{DXD}$ | PCM data output delay | 5 | — | 25 | | |
| 32 | $t_{DXH}$ | PCM data output hold time | 5 | — | 25 | | |
| 33 | $t_{DXZ}$ | PCM data output delay to high-Z | 0 | — | 10 | | 3 |
| 34 | $t_{DRS}$ | PCM data input setup time | 15 | — | $t_{PCY}$–10 | | |
| 35 | $t_{DRH}$ | PCM data input hold time | 5 | — | $t_{PCY}$–20 | | |
| | $t_{FST}$ | Narrowband PCLK or frame sync jitter time | –60 | — | 60 | | |
| | | Wideband PCLK or frame sync jitter time | –30 | — | 30 | | |

**Table 18 - PCM Specifications**

***Note:***

1. *Supported PCM clock (PCLK) frequencies are listed in "PCM Highway" on page 50.*
2. *$\overline{TSCX}$ is delayed from FS by a typical value of* N • $t_{PCY}$*, where N is the value stored in the time/clock slot register.*
3. *$\overline{TSCX}$ is an open drain driver. The $t_{TSO}$ is defined as the delay time the output driver turns off after the PCLK transaction. The actual delay time is dependent on the load circuitry. The maximum load capacitance on $\overline{TSCX}$ is 150 pF and the minimum pull-up resistance is 360 Ω.*

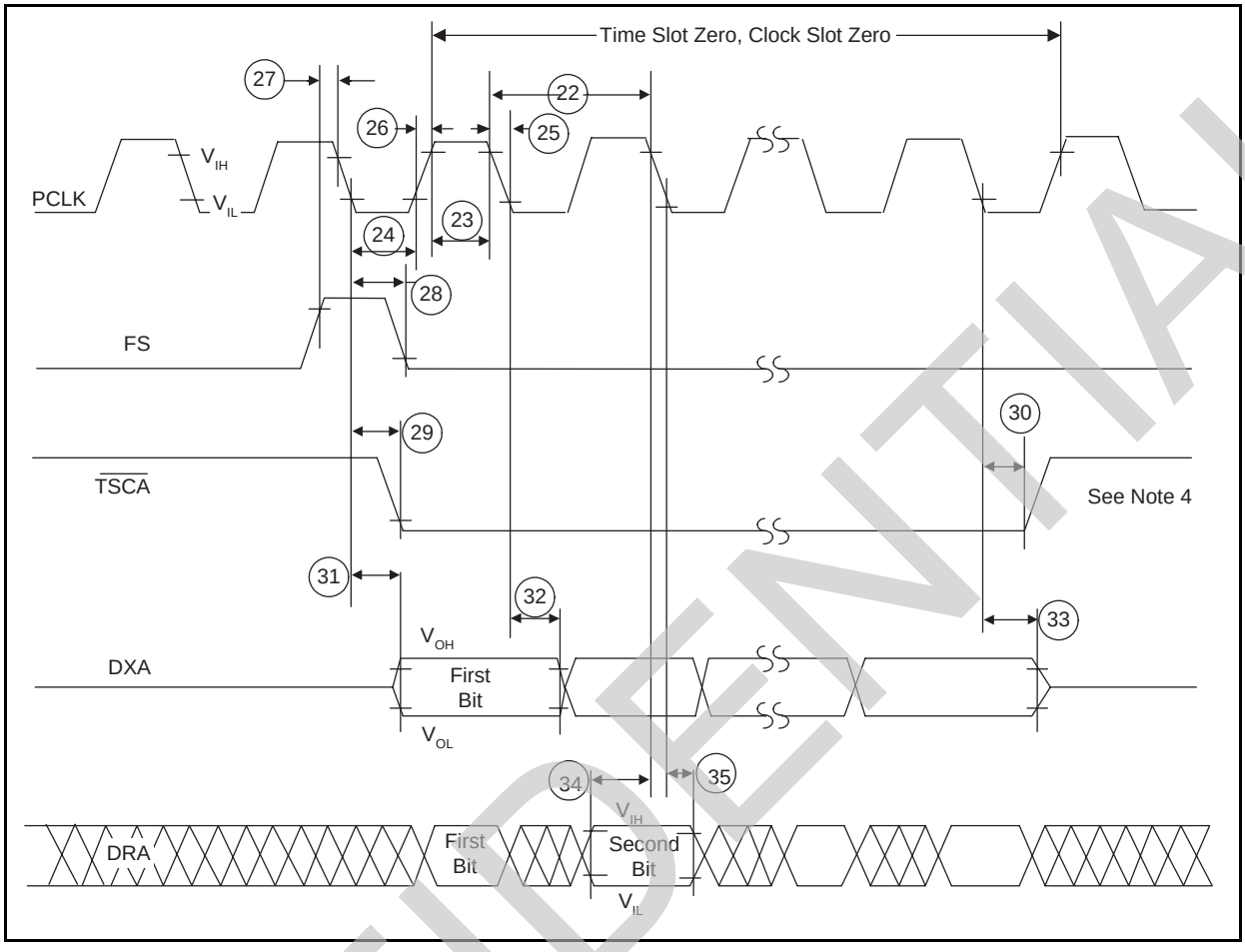



**Figure 30 - PCM Highway Timing for XE = 0 (Transmit on Negative PCLK Edge)**

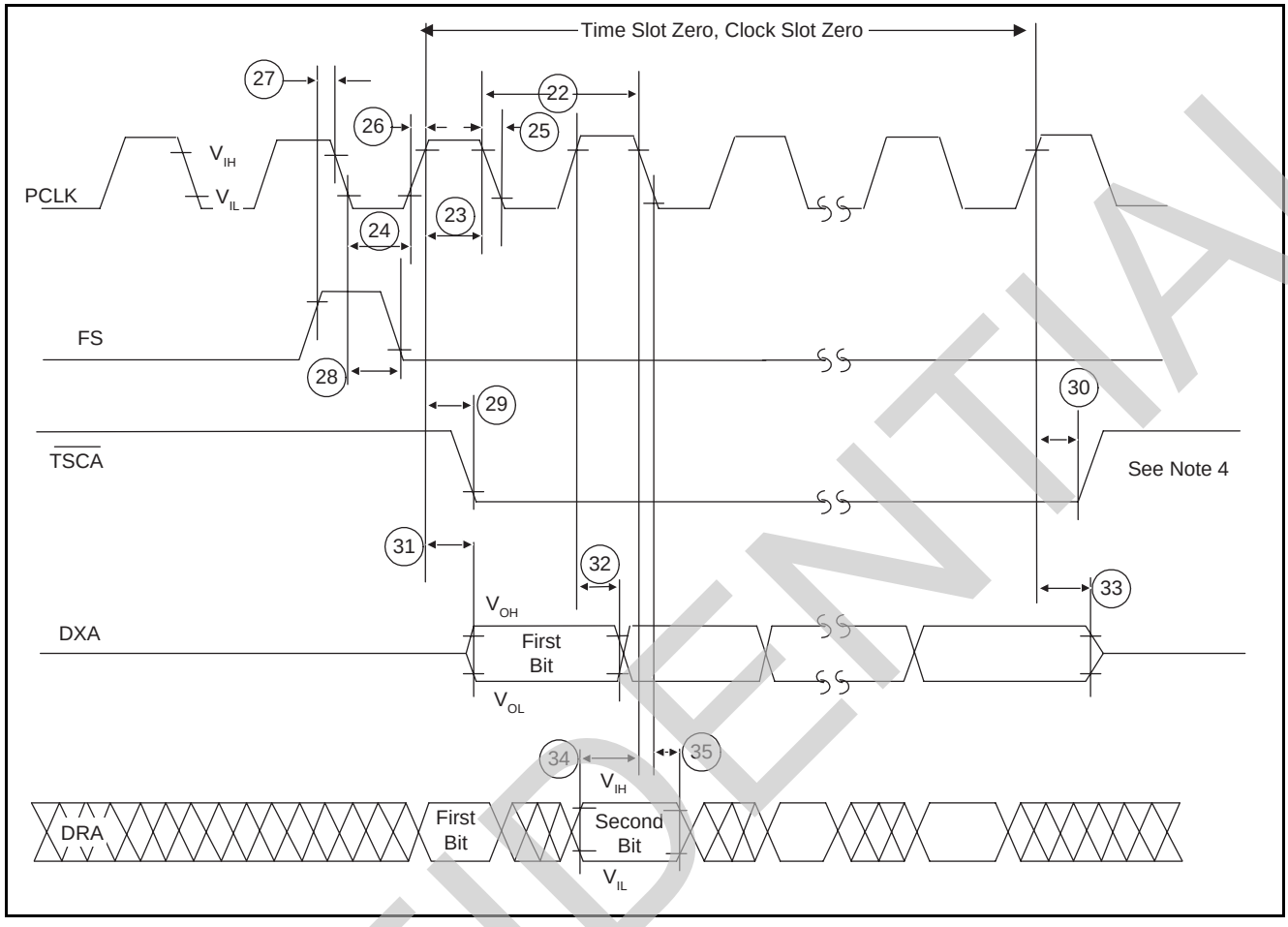



**Figure 31 - PCM Highway Timing for XE = 1 (Transmit on Positive PCLK Edge)**

## 11.0 P-Bus and GPIO Interfaces

The SLAC utilizes a digital control bus (P-Bus) to send control signals to SLIC devices. The P-Bus interface uses a 4 bit parallel bus (SEL, P[2:0]) and eight individual load or chip select pins (LD[7:0]) to control the FXS state and Switch state of up to eight SLIC devices. The SEL signal determines whether the P[2:0] value is assigned to the FXS state (SEL=0) or the Switch state (SEL=1). The P[2:0] and SEL values are latched inside the SLIC on the rising edge of the active low LD[n] signal. The P-Bus operates continuously so that each channel's FXS and Switch states are automatically refreshed every 128 msec or whenever a SLIC mode changes.

Each channel is assigned two general purpose SLAC IO pins, IOn_0 and IOn_1. IOn_0 can be configured as either a CMOS input, a CMOS output, or an open drain 50 mA relay driver. IOn_1 can be configured as either a CMOS input or CMOS output.

| Pin Name | Type | State in Reset | Description | |
|---|---|---|---|---|
| P[2:0] | O | 0 | P-Bus for controlling SLIC FXS and SLIC Switch states. | |
| SEL | O | 0 | 0 = P-Bus defines SLIC FXS state.<br>1 = P-Bus defines SLIC Switch state. | |
| LD[7:0] | O | 1 | Active Low Load signal for FXS and Switch states.<br>The P[2:0] and SEL pin values are latched inside the SLIC on the rising edge of LD[n]. | |
| IO1_[1:0] | I/O | Input | SLAC Input/Output for Channel 1 | These pins change state on the rising edge of FS. |
| IO2_[1:0] | I/O | Input | SLAC Input/Output for Channel 2 | |
| IO3_[1:0] | I/O | Input | SLAC Input/Output for Channel 3 | |
| IO4_[1:0] | I/O | Input | SLAC Input/Output for Channel 4 | |
| IO5_[1:0] | I/O | Input | SLAC Input/Output for Channel 5 | |
| IO6_[1:0] | I/O | Input | SLAC Input/Output for Channel 6 | |
| IO7_[1:0] | I/O | Input | SLAC Input/Output for Channel 7 | |
| IO8_[1:0] | I/O | Input | SLAC Input/Output for Channel 8 | |

**Table 19 - P-Bus and SLAC IO Pins**

P-Bus timing is derived from an internal 49.152 MHz SLAC clock and the 8 kHz FS input. The clock is used to generate the timing for the P[2:0], SEL, and LD[n] signals for each channel. The 8 kHz FS timing reference is used to generate the 16 msec delay between channel loads (see Figure 32 and Figure 33).

When a command is written which initiates a change to an FXS or Switch state, the new value is written to the SLIC device within 500 µS.

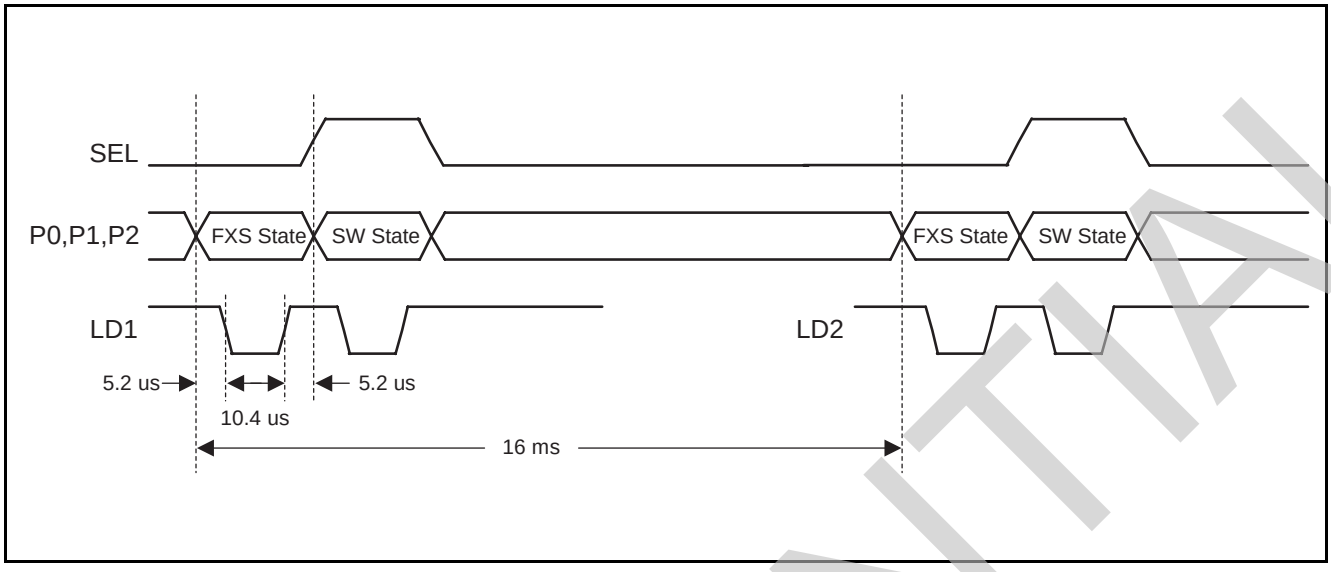



**Figure 32 - Channel Timing for P-Bus SLIC Interface**

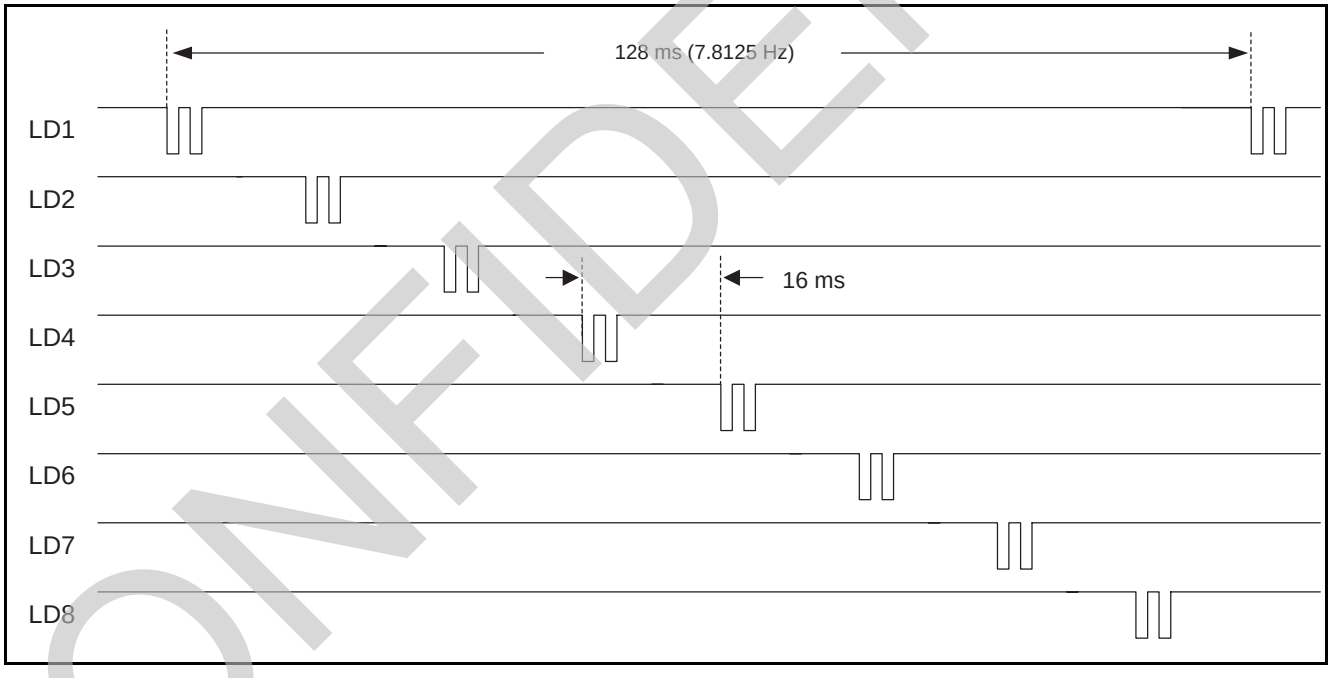



**Figure 33 - Global Timing for SLIC Device Bus Interface**

***Note:***

*An additional P-bus interaction will occur in no more than 625 µs following a drive state change request. Then, the affected LD line will return to its normal 128 ms refresh cycle.*

### 11.1 SLIC Device Bus Timing Specifications

Pictorial definitions for these parameters can be found in Figure 34.

| Timing Diagram No. | Symbol | Signal | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | $tr_{SLD}$ | LD[1:8] | Rise time | | | 2 | µs |
| 2 | $tf_{SLD}$ | LD[1:8] | Fall time | | | 2 | |
| 3 | $t_{SLDPW}$ | LD[1:8] | Pulse width | 3 | | | |
| 4 | $t_{SDXSU}$ | P0, P1, P2, SEL | Setup time | 2 | | | |
| 5 | $t_{SDXHD}$ | P0, P1, P2, SEL | Hold time | 2 | | | |
| 6 | $t_{SDXPW}$ | P0, P1, P2, SEL | Pulse width | 7 | | | |

**Table 20 - SLIC Device Bus Timing Specifications**

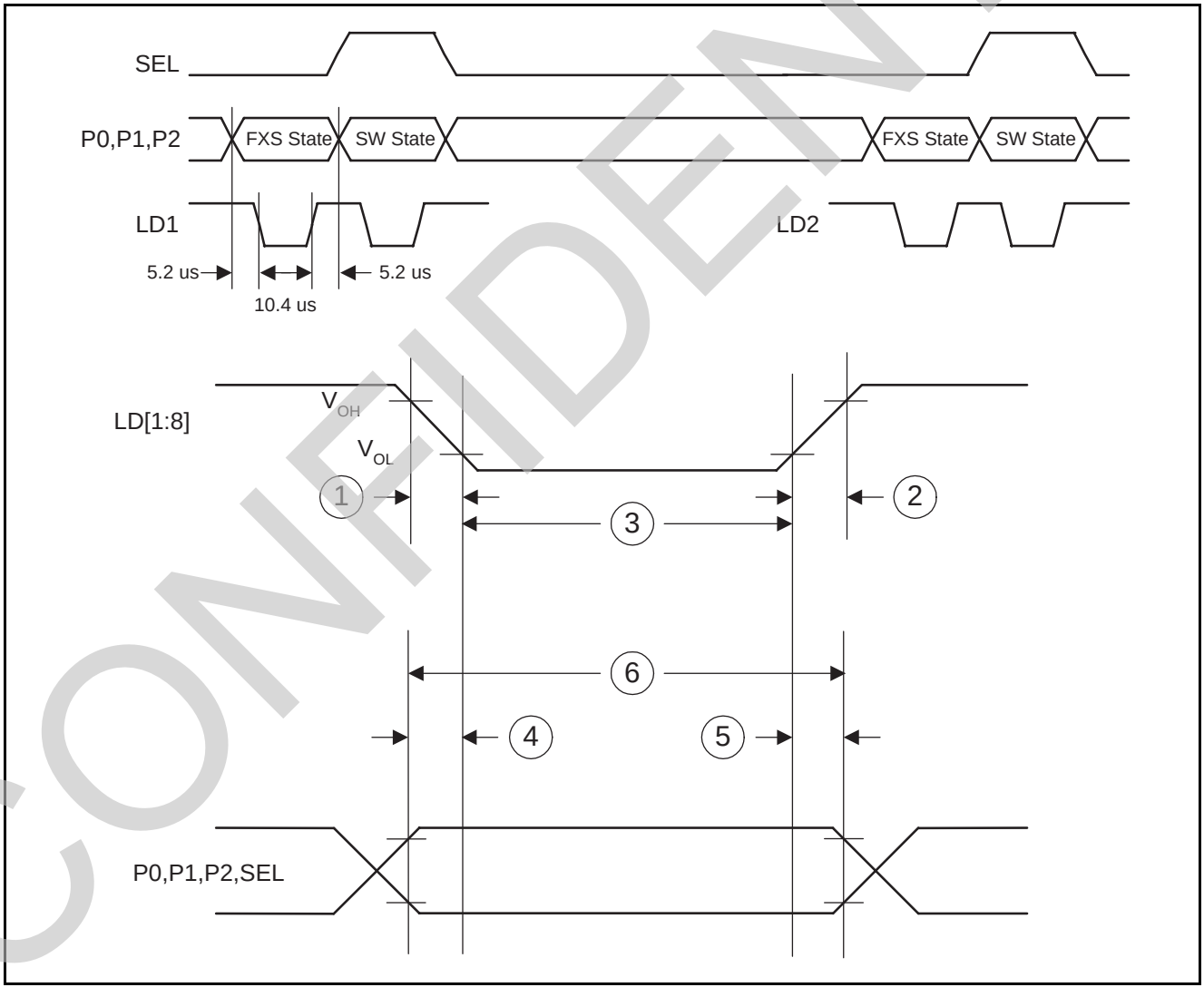



**Figure 34 - SLIC Device Bus Timing Waveform**

## 12.0 Relay Drivers

The IO[1:8]_0 pins can be programmed as open drain relay drivers. They are capable of sinking 50 mA of current @ 0.7 V.

Built-in integrated flyback diodes eliminate the need for external diodes across the relay coils.

The IO[1:8]_1 pins are capable of sinking 10 mA as an output. They can be used with an external transistor to drive a relay.

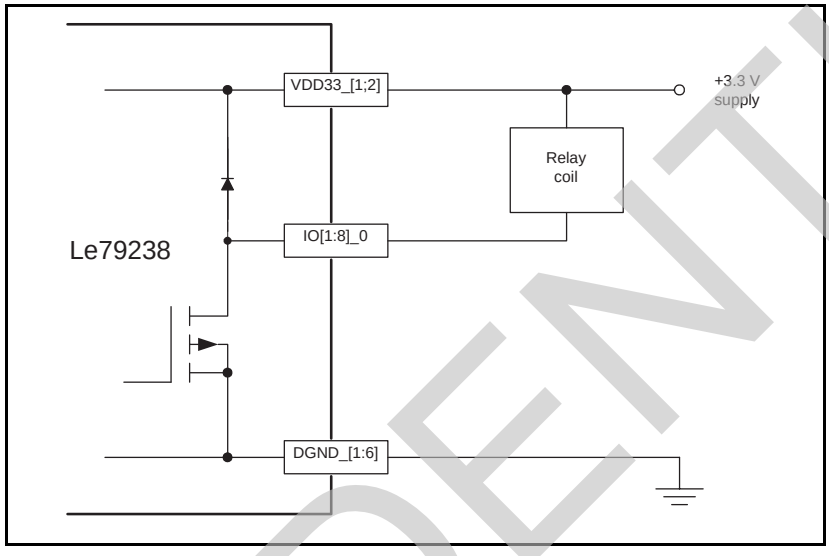
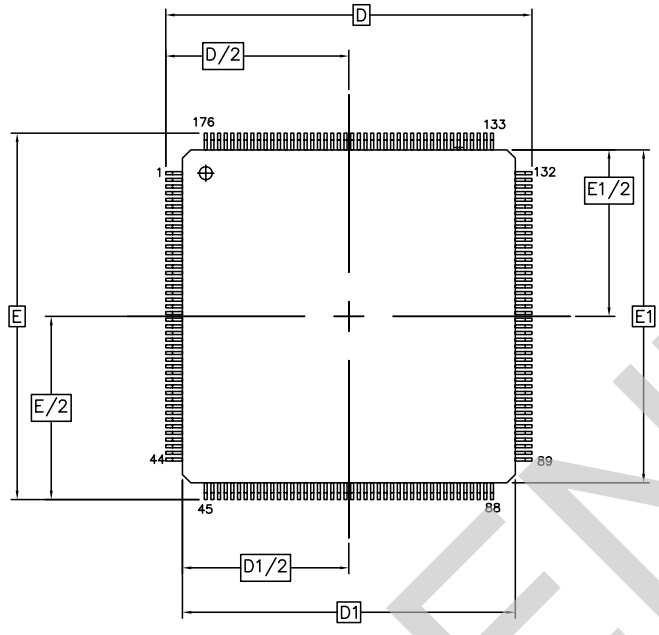
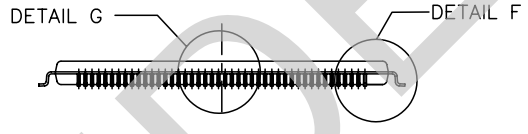



**Figure 35 - Open Drain Relay Drivers**

## 13.0 Physical Dimensions

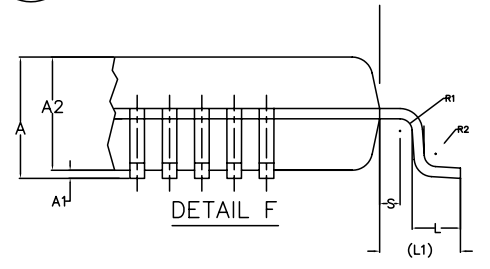
### 13.1 176-Pin LQFP

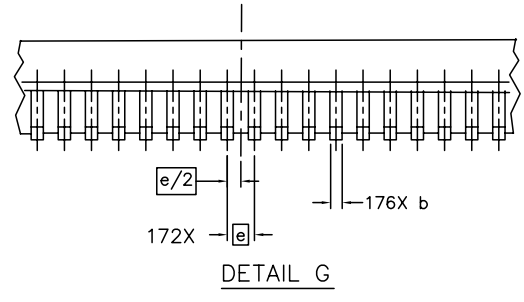



| DIM | MIN | NOM | MAX | DIM | MIN | NOM | MAX |
|---|---|---|---|---|---|---|---|
| A | ---- | | 1.6 | L1 | | 1 REF | |
| A1 | 0.05 | | 0.15 | R1 | 0.08 | | --- |
| A2 | 1.35 | 1.4 | 1.45 | R2 | 0.08 | | 0.2 |
| b | 0.13 | 0.18 | 0.23 | S | 0.2 | | --- |
| b1 | 0.13 | 0.16 | 0.19 | | | | |
| c | 0.09 | | 0.2 | | | | |
| c1 | 0.09 | | 0.16 | | | | |
| D | 22 BSC | | | | | | |
| D1 | 20 BSC | | | | | | |
| e | 0.4 BSC | | | | | | |
| E | 22 BSC | | | | | | |
| E1 | 20 BSC | | | | | | |
| L | 0.45 | 0.6 | 0.75 | | | | |

NOTE:
ALL DIMENSION IN MM, ANGLES IN DEGREES
DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M 1994

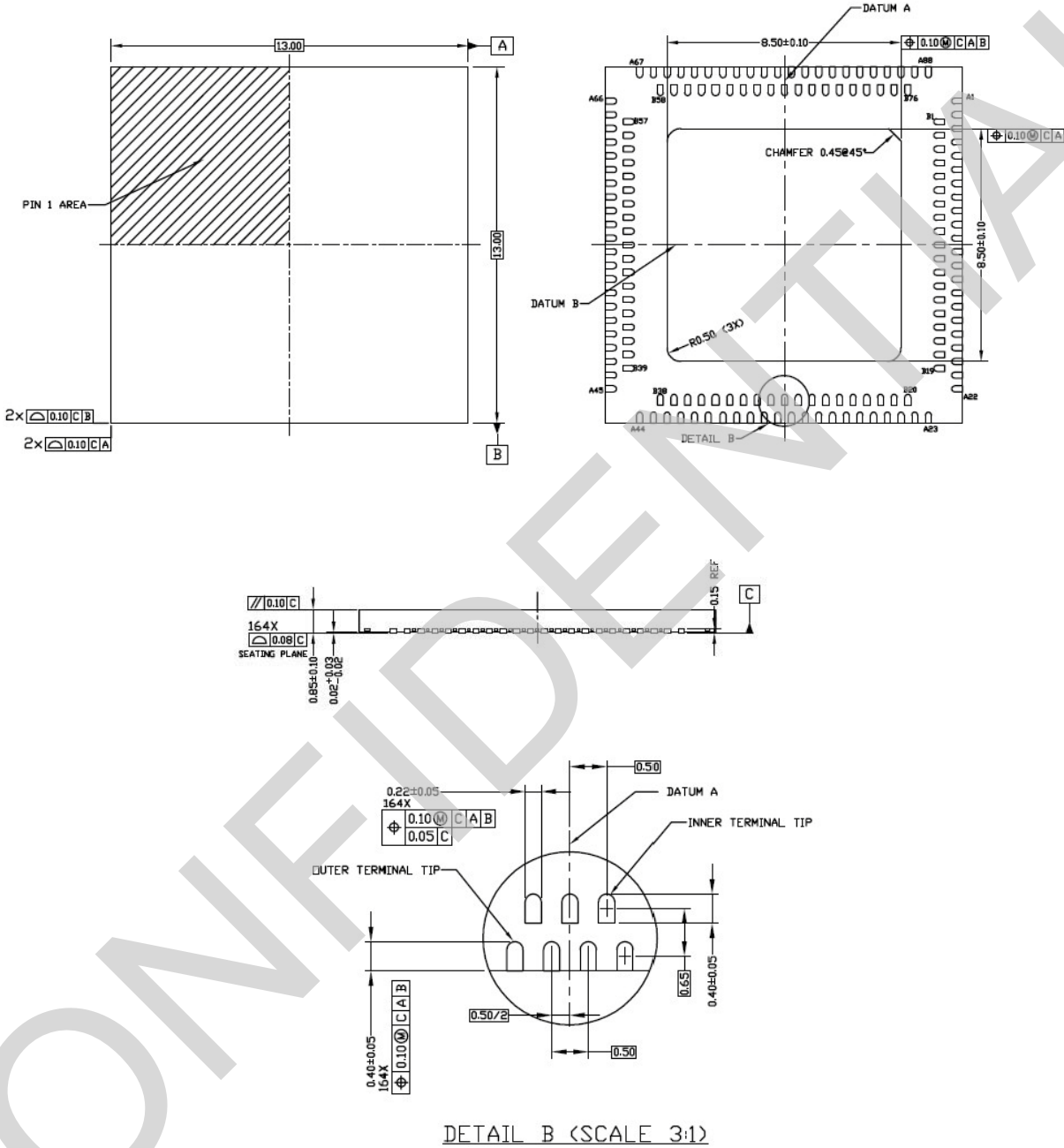



Note: Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

## 13.2 164-Pin LGA

See 4.1, “Green Package Assembly“ for additional information on this package.



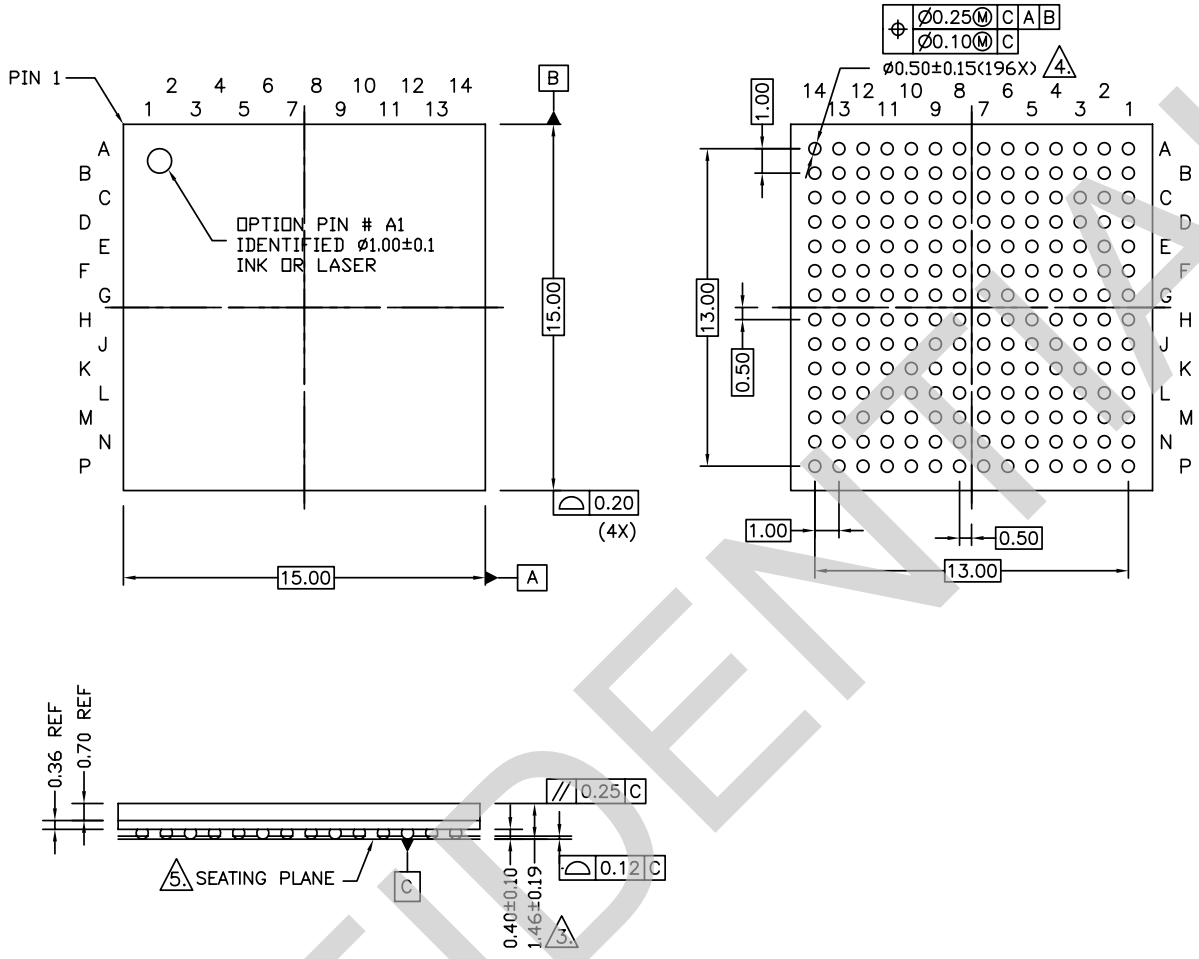

DETAIL B (SCALE 3:1)

NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5–1994
   ALL DIMENSIONS ARE IN MILLIMETERS ° IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

Note: Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

### 13.3 196-Pin BGA




NOTES :

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
2. SOLDER BALL POSITION DESIGNATION PER JESD 95–1, SPP–010.
3. THIS DIMENSION INCLUDES STAND–OFF HEIGHT, PACKAGE BODY THICKNESS AND LID HEIGHT, BUT DOES NOT INCLUDE ATTACHED FEATURES, E.G., EXTERNAL HEATSINK OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AN ATTACHED FEATURE.
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
5. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. ALL DIMENSIONS ARE IN MILLIMETERS.

Note: Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings will vary with the mold tool used in manufacturing.

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