Le87402

Datasheet

PLC Dual Channel Line Driver BD870 Series

May 2018

Microsemi

Power Matters.™

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 8.0

Revision 8.0 was published in May 2018. The format of this document was updated to the latest template.

1.2 Revision 7.0

Revision 7.0 was published in November 2015. The following is a summary of changes done in revision 7.0 of this document.

- Added package thermal information in Electrical Specifications (see page 8).
- Content in Class GH Operation (see page 5) is re-written for clarity.

1.3 Revision 6.0

Revision 6.0 was published in February 2014. The following is a summary of changes done in revision 6.0 of this document.

- Edited the figure, 28-pin QFN Physical Dimensions (see page 15) to show all information.
- Title of Figure 2 (see page 6) is corrected to read GH operation.

1.4 Revision 5.0

Revision 5.0 was published in November 2013. The following is a summary of changes done in revision 5.0 of this document.

- Updated RoHS statement in the section, Ordering Information (see page 19).
- Usable VS supply voltage range is increased in Operating Ranges (see page 9).
- Defined R_{REF} in the section, ELectrical Specifications (see page 8).
- Added a new section, Internal Reference Current (see page 17).

1.5 Revision 4.0

Revision 4.0 was published in June 2013. The following is a summary of changes done in revision 4.0 of this document.

- Updated the section, Class GH Operation (see page 5).
- Updated the table, Pin Descriptions (see page 14).
- Added the section, Performance Characteristics (see page 10).

1.6 Revision 3.0

Revision 3.0 was published in April 2013. Tape and Reel diagram is added in, 28-pin QFN Physical Dimensions (see page 15).

1.7 Revision 2.0

Revision 2.0 was published in January 2013. The following is a summary of changes done in revision 2.0 of this document.

- Changed descriptions of Class H to Class GH operations in Product Overview (see page 3).
- Updated the Le87402 Block Diagram (see page 3).
- Edited the table, Operating Ranges (see page 9).
- Updated the figure, Basic Test Circuit (see page 10).
- Updated figure, Typical Application Circuit - Channel A/B (see page 18).
- Added descriptions of GH Operations (see page 5).

1.8 Revision 1.0

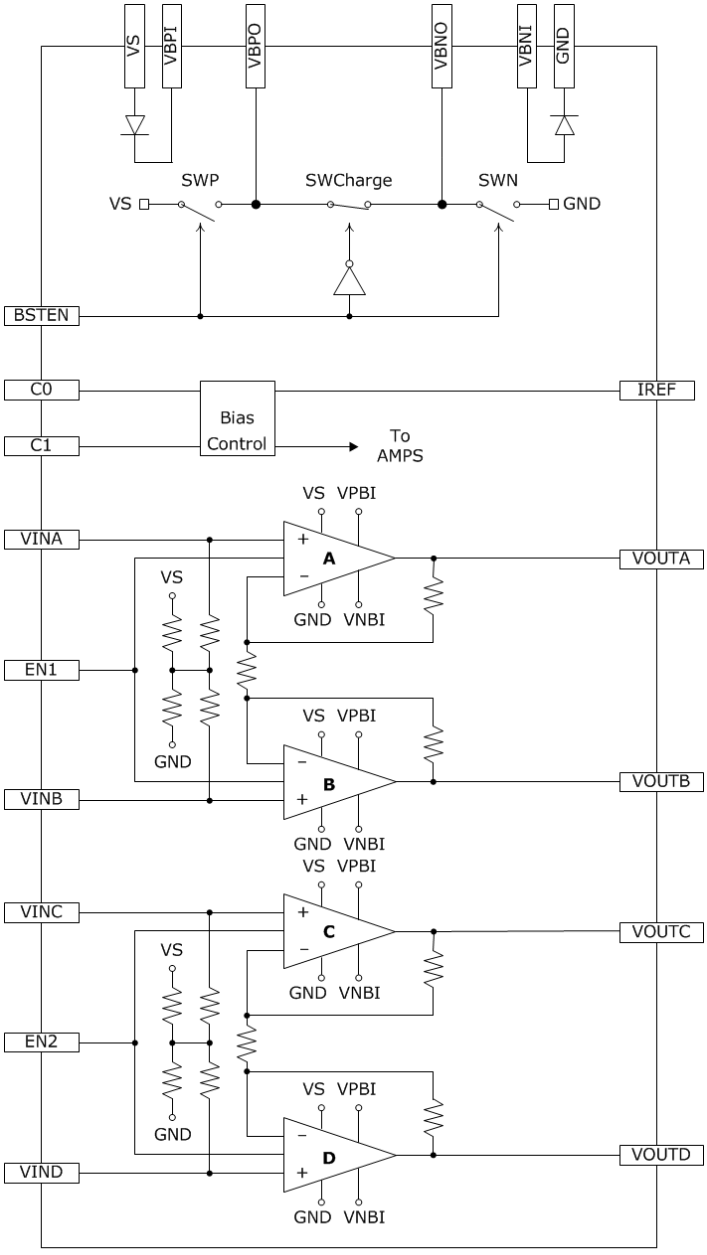
Revision 1.0 was published in November 2013. It was the first publication of this document.

2 Product Overview

Le87402 is a dual-channel line driver designed to work in home plug alliance HPAV2 systems, G.HN and MOCA. Each channel can be enabled independently; allowing multiple-in, multiple-out (MIMO) or single-in, single-out (SISO) operations. The Le87402 can drive a line impedance of 100 Ω down to 12 Ω through a proper transformer and delivers superior performance with power efficiency using Class GH operation.

The following figure shows the block diagram of Le87402

Figure 1 • Le87402 Block Diagram



2.1 Features

Le87402 has the following important features.

- Designed for HPAV2 standard
- MIMO or SISO operation
- Dual channel architecture
- 28-pin, 4 × 5 mm QFN package
- Low power operation
- Class GH operation
- Supports HPAV2 power save mode
- Independent channel enable/disable control
- Capable of driving line impedance between 12 Ω to 100 Ω
- Operations to 86 MHz
- 10 V to 12 V operation

2.2 Applications

The following applications use Le87402.

- Power line communications
- Home networking

3 Functional Descriptions

The following sections describe functionalities of Le87402.

3.1 Operation States

Operation state control is depicted in the following table. For active operation, each channel will either be in enable state (power-up mode) or disable state (power-down mode). A standby state (long-term sleep mode) is also provided. EN1 and EN2 independently control each channel's power mode as follows:

- EN1 = 0, channel A/B in power-down mode; EN1 = 1, channel A/B in power-up mode
- EN2 = 0, channel C/D in power-down mode; EN2 = 1, channel C/D in power-up mode

C0 and C1 control state selection and their setting applies to both channels. A setting of C0 = C1 = 0 overrides EN1/2 and places both channels in standby state. Standby is the default state when power is initially supplied.

Table 1 • Operation State Control

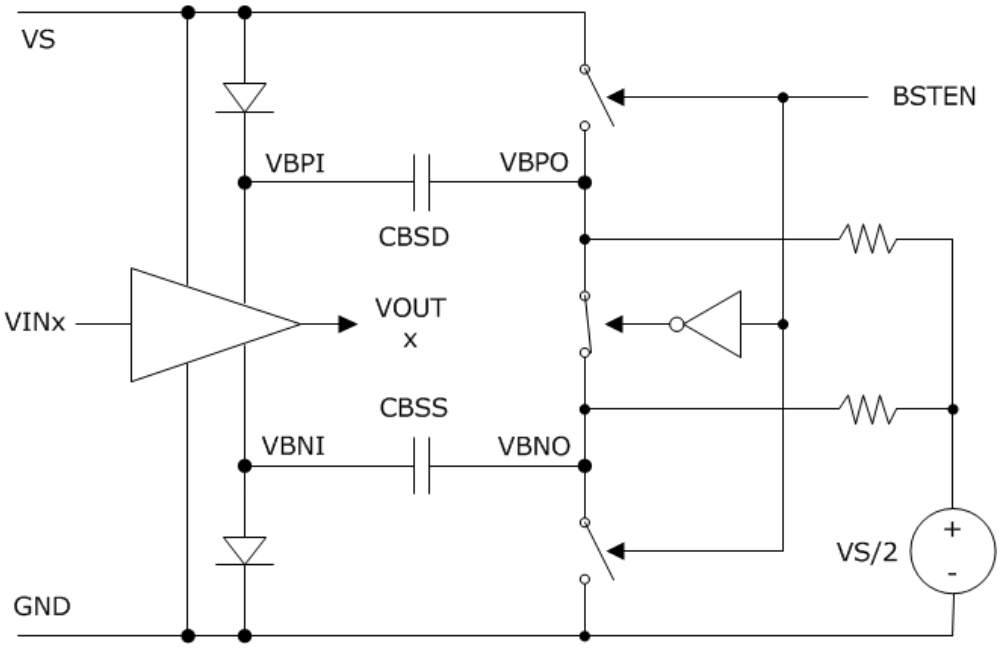
EN1 or EN2	C1	C0	Device State	Mode
1	1	1	Enable Full Power	Power-up
1	0	1	Enable 90% Power	
1	1	0	Enable 80% Power	
X	0	0	Standby	Sleep
0	1	1	Disable	Power-down
0	1	0		
0	0	1		

Note: X = Do not care.

3.2 Class GH Operation

The device operates and drives signals using a low-voltage supply. The device includes circuitry that stores voltage on external boost capacitors. When the capacitors are switched on, the supply to the output of the drive amplifiers is increased; as if a high supply in Class G operation is switched on , similar to a Class H operation, thereby avoiding saturation and any associated distortion. The GH operation is shown in the following figure. VS is the external low-voltage supply. When BSTEN is low, external boost capacitors CBSD and CBSS are charged up, each to about half of the VS potential. When BSTEN is high, the supplies to the drive amplifiers of the output stage are boosted to the charged value. The timing diagram is shown in Timing Diagram for Class-H Operation (see page 7).

Figure 2 • Class GH Operation



3.3 Boost Capacitor

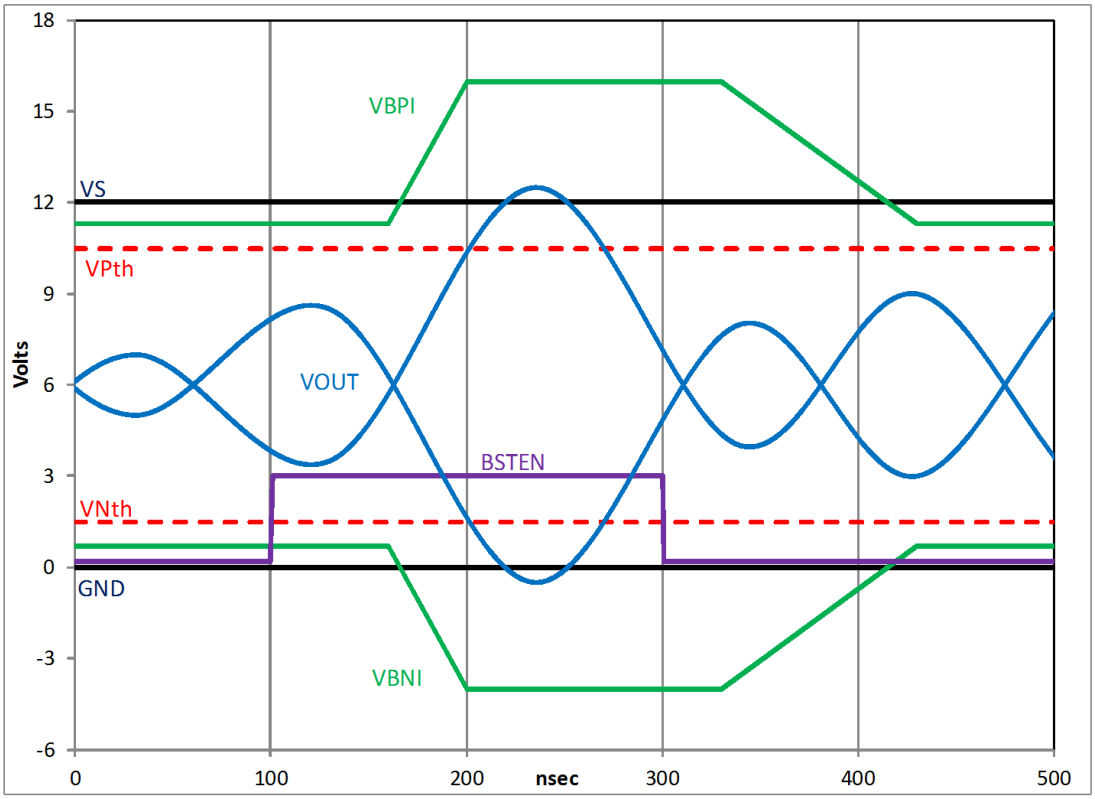
The minimum value for the boost capacitors (CBSD and CBSS) is dependent on the amplitude statistics of the transmitted waveform. There is no maximum value for the boost capacitor.

3.4 Operation Without Boosting

The device may be used in an application that does not require the boosting supply function. When operating the device without boosting, the following actions are allowed.

- Externally, tie VBPI pin to VS and VBNI pin to GND. This enables a wider VOUT range at the same VS voltage.
- External boosting capacitors, CBSD and CBSS, can be removed.
- VS can be increased beyond the operating ranges shown in Operating Ranges (see page 9), but must remain within the absolute maximum ratings shown in Absolute Maximum Ratings (see page 9).

Figure 3 • Timing Diagram for Class GH Operation



Notes on Class GH Operation:

- VS is the voltage supply to the chip and must meet operating range restrictions listed in Operating Ranges (see page 9).
- VBPI and VBNI function as supply rails to the line driver amplifiers. When BSTEN is low, VBPI = VS - Vdiode and VBNI = GND + Vdiode where Vdiode is about 1 V. When BSTEN is high, VBPI and VBNI are boosted beyond the chip supply rails through external boosting capacitors.
- VPth and VNth mark the VOUT range limit while BSTEN is low, as shown in preceding figure. VOUT exceeds the thresholds if BSTEN is set high with an adequate warning time before the event. A 100 ns warning time is shown in preceding figure.

4 Electrical Specifications

The following sections provide the available electrical specifications for Le87402. The following table gives the device parameters, conditions, and the limits.

VS = 12 V, R_{REF} = 75 kΩ, and if not specified, the device is in enable full power state using the basic test circuit. Typical conditions are: T_A = 25 °C. Minimum/Maximum parameters: T_A = 0 °C to 85 °C.

Table 2 • Electrical Specifications

Parameter	Condition	Minimum	Typical	Maximum	Unit
Supply Current					
I_{VS} (per channel)	Quiescent, VINA/B and VINC/D floating				
– Enable full power state		40	57	73	mA
– Enable 90% power state		36	51	66	
– Enable 80% power state		32	46	59	
– Enable 80% power state	VS = 10 V, R_{REF} = 130 kΩ		42		mA
– Disable state		0.7	1.0	1.4	mA
Standby state (per device)		0.4	0.65	1.0	mA
Control Input (C0/1, EN1/2, BSTEN) Characteristics					
Internal 50 kΩ pull-down on all control inputs					
V_{IH}		1.2		3.6	V
V_{IL}		–0.3		0.6	V
I_{IH}			75	120	µA
I_{IL}			10	20	µA
Channel Input (VINA/B, VINC/D) Characteristics					
Input offset voltage		–35		35	mV
Differential input impedance	VINA – VINB – VINC – VIND	13	15	18	kΩ
Channel Output (VOUTA/B, VOUTC/D) Characteristics					
Output voltage	Boosting[1]		12.5		V_{PK}
	Not boosting, BSTEN = 0		8		V_{PK}
Output current	RLoad = 10 Ω		600		mA
Disabled output impedance[1]	Differential		560		Ω
Channel Dynamic Characteristics					
Voltage gain	VOUT/VIN at 1 MHz	5.5	6.5	7.5	V/V
Bandwidth[1]	–3 dB		95		MHz
Input referred noise[1]	Differential		15		nV /√Hz
MTPR[1]	Pload = 40 mW 0.5 MHz to 30 MHz 30 MHz to 86 MHz		 –62 –32		 dBc dBc
Enable time[1]	Between disable and any power-up state		500		ns
Disable time[1]			500		ns
Boost Characteristics					
BSTEN warning time[1]	Time from BSTEN to VOUT crossing threshold		100		ns

Thermal Shutdown		
Thermal shutdown temperature[1]	170	°C

Note: 1. Guaranteed by design and device characterization.

Absolute Maximum Ratings

Stresses above the values listed in the following table can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods can affect device reliability. The following table shows the absolute maximum ratings of Le87402.

Table 3 • Absolute Maximum Ratings

Parameter	Value
Storage temperature	–65 °C ≤ TA ≤ 150 °C
Operating junction temperature	– 40 °C ≤ TJ ≤ 150 °C[1]
VS to GND	– 0.3 V to 16 V
Driver inputs VINA/B/C/D	VS to GND
Control inputs C0/1, EN1/2, BSTEN with respect to GND	– 0.3 V to 4 V
Continuous driver output current	200 mArms
Maximum device power dissipation, continuous [2] – T_A = 85 °C, P_D	1.7 W
Junction to ambient thermal resistance [2,3], Θ_{JA}	29.7 °C/W
Junction to board thermal resistance [2], Θ_{JB}	13.1 °C/W
Junction to case bottom (exposed pad) thermal resistance, $\Theta_{JC(BOTTOM)}$	3.7 °C/W
Junction-to-top characterization parameter[2], Ψ_{JT}	0.3 °C/W
ESD immunity (human body model)	JESD22 Class 2 compliant
ESD immunity (charge device model)	JESD22 Class IV compliant

Notes:

1. Continuous operation above 145°C junction temperature may degrade long term reliability of the device.
2. See the following section.
3. No air flow.

4.1 Thermal Resistance

The thermal performance of a thermally enhanced package is assured through optimized printed circuit board layout. Specified performance requires that the exposed thermal pad is soldered to an exposed copper surface of same size, which, in turn, conducts heat through multiple vials to larger internal copper planes.

4.2 Operating Ranges

Microsemi guarantees the performance of this device over 0 °C to 85 °C temperature range by conducting electrical characterization and a single insertion production test coupled with periodic sampling. These procedures comply with the Telcordia GR-357-CORE generic requirements for assuring the reliability of components used in telecommunications equipment.

Table 4 • Operating Ranges

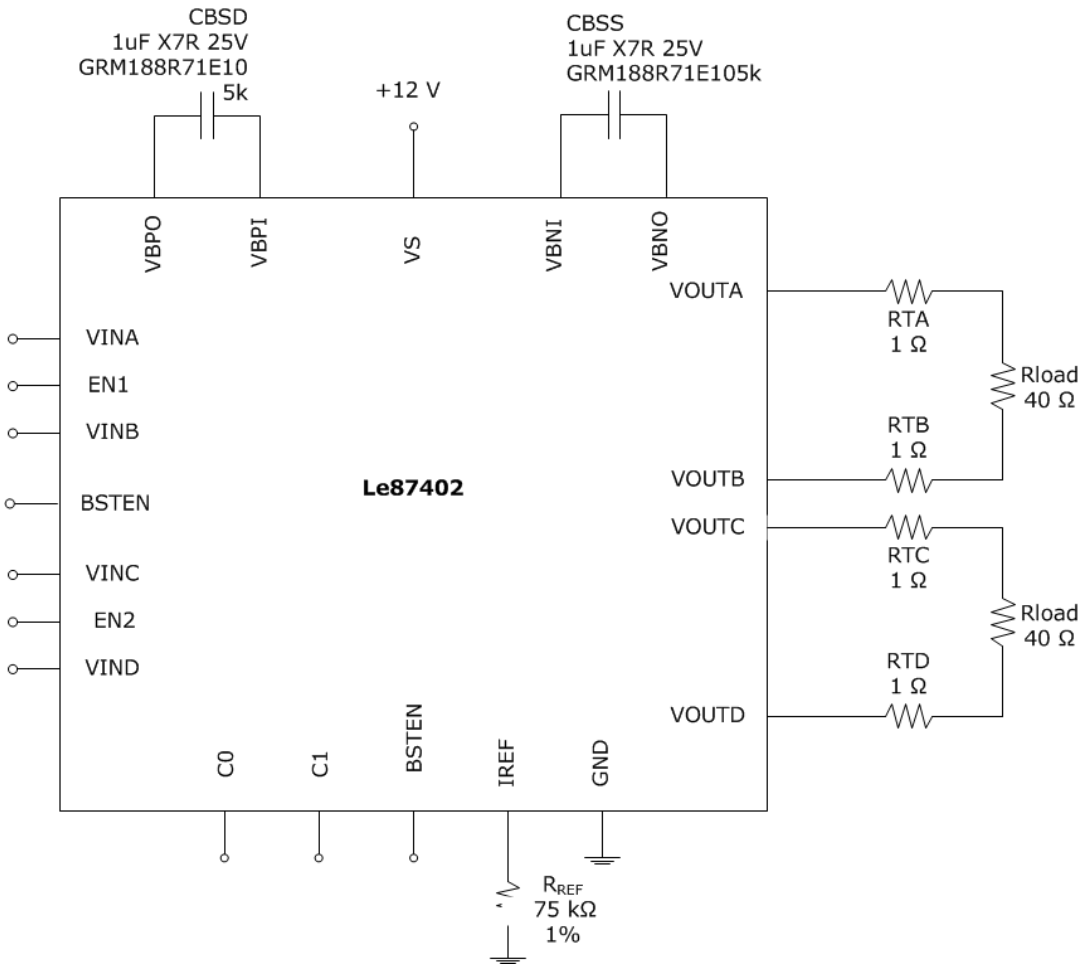
Ambient temperature	0 °C to 85 °C
VS with respect to GND	10 V to 12 V, +/- 5%

MIMO operation has the same device specification as SISO operation. The difference is that more power is delivered to the line in SISO operation.

4.3 Test Circuit

The following figure shows the basic test circuit.

Figure 4 • Basic Test Circuit



4.4 Performance Characteristics

The following graphs show typical device performance characteristics using the Basic Test Circuit (see page 10). Plotted performance is representative of either of the channels. Differential Gain (see page 11) plots device gain performance versus frequency. Supply Power Versus Load Power (see page 11) plots line driver power to the load; with one channel operating in the full power state and loaded with 40 Ω. Disabled Output Impedance Applications (see page 12) plots output impedance versus frequency in the disabled state.

Figure 5 • Differential Gain

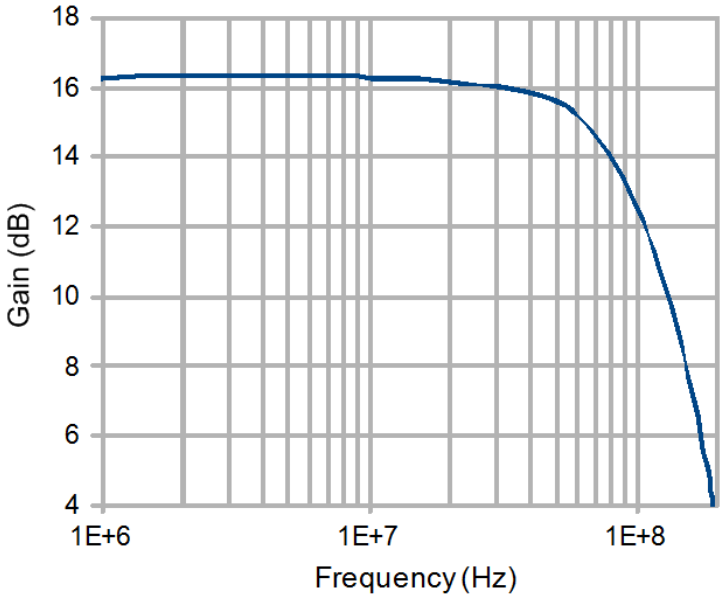


Figure 6 • Supply Power Versus Load Power

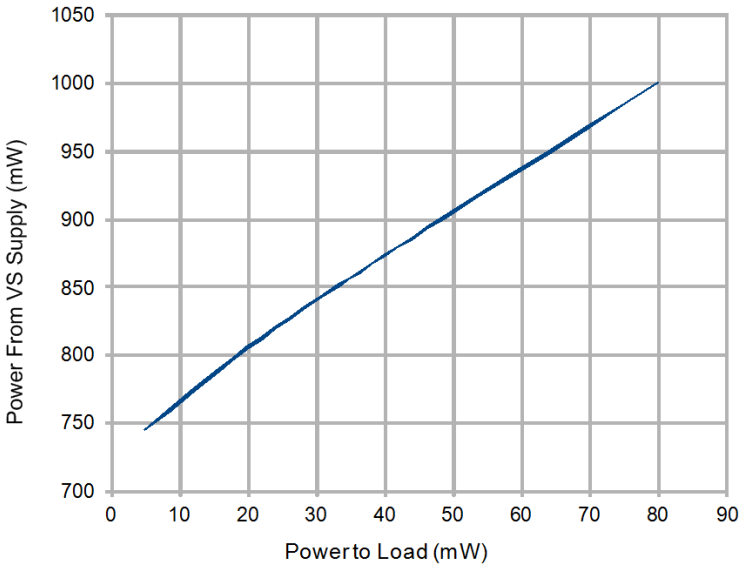
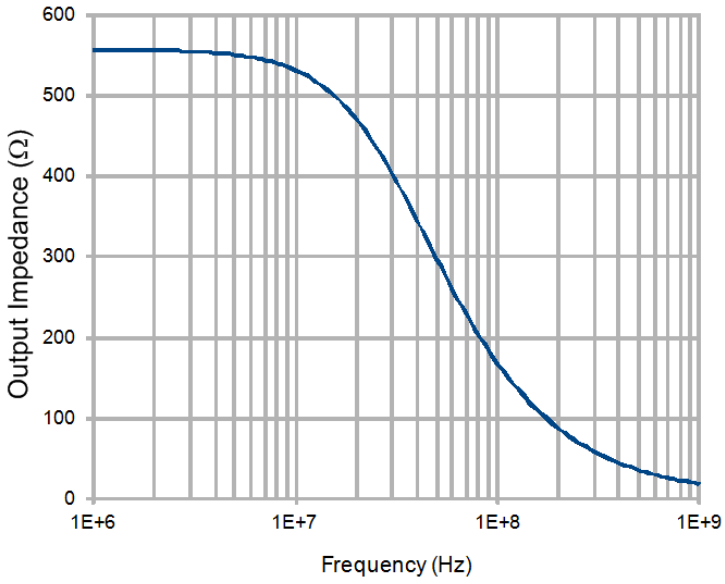


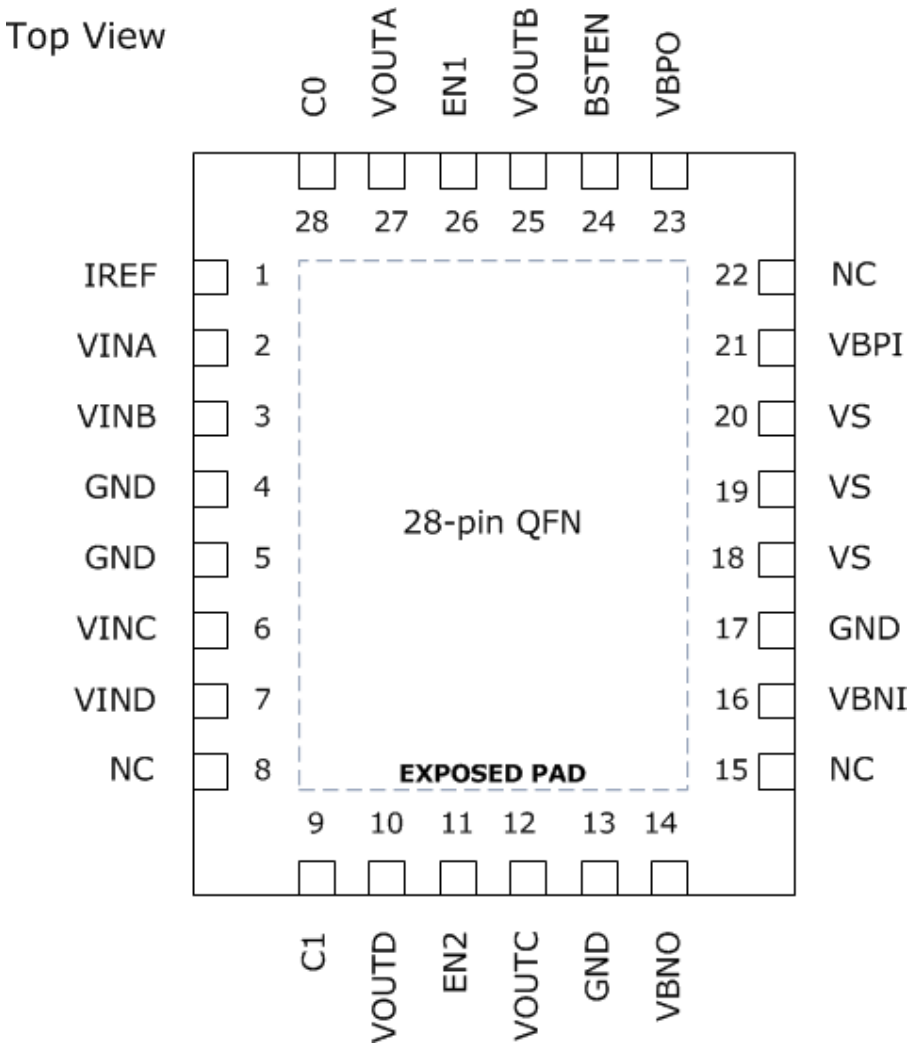
Figure 7 • Disabled Output Impedance Applications



5 Pin Descriptions

The following figure shows the pin diagram for Le87402.

Figure 8 • Le87402 Pin Diagram



Note: 1. Pin 1 is marked for orientation.

2. The device incorporates an exposed die pad on the underside of its package. The pad acts as a heat sink and must be connected to a copper plane through thermal vials for proper heat dissipation. It is electrically isolated and may be connected to GND.

The following table lists the pin name, corresponding pin number, type, and the descriptions.

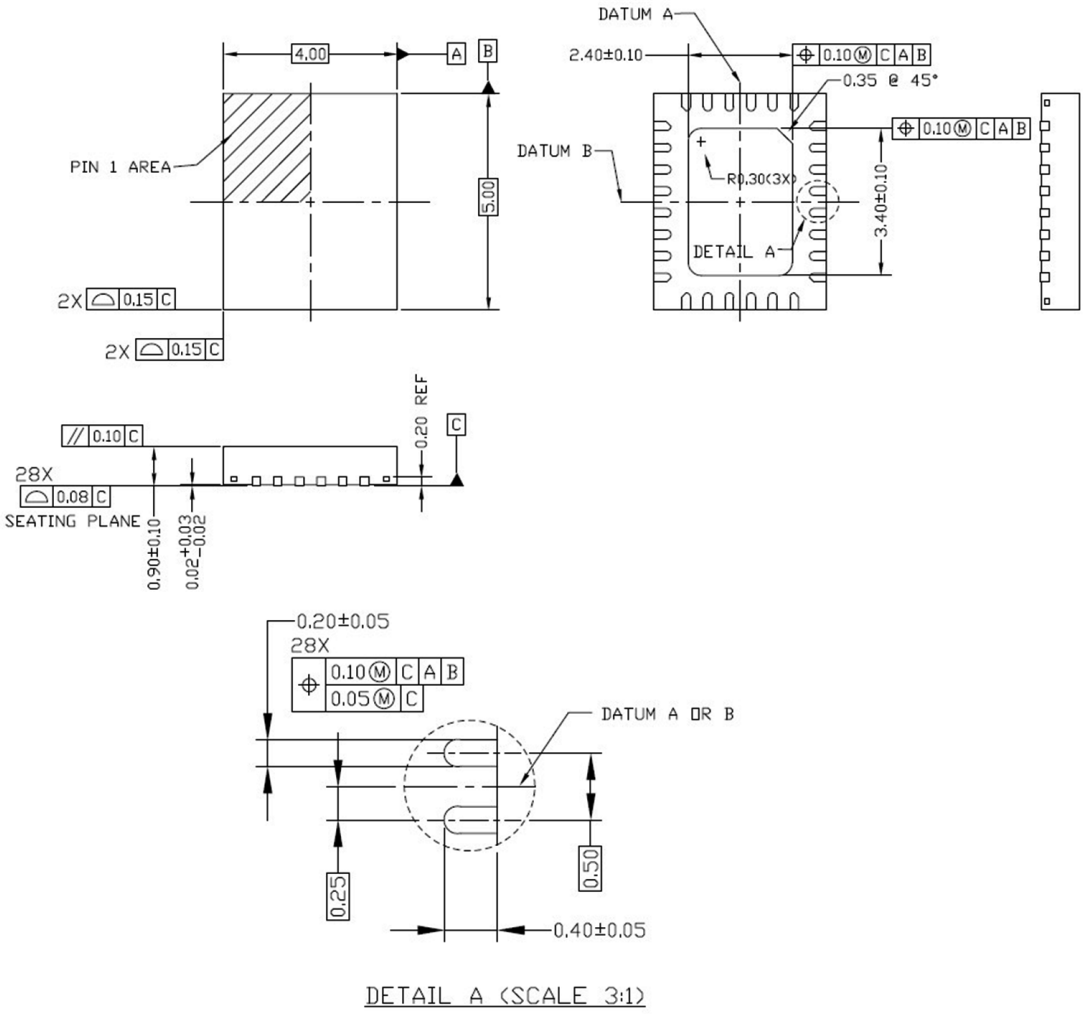
Table 5 • Pin Descriptions

Pin Name	Pin #	Type	Description
IREF	1	Input	Device internal reference current. Connect resistor R_{REF} to GND
EN1	26	Input	Channel A and B enable/disable control
EN2	11	Input	Channel C and D enable/disable control
VINA	2	Input	Amplifier A input
VINB	3	Input	Amplifier B input
VINC	6	Input	Amplifier C input
VIND	7	Input	Amplifier D input
VOUTA	27	Output	Amplifier A input
VOUTB	25	Output	Amplifier B input
VOUTC	12	Output	Amplifier C input
VOUTD	10	Output	Amplifier D input
C0, C1	28,9	Inputs	Sets operation state when channel is enabled
VBPO	23	Output	Connect a capacitor to VBPI
VBPI	21	Input	Connects to V S through an internal diode
VS	18,19,20	Power	Power supply
GND	4,5,13,17	Ground	Low noise analog ground
VBNI	16	Input	Connects to GND through an internal diode
VBNO	14	Output	Connects a capacitor to VBNI
BSTEN	24	Input	Boost enable
NC	8,15,22	NA	No connect

6 Package Information

The following figure shows the outline drawing of the LE87402 device.

Figure 9 • 28-pin QFN Physical Dimensions



NOTES:

1. DIMENSIONING AND TOLERANCE IS IN CONFORMANCE TO ASME Y14.5–1994
   ALL DIMENSIONS ARE IN MILLIMETERS ° IN DEGREES
2. DIMENSION OF LEAD WIDTH APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP (BOTH ROWS). IF THE TERMINAL HAS OPTIONAL RADIUS ON THE END OF THE TERMINAL, THE LEAD WIDTH DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA

Note: Packages may have mold tooling markings on the surface. These markings have no impact on the form, fit or function of the device. Markings vary with the mold tool used in manufacturing.

6.1 Package Assembly

The green package devices are assembled with enhanced, environmental compatible lead-free, halogen-free, and antimony-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes.

Refer to IPC/JEDEC J-Std-020 for recommended peak soldering temperature and solder reflow temperature profile.

7 Design Considerations

The Le87402 integrates two sets of high-power line driver amplifiers. The amplifiers are designed for low distortion for signals up to 86 MHz. A typical application interface circuit (for one channel) is shown in Typical Application Circuit (see page 18). The amplifiers have identical positive gain connections with common-mode rejection. Any DC input errors are duplicated and create common-mode rather than differential line errors.

7.1 Internal Reference Current

Resistor R_{REF} sets the internal reference current for both channels of the Le87402 device. The standard value for R_{REF} is 75 kΩ, this value was used for all specifications in this data sheet. Increasing the value of R_{REF} not only reduces device power dissipation but also lowers the available drive bandwidth. Do not exceed an R_{REF} value above 130 kΩ.

7.2 Input Considerations

The driving source impedance should be less than 100 nH to avoid any ringing or oscillation.

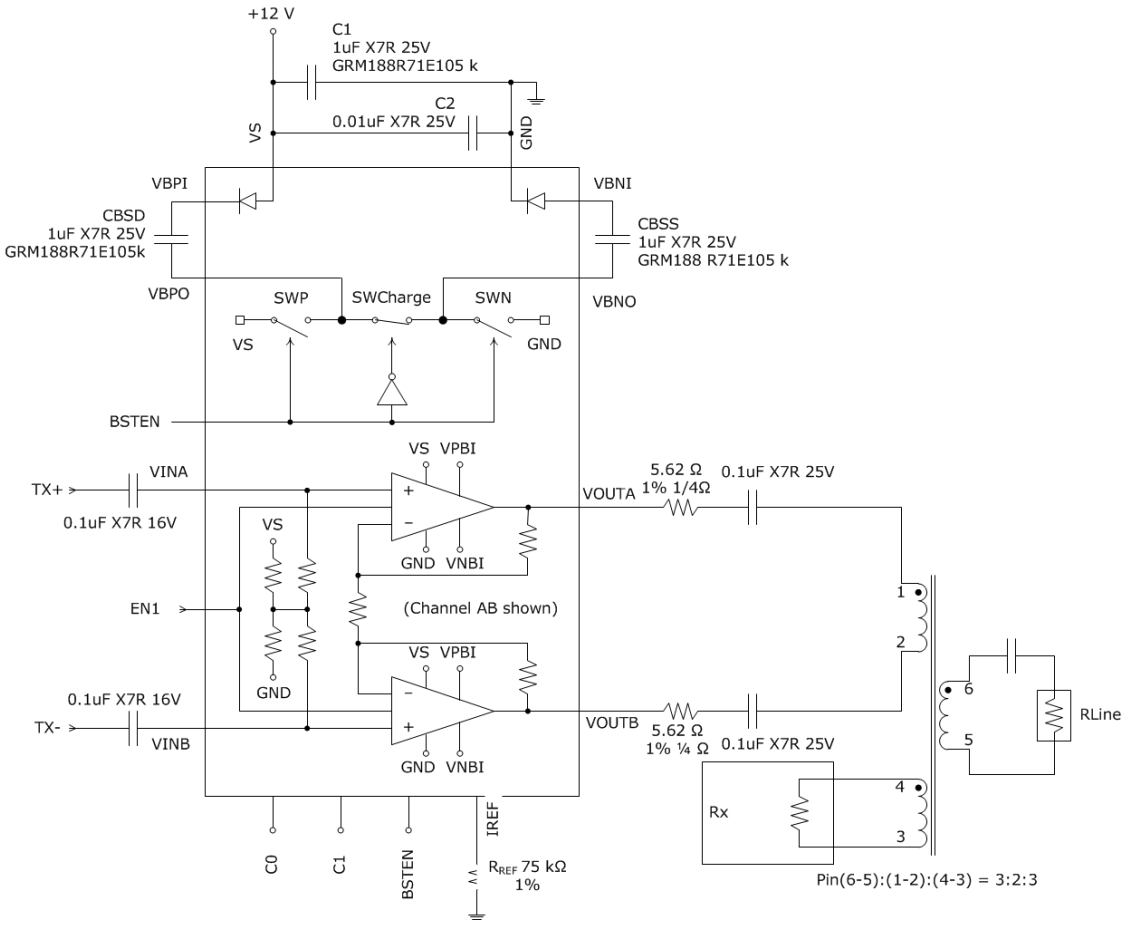
7.3 Output Driving Considerations

The internal metallization is designed to drive 200 mArms sinusoidal current and there is no current limit mechanism. Driving lines without a series resistor is not recommended. If a DC current path exists between the two outputs, a DC current can flow through the outputs. To avoid DC current flow, the most effective solution is to place DC blocking capacitors in series with the output as shown in the following figure.

7.4 Power Supplies and Component Placement

The power supplies should be well bypassed; with decoupling placed close to the Le87402. The following figure shows the typical application circuit for Le87402.

Figure 10 • Typical Application Circuit - Channel A/B



Note: In this figure only one channel of the two channel device is shown.

8 Ordering Information

The following list shows the ordering part numbers to be used while ordering Le87402.

- Le87402MQC 28-pin QFN Green Pkg. Tray
- Le87402MQCT 28-pin QFN Green Pkg. Tape and Reel

Note: The preceding ordering part number is for ordering the tape and reel packing system.

The green package is halogen free and meets RoHS 2 directive 2011/65/EU of the European Council to minimize the environmental impact of electrical equipment.

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