M02050-15

3.3/5V Limiting Amplifier for Aplications to 2.5 Gbps

Preliminary **- Rev V5P**

Applications

- 2.5 Gbps STM-16/OC-48 SDH/SONET
- 1.06, 2.12 and 4.24 Gbps Fibre Channel
- 1.25 Gbps Ethernet
- 2.67 Gbps SDH/SONET with FEC

Features

- Operates with a 3.3 or 5V supply
- 4 mV typical input sensitivity at 2.5 Gbps
- PECL outputs
- Rate Selection for ≤ 1.25 Gbps operation
- Average Receive power monitor output ($RSSI_{AVG}$)
- Peak-to-peak Receive power monitor output ($RSSI_{PP}$)
- On-chip DC offset cancellation circuit
- Low power (< 180 mW at 3.3V)
- Programmable CML Output Amplitude Level
- Output Jam Function
- 16 pin 3x3 QFN package

The M02050-15 is an integrated high-gain limiting amplifier. The M02050-15 features PECL outputs and is intended for use in applications to 2.5 Gbps. Full output swing is achieved even at minimum input sensitivity. The M02050-15 can operate with a 3.3V or 5V supply.

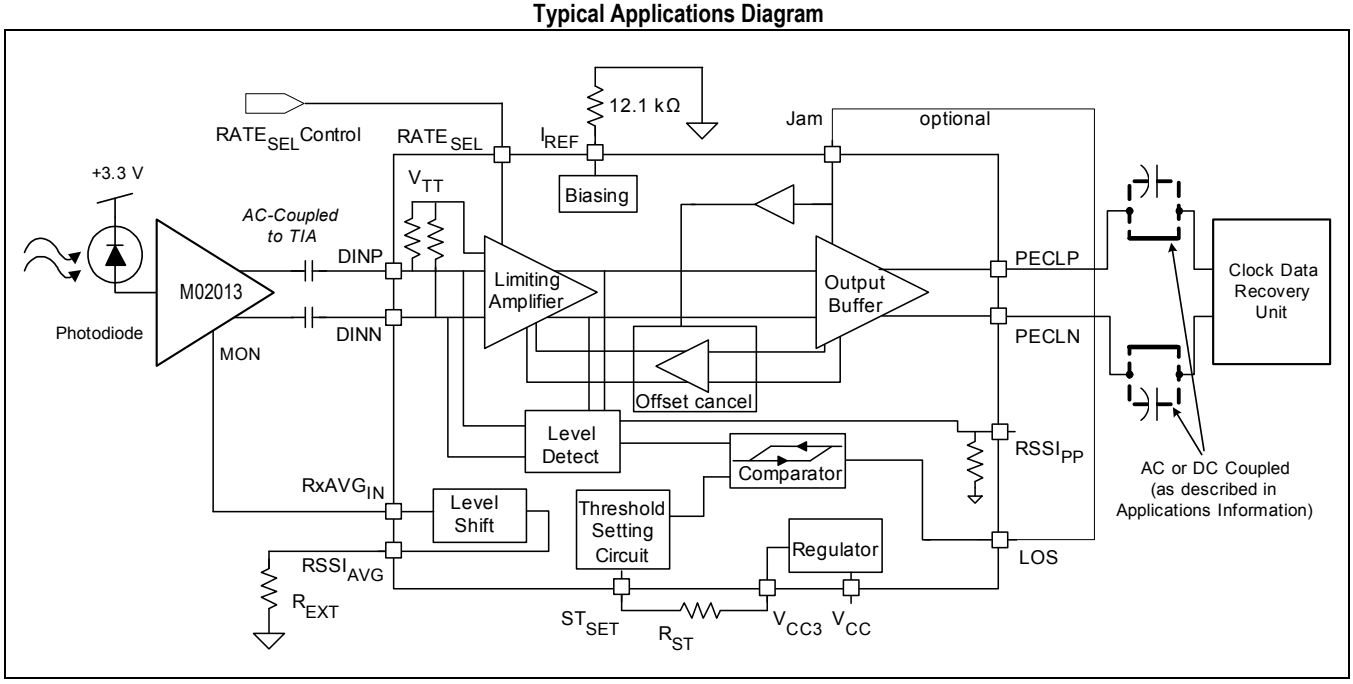
Rate select is supported for SFP applications and/or to achieve optimum sensitivity at data rates ≤ 1.25 Gbps. When rate select is high, optimum sensitivity is achieved at 2.5 Gbps.

The M02050-15 also includes two analog RSSI outputs proportional to either the average or peak to peak input signal and a programmable signal-level detector allowing the user to set thresholds at which the logic outputs are enabled.

Other available solutions: M02049-15 3.3/5V Limiting Amplifier for Applications to 4.3 Gbps (CML outputs)
M02040-15 3.3/5V Limiting Amplifier for Applications to 2.125 Gbps (PECL outputs)
M02043-15 3.3/5V Limiting Amplifier for Applications to 4.3 Gbps (CML outputs)

1.25 Gbps and 4.25 Gbps SFP reference designs available on MACOM's website.

Typical Applications Diagram



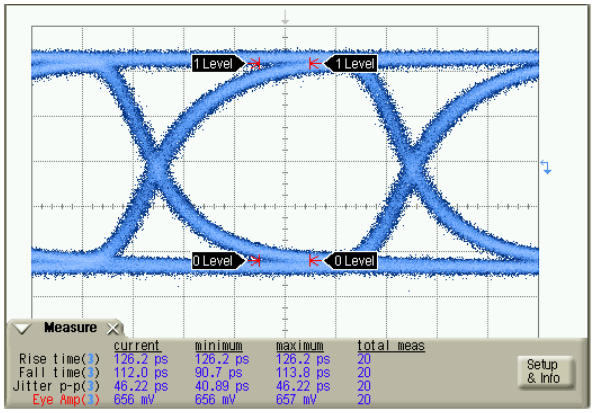
Ordering Information

Part Number	Package	Operating Temperature
M02050-15 *	M02050-15 in QFN16 package	–40 °C to 85 °C
M02050-15EVM	Evaluation board with M02050-15	–40 °C to 85 °C
* The letter "G" designator after the part number indicates that the device is RoHS-compliant.		

Revision History

Revision	Level	Date	Description
V5P	Preliminary	May 2015	Updated logos and page layout. No content changes.
D (V4P)	Preliminary	April 2005	Separated the M02049 and M02050 data sheets. New document number for the M02049 is 02049-15-DSH-002-D. Update the following DC specifications: I_{CC}, R_{IN}DIFF and V_{OH}. Update the following ac specifications: $V_{IN(MIN)}$, v_n, V_{LOS}, HYS, DJ, RJ, t_r/t_f, T_{LOS_ON}, and T_{LOS_OFF}. Update R_{ST} and RSSI values for this revision of the part.

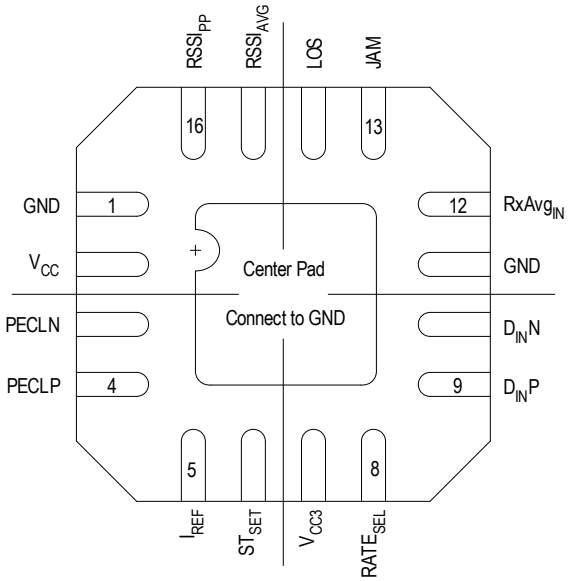
M02050 Typical Eye Diagram



10 mV_{PP} differential input
2.5 Gbps

150 mV/div
80 ps/div

M02050-15 Pin Configuration



1.0 Product Specification

1.1 Absolute Maximum Ratings

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

NOTE: The package bottom must be adequately grounded to ensure correct thermal and electrical performance, and it is recommended that vias are inserted through to a lower ground plane.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{CC}	Power supply voltage (V_{CC}-GND)	-0.5 to +5.75V	V
T_{STG}	Storage temperature	-65 to +150	°C
PECLP, PECLN	PECL Output pins voltage	V_{CC} - 2 to V_{CC} + 0.4	V
I(PECLP), I(PECLN)	PECL Output pins maximum continuous current (delivered to load)	30	mA
|DINP - DINN|	Data input pins differential voltage	0.80	V
DINP, DINN	Data input pins voltage meeting |DINP - DINN| requirement	GND to V_{CC3} + 0.4	V
ST_{SET}	Signal detect threshold setting pin voltage	GND to V_{CC} + 0.4	V
JAM	Output enable pin voltage	GND to V_{CC} + 0.4	V
LOS	Status Output pins voltage	GND to V_{CC} + 0.4	V
Rate_Sel	Rate Select input pin voltage	GND to V_{CC} + 0.4	V
I_{REF}	Current into Reference input	+0 to -120	µA
$I(RSSI_{AVG})$	Current into RSSIavg input	+0 to -3	mA
$RSSI_{PP}$	$RSSI_{PP}$ pin voltage	GND to +3.6	V
I(LOS)	Current into Loss of Signal pin	+1500 to -100	µA

1.2 Recommended Operating Conditions

Table 1-2. Recommended Operating Conditions

Parameter	Rating	Units
Power supply: (V_{CC}-GND) (apply no potential to V_{CC3}) or (V_{CC3}-GND) (connect V_{CC} to same potential as V_{CC3})	+5V ± 7.5% or +3.3V ± 7.5%	V
Junction temperature	-40 to +110	°C
Operating ambient	-40 to +85	°C

1.3 DC Characteristics

V_{CC} = +3.3V ± 7.5% or +5V ± 7.5%, T_A = -40°C to +85°C, unless otherwise noted.
Typical specifications are for V_{CC} = 3.3V, T_A = 25°C, unless otherwise noted.

Table 1-3. DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current	Includes PECL load	–	54 (1)	TBD	mA
$V_{OUTLpecl}$	PECL Output Low Voltage (PECLP, PECLN)	Single ended; 50 Ω load to V_{CC}-2V	V_{CC}-1.81	V_{CC}-1.71	V_{CC}-1.62	V
$V_{OUTHpecl}$	PECL Output High Voltage (PECLP, PECLN)	Single ended; 50Ω load to V_{CC}-2V	V_{CC}-1.025	V_{CC}-0.952	V_{CC}-0.88	V
R_{IN}DIFF	Differential Input Resistance	Measured between DINP and DINN	90	115	135	Ω
V_{OH}	LOS Output High Voltage	External 4.7-10 kΩ pull up to V_{CC}	2.75	V_{CC}	–	V
V_{OL}	LOS Output Low Voltage	External 4.7-10 kΩ pull up to V_{CC}	0	–	0.4	V
V_{IH}	Logic Input High Voltage JAM, $RATE_{SEL}$		2.7	–	V_{CC}	V
V_{IL}	Logic Input Low Voltage JAM, $RATE_{SEL}$		–	–	0.8	V

Notes:

1. $RATE_{SEL}$ high (high bandwidth operation). Typical supply current decreases by 1.5 mA in low rate mode.

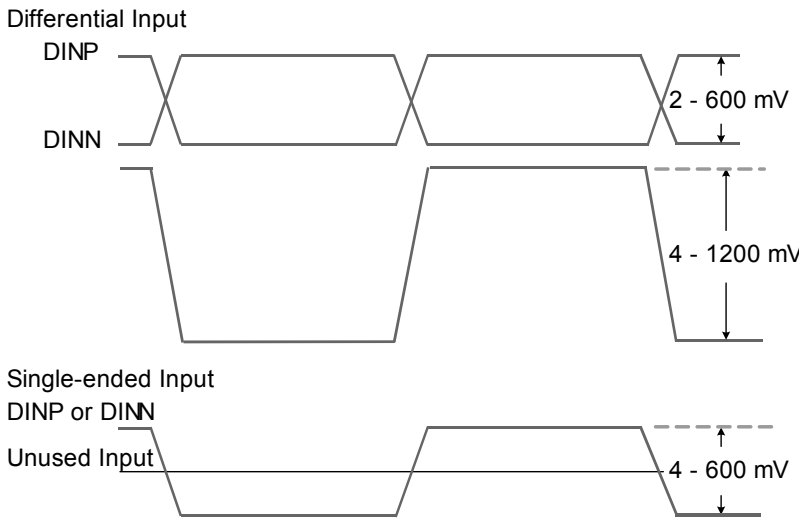
1.4 AC Characteristics

V_{CC} = +3.3V ± 7.5% or +5V ± 7.5%, T_A = -40°C to +85°C, input bit rate = 2.5 Gbps 2^{23}-1 PRBS high rate mode ($RATE_{SEL}$ = High) unless otherwise noted.
Typical specifications are for V_{CC} = 3.3V, T_A = 25°C, unless otherwise noted.

Table 1-4. AC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN(MIN))}$	Differential Input Sensitivity	1.25 Gbps, BER < 10^{-12}, low rate mode (RATESEL = low)	–	2	–	mV
		2.5 Gbps, BER < 10^{-12}	–	4	7	mV
$V_{I(MAX)}$	Input Overload	BER < 10^{-12}, differential input 2.5 Gbps	1200	–	–	mV
		BER < 10^{-12}, single-ended input, 2.5 Gbps	600	–	–	mV
v_n	RMS Input Referred Noise	$RATE_{SEL}$ = high	–	280	–	μV_{RMS}
V_{LOS}	Loss of Signal Programmable Range	Differential inputs	5	–	75	mV
HYS	Signal Detect Hysteresis	electrical; across LOS programmable range	2	3.5	5.5	dB
RSSIpp	Peak-to-peak received signal strength indicator range	Differential input signal range	4	–	100	mV
RSSIavg	Average received signal strength indicator range	± 15% accuracy ± 20% accuracy	5 0.5	– –	500 2	µA mA
BW_{LF}	Small-Signal –3dB Low Frequency Cutoff	Excluding AC coupling capacitors	–	25	–	kHz
DJ	Deterministic Jitter (includes DCD)	K28.5 pattern at 2.5 Gbps, 10 mV_{PP} input	–	–	25	ps
RJ	Random Jitter	10 mV_{PP} input	–	4.7	–	ps_{RMS}
t_r / t_f	Data Output Rise and Fall Times	20% to 80%; outputs terminated into 50 Ω; 10 mV_{PP} input $RATE_{SEL}$ = High $RATE_{SEL}$ = Low	 – –	 90 150	 110 200	ps
$T_{RATESEL}$	Rate select assert / deassert time	Time from when rate select is asserted high or low until amplifier is performing at selected bandwidth	–	–	10	µs
T_{LOS_ON}	Time from LOS state until LOS output is asserted	LOS assert time after 1 V_{PP} input signal is turned off; signal detect level set to 10 mV	2.3	–	80	µs
T_{LOS_OFF}	Time from non-LOS state until LOS is deasserted	LOS deassert time after input crosses signal detect level; signal detect set to 10 mV with applied input signal of 20 mV_{PP}	2.3	–	80	µs

Figure 1-1. Data Input Requirements

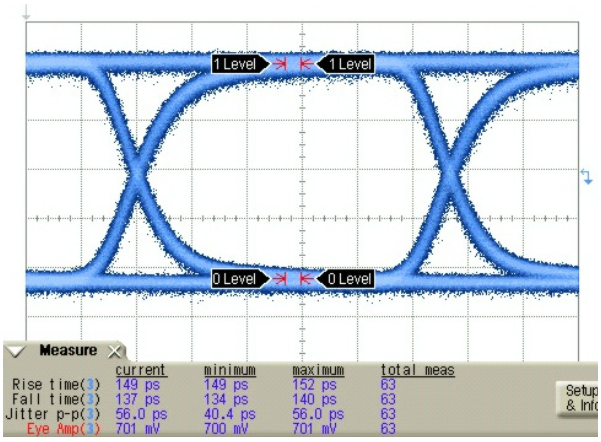


Note:

For single-ended input connections.
When connecting to the used input with AC-coupling, the unused input should be AC-coupled through 50 Ω to the supply voltage of the TIA;
When connecting to the used input with DC-coupling, the unused input should be DC-coupled through 50 Ω to a voltage equal to the common mode level of the used input.

1.5 Typical Eye Diagrams

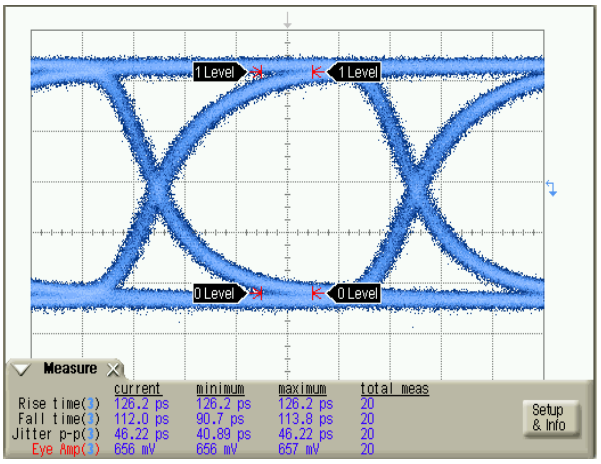
Figure 1-2. M02050 1.25 Gbps in Low Rate Mode



10 mV_{PP} differential input
1.25 Gbps

160 mV/div
140 ps/div

Figure 1-3. M02050 2.5 Gbps High Rate Mode



10 mV_{PP} differential input
2.5 Gbps

150 mV/div
80 ps/div

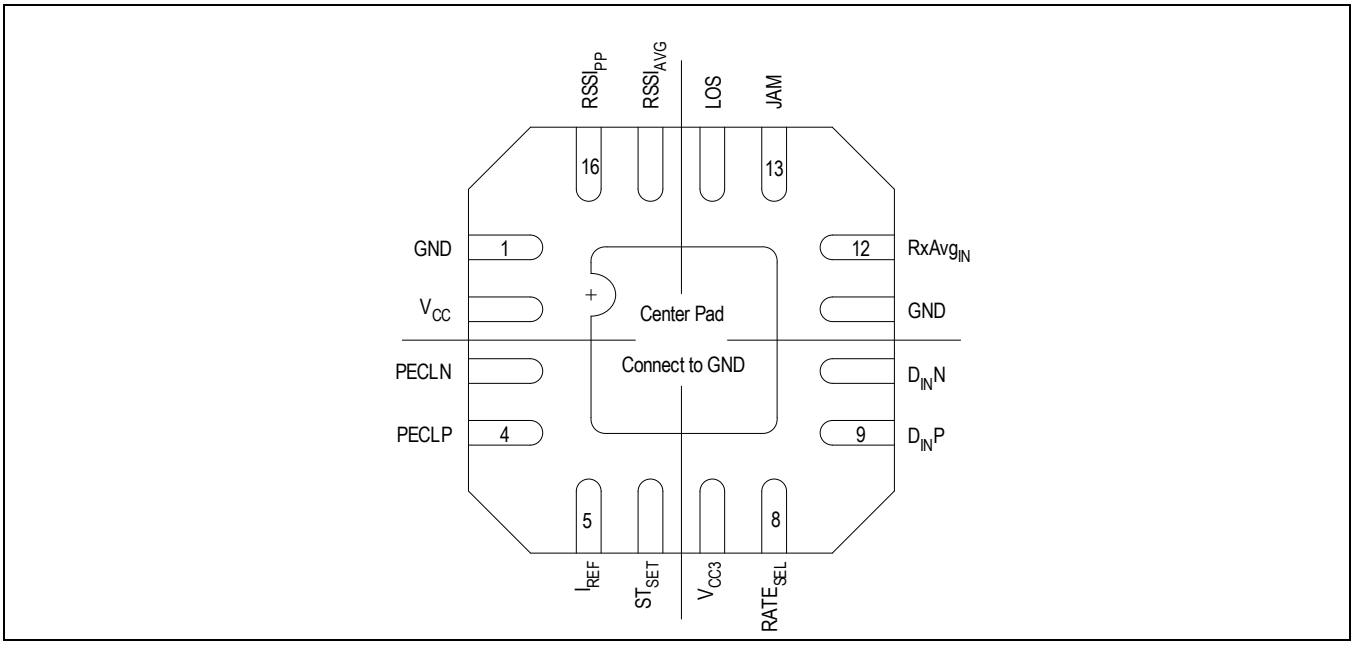
Preliminary Information—Subject to Change

2.0 Pin Definitions

Table 2-1. Pin Descriptions

QFN Pin#	Name	Function
1	GND	Ground.
2	V_{CC}	Power supply. Connect to either +5V or +3.3V.
3	PECLN	Inverting PECL data output.
4	PECLP	Non-inverting PECL data output.
5	I_{REF}	Internal reference current. Must be connected to ground through a 12.1 kΩ 1% resistor.
6	ST_{SET}	Loss of signal threshold setting input. Connect a 1% resistor between this pin and V_{CC3} to set loss of signal threshold.
7	V_{CC3}	Power supply input for 3.3V applications or the output of the internally regulated 3.3V voltage when V_{CC} = 5V. Connect directly to supply for 3.3V applications (internal regulator not in use). Do not connect to power supply if V_{CC} = 5V.
8	$RATE_{SEL}$	Rate select. When low or floating, the device is in low-rate mode (data rates ≤ 1.25 Gbps) and has reduced bandwidth. When high, the device is in full-rate mode with full bandwidth. Internal 80 kΩ resistor to ground. Drive with a current limited source as described in Section 4.1.4.
9	DINP	Non-inverting data input. Internally terminated with 50 Ω to V_{TT}.
10	DINN	Inverting data input. Internally terminated with 50 Ω to V_{TT}.
11	GND	Ground.
12	$RxAVG_{IN}$	Average power monitor input. Connect to monitor output of TIAs that produce a current (sink) mirror replica of the photodiode current. Leave floating if not used.
13	JAM	Output disable. When high, data outputs are disabled (with non-inverting output held high and inverting output held low). Connect to LOS output to disable outputs with loss of signal. Outputs are enabled when JAM is low or floating. Internal 150 kΩ resistor to ground.
14	LOS	Loss of signal output. Goes high when input signal falls below threshold set by ST_{SET}. Open collector TTL with internal 80 kΩ pull-up resistor to V_{CC}.
15	$RSSI_{AVG}$	Receiver average input power monitor. Provides a current source mirror of the current at $RxAVG_{IN}$. Connect a resistor to ground to set the full scale voltage to the desired level at maximum average input power.
16	$RSSI_{PP}$	Receiver peak-to-peak input voltage monitor. Provides a DC voltage (ground referenced) proportional to the peak-to-peak input voltage swing.
17	Center Pad	Ground. Must be connected to ground for proper operation.

Figure 2-1. M02050-15 Pinout - 16 Pin (3 x 3 mm) QFN Top View



3.0 Functional Description

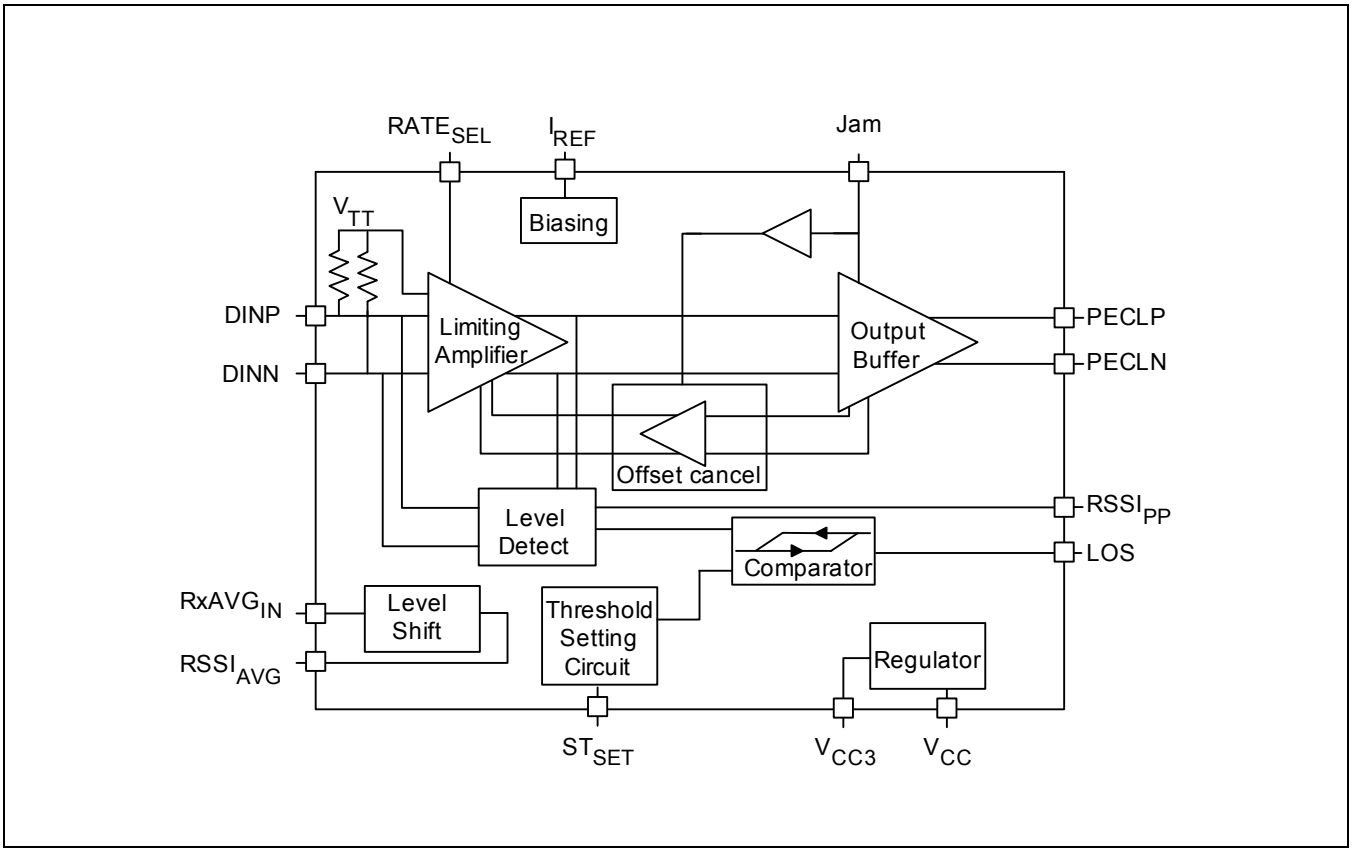
3.1 Overview

The M02050-15 is an integrated high-gain limiting amplifier. The M2050 features PECL outputs and is intended for use in applications to 2.5 Gbps. Full output swing is achieved even at minimum input sensitivity. The M02050-15 can operate with a 3.3V or 5V supply.

Rate select is supported for SFP applications and/or to achieve optimum sensitivity at data rates ≤ 1.25 Gbps. When rate select is high, optimum sensitivity is achieved at 2.5 Gbps.

The M02050-15 also includes two analog RSSI outputs proportional to either the average or peak to peak input signal and a programmable signal-level detector allowing the user to set thresholds at which the logic outputs are enabled.

Figure 3-1. Block Diagram Example



3.2 Features

- Operates with a 3.3 or 5V supply
- 4 mV typical input sensitivity at 2.5 Gbps
- PECL outputs
- Rate Selection for ≤ 1.25 Gbps operation
- Average Receive power monitor output ($RSSI_{AVG}$)
- Peak-to-peak Receive power monitor output ($RSSI_{PP}$)
- On-chip DC offset cancellation circuit
- Low power (< 180 mW at 3.3V)
- Programmable CML Output Amplitude Level
- Output Jam Function
- 16 pin 3x3 QFN package

3.3 General Description

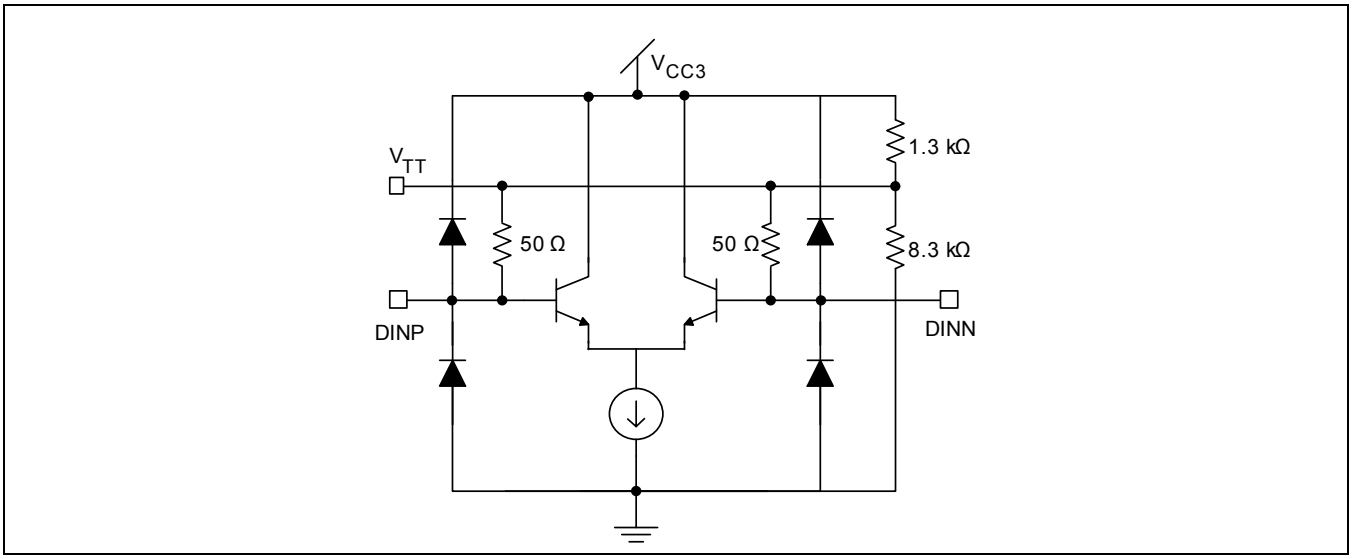
The M02050-15 is a high-gain limiting amplifier for applications up to 2.5 Gbps, and incorporates a limiting amplifier, an input signal level detection circuit and also a fully integrated DC-offset cancellation loop that does not require any external components. The M02050-15 features PECL data outputs.

The M02050-15 provides the user with the flexibility to set the signal detect threshold. Optional output buffer disable (squelch/jam) can be implemented using the JAM input.

3.3.1 Inputs

The data inputs are internally connected to V_{TT} via 50 Ω resistors, and generally need to be AC coupled. Referring to Figure 3-2, the nominal V_{TT} voltage is 2.85V because of the internal resistor divider to V_{CC3}, which means this is the DC potential on the data inputs. See the applications information section for further details on choosing the AC-coupling capacitor.

Figure 3-2. CML Data Inputs



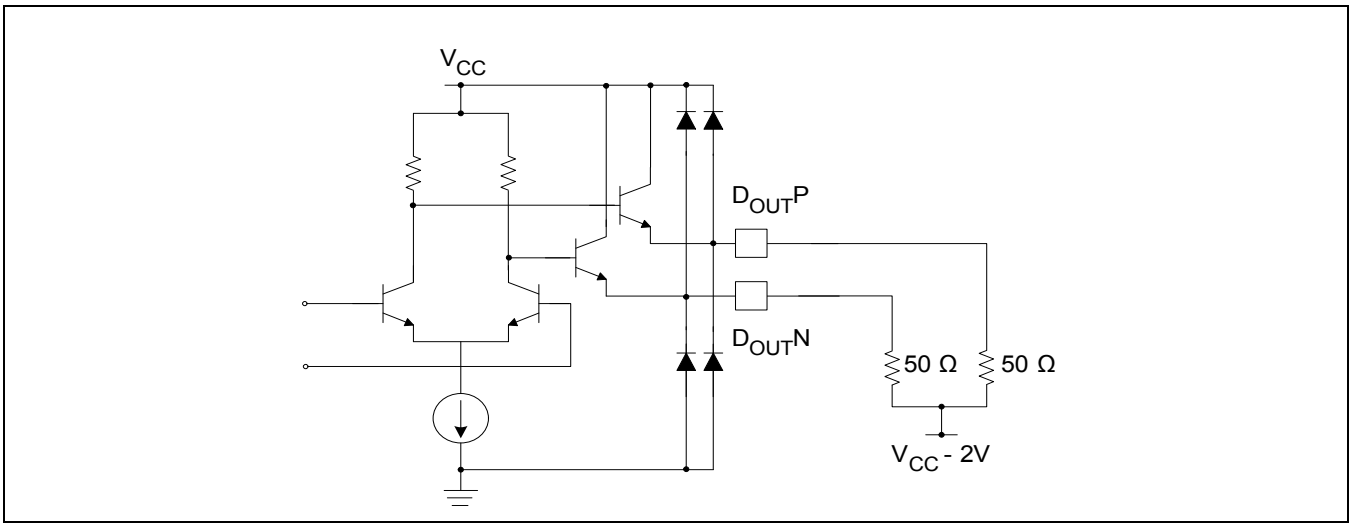
3.3.2 DC Offset Compensation

The M02050-15 contains an internal DC autozero circuit that can remove the effect of DC offsets without using external components. This circuit is configured such that the feedback is effective only at frequencies well below the lowest frequency of interest. The low frequency cut off is typically 25 kHz.

3.3.3 PECL Outputs

The M02050-15 features 100k/300k PECL compliant outputs as shown in Figure 3-3. The outputs may be terminated using any standard AC or DC-coupling PECL termination technique. AC-coupling is used in applications where the average DC content of the data is zero e.g. SONET. The advantage of this approach is lower power consumption, no susceptibility to DC drive and compatibility with non-PECL interfaces.

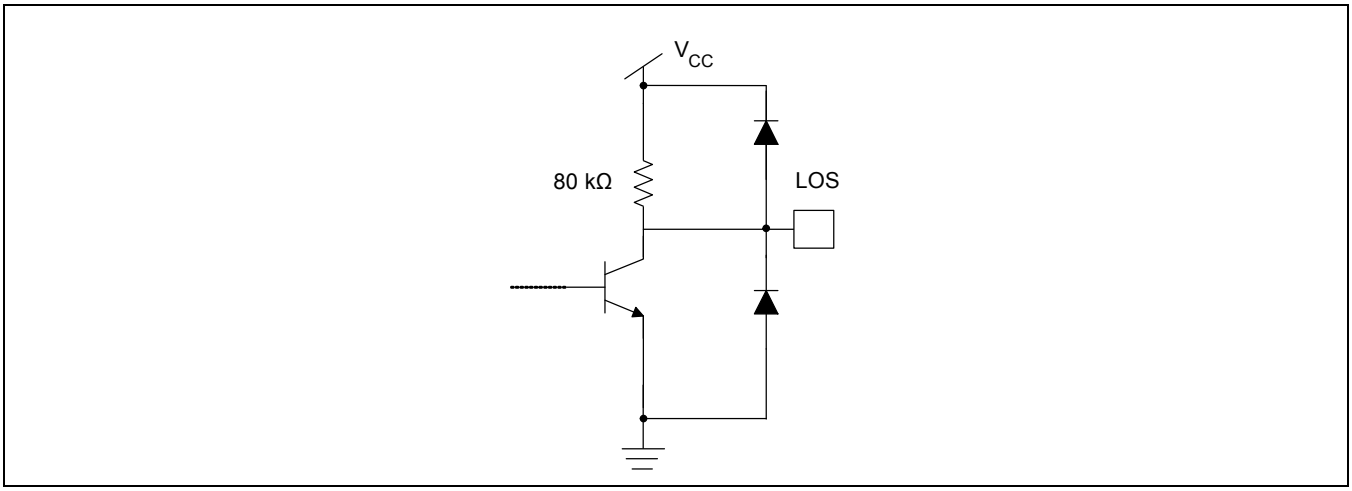
Figure 3-3. PECL Data Outputs



3.3.4 Loss of Signal (LOS)

The M02050-15 features input signal level detection over an extended range. Using an external resistor, R_{ST}, between pin ST_{SET} and V_{CC3} (Figure 3-5) the user can program the input signal threshold. The signal detect status is indicated on the LOS output pin shown in Figure 3-4. The LOS signal is active when the signal is below the threshold value. The signal detection circuitry has the equivalent of 3.5 dB (typical) electrical hysteresis.

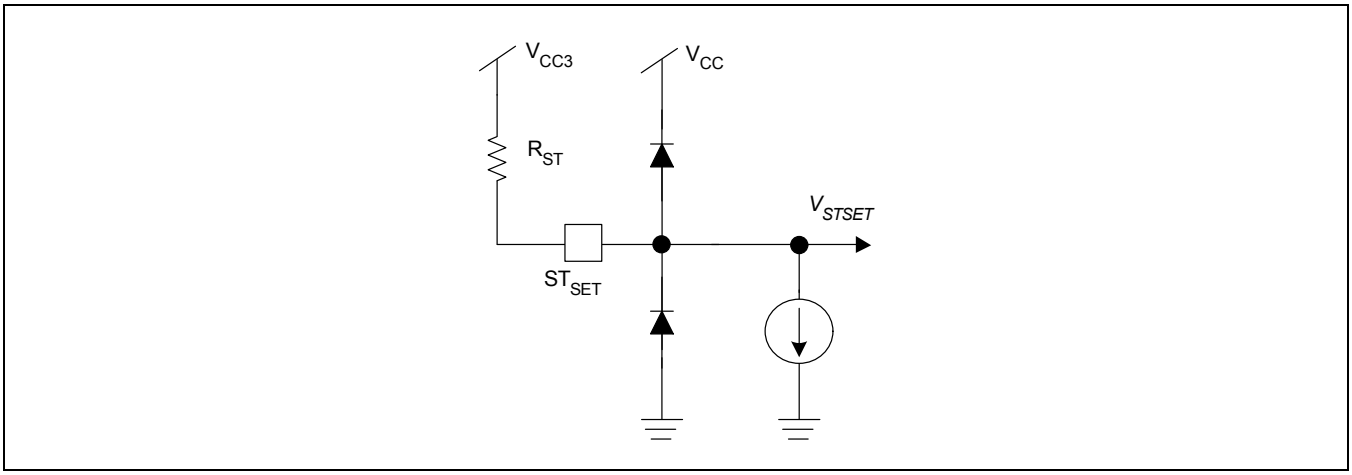
Figure 3-4. LOS Output



R_{ST} establishes a threshold voltage at the ST_{SET} pin as shown in Figure 3-5. Internally, the input signal level is monitored by the Level Detector (which also outputs the $RSSI_{PP}$ voltage). As described in the $RSSI_{PP}$ section, this voltage is proportional to the input signal peak to peak value. The voltage at ST_{SET} is internally compared to the signal level from the Level Detector. When the Level Detect voltage is less than $V_{(STSET)}$, LOS is asserted and will stay asserted until the input signal level increases by a predefined amount of hysteresis. When the input level increases by more than this hysteresis above $V_{(STSET)}$, LOS is deasserted. See the applications information section for the selection of R_{ST}.

Note that ST_{SET} can be left open if the loss of signal detector function is not required. In this case LOS would be low.

Figure 3-5. STset Input



3.3.5 Peak to Peak Received Signal Strength Indicator ($RSSI_{PP}$)

The $RSSI_{PP}$ output voltage is logarithmically proportional to the peak to peak level of the input signal. It is not necessary to connect an external capacitor to this output. Internally, the RSSI voltage is compared with a user selectable reference to determine loss of signal as described in the previous section.

Figure 3-6. $RSSI_{PP}$ Output

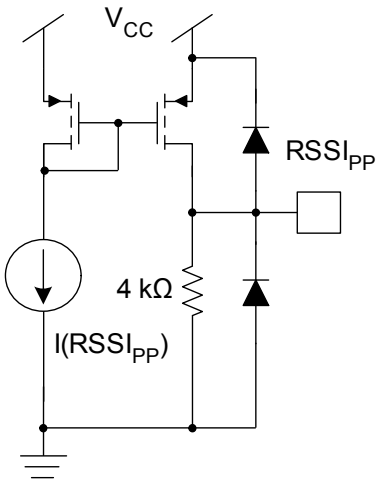


Figure 3-7. Typical $RSSI_{PP}$ Transfer Function

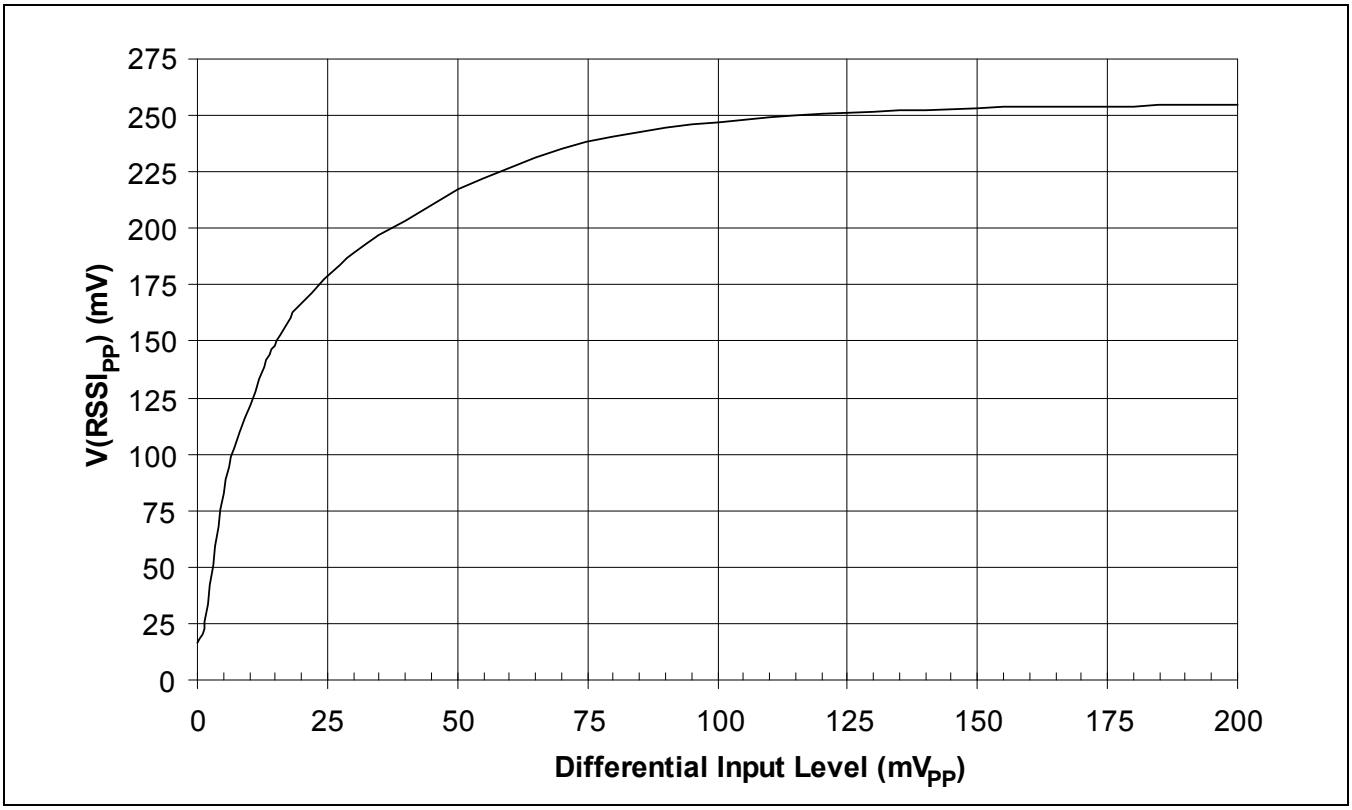


Figure 3-8. Typical $RSSI_{PP}$ Transfer Function (Low Input Level)

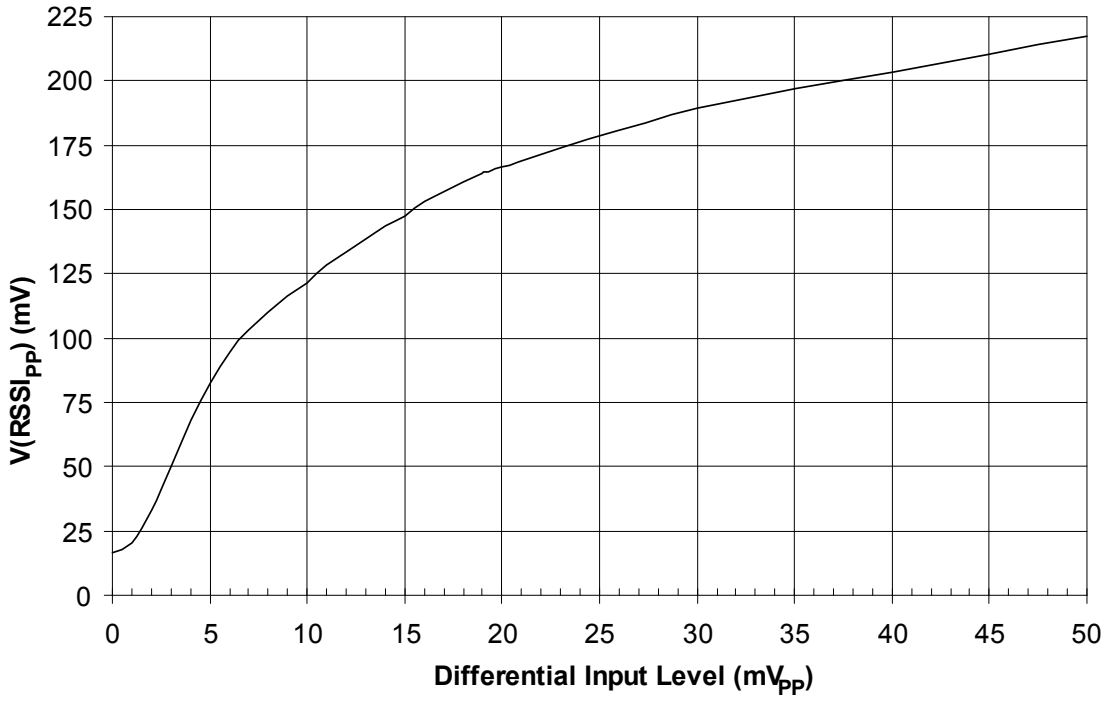
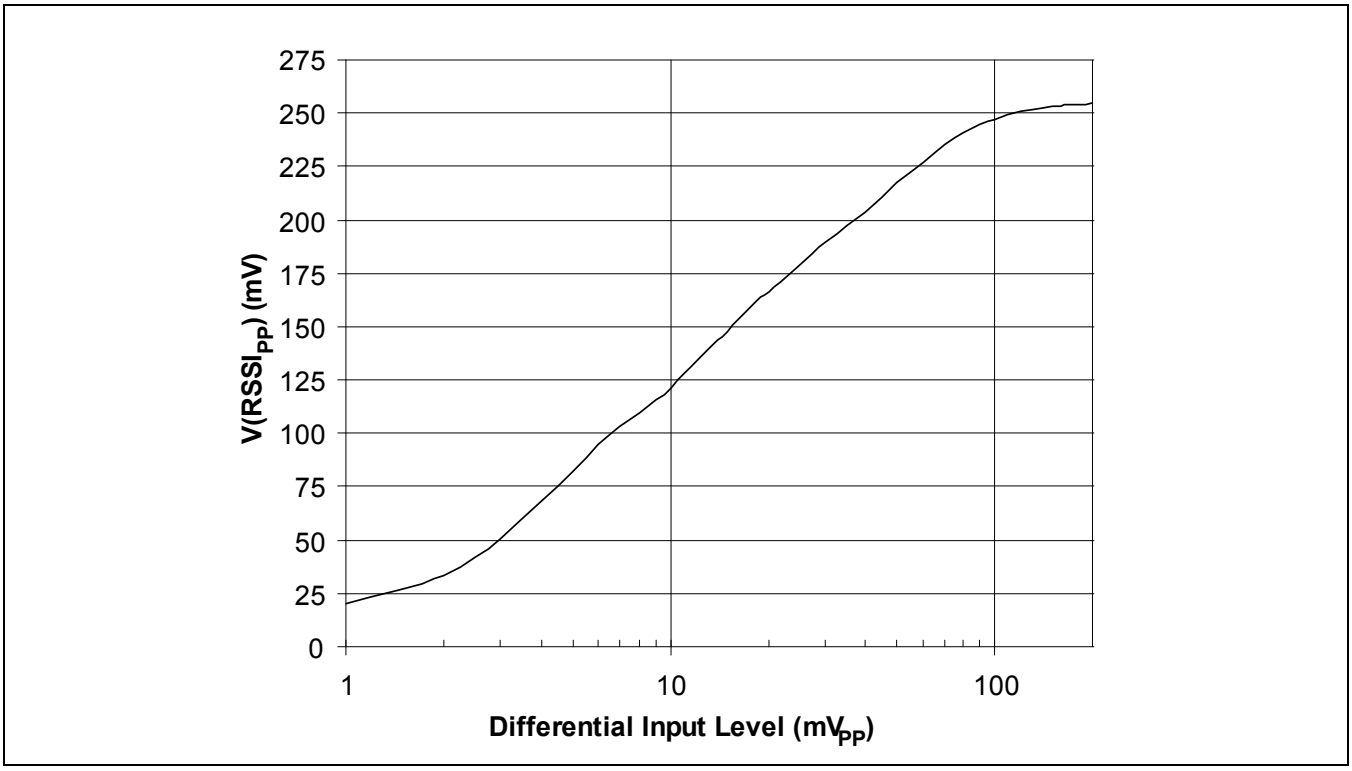


Figure 3-9. Typical $RSSI_{PP}$ Transfer Function (Log Scale)

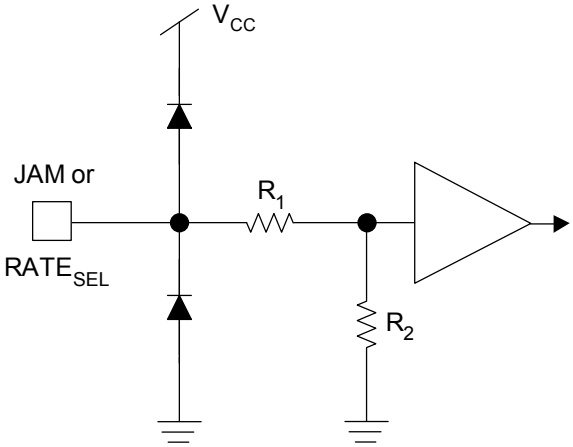


3.3.6 JAM Function

When asserted, the active high power down (JAM) pin forces the outputs to a logic “one” state. This ensures that no data is propagated through the system. The loss of signal detection circuit can be used to automatically force the data outputs to a high state when the input signal falls below the threshold. The function is normally used to allow data to propagate only when the signal is above the user's bit-error-rate requirement. It therefore inhibits the data outputs toggling due to noise when there is no signal present (“squelch”).

In order to implement this function, LOS should be connected to the JAM pin shown in Figure 3-10, thus forcing the data outputs to a logic “one” state when the signal falls below the threshold.

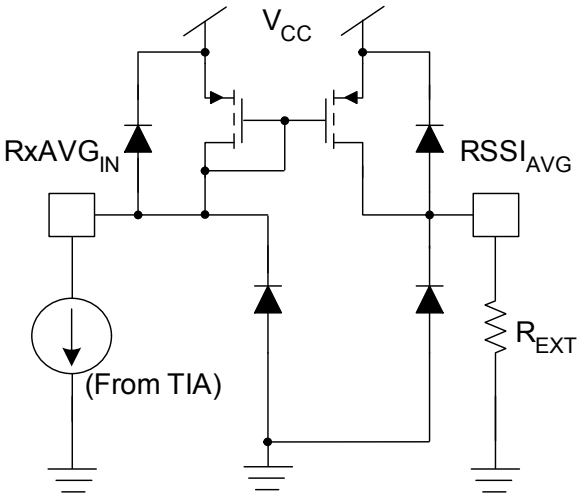
Figure 3-10. JAM and $RATE_{SEL}$ Input



3.3.7 Average Received Signal Strength Indicator ($RSSI_{AVG}$)

The $RSSI_{AVG}$ output current is a mirrored version of the $RxAVG_{IN}$ current from compatible TIAs. It sources rather than sinks the current making it compatible with DDMI type interfaces.

Figure 3-11. $RSSI_{AVG}$ Output



3.3.8 Voltage Regulation

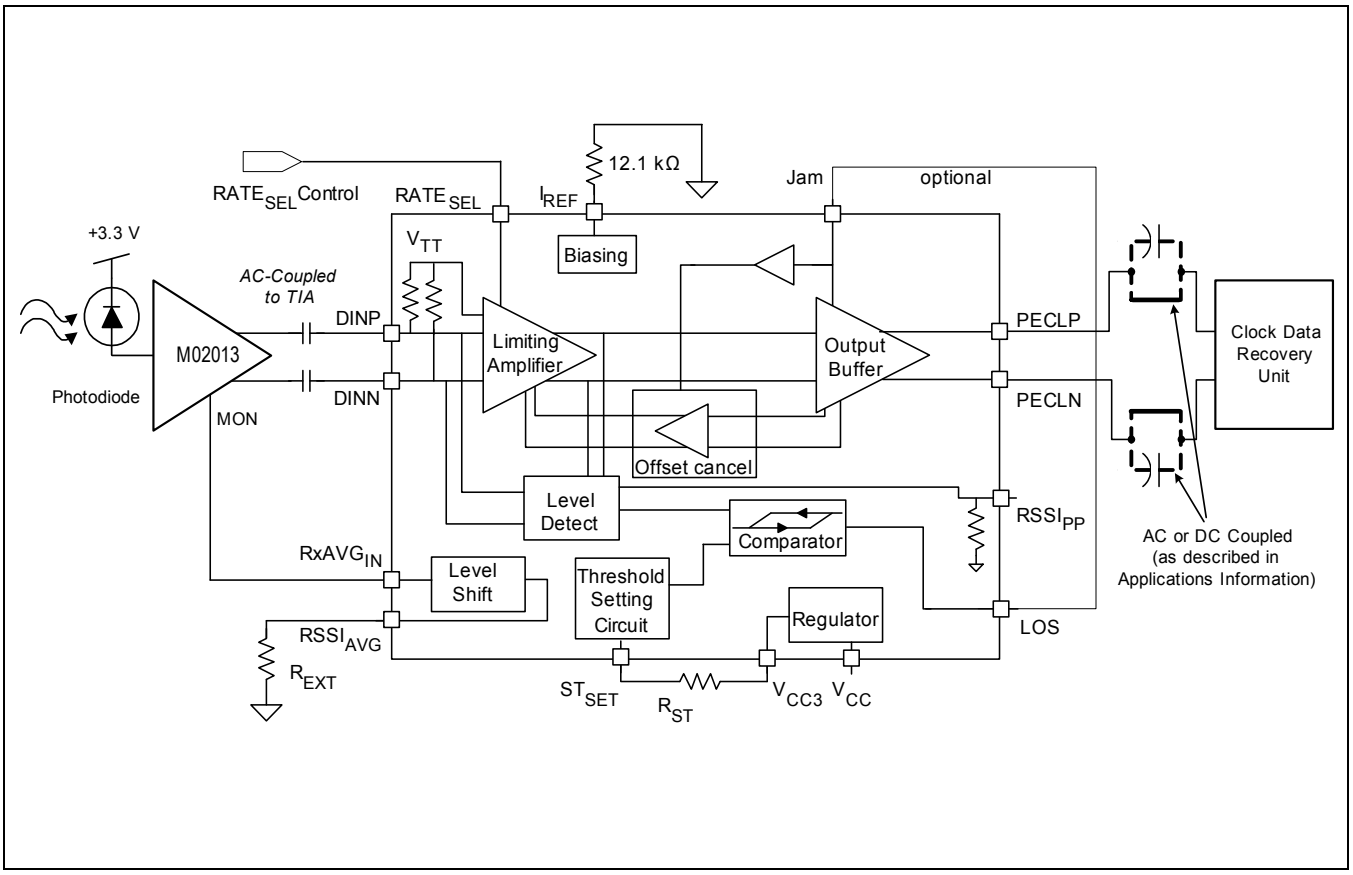
The M02050-15 contains an on-chip voltage regulator to allow both 5V and 3.3V operation. When used at 5V, the on-chip regulator is enabled and the digital inputs and outputs are compatible with TTL 5V logic levels.

4.0 Applications Information

4.1 Applications

- 2.5 Gbps STM-16/OC-48 SDH/SONET
- 1.06, 2.12 and 4.24 Gbps Fibre Channel
- 1.25 Gbps Ethernet
- 2.67 Gbps SDH/SONET with FEC

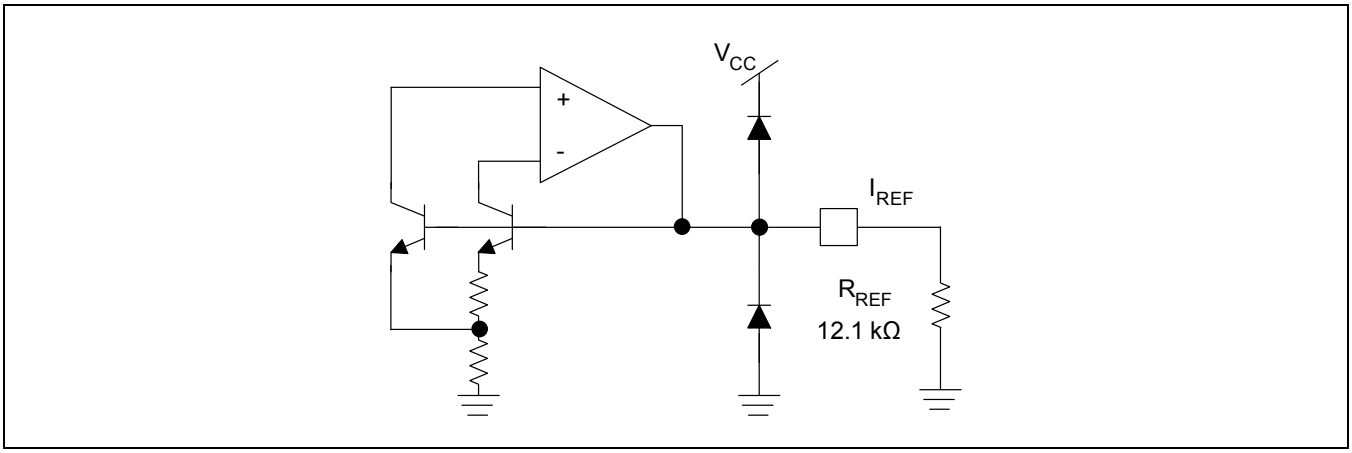
Figure 4-1. Typical Applications Diagram



4.1.1 Reference Current Generation

The M02050-15 contains an accurate on-chip bias circuit that requires an external 12.1 kΩ 1% resistor, R_{REF}, from pin I_{REF} to ground to define an on-chip reference current.

Figure 4-2. Reference Current Generation



4.1.2 Connecting V_{CC} and V_{CC3}

For 5V operation, the V_{CC} pin is connected to an appropriate 5V ± 7.5% supply. No potential should be applied to the V_{CC3} pin. The only connection to V_{CC3} should be R_{ST} as shown in Figure 3-5.

When V_{CC} = 5V all logic outputs and the data outputs are 5V compatible while the CML data inputs are still referenced to 3.3V from the internal regulator (see Figure 3-2). For low power operation, V_{CC} and V_{CC3} should be connected to an appropriate 3.3V ± 7.5% supply. In this case all I/Os are 3.3V compatible.

4.1.3 Choosing an Input AC-Coupling Capacitor

When AC-coupling the input the coupling capacitor should be of sufficient value to pass the lowest frequencies of interest, bearing in mind the number of consecutive identical bits, and the input resistance of the part. For SONET data, a good rule of thumb is to chose a coupling capacitor that has a cut-off frequency less than 1/(10,000) of the input data rate. For example, for 2.5 Gbps data, the coupling capacitor should be chosen as:

$f_{CUTOFF} \leq (2.5x10^9 / 10x10^3) = 250x10^3$

The -3 dB cutoff frequency of the low pass filter at the 50 Ω input is found as:

$f_{3dB} = 1/ (2 * \pi * 50\ \Omega * C_{AC})$

so solving for C where $f_{3dB} = f_{CUTOFF}$

$C_{AC} = 1/ (2 * \pi * 50\ \Omega * f_{CUTOFF})$ EQ.1

and in this case the minimum capacitor is 12 nF.

For Ethernet or Fibre Channel, there are less consecutive bits in the data, and the recommended cut-off frequency is 1/(1,000) of the input data rate. This results in a minimum capacitor of 1.5 nF for 2.125 Gbps Fibre Channel.

Multirate applications down to 155 Mbps

In this case, the input coupling capacitor needs to be large enough to pass 15 kHz ($155x10^6/10,000$) which results in a capacitor value of 0.2 µF. However, because this low pass frequency is close to the 25 kHz low pass frequency of the internal DC servo loop, it is preferable to use a larger input coupling capacitor such as 1 µF which provides an input cutoff frequency of 3.1 kHz. This separates the two poles sufficiently to allow them to be considered independent. This capacitor should also have a 10 nF capacitor in parallel to pass the higher frequency data (in the multirate application) without distortion.

In all cases, a high quality coupling capacitor should be used as to pass the high frequency content of the input data stream.

4.1.4 Using Rate Selection

Because of the performance of PECL outputs, the M02050-15 should not be used at data rates above 2.5 Gbps. When the $RATE_{SEL}$ pin (shown in Figure 3-10) is driven high, the M02050-15 bandwidth is set to its maximum which allows the M02050-15 to operate at data rates up to 2.5 Gbps. Because of the nature of the ESD structure on this pin, if it is driven by a device with I_{OL} or I_{OH} > 2 mA then a 1 kΩ to 10 kΩ resistor should be used in series with the $RATE_{SEL}$ pin. If rate selection is not used and the part is configured for high bandwidth only, the $RATE_{SEL}$ pin should be connected to V_{CC} using a 1 kΩ to 10 kΩ resistor. When operating at data rates ≤ 1.25 Gbps, then $RATE_{SEL}$ should be left floating (do not tie low). This enables low-rate mode which reduces the bandwidth (and thus the noise level) of the part.

4.1.5 Using $RSSI_{AVG}$

As shown in the typical applications circuit (Figure 4-1), when interfacing to a TIA that features a “MON” output such as the M02013 or M02016, the M02050-15 can reference the current sunk into the TIA “MON” output and produce a proportional current at the M02050-15 $RSSI_{AVG}$ output. The current is sourced into resistor R_{EXT} to ground creating a voltage suitable for DDMI applications. R_{EXT} should be chosen as:

R_{EXT} = 1/(maximum current into $RSSI_{AVG}$) EQ.2

This keeps the voltage at $RSSI_{AVG}$ between 0 and 1 V.

4.1.6 Setting the Signal Detect Level

Using Figure 4-3, the value for R_{ST} is chosen to set the LOS threshold at the desired value. The resulting hysteresis is also shown in Figure 4-3.

From Figure 4-3, it is apparent that small variations in R_{ST} cause significant variation in the LOS threshold level, particularly for low input signal levels. This is because of the logarithmic relationship between the RSSI voltage and the input signal level. It is recommended that a 1% resistor be used for R_{ST} and that allowance is provided for LOS variation, particularly when the LOS threshold is near the sensitivity limit of the M02050-15.

Example R_{ST} resistor values are given in Table 4-1.

Table 4-1. LOS Assert Levels for Various R_{ST} Resistor Values

VIN (mV pp) differential	R_{ST} (kΩ)
5.0	7.50
10.3	6.98
19.4	6.49
32.6	6.04
45.8	5.76

Figure 4-3. Loss of Signal Characteristic (Extended Range)

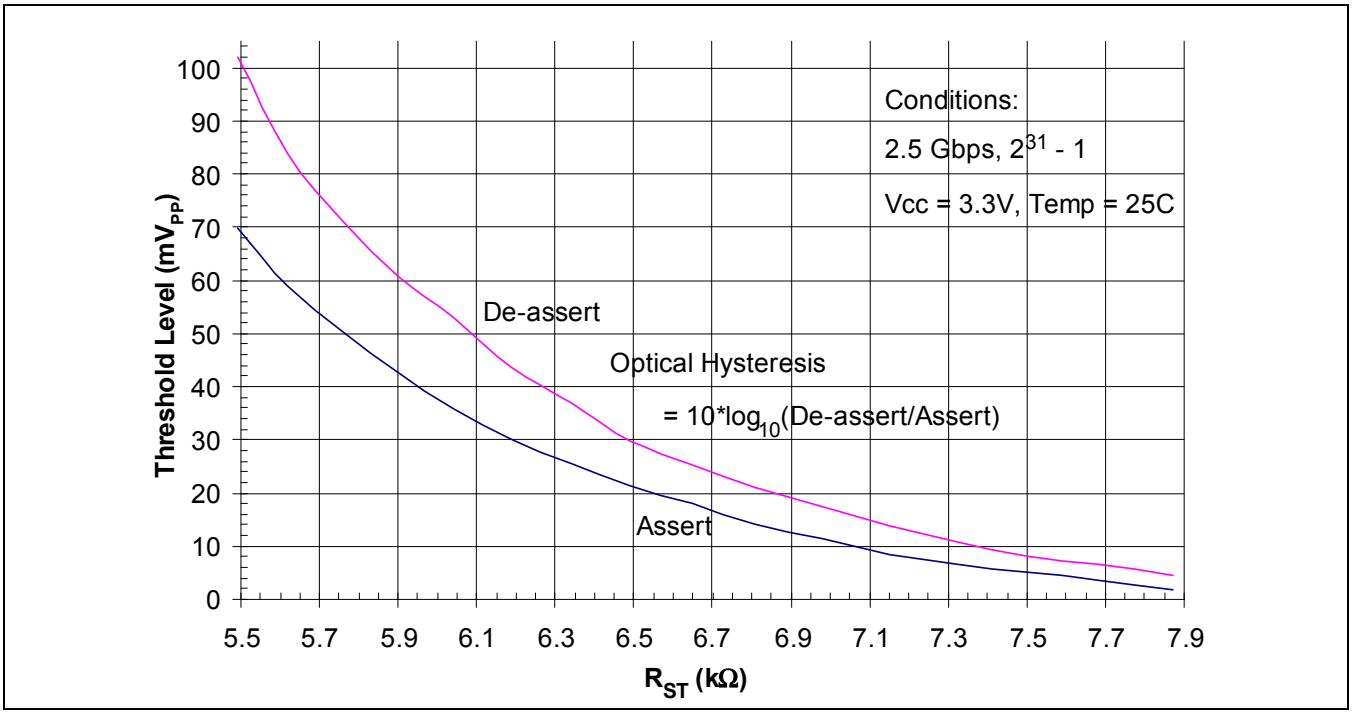


Figure 4-4. Loss of Signal Characteristic (Low Input Signal)

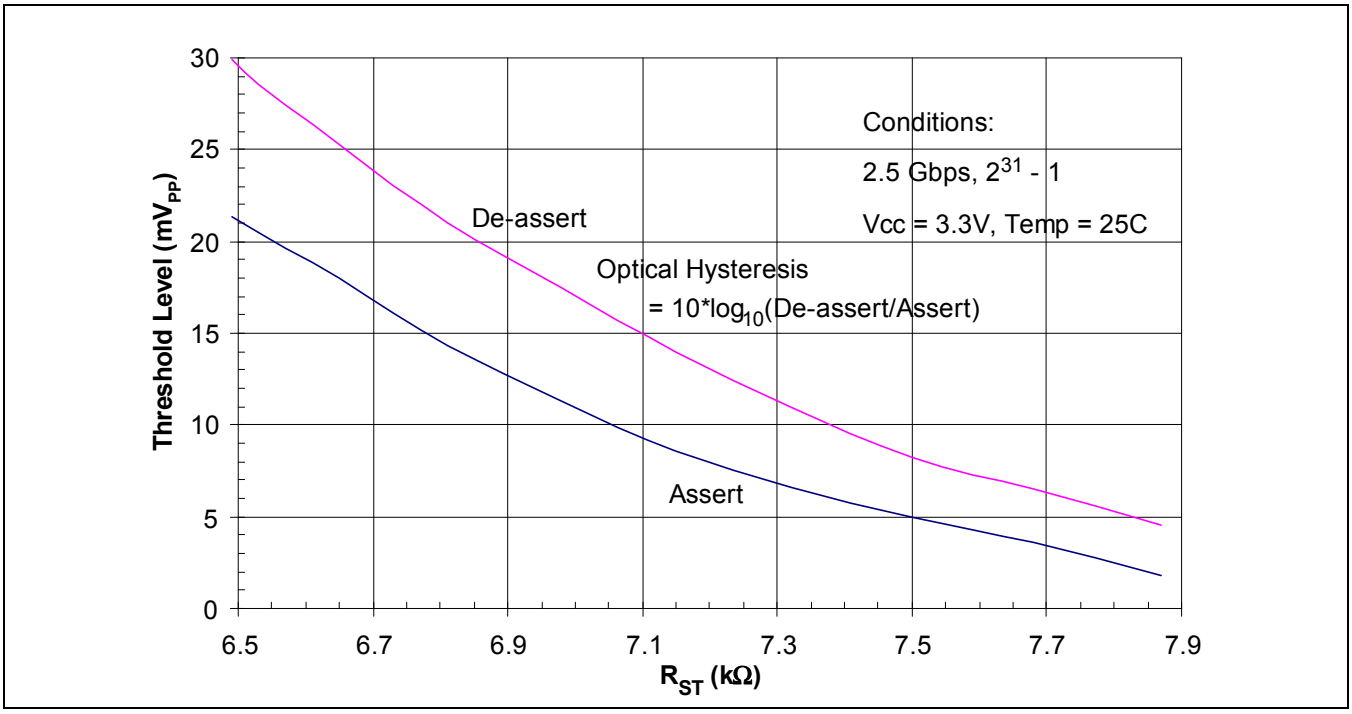
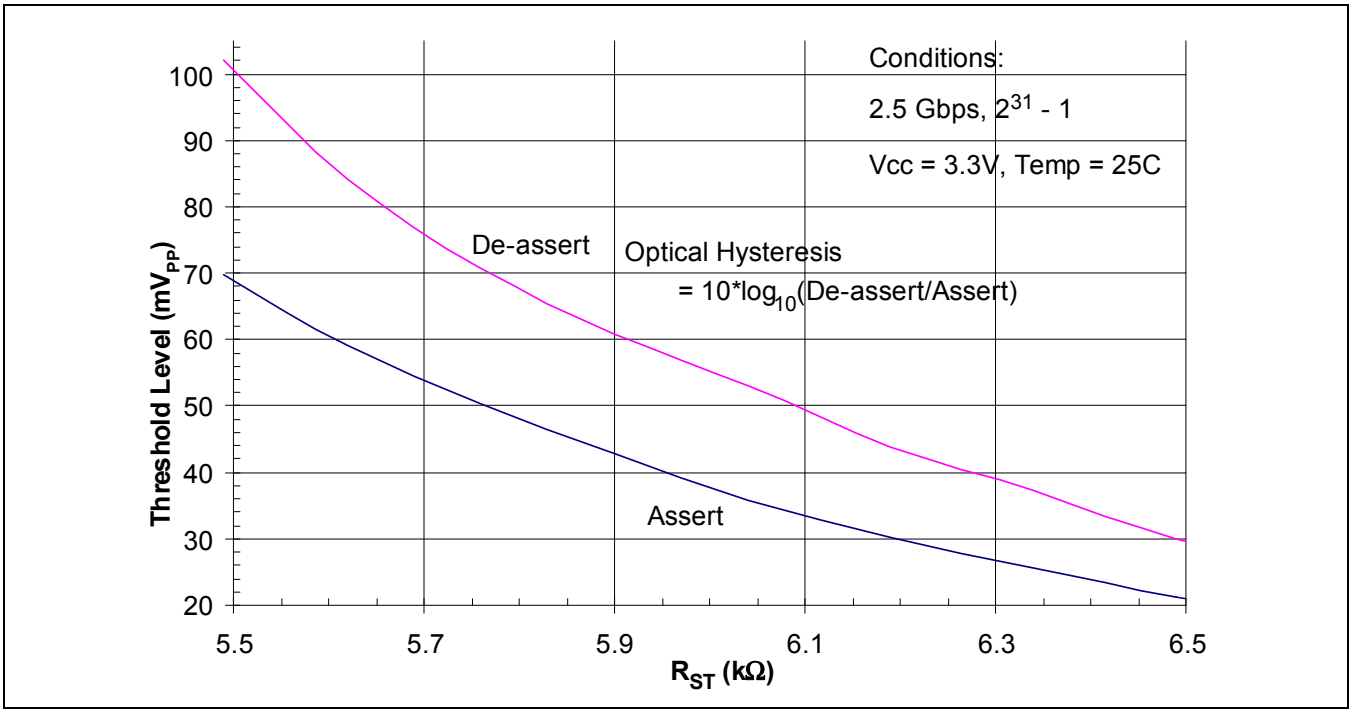


Figure 4-5. Loss of Signal Characteristic (High Input Level)



4.1.7 PECLP and PECLN Termination

The outputs of the M02050-15 are PECL compatible and any standard AC or DC-coupling termination technique can be used. Figure 4-6 and Figure 4-7 illustrate typical AC and DC terminations.

AC-coupling is used in applications where the average DC content of the data is zero e.g. SONET. The advantage of this approach is lower power consumption, no susceptibility to DC drift and compatibility with non-PECL interfaces. Figure 4-6 shows the circuit configuration and Table 4-2 lists the resistor values. If using transmission lines other than 50 Ω, the shunt terminating resistance Z_T should equal twice the impedance of the transmission line (Z_O).

DC-coupling can be used when driving PECL interfaces and has the advantage of a reduced component count. A Thevenin termination is used at the receive end to give a 50 Ω load and the correct DC bias. Figure 4-7 shows the circuit configuration and Table 4-2 the resistor values.

Alternatively, if available, terminating to V_{CC} - 2V as shown in Figure 4-8 has the advantage that the resistance value is the same for 3.3 V and 5 V operation and it also has performance advantages at high data rates.

Table 4-2. PECL Termination Resistor Values

Supply	Output Impedance	$R_{PULL-DOWN}$	Z_T	R_{TA} / R_{TB}	R_T / R_B
5V	50 Ω	270 Ω	100 Ω	2.7 kΩ / 7.8 kΩ	82 Ω / 130 Ω
3.3V	50 Ω	150 Ω	100 Ω	2.7 kΩ / 4.3 kΩ	130 Ω / 82 Ω

Figure 4-6. AC-Coupled PECL Termination

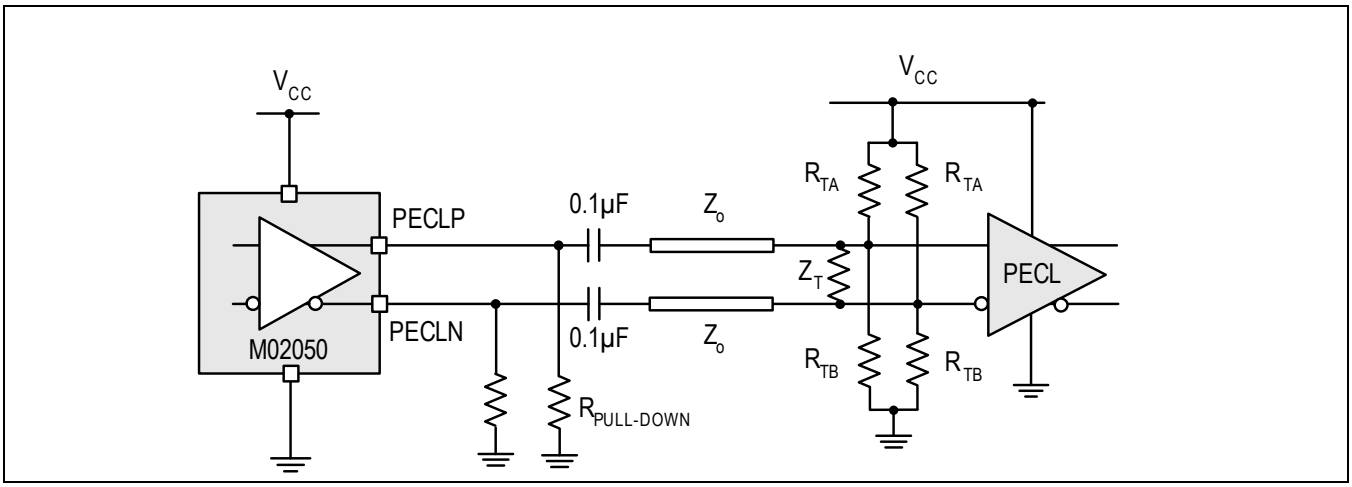


Figure 4-7. DC-Coupled PECL Termination

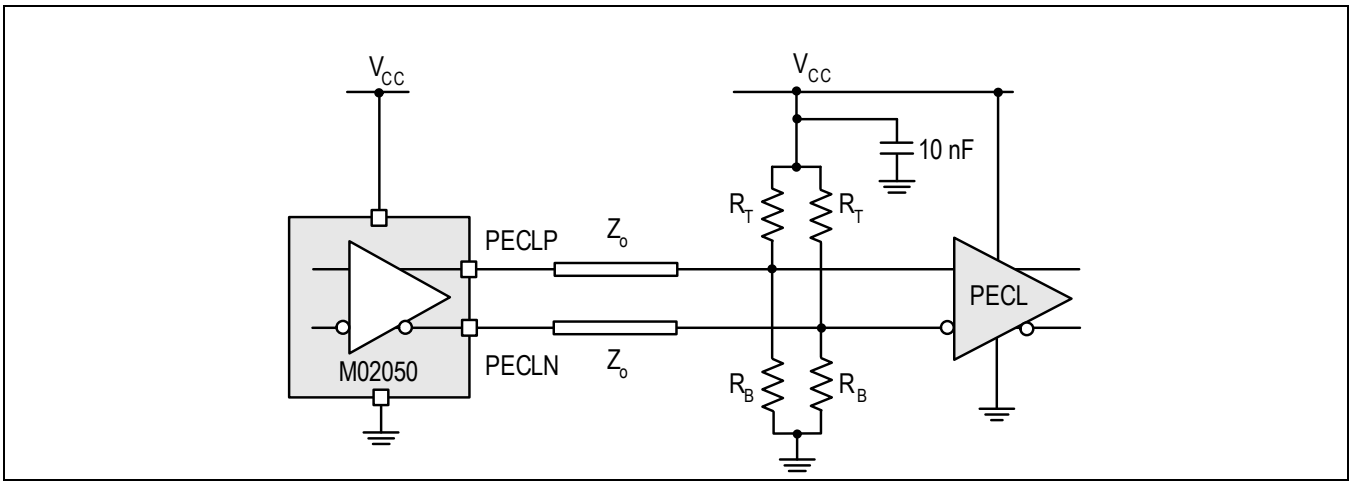
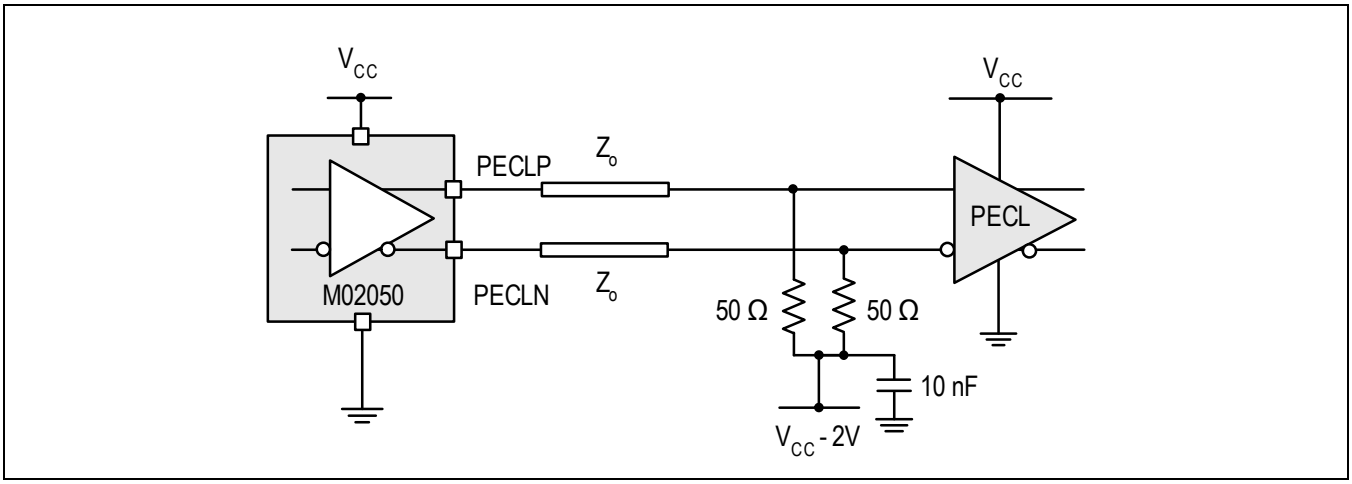
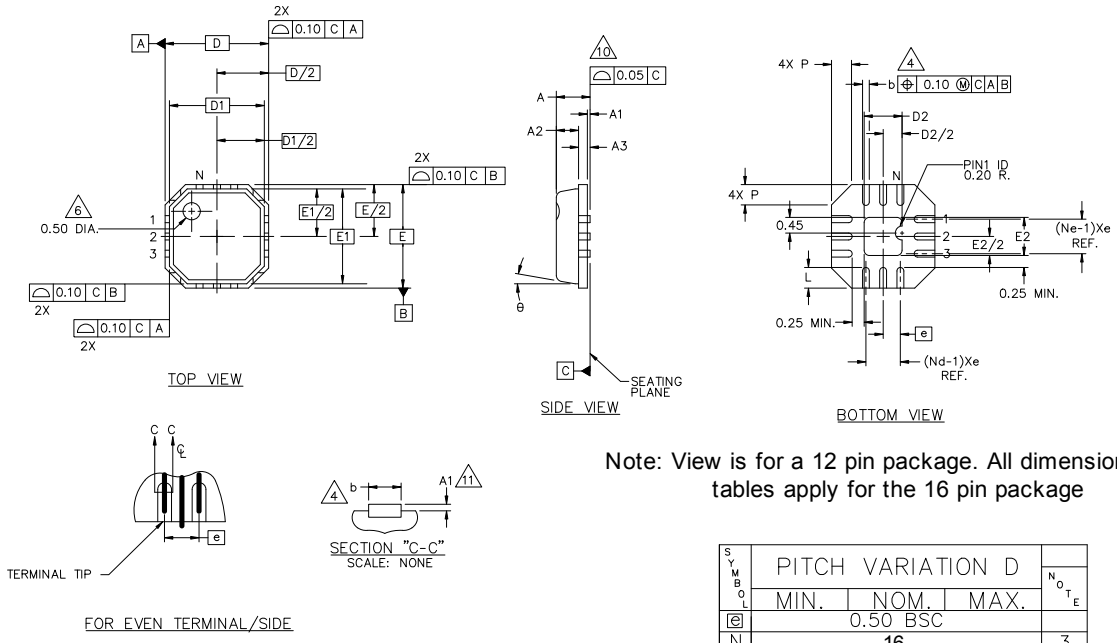


Figure 4-8. Alternative PECL Termination



5.0 Package Specification

Figure 5-1. Package Information



Note: View is for a 12 pin package. All dimensions in the tables apply for the 16 pin package

SYMBOL	PITCH VARIATION D			NOTE
	MIN.	NOM.	MAX.	
e		0.50 BSC		
N		16		3
Nd		4		3
Ne		4		3
L	0.30	0.40	0.50	
b	0.18	0.23	0.30	4
D2	1.35	1.50	1.65	
E2	1.35	1.50	1.65	

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	-	0.85	0.90	
A1	0.00	0.01	0.05	11
A2	-	0.65	0.70	
A3		0.20 REF.		
D		3.00 BSC		
D1		2.75 BSC		
E		3.00 BSC		
E1		2.75 BSC		
θ			12°	
P	0.24	0.42	0.60	

NOTES:

2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. - 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. THE SHAPE SHOWN ON FOUR CORNERS ARE NOT ACTUAL I/O.
9. PACKAGE WARPAGE MAX 0.05mm.
10. APPLIED FOR EXPOSED PAD AND TERMINALS.
    EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
11. APPLIED ONLY FOR TERMINALS.