

FEATURES

- Wide Input Voltage from 3V to 8.5V
- Adjustable Output Voltage from 0.6V to 5.5V
- 6A Continuous Output Current
- Constant On Time (COT) Control
- Force Continuous Conduction Mode (FCCM) for Light Load
- Stable with low ESR Ceramic Capacitors
- 1.4MHz Switching Frequency
- Pre-Biased Start-Up
- Power Good (PG) Indicator
- Programable Soft-Start Time
- Cycle-by-Cycle Current Limit Protection
- Short Circuit and Over-Load Hiccup Protection
- Thermal Shutdown Protection
- LGA-19 (3mm×3.1mm×1.7mm) Package
- Pb-Free RoHS Compliant

APPLICATIONS

- PoL Power Supply
- Data Center
- Solid-State and Hard Disk Drives
- Industrial & Medical System

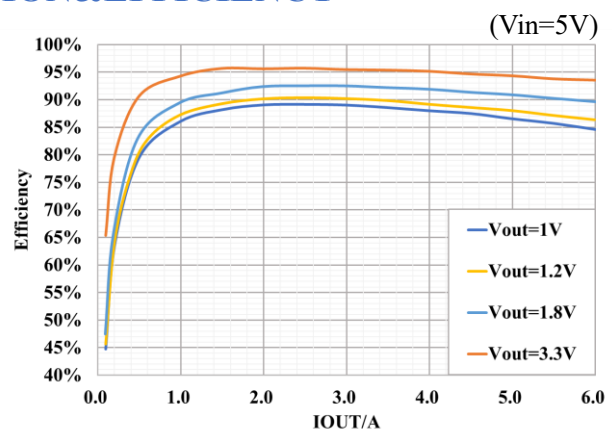
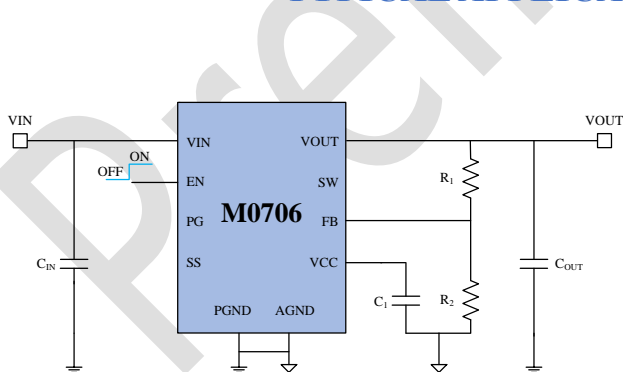
DESCRIPTION

The M0706 is a 6A step-down switching mode Power SoC (System on Chip) with integrated power MosFETs, inductor in LGA-19 package. The input voltage is from 3V to 8.5V and the switching frequency is fixed at 1.4MHz.

The M0706 provides high efficiency with Constant On Time (COT) control mode for fast transient response and good loop stability. For M0706, it works on FCCM which keeps low output ripple.

The M0706 indicates faults by PG and provides short circuit and over-load hiccup protection and over temperature shutdown protection.

TYPICAL APPLICATION&EFFICIENCY



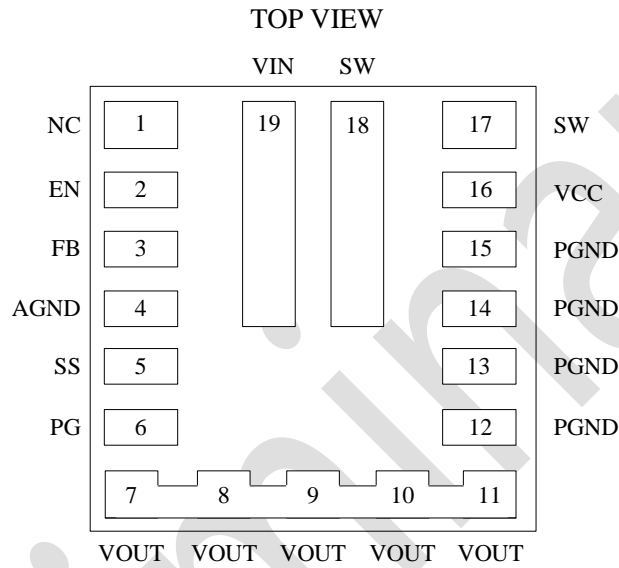


ORDERING INFORMATION

PART NUMBER	TOP MARKING	PACKAGE	MOQ	MSL
M0706DLFF	M0706 YWWLLL	LGA-19 (3mm×3.1mm×1.7mm)	3000/ Tape & Reel	3

NOTES: Y: Year, WW: Week, LLL: Lot Number.

PACKAGE REFERENCE

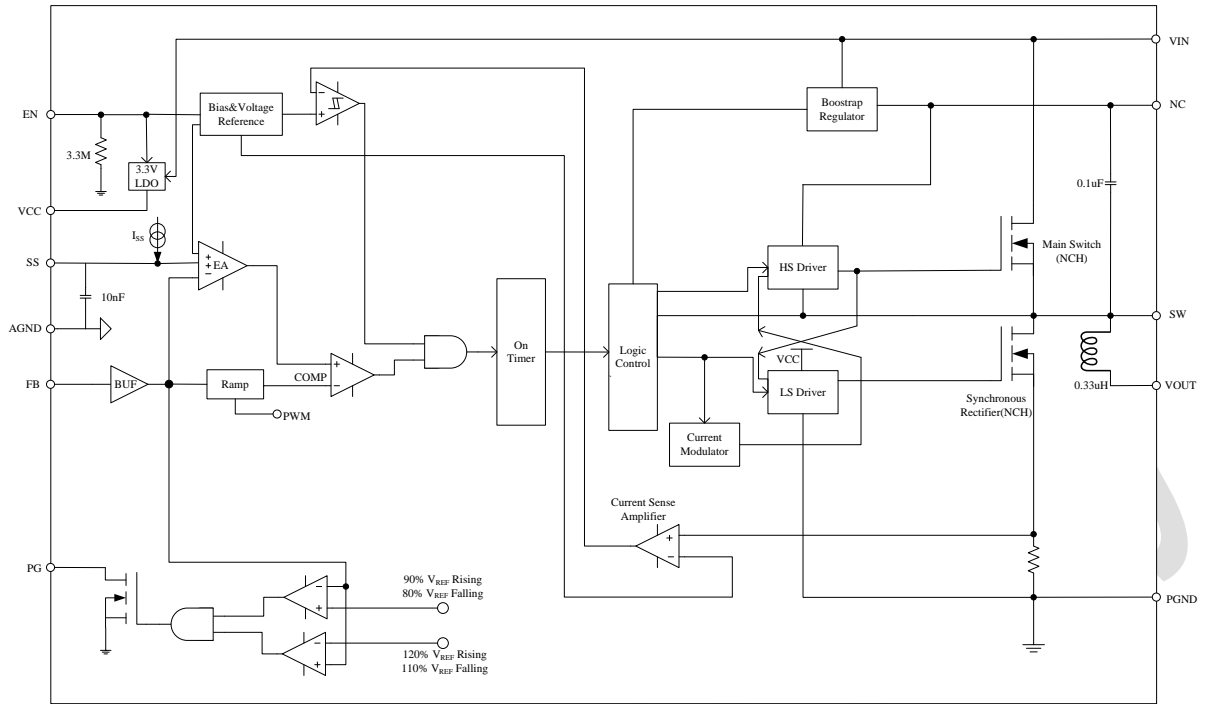


**PIN FUNCTIONS**

PIN #	NAME	DESCRIPTION
1	NC	Not Connected.
2	EN	Enable Control. Pulling this pin low shuts the chip down. Pulling it high enables the chip.
3	FB	Feedback. Connect this pin with an external resistor divider from the output to AGND to set the output voltage.
4	AGND	Analog Ground.
5	SS	Soft Start. A decoupling ceramic capacitor is recommended to be placed close to this pin. The capacitance determines the soft-start time.
6	PG	Power Good. The output of PG is an open drain, a pull-up resistor to power source is needed if used.
7,8,9,10,11	VOUT	Output Voltage. Connect this pin with the load. Output capacitors are recommended to be placed between VOUT and PGND
12,13,14,15	PGND	Power Ground.
16	VCC	LDO Output. An output capacitor to AGND is recommended to be placed close to VCC directly.
17,18	SW	Internal SW Pad.
19	VIN	Input Voltage. VIN supplies power to all the internal control circuitry and the power switch. A decoupling capacitor to ground is recommended to be placed close to VIN directly.



FUNCTIONAL BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

	SYMBOL	MIN	MAX	UNIT
Voltage at Pins	V _{IN}	-0.3	10	V
Voltage at Pins	V _{EN}		V _{IN}	V
Voltage at Pins	V _{SW}	-0.3	V _{IN} +0.7	V
Voltage at Other Pins		-0.3	4	V
Junction Temperature Range	T _J	-40	125	°C
Storage Temperature Range	T _S	-55	150	°C
Power Dissipation (T _A =+25°C)	P _D Notes 1)		3.13	W

RECOMMENDED OPERATING CONDITIONS

	SYMBOL	MIN	MAX	UNIT
Input Voltage Range	V _{IN}	3	8.5	V
Output Voltage Range	V _{OUT}	0.6	5.5	V
Output Current	I _{OUT}		6	A
Junction Temperature Range	T _J	-40	125	°C

THERMAL RESISTANCE

	SYMBOL	MIN	MAX	UNIT
Junction to Ambient	θ _{JA} Notes 2)		32	°C/W
Junction to Case	θ _{JC} Notes 2)		1	°C/W

NOTES:

- 1) The maximum allowable continuous power dissipation at any ambient temperature (T_A) is calculated by $P_D(\max) = (T_J(\max) - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the power module will go into thermal shutdown.
- 2) Measured on EVB, 4-layer 2oz.

**ELECTRICAL CHARACTERISTICS** $V_{IN}=5V$, $V_{OUT}=1V$, $T_A=25^{\circ}C$, unless otherwise noted.

PARAMETERS	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}		3		8.5	V
VCC under Voltage Lockout Threshold	V_{CCUVLO}	V_{CC} Increasing	2.7	2.8	2.9	V
VCC under Voltage Lockout Hysteresis				325		mV
VCC Regulator	VCC			3.4		V
Shutdown Current	I_{SD}	$V_{EN}=0$			5	μA
Quiescent Current (No Switching)	I_Q	$V_{FB}=0.65V$		100	150	μA
EN On Threshold		V_{EN} Increasing	1.1	1.25	1.4	V
EN Off Threshold		V_{EN} Decreasing	0.9	1	1.1	V
EN Internal Pull-Down Resistor				3.3		$M\Omega$
Feedback Voltage	V_{FB_REF}	$T_J=25^{\circ}C$	594	600	606	mV
Feedback Current	I_{FB}	$V_{FB}=700mV$		10	100	nA
Valley Current Limit				8		A
Switching Frequency	F_{SW}		1.2	1.4	1.6	MHz
Soft-Start Current	I_{SS}		4	6	8	μA
PG Output Low Voltage		sink 4mA			0.4	V
PG High Threshold	V_{PGH_R}	V_{FB} Rising, V_{FB} in respect to V_{FB_REF} , $V_{OUT} < Target$	85	90	95	%
	V_{PGH_F}	V_{FB} Falling, V_{FB} in respect to V_{FB_REF} , $V_{OUT} > Target$	105	110	115	%
PG Low Threshold	V_{PGL_R}	V_{FB} Rising, V_{FB} in respect to V_{FB_REF} , $V_{OUT} > Target$	115	120	125	%
	V_{PGL_F}	V_{FB} Falling, V_{FB} in respect to V_{FB_REF} , $V_{OUT} < Target$	75	80	85	%
PG Delay	T_{PG_DELAY}			45		μs
Thermal Shutdown				150		$^{\circ}C$
Thermal Shutdown Hysteresis				20		$^{\circ}C$



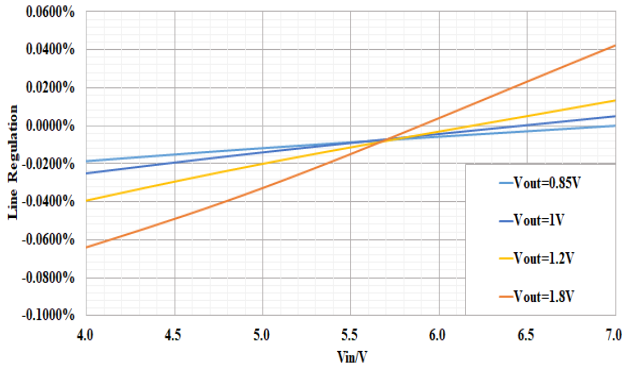
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN}=5V$ and $V_{OUT}=1.2V$, $T_A=25^{\circ}C$, unless otherwise noted.

Line Regulation

$V_{OUT}=0.85V/1V/1.2V/1.8V$, $I_{OUT}=6A$,

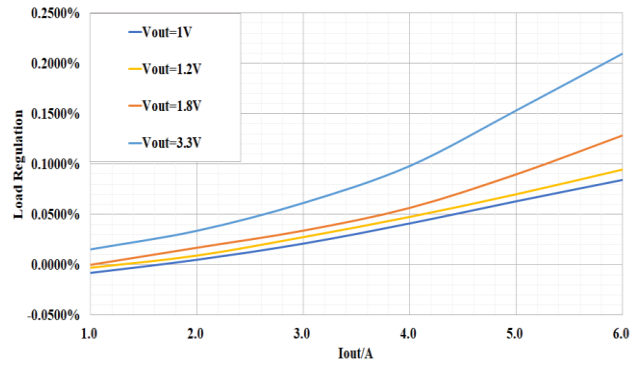
$V_{IN}=4V\sim 7V$



Load Regulation

$V_{IN}=5V$, $V_{OUT}=1V/1.2V/1.8V/3.3V$,

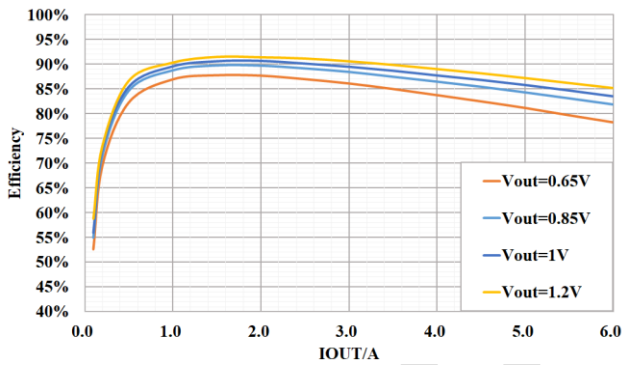
$I_{OUT}=1A\sim 6A$



Efficiency

$V_{IN}=3.3V$, $V_{OUT}=0.65V/0.85V/1V/1.2V$,

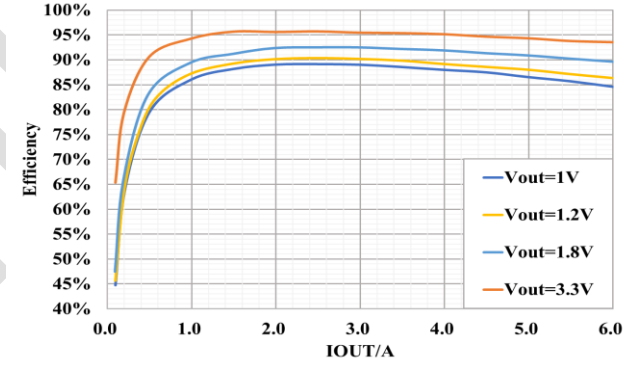
$I_{OUT}=0A\sim 6A$



Efficiency

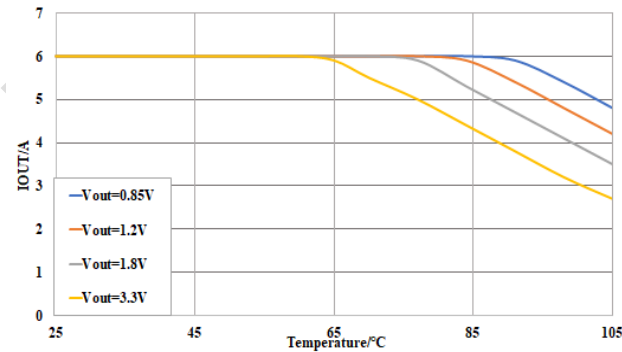
$V_{IN}=5V$, $V_{OUT}=1V/1.2V/1.8V/3.3V$,

$I_{OUT}=0A\sim 6A$



Thermal Derating

$V_{IN}=5V$, $V_{OUT}=0.85V/1.2V/1.8V/3.3V$



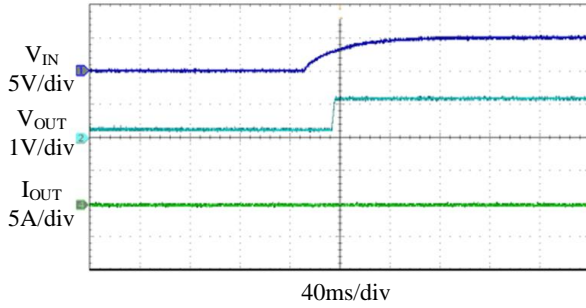


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN}=5V$ and $V_{OUT}=1.2V$, $T_A=25^{\circ}C$, unless otherwise noted.

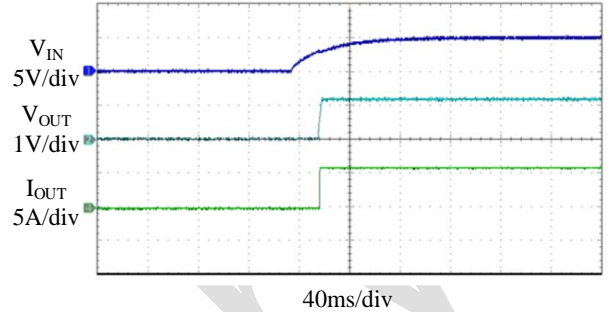
VIN Start-up

$I_{OUT}=0A$



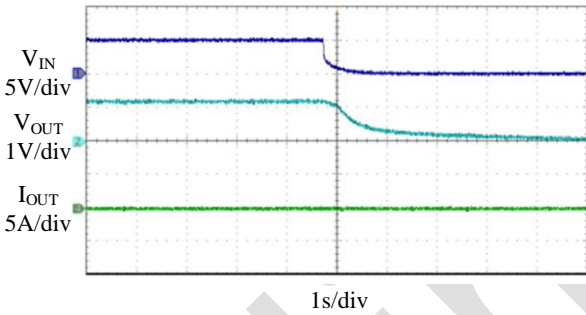
VIN Start-up

$I_{OUT}=6A$



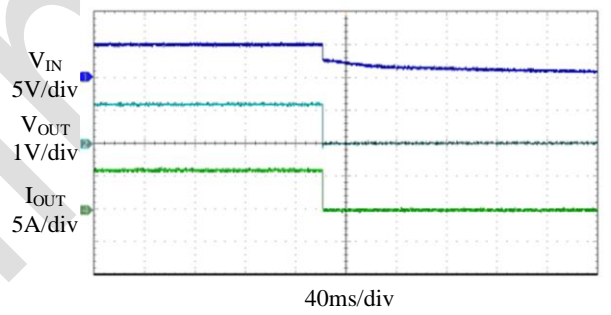
VIN Shutdown

$I_{OUT}=0A$



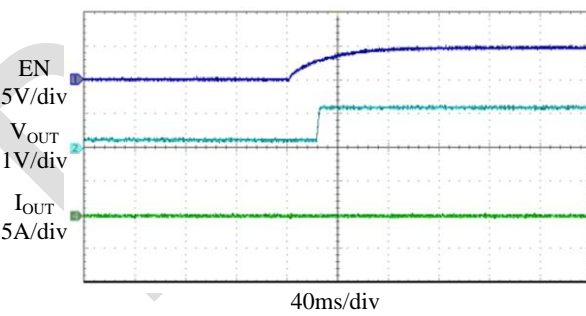
VIN Shutdown

$I_{OUT}=6A$



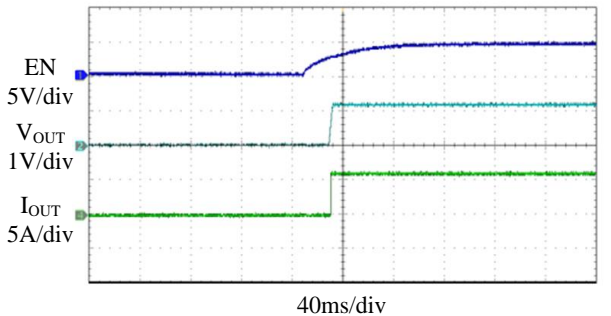
EN Start-up

$I_{OUT}=0A$



EN Start-up

$I_{OUT}=6A$



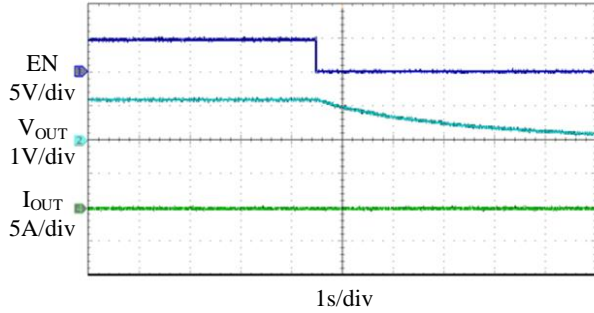


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

$V_{IN}=5V$ and $V_{OUT}=1.2V$, $T_A=25^{\circ}C$, unless otherwise noted.

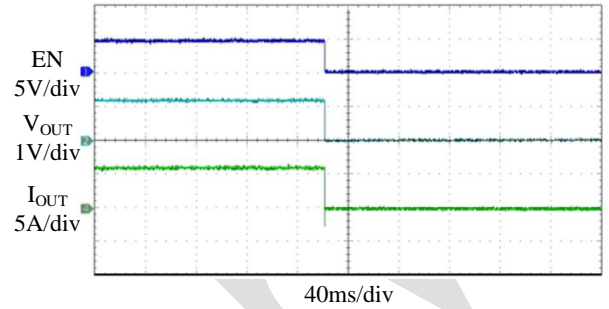
EN Shutdown

$I_{OUT}=0A$



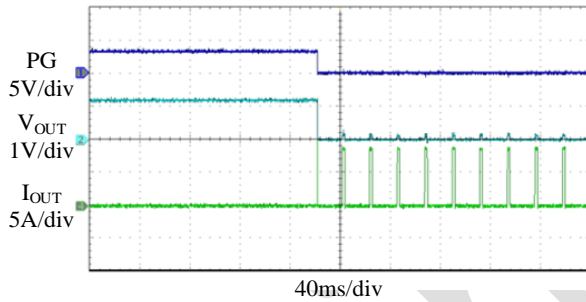
EN Shutdown

$I_{OUT}=6A$



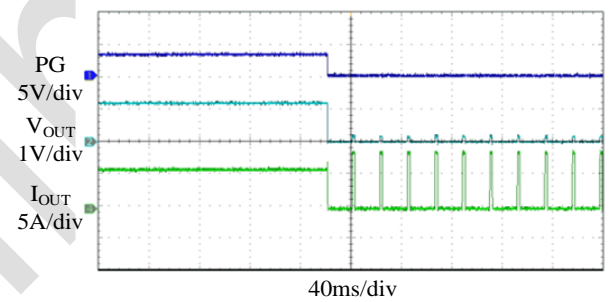
SCP Entry

$I_{OUT}=0A$



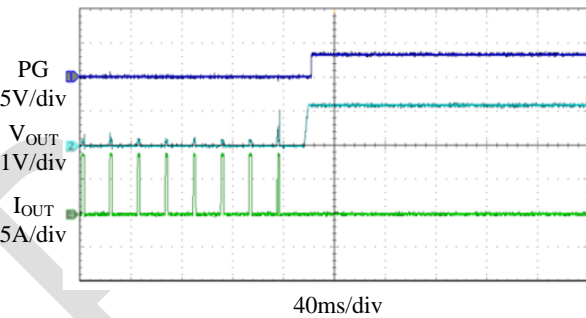
SCP Entry

$I_{OUT}=6A$



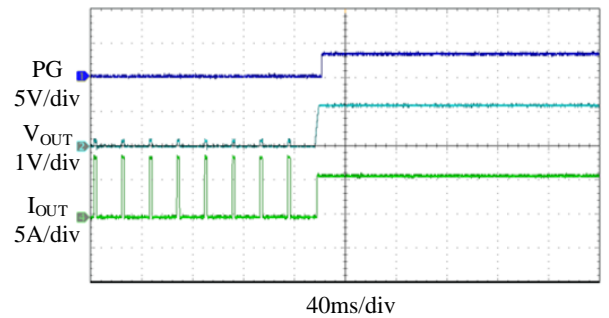
SCP Recovery

$I_{OUT}=0A$



SCP Recovery

$I_{OUT}=6A$



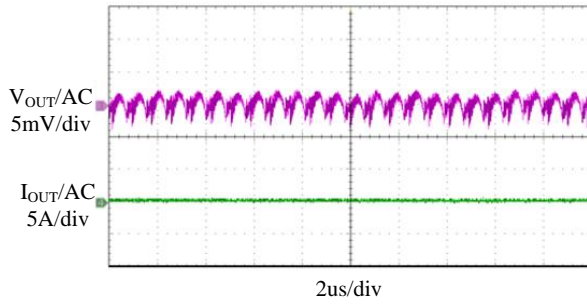


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

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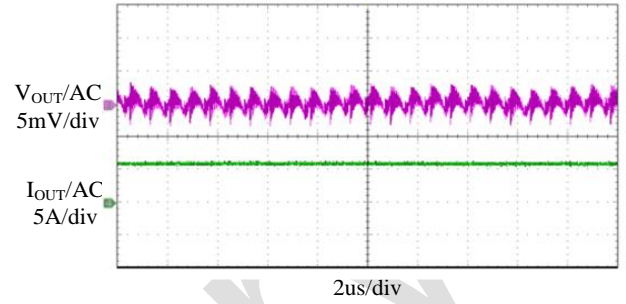
VOUT Ripple

$I_{OUT}=0A$



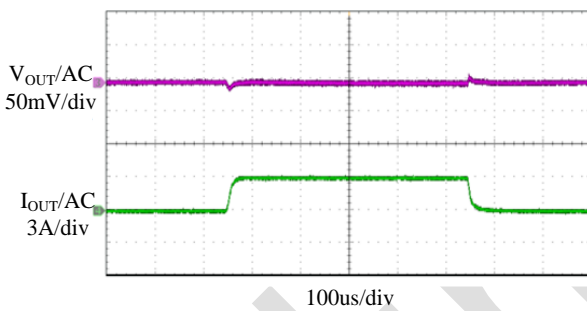
VOUT Ripple

$I_{OUT}=6A$



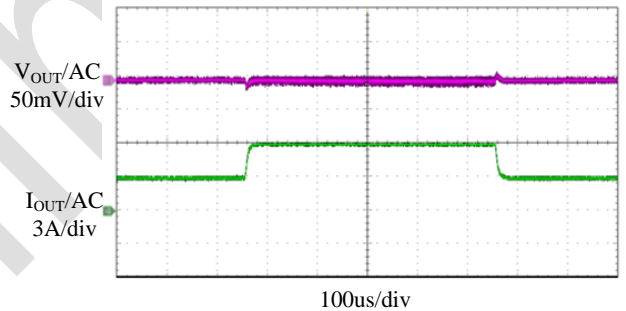
Load Transient

$I_{OUT}=0A$ to $3A$, $2.5A/\mu s$



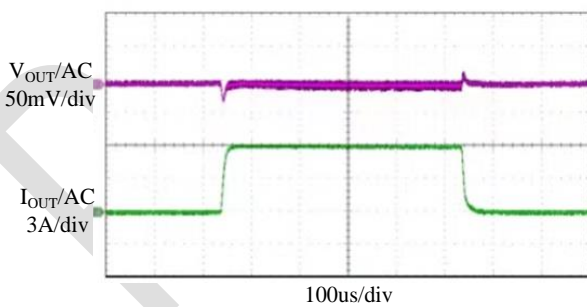
Load Transient

$I_{OUT}=3A$ to $6A$, $2.5A/\mu s$



Load Transient

$I_{OUT}=0A$ to $6A$, $2.5A/\mu s$





OPERATION

The M0706 is a 6A synchronous step-down switching mode Power SoC with integrated High-Side and Low-Side power MosFETs and inductor in LGA-19 package. FB resistor divider and input and output capacitors are needed to complete the design over 3V to 8.5V input voltage range. The M0706 supports output voltage of 0.6V to 5.5V with the fixed switching frequency of 1.4MHz.

M0706 works on COT control mode that offers excellent transient response over the wide range of input voltage. M0706 operates in Force Continuous Conduction Mode which keeps low output ripple. And M0706 has 1.2ms soft-start timer internally. The soft start time also can be programmed by the capacitor externally.

Fully integrated protection features include OCP, UVP and OTP and all these faults can be indicated by PG. The protection function details are shown below.

OVER CURRENT PROTECTION (OCP)

M0706 has a typical 8A cycle-by-cycle Low-Side valley limit protection. When the Low-Side MosFET reaches the current limit, M0706 will enter hiccup mode. It will stop switching for a pre-determined period of time and automatically start up again. It always starts up with soft-start to limit inrush current and avoid output overshoot.

OVER TEMPERATURE PROTECTION (OTP)

M0706 will stop switching when the junction temperature exceeds 150 °C. The device will power up again when the junction temperature drops below 130°C.



USER GUIDE

Output Voltage

The output voltage is set by the external feedback resistor divider as the typical application circuit on Page 1. The bottom feedback resistor R_2 can impact the loop stability, R_2 is recommended to be between 2k Ω and 100k Ω . For any chosen R_2 , the top feedback resistor R_1 can be calculated as:

$$R_1 = R_2 \cdot \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: FB Resistor Values for Common Output Voltages.

$V_{OUT}(V)$	$R_1(k\Omega)$	$R_2(k\Omega)$	$C_{FF}(pF)$
3.3	20	4.44	56
2.5	20	6.34	56
1.8	20	10	56
1.5	20	13	56
1.2	20	20	56
1.0	20	30	56

And a feedforward capacitor C_{FF} is recommended for better load transient response, which typical value is 56pF. A 1k Ω feedforward resistor R_f connected to FB is also recommended for better loop stability.

Input Capacitor

The input current of the step-down converter is discontinuous with sharp edges, therefore an input filter capacitor is necessary. For better performance, low ESR ceramic capacitor with X5R or X7R dielectrics are highly recommended because of their lowest temperature variations. The RMS current of the input capacitor is calculated:

$$I_{CIN_RMS} = I_{OUT} \sqrt{D(1-D)}$$

in which D is the Duty Cycle and when the current is continuous, $D = V_{OUT}/V_{IN}$; I_{OUT} is the output load current. As the equation above, when D is 0.5, the highest RMS current is approximately:

$$I_{CIN_RMS} = \frac{1}{2} \times I_{OUT}$$

So, it is recommended to choose the capacitor with the RMS current rating higher than $1/2 I_{OUT}$.

The power dissipation on the input capacitor can be estimated with the RMS current and the ESR resistor.

Electrolytic or tantalum capacitors can also be used. Small size ceramic capacitor ranging from 10nF to 0.1 μ F is recommended to be placed closed to V_{IN} and PGND. The input voltage ripple caused by the capacitor can be calculated as:

$$\Delta V_{CIN} = \frac{I_{OUT}}{F_{SW} \cdot C_{IN}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

in which, F_{SW} is switching frequency of 1.4MHz.

Output Capacitor

Output capacitors are required to keep stable output voltage. To minimize the output voltage ripple, low ESR ceramic capacitors should be used. The output voltage ripple can be estimate as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8F_{SW}^2 C_{OUT} L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

In which, $L = 0.33\mu$ H.

If electrolytic or tantalum capacitors are used, the ESR will dominate the output voltage ripple as:

$$\Delta V_{OUT} = R_{ESR} \cdot \frac{V_{OUT}}{F_{SW} L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Enable Control

When input voltage is above the under-voltage-lock-out threshold, M0706 can be enabled by pulling the EN pin to above 1.25V and will be disabled if the EN pin is below 1V. It is recommended to pull up to V_{IN} with the resistor about 100k Ω .

Power Good Indicator

M0706 has an open drain PG indicator. PG will be pulled up if output voltage is within $\pm 10\%$ of regulation, otherwise PG is pulled down by internal NMOS. A pull-up resistor to V_{IN} or V_{OUT} is needed if used and it is recommended to choose the resistor about 100k Ω .

Soft Start Time

M0706 has 1.2ms default soft-start time internally. The time can be increased by adding an external capacitor



8.5V Input, 6A Step Down DC-DC Power SoC with Integrated Inductor

C_{SS} between SS and AGND. C_{SS} can be calculated as:

$$C_{SS}(nF) = \frac{T_{SS}(ms) \times 6(\mu A) \times 0.83}{0.6(V)} - 10nF$$

Pre-Biased Start-Up

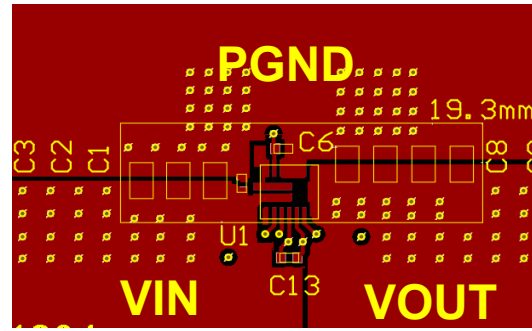
The M0706 is designed for start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the internal BST voltage is refreshed and charged, and the voltage on the SS capacitor is charged as well. If the internal BST voltage exceeds its rising threshold voltage and the SS capacitor voltage exceeds the sensed voltage at FB, the part begins working normally.

PCB Layout Guide

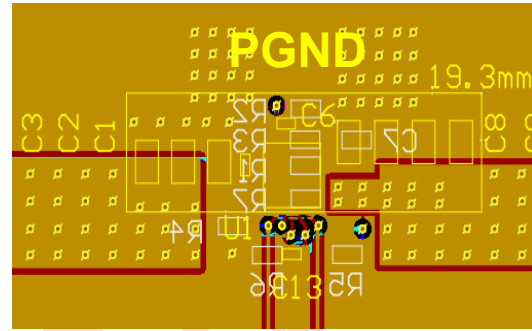
To optimize the electrical and thermal performance, some PCB layout guidelines should be considered as below:

1. Use wide trace for the high current paths and keep it as short as possible. It helps to minimize the PCB conduction loss and thermal stress.
2. Place the input decoupling capacitor close to VIN and PGND.
3. Connect all feedback network to FB shortly and directly and keep it as close to the Power IC as possible.
4. Keep the components away from the SW to prevent stray capacitive noise pick-up.
5. The PGND should be connected to a strong ground plane for better heat dissipation and noise protection.

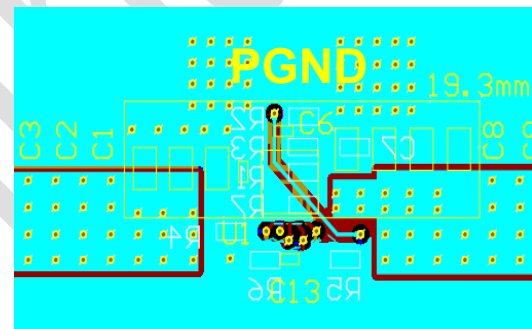
Figure 1 gives a good example of the recommended layout.



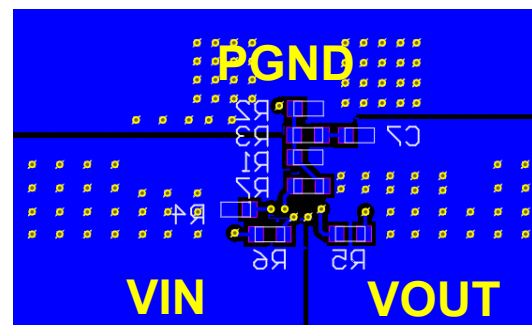
(a) Top Layer



(b) Inner Layer 1



(c) Inner Layer 2



(d) Bottom Layer

Figure 1. Recommended Layout



TYPICAL APPLICATION

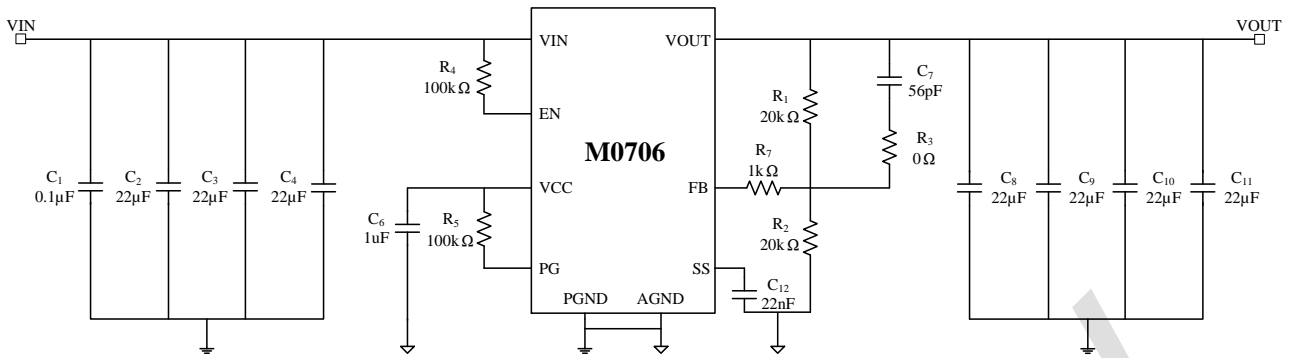


Figure 2. Typical Application Circuits of M0706 for 1.2V Output

Table 2: M0706 Reference Design for 5V Input

VOUT	CIN	COUT	TARGET VOUT RIPPLE	R1	R2
3.3V	3×22µF	5×22µF	35mV	20kΩ	4.44kΩ
1.8V	3×22µF	4×22µF	20mV	20kΩ	10kΩ
1.2V	2×22µF	3×22µF	12mV	20kΩ	20kΩ
1.0V	2×22µF	3×22µF	12mV	20kΩ	30kΩ

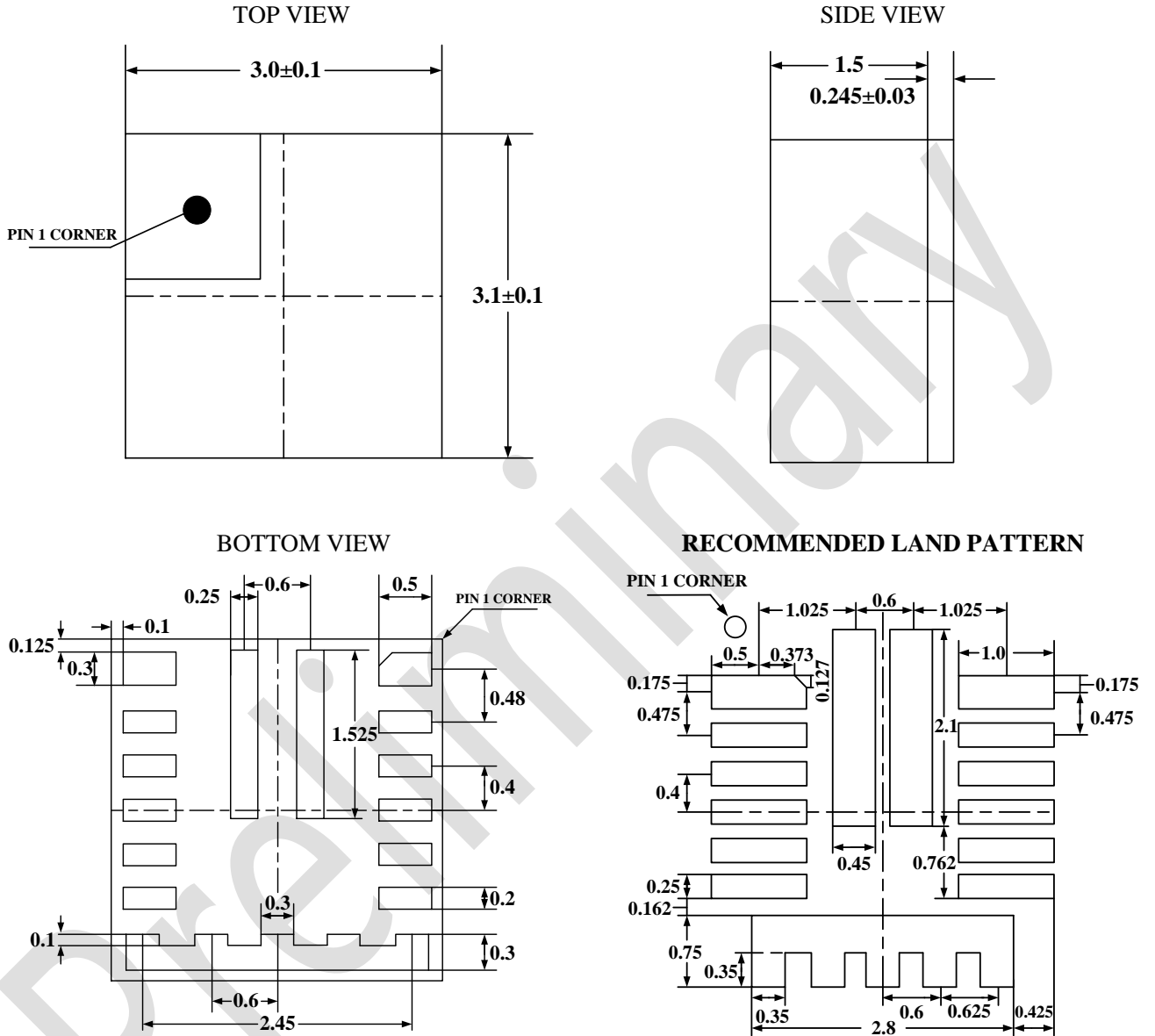
NOTES:

CIN is the sum of the input capacitors, COUT is the sum of the output capacitors, please refer to Figure 2 for parameters of other components.



PACKAGE INFORMATION

LGA-19 (3mm×3.1mm×1.7mm) Package

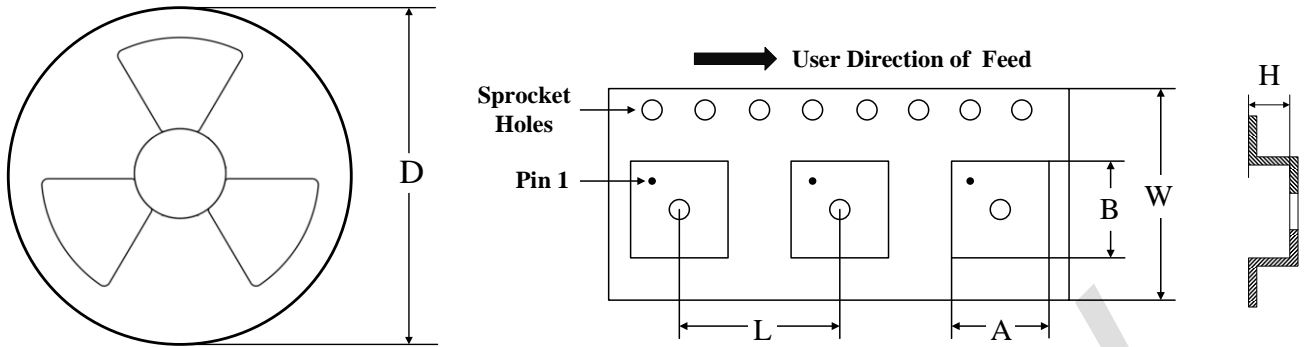


NOTES:

All dimensions are in MM.



CARRIER INFORMATION



PART NUMBER	PACKAGE	QUANTITY /REEL	D	A	B	L	W	H
M0706DLFF	LGA-19 (3mm×3.1mm×1.7mm)	3000	13 in	3.25mm	3.25mm	8mm	12mm	2.06mm