MOS INTEGRATED CIRCUITS

M 082
M 083
M 086

PRELIMINARY DATA

TONE GENERATOR

- M 082 (30% Duty Cycle) 13 TONE OUTPUTS
- M 083 (50% Duty Cycle) 13 TONE OUTPUTS
- M 086 (50% Duty Cycle) 12 TONE OUTPUTS
- SINGLE POWER SUPPLY
- WIDE SUPPLY VOLTAGE OPERATING RANGE
- LOW POWER DISSIPATION < 500 mW
- HIGH OUTPUT DRIVE CAPABILITY
- HIGH ACCURACY OF OUTPUT FREQUENCIES: ERROR LESS THAN ± 0.069%
- INPUT PROTECTED AGAINST STATIC CHARGES
- LOW INTERMODULATION

The M 082, M 083 and M 086 are monolithic tone generators specifically designed for electronic organs. Constructed on a single chip using low threshold N-channel silicon gate technology they are supplied in a 16 lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS*

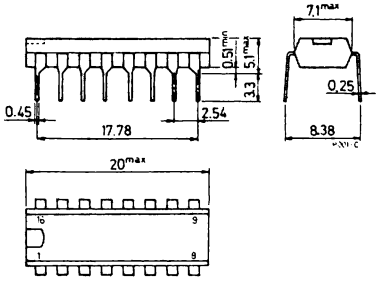
V_I	Voltage on any pin relative to V_{SS} (GND)	+20 to -0.3	V
T_{op}	Operating temperature	0 to 50	°C
T_{stg}	Storage temperature	-65 to 150	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING NUMBERS: M 082 B1
M 083 B1
M 086 B1

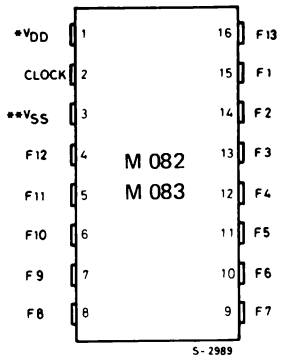
MECHANICAL DATA

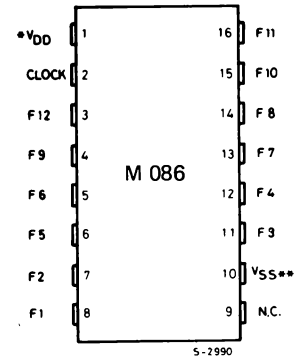
Dimensions in mm



M 082
M 083
M 086

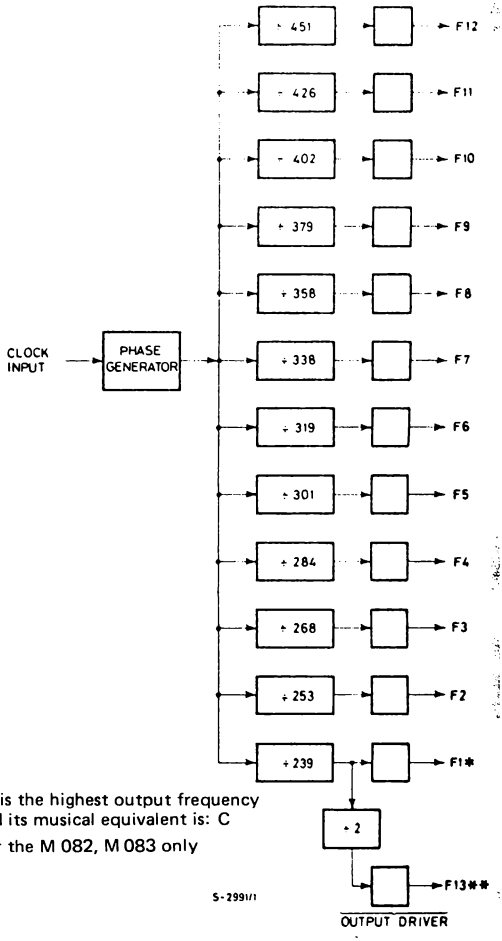
CONNECTION DIAGRAMS





* V_{DD} is the highest supply voltage
** V_{SS} is the lowest supply voltage

BLOCK DIAGRAM



* F1 is the highest output frequency and its musical equivalent is: C
** For the M 082, M 083 only

RECOMMENDED OPERATING CONDITIONS

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
V_{SS}	Lowest supply voltage		0		0	V
V_{DD}	Highest supply voltage		+10	+12	+14	V

ELECTRICAL CHARACTERISTICS ($0°C \leq T_{amb} \leq 50°C$; $V_{SS}=0V$; $V_{DD}=+10V$ to $+14V$ unless otherwise specified)

Parameter		Test conditions	Values			Unit	Fig.
			Min.	Typ.	Max.		
V_{IL}	Input clock, low		V_{SS}		$V_{SS}+1$	V	1
V_{IH}	Input clock, high		$V_{DD}-1$		V_{DD}	V	
t_r, t_f	Input clock rise and fall times 10%to 90%	4.5 MHz			30	ns	1
t_{on}, t_{off}	Input clock on and off times	4.5 MHz		111		ns	1
C_I	Input capacitance			5	10	pF	
V_{OH}	Output high	0.75 mA	$V_{DD}-1$		V_{DD}	V	2
V_{OL}	Output low	0.70 mA	V_{SS}		$V_{SS}+1$	V	2
t_{ro}, t_{fo}	Output rise and fall times 500 pF load		250		2500	ns	3
t_{on}, t_{off}	Output duty cycle	M 082		30		%	
		M 083, M 086		50			
I_{DD}	Supply current			24	35	mA	*
f_I	Input clock frequency		100	4000.48	4500	kHz	

* Output unloaded.

Fig. 1 Input clock waveform

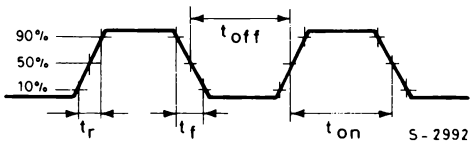


Fig. 2 - Output signal d.c. loading

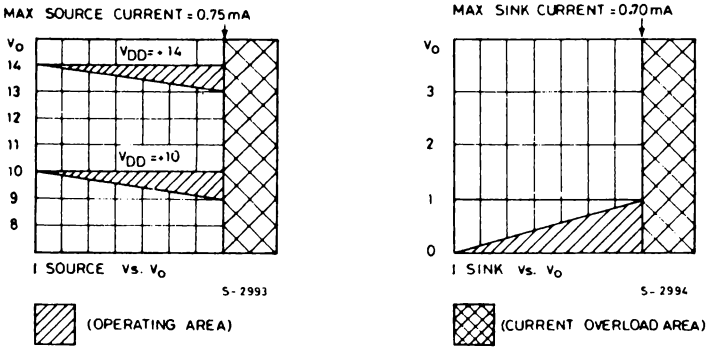


Fig. 3 - Output loading