PRELIMINARY DATA

1024 BIT - NON VOLATILE RANDOM ACCESS MEMORY

- 256 x 4 ORGANIZATION, FULLY DECODED
- OPERATING MODES: READ, MODIFY
- MODIFY MODE PERFORMS SIMULTANEOUS WRITING AND ERASURE ON THE ADDRESSED WORD
- INPUT LATCHES FOR ADDRESSES AND DATA IN
- OUTPUT DATA LATCHED
- ACCESS TIME: M 120-2: 450 ns — M 120: 700 ns
- WORD MODIFY TIME: LESS THAN 100 msec. END OF MODIFY OPERATION IS INDICATED BY A FLAG (MODIFY END)
- 10^4 MODIFY CYCLES PER WORD
- DATA RETENTION ONE ORDER OF MAGNITUDE HIGHER THAN MNOS TECHNOLOGY
- N-CHANNEL, SI-GATE, DOUBLE POLY-SILICON MOS TECHONOLOGY
- TTL-COMPATIBLE, OPEN DRAIN OUTPUTS
- POWER SUPPLY V_{DD}= 12V ± 10% , V_{PP}= 25V ± 5%
- LOW POWER CONSUMPTION: 300 mW PEAK POWER FROM V_{PP} (DURING WRITE OPERATION ONLY)
  350 mW ACTIVE POWER FROM V_{DD}
  STANDBY POWER LESS THAN 100 mW

The M 120 is a non volatile memory which the user can consider as a RAM with a fast access time and an much slower write cycle.The device operates with an address strobe control ($\overline{AS}$) and has no limit on the maximum period of $\overline{AS}$. The $\overline{AS}$ control performs the Chip Select (CS) function as well; the device is de-selected (standby mode) by a high level on $\overline{AS}$. Both read and modify cycles begin on the falling edge of $\overline{AS}$; if R/$\overline{W}$ remains true, while $\overline{AS}$ is active, a read cycle occurs; if, instead, R/$\overline{W}$ is false while $\overline{AS}$ is active a modify cycle starts. Data on the data bus are latched during the rising edge of R/$\overline{W}$, then an internal circuitry performs a comparison between "old", and "new" data and, according to the result, writes or erases or leaves unchanged each single bit of the word. If writing is necessary on one bit and an erasure on another, both operations are performed simultaneously. After the rising edge of R/$\overline{W}$, addresses and data are latched internally and no external holding is necessary during the modify time. Since modify time lengthens during the device lige, the "modify end" control, which outputs a high level at the end of the cycle, can be used to speed up system operations. As long as ME is low the device is internally disconnected from buses and controls. The device is available in 18-lead dual in-line ceramic package (metal seal) and ceramic package (frit seal).

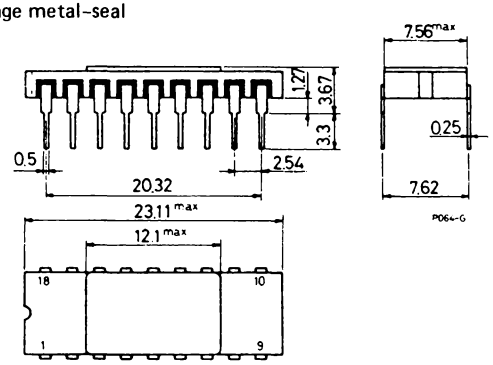
ABSOLUTE MAXIMUM RATINGS

V_I	Input voltage	-0.5 to 20	V
P_{tot}	Total power dissipation	0.5	W
T_{stg}	Storage temperature range	-65 to 150	°C
T_{op}	Operating temperature range	0 to 70	°C

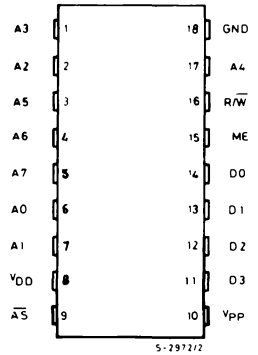
ORDERING NUMBERS: M 120 F1 for dual in-line ceramic package (frit seal)
M 120 D1 for dual in-line ceramic package (metal seal)
M 120-2 F1 for dual in-line ceramic package (frit seal)
M 120-2 D1 for dual in-line ceramic package (metal seal)

MECHANICAL DATA (dimensions in mm)

Dual in-line ceramic package metal-seal



PIN CONNECTIONS



DC AND OPERATING CHARACTERISTICS (T_{amb} = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{PP} = 25V ± 5%)

Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
I_{DD1}	V_{DD} supply current				30	mA
I_{PP1}	V_{PP} supply current				12	mA
I_{DD2}	Standby V_{DD} supply current				10	mA
I_{PP2}	Standby V_{PP} supply current				5	mA
V_{IH}	Input high voltage		2.4	5		V
V_{IL}	Input low voltage		-0.3	0	0.6	V
V_{OL}	Output low voltage	I_L = 1.6 mA			0.4	V
I_{LI}	Input load current				10	µA
I_{LO}	Output leakage current				10	µA

AC CHARACTERISTICS

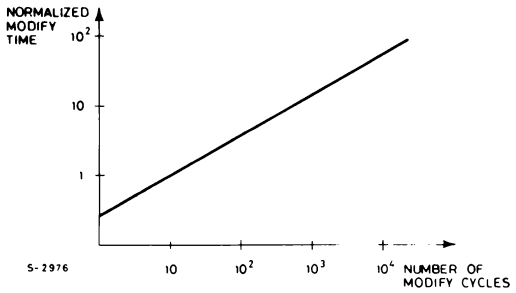
Parameter		M 120-2		M 120		Unit
		Min.	Max.	Min.	Max.	
t_{ACC}	Access time from address strobe		450		700	ns
t_{ASL}	Address strobe active time	450		700		ns
t_{ASH}	Address strobe inactive time	160		300		ns
t_{OFF}	Output buffer turn-off delay		100		150	ns
t_s	Set-up time		20		40	ns
t_h	Hold time		80		150	ns
t_{WR}	Write time (1)	2	100	2	100	ms
t_{D1}	$\overline{AS}$ to R/$\overline{W}$ delay (2) (3) (4)	100	350	200	600	ns
t_P	Modify pulse width (3) (4)	200		300		ns
t_{SW}	R/$\overline{W}$ to $\overline{AS}$ rising edge	200		300		ns
t_{D2}	ME turn-on delay		100		200	ns

Notes:
1) $t_{WR\ max}$ is 2 ms for the first 10 modify cycles and increases to 100 ms according to Figure 1.
2) R/$\overline{W}$ is internally disabled up to $t_{D1\ min}$ but can change before $t_{D1\ min}$ and even before the falling edge of $\overline{AS}$.
3) If $t_{D1} \leq t_{D1\ max}$ then D_{OUT} remains floating and there is no conflict between D_{OUT} and D_{IN}; in this mode, D_{IN} can be stable within $t_{ASL\ min}$; otherwise it must be

$$t_P \ t_{OFF} + t_{tr} + t_s$$

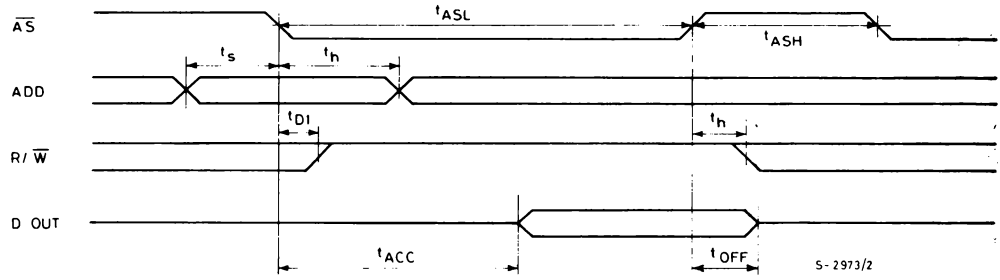
where
t_{tr} is the transition time for the data bus.
4) It must be $t_P + t_{D1} \geq t_{ASL\ min}$.

Fig. 1 - Plot of modify time vs. number of modify cycles

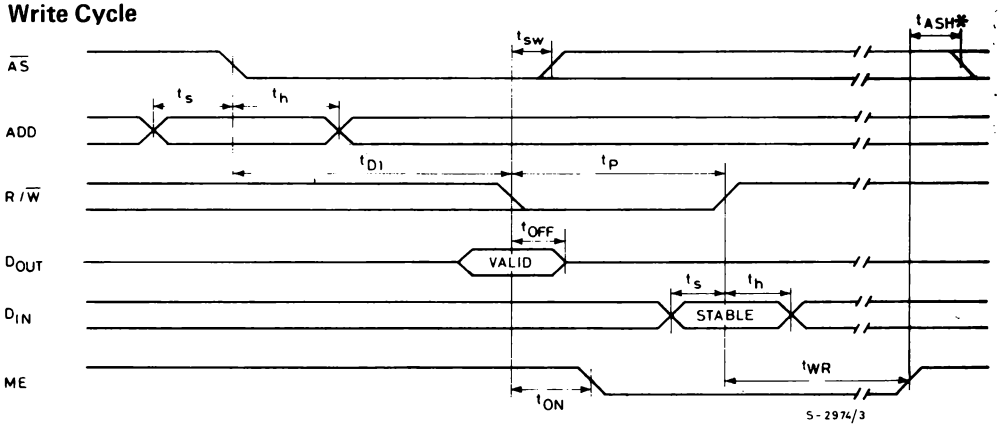


TIMING WAVEFORMS

Read Cycle



Write Cycle



* The first negative edge of $\overline{AS}$ following the end of a modify cycle must commence at least t_{ASH} after the positiv edge of ME.