Monitor Development
Display & Development Division
IMES Co., Ltd.

TFT Color LCD Module M121-55HB Product Specifications

30.8cm(12.1inch) SVGA(800x600)

SEP 28, 2000

Rev. & date		Content of change
Rev. 1.0	SEP 21, 2000	Initial Release
Rev. 2.0	SEP 25, 2000	Power Requirement Correction
Rev. 3.0	SEP 28, 2000	Viewing Angle, Lamp Current Change
Rev. 4.0	OCT 11, 2000	VDD Power change

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P/N: 7BD55HB0
EC : 6V22042

Scope

M121-55HB is a TFT LCD color module to be designed to realize the largest screen on A4 size notebook style personal computer, PC monitor and industry application. In addition to its large screen, the characteristics of this module are high luminance, light weight, slim/thin outline, low power consumption and high resolution of SVGA (800x600) capability.

Features

- . 30.8cm(12.1 inch) diagonal
- . Native 262k colors (R/G/B 6 bit each)
- . SVGA 800 x 600 pixels
- . Low Reflection (Black Matrix)
- . Two lamps backlight
- . 360 cd/m² high luminance
- . 278mm x 205mm x 13mm typ.
  (Need min. 3mm clearance from lamp cables)
- . 475 g typ.
- . 8.29 W typ.

Application

- . Notebook PCs
- . Monitors

Notes

- . The construction of M121-55HB is to add a TTL RGB to LVDS conversion card to M121-55DB (LVDS input) TFT LCD Module.

This module does not contain an inverter card for backlight.
The LCD cell is supplied from IBM.

1. Characteristics Summary

Screen Diagonal	30.8cm (12.1")
Active Area	246.0mm(H) x 184.5mm(V)
Pixel Format	800(x3) x 600
Pixel Pitch	0.3075(per one triad) x 0.3075
Pixel Arrangement	R,G,B Vertical Stripe
Display Mode	Normally White
White Luminance	360 cd/m^2 typ. (CFL Discharge Current = 5.5 mA_{rms} x2)
Contrast Ratio	200 : 1 typ.
Viewing Angle [Degrees] K:Contrast Ratio	Horizontal (Right) 50 min K>=10 (Left) 50 min Vertical (Upper) 15 min K>=10 (Lower) 30 min
Optical Rise Time/Fall Time	30 msec typ.
Nominal Input Voltage VDD	 +3.3 V
Power Consumption (w/o inverter) (VDD line + two lamps input line)	 8.29 W typ.
Weight	475 grams typ.
Physical Size	278mm x 205mm x 13mm typ. (Need min 3mm clearance from lamp cables.
Electrical Interface	Digital Video Signals(6-bit for each color R/G/B) Sync. Signal (x4)
Supported colors	Native 262k colors
Screen Criteria	DOT defect: LIT : 6 UNLIT : - Total DOT Defect : 15 Double LIT : 2 Double UNLIT : - Distance LIT : 3 , 20mm Line Defect: No line Defect
Backlight lamp life (Luminance becomes half value of initial value.)	30,000 Hours under following condition. - Temp = 25 degC - Continuos power on
Temperature Range Operating Storage	 +0 to +50 degC -20 to +60 degC

2. Absolute Maximum Ratings

Electrical Absolute Maximum Ratings

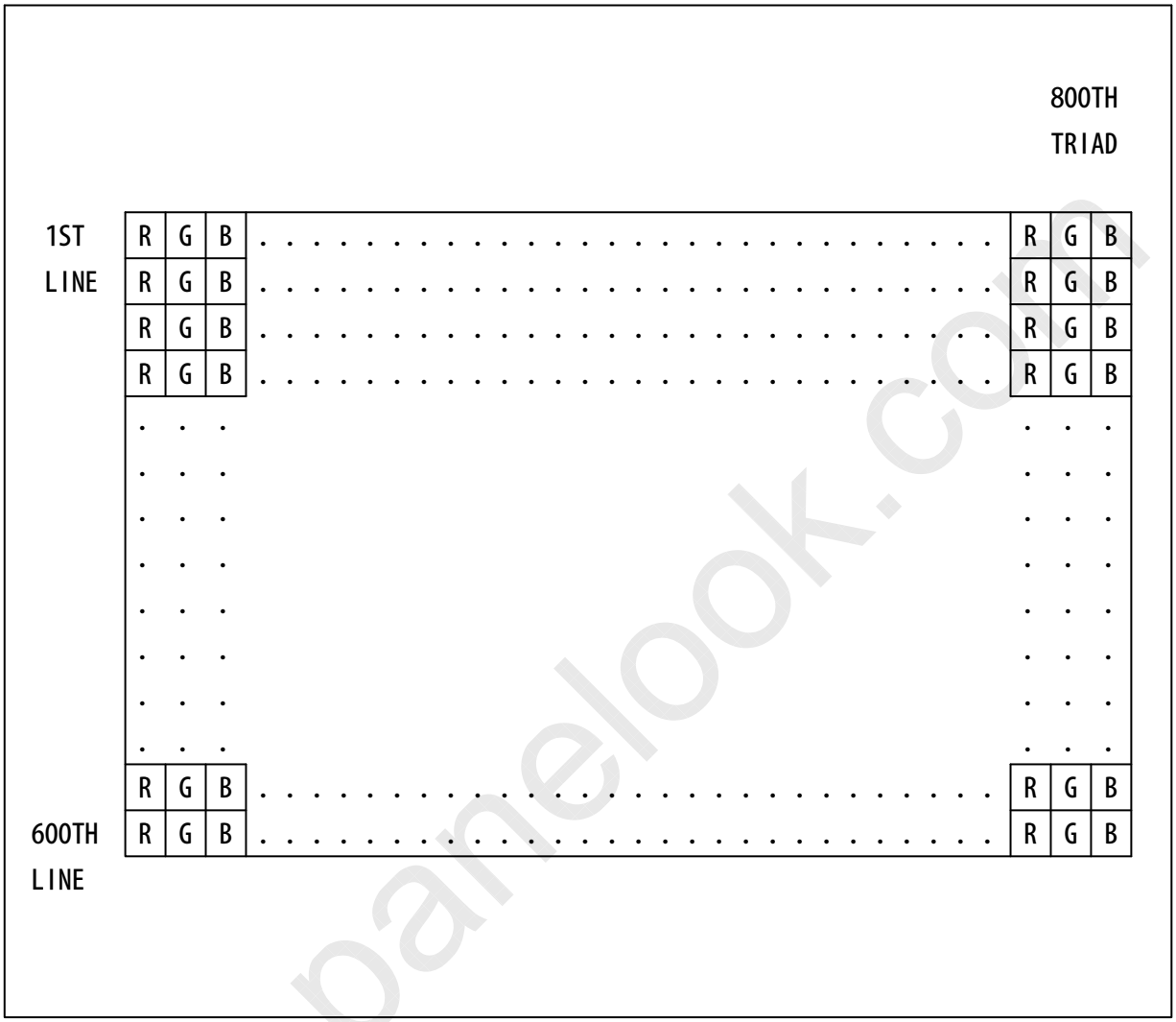
Rating	Symbol	Value	Unit	Conditions
Supply Voltage	VDD	-0.3 to +4.0	V	
Lamp ignition voltage	Vcfl	1500	Vrms	At 0 degreeC
CFL Discharge Current	Icfl	6.0	mArms	Exclude inrush current
CFL Inrush Current	Ircfl	30	mA0-p	With Max. duration = 50 (mSec)
CFL Driving Frequency	Fcfl	30 to 70	kHz	At 25 degreeC
Static Electricity				Operators should be grounded in handling the TFT LCD Module

Environmental Absolute Maximum Ratings

Rating	Symbol	Value	Unit	Conditions
Storage Temperature	TST	-20 to +60	degC	At the glass surface
Operation Temperature	TOP	0 to +50	degC	At the glass surface
Operation Humidity		8 to 95	%RH	Max wet bulb temp. 29 degC No condensation
Vibration		1.5	G	10-200Hz, X, Y, Z (Note1)
Trapezoidal Shock		50	G	18msec, +/-X, Y, Z (Note1)
Corrosive Gas		Not Acceptable		

Note 1: At testing Vibration and Shock, the fixture in holding the Module to be tested have to be hard rigid enough so that the Module would not be twisted or bent by the fixture.

3. Color Arrangement



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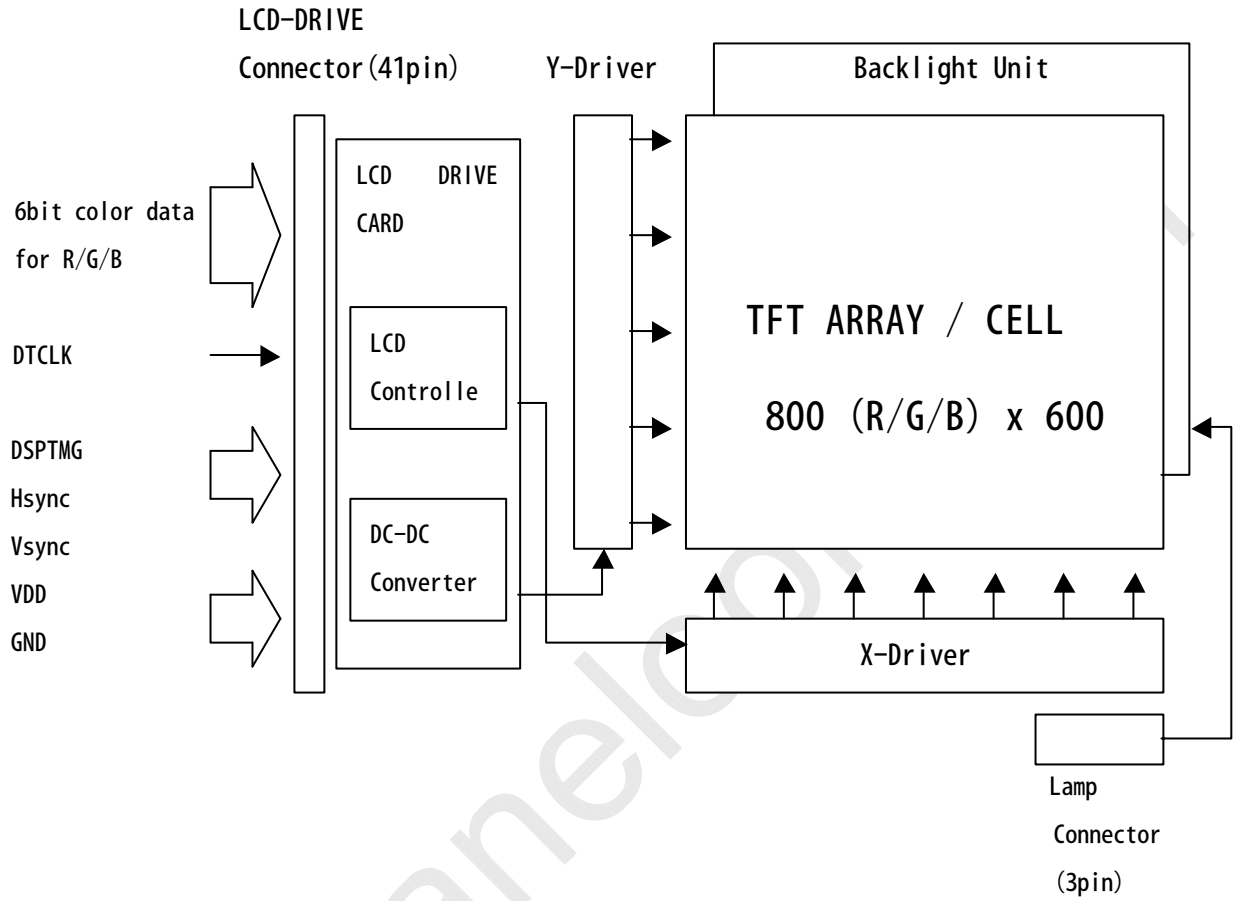
4. Block Diagram



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5. Signal Interface

5.1 Connectors

Physical interface is described as for the connector on module.
These connectors are capable of accommodating the following signals and will be following components.

	Supplier Name	Supplier' s Part Number
LCD Drive Connector	HIROSE	DF9B-41P-1V
Mating Connector	HIROSE	DF9B-41S-1V

	Supplier Name	Supplier' s Part number
Lamp Connector	JST	SBH-001T-P0.5
Mating connector	JST	SM04(4.0)B-BHS-1-TB

5.2 Signal for LCD Drive Connector

Pin#	Signal Name	Pin#	Signal name
1	GND	2	-DTCLK
3	GND	4	HSYNC
5	VSYNC	6	GND
7	GND	8	GND
9	+RED0	10	+RED1
11	+RED2	12	GND
13	+RED3	14	+RED4
15	+RED5	16	GND
17	GND	18	GND

19	+GREEN0	20	+GREEN1
21	+GREEN2	22	GND
23	+GREEN3	24	+GREEN4
25	+GREEN5	26	GND
27	GND	28	GND
29	+BLUE0	30	+BLUE1
31	+BLUE2	32	GND
33	+BLUE3	34	+BLUE4
35	+BLUE5	36	GND
37	+DSPTMG	38	Reserved
39	VDD (+3.3V)	40	VDD (+3.3V)
41	Reserved		

Note 1: 'Reserved' pins are not allowed to connect any other line.

Note 2: Voltage levels of all input signals are CMOS compatible (except VDD).

This module shall contain column are row drivers to address any given pixel. The host attached PC system shall supply 18 bits (6bits per each color) data and 4-sync signals to these drivers and power supply for backlight. These interface signals and their timing relationship are described below.

Pin No.	Signal Name	Description
15	+RED5	Red Data 5 (MSB)
14	+RED4	Red Data 4
13	+RED3	Red Data 3
11	+RED2	Red Data 2
10	+RED1	Red Data 1
9	+RED0	Red Data 0 (LSB)
		Red-Pixel-Data Each red pixel's brightness data consists of these 6 bits pixel data.

25 24 23 21 20 19	+GREEN5 +GREEN4 +GREEN3 +GREEN2 +GREEN1 +GREEN0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB)	
		Green-Pixel-Data	Each Green pixel' s brightness data consists of these 6 bits pixel data.
35 34 33 31 30 29	+BLUE5 +BLUE4 +BLUE3 +BLUE2 +BLUE1 +BLUE0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB)	
		Blue-Pixel-Data	Each Blue pixel' s brightness data consists of these 6 bits pixel data.
2	-DTCLK	Data Clock	The typical frequency is 40.00MHz. The signal is used to strobe the pixel data and +DSPTMG signals. All pixel data shall be valid at the falling edge when the +DSPTMG signal is high.
37	+DSPTMG	Display Timing	This signal strobed at falling edge of DTCLK. When the signal is high, the pixel data shall be valid to be displayed.
5	VSYNC	Vertical Sync	The signal is synchronized to DTCLK.
4	HSYNC	Horizontal Sync	The signal is synchronized to DTCLK.
39, 40	VDD	+3.3V	
1, 3, 6, 7, 8, 12, 16, 17, 18, 22, 26, 27, 28, 32, 36	GND	Signal Ground	
38, 41		Reserved	No connection (Signal reserved)

Note: Output signals from system shall be low or Hi-Z state when VDD is off.

5.3 Signal Specification

voltage levels of all input signals are CMOS compatible (except VDD).
Each signal characteristics are as follows;

Parameter	Condition		Min.	Max.	Unit
Vih	High level input voltage	R/G/B, DTCLK DSPTMG, H/V SYNC	0.7xVDD	VDD	V
Vil	Low level input voltage	R/G/B, DTCLK DSPTMG, H/V SYNC	0	0.2xVDD	V
Iih	High level input current	R/G/B, DTCLK DSPTMG, H/V SYNC	-	50	uA
Iil	Low level input current	R/G/B, DTCLK DSPTMG, H/V SYNC	-	-50	uA

5.4 Signal for Lamp Connector

Pin No.	Signal Name	Description
1	Lamp high 1	For Lamp 1
2	Lamp High 2	For Lamp 2
4	Lamp Low	For Lamp 1&2

6. Lamp Interface Specification and Guide Line for CFL Inverter

Parameter Name	Symbol	Min.	Typ.	Max.	Unit	Note
CFL Kick-off Voltage	Vs	-	-	1,100	Vrms	T_{amb}=25degC*4
		-	-	1,500		T_{amb}=0degC*4
CFL Discharge Current (per one lamp)	Icfl	1.5*6	-	6.0	mArms	Total operating range
		-	5.5	-		Screen 360cd/m^2, at T_{amb}=25degC
CFL Discharge Voltage	Vcfl	-	630	-	Vrms	Screen 360cd/m^2, at T_{amb}=25degC
CFL Power Consumption (two lamps)	Pcfl	-	6.94	-	W	Screen 360cd/m^2, at T_{amb}=25degC
CFL Discharge Frequency	Fcfl	30	40	70*6	kHz	Reference*5

Note

*1 All of characteristics listed are measured under the condition using the IMES inverter (IMES P/N 6M000704).

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CFL, for instance, becomes more than 1 [M ohm] when CFL is damaged.

*4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.

*5 CFL discharge frequency must be carefully chosen so as not to produce interfering noise stripes on the screen.

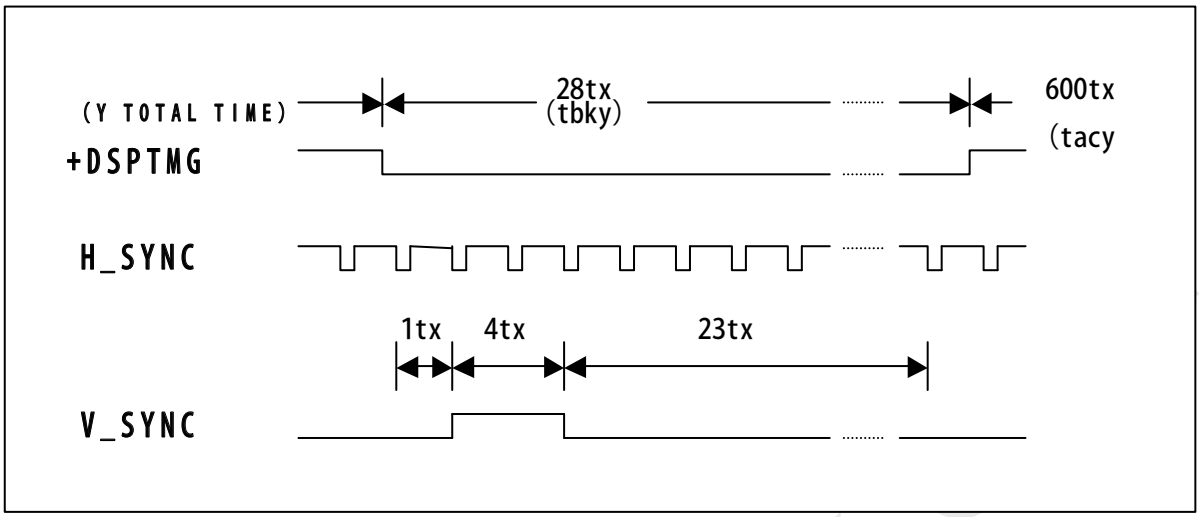
*6 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

7. Interface Timings

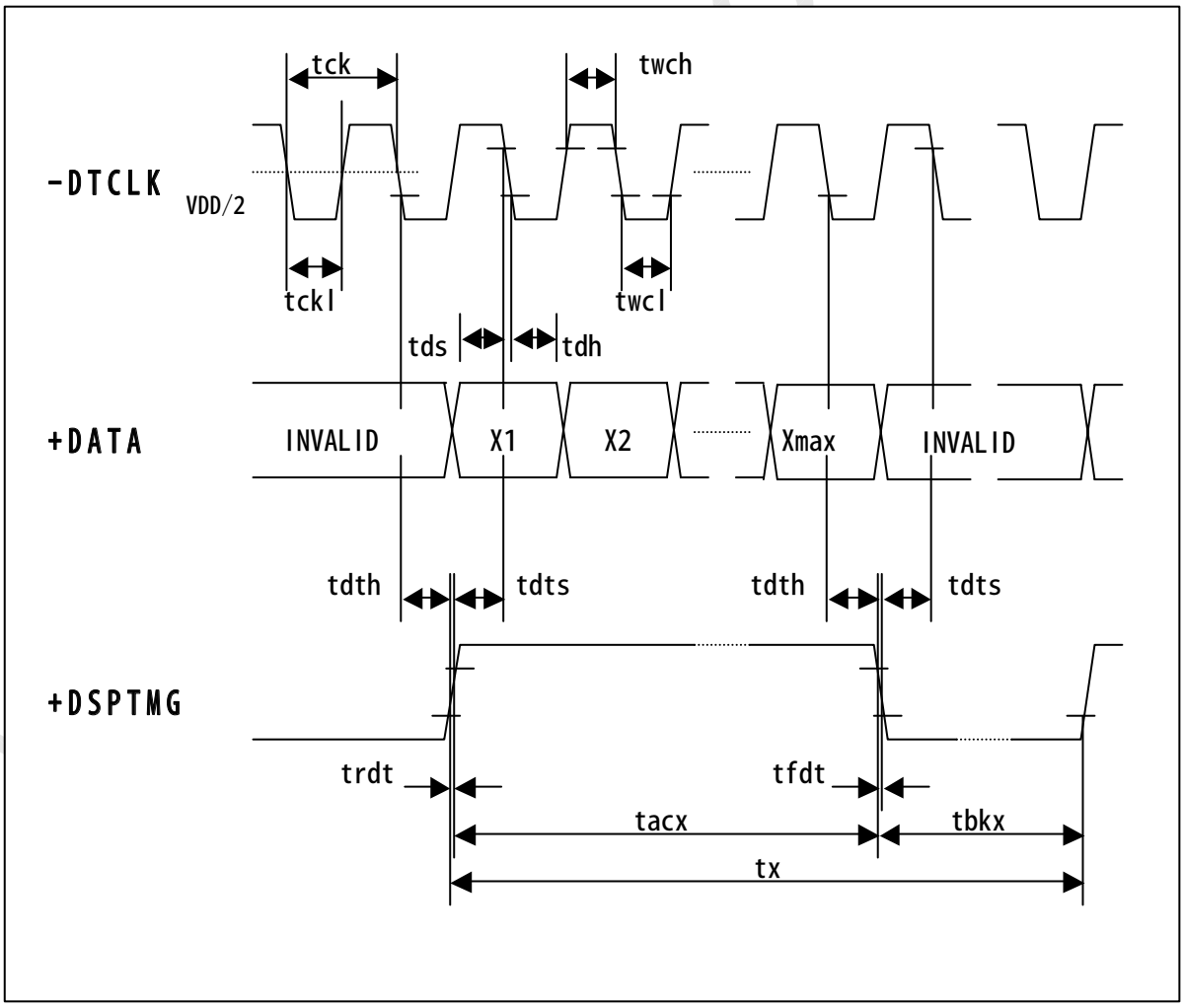
Basically, interface timings should match the VESA 800 x 600 60Hz manufacturing guideline timing.

Symbol	Signal Description	MIN	TYP	MAX	UNIT
f_{dck}	DTCLK frequency	36.00	40.00	40.20	MHz
t_{ck}	DTCLK cycle time	23.81	25.00	27.77	nsec
t_{wd}	DTCLK low width	5.00			nsec
t_{wch}	DTCLK high width	5.00			nsec
Duty-dck	DTCLK Duty(tckl/tck)	40	50	60	%
t_{ds}	Data set up time	5.00			nsec
t_{dh}	Data hold time	5.00			nsec
t_{rdt}	DSPTMG rise time			5.00	nsec
t_{fdt}	DSPTMG fall time			5.00	nsec
t_{dts}	DSPTMG set up time	5.00			nsec
t_{dth}	DSPTMG hold time	5.00			nsec
t_x	X total time	848	1056	1088	tck
t_{acx}	X active time		800		tck
t_{blox}	X blank time	48	256	288	tck
H_s	H-sync frequency	35.16	37.88	38.46	KHz
H_w	H-sync width	8	128	152	tck
H_{fp}	H-sync front porch	8	40	272	tck
H_{bp}	H-sync back porch	8	88	272	tck
t_y	Y total time	611	628	1025	tx
t_{acy}	Y active time		600		tx
t_{bly}	Y blank time		28		tx
V_{sync}	Frame rate	56.25	60.00	61.00	Hz
V_w	V-sync width	1	4	7	tx
V_{fp}	V-sync front porch	1	1	415	tx
V_{bp}	V-sync back porch	9	23	29	tx

7.1 Horizontal Timing



7.2 Vertical Timing



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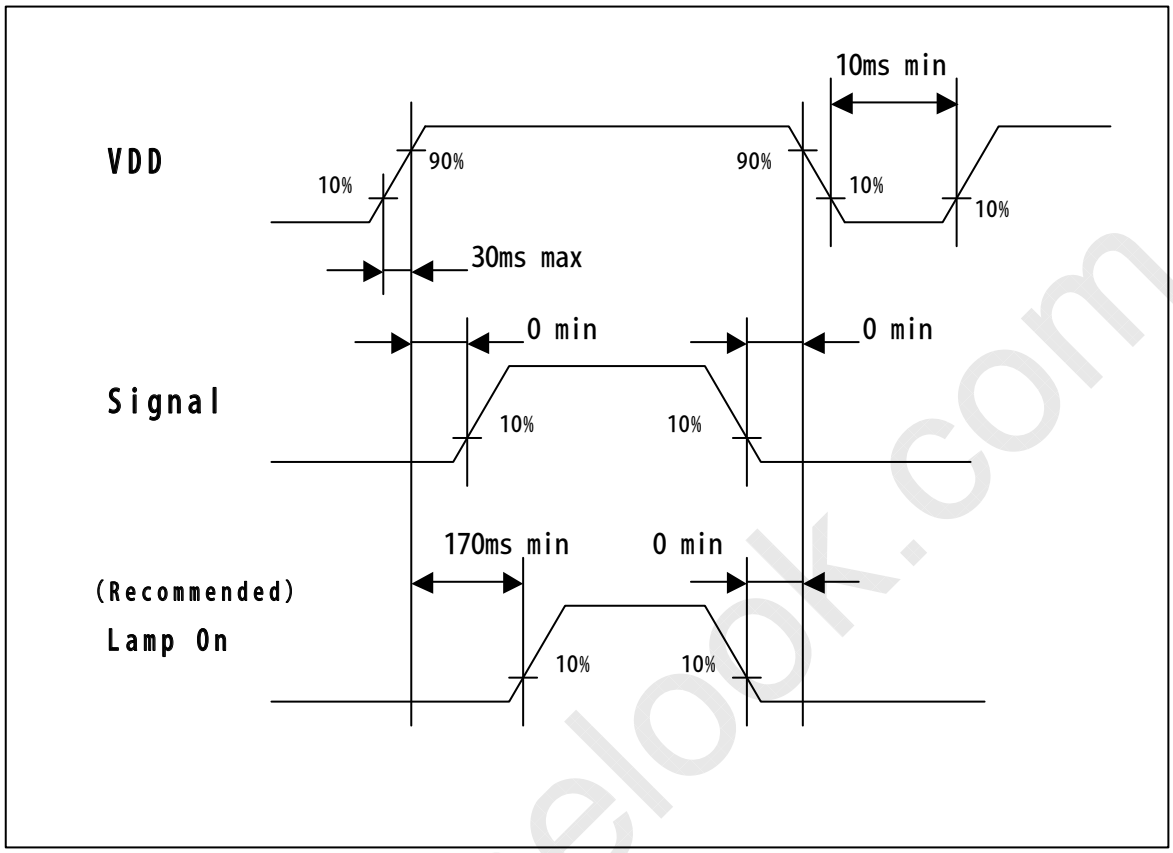
8. Power Requirement

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
VDD	Logic/LCD Drive Voltage	+3.0	+3.3	+3.6	V	Load Capacitance 20uF
PDD	VDD Power	0.82	0.93	1.05	W	64-Gray Scale (Note 1)
PDD	VDD Power	1.15	1.35	1.5	W	Sub-pixel vertical stripe (Note 1)
PDDmax	VDD Power max			1.63	W	Sub-pixel vertical stripe (Note 2)
IDDmax	IDD Current max			454	mA	Sub-pixel vertical stripe (Note 2)
PL	Lamp Power		3.47		W	Per one lamp
PDD+PL	Total Power		8.29		W	Two lamps
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	mVp-p	
VDDns	Allowable Logic/LCD Drive Ripple Noise			100	mVp-p	

Note 1: VDD=+3.3V

Note 2: VDD=+3.6V

9. Power ON/OFF sequence



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10. Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots .
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or creak if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling .
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be darnaged.
10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module. Also be sure to support the metal frame of the TFT Module (by hand, for example) just at the reverse side of the Connector so that the Module itself is not twisted nor bent Otherwise the TFT Module may be damaged.
11) At and after installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bent the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

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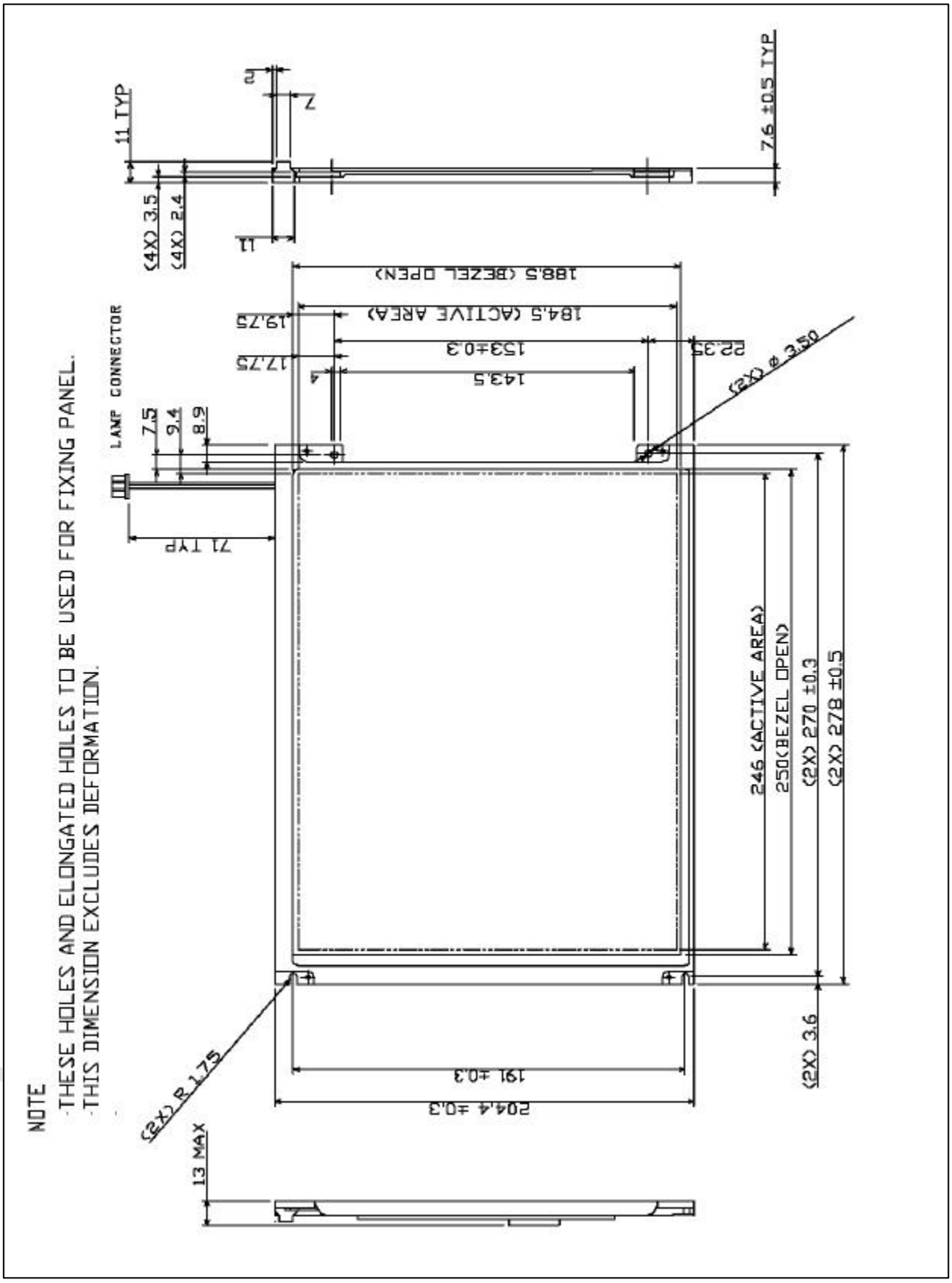
11. Reference Drawing



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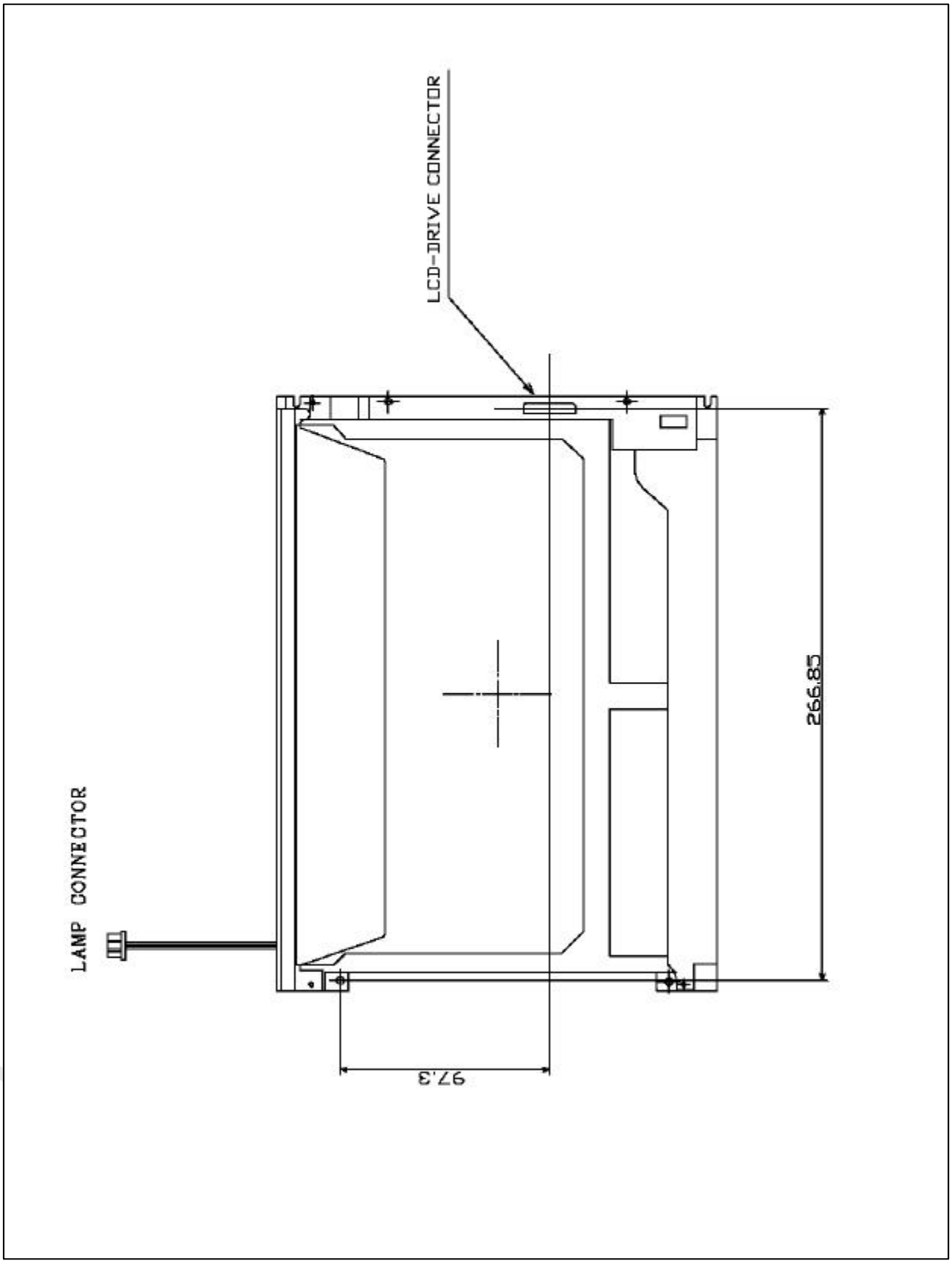

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