

Document Title	M133NWF2 R0 Product Information				1/31
Document No.		Issue date	2013/10/24	Revision	00

Product Information

To:

Product Name: M133NWF2 R0

Document Issue Date: 2013/10/24

Customer		InfoVision Optoelectronics
<u>SIGNATURE</u>		<u>SIGNATURE</u>
		QA
		PREPARED BY FAE
Please return 1 copy for your confirmation		
with your signature and comments.		

Note: 1. Please contact IVO Corp. before designing your product based on this product.

2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by IVO for any intellectual property claims or other problems that may result from application based on the module described herein.



Document Title	M133NWF2 R0 Product Information				2/31
Document No.		Issue date	2013/10/24	Revision	00

Revision	Date	Page	Old Description	New Description	Remark
00	2013/10/24	all		First issue.	



Document Title	M133NWF2 R0 Product Information				3/31
Document No.		Issue date	2013/10/24	Revision	00

Contents

1.0	General Descriptions	4
2.0	Absolute Maximum Ratings	
3.0	Pixel Format Image	
4.0	Optical Characteristics	9
5.0	Backlight Characteristics	
6.0	Electrical Characteristics	
7.0	Interface Timings	
8.0	Power Consumption	
	Power ON/OFF Sequence	
	Mechanical Characteristics	
	Package Specification	
	Lot Mark	
	General Precaution	
14.0	EDID Data Structure	28



Document Title	M133NWF2 R0 Product Information				4/31
Document No.		Issue date	2013/10/24	Revision	00

1.0 General Descriptions

1.1 Introduction

The M133NWF2 R0 is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. It is composed of a TFT LCD panel, a timing controller, voltage reference, common voltage, column driver, and row driver circuit. This TFT LCD has a 13.3-inch diagonally measured active display area with FHD resolution (1,920 horizontal by 1,080 vertical pixels array).

1.2 Features

- 13.3" TFT-LCD Panel
- LED Backlight System
- Supported FHD Resolution
- Compatible with ROHS Standard
- Supported eDP 1.2 Electrical Interface

1.3 Product Summary

Items	Specifications	Unit	Remark
Screen Diagonal	13.3	Inch	-
Active Area	293.76(H) x 165.24(V)	mm	-
Pixels (H x V)	1,920 (RGB) x 1,080	-	-
Pixel Pitch	0.153(H) x 0.153(V)	mm	-
Pixel Arrangement	R.G.B. Vertical Stripe	-	-
Display Mode	Normally Black	-	-
White Luminance	250 (Typ.)	cd/m ²	5 Points Average
Contrast Ratio	800 (Typ.)	-	-
NTSC	72 (Typ.)	%	-
Response Time	25 (Typ.)	ms	-
Input Voltage	+3.3 (Typ.)	V	-
Power Consumption	4.0 (Max.)	W	-
Weight	320 (Max.)	g	-
Outline Dimension	305.348(Typ.)x178.562(Typ.)x5.2(Max.)	mm	
(H x V x D)	303.346(Typ.)xT76.362(Typ.)x3.2(Wax.)	111111	-
Electrical Interface (Logic)	eDP1.2	ı	-
Support Color	16.7M	-	-
Surface Treatment	HC, Hardness 3H	-	-

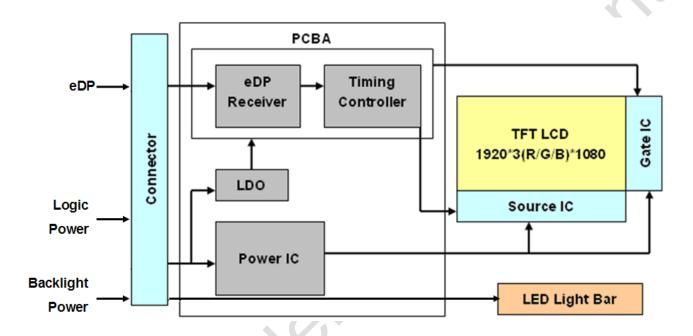


Document Title	M133NWF2 R0 Product Information				5/31
Document No.		Issue date	2013/10/24	Revision	00

1.4 Functional Block Diagram

Figure 1 shows the functional block diagram of the LCD module.

Figure 1 Block Diagram





Document Title	M133NWF2 R0 Product Information				6/31
Document No.		Issue date	2013/10/24	Revision	00

2.0 Absolute Maximum Ratings

Table 1 Electrical Absolute Rating

Item	Symbol	Min.	Max.	Unit	Note
Logic Supply Voltage	V_{DD}	-0.3	3.6	V	
Logic Input Signal Voltage	-	-0.3	2.4	V	
Supply V _{LED} Voltage	V_{LED}	-0.3	24.8	V	(1),(2)
LED Forward Voltage	V _F	2.7	3.1	V	
LED Forward Current	I _F	-	- C	mA	

Note (1) Permanent damage may occur to the LCD module if beyond this specification. Functional operation should be restricted to the conditions described under normal operating conditions. (2)Operating temperature is 25°C, humidity is 55%.

Table 2 Absolute Ratings of Environment

Item	Symbol	Min.	Max.	Unit	Conditions
Operating Temperature	TOP	0	60	${\mathbb C}$	
Operating Humidity	HOP	10	80	%RH	(4) (2) (2)
Storage Temperature	TST	-20	60	${\mathbb C}$	(1),(2),(3)
Storage Humidity	HST	10	90	%RH	
Vibration(non-operating)	Vnop	-	1.5	G	(4)
Shock(non-operating)	Snop	-	220G	G	(5)

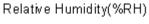
Note (1) Maximum Wet-Bulb should be 39 ℃. No condensation.

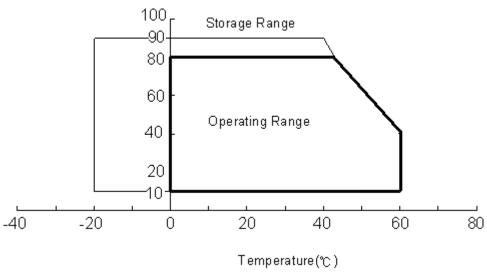
- (2) When you apply the LCD module for OA system. Please make sure to keep the temperature of LCD module is less than 60° C
- (3) Storage /Operating temperature:



Document Title	M133NWF2 R0 Product Information				7/31
Document No.		Issue date	2013/10/24	Revision	00

Figure 2 Absolute Ratings of Environment of the LCD Module





- (4) 10-500Hz, random vibration, 30min for X, Y, Z axis.
- (5) 2ms, half sine wave, one time for X, Y, Z axis.



Document Title	M133NWF2 R0 Product Information				8/31
Document No.		Issue date	2013/10/24	Revision	00

3.0 Pixel Format Image

Figure 3 shows the relationship of the input signals and LCD pixel format image.

Figure 3 Pixel Format

R+G+B Dots=1 Pixel



Document Title	M133NWF2 R0 Product Information				9/31
Document No.		Issue date	2013/10/24	Revision	00

4.0 Optical Characteristics

The optical characteristics are measured under stable conditions as following notes.

Table 3 Optical Characteristics

Item	Conditio	ns	Min.	Тур.	Max.	Unit	Note
	Horizontal	θ *+	80	85	-		
Viewing Angle	Honzoniai	θ _{x-}	80	85	-	dograo	(1) (2)
(CR>10)	Vertical	θ _{y+}	80	85	-	degree	(1),(2)
	vertical	θ _{y-}	80	85	-		
Contrast Ratio	Center		500	800	-	-	(1), (3)
Response Time	Rising + Fallin	g	ı	25	50	ms	(1), (4)
	Red x			0.640) -	
	Red y			0.330		-	(4)
Color	Green x	Green x		0.300	Тур.	-	(1)
Color	Green y		-0.03	0.612	+0.03	-	Viewing Normal
Chromaticity (CIE1931)	Blue x		*	0.150		-	Angle ($\Theta x =$
(CIE 1931)	Blue y		X	0.060		-	Arigie ($\Theta x = \Theta y = 0^{\circ}$)
	White x		0.283	0.313	0.343	-	Oy=0)
	White y		0.299	0.329	0.359	-	
White Luminance	5 Points Average		220	250	-	cd/m^2	(1), (5)
Luminance	5 Points		80	ı	-	%	(1) (6)
Uniformity	13 Points		60	-	-	/0	(1), (6)

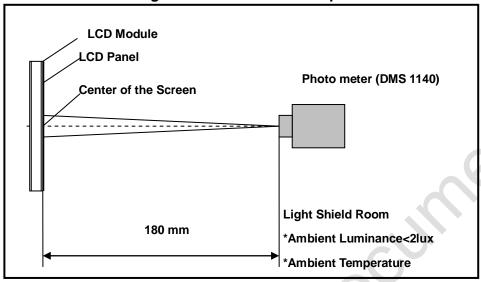
Note (1) Measurement Setup:

The LCD module should be stabilized at given temperature (25° C) for 15 minutes to Avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 15 minutes in a windless room.



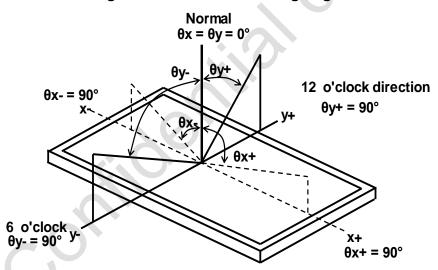
Document Title	M133NWF2 R0 Product Information				10/31
Document No.		Issue date	2013/10/24	Revision	00

Figure 4 Measurement Setup



Note (2) Definition of Viewing Angle

Figure 5 Definition of Viewing Angle



Note (3) Definition of Contrast Ratio (CR)

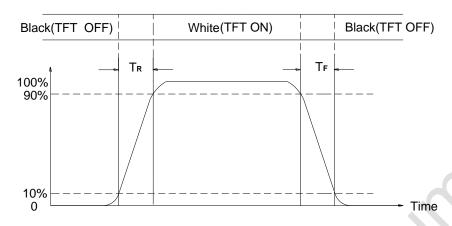
The contrast ratio can be calculated by the following expression Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255, L0: Luminance of gray level 0

Note (4) Definition of Response Time (T_R, T_F)

Document Title	M133NWF2 R0 Product Information				11/31
Document No.		Issue date	2013/10/24	Revision	00

Figure 6 Definition of Response Time



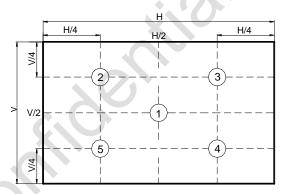
Note (5) Definition of Luminance White (Ref: Active area)

Measure the luminance of gray level 255 at 5 points.

Display Luminance=(L1+L2+L3+L4+L5) / 5

H—Active Area Length V—Active Area Width L—Measurement Point Luminance

Figure 7 Measurement Locations Of 5 Points



Note (6) Definition of Luminance Uniformity (Ref: Active area)

Measure the luminance of gray level 255 at 5 points.

UNF(5Point s) =
$$\frac{\text{Min}(L1, L2, \dots L5)}{\text{Max}(L1, L2, \dots L5)}$$

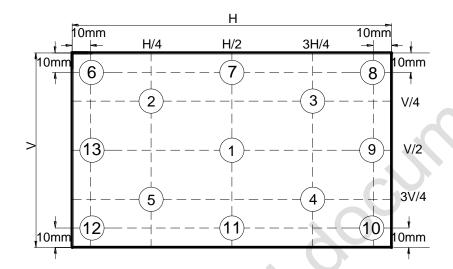
Measure the luminance of gray level 255 at 13 points.

UNF(13Points) =
$$\frac{\text{Min}(L1, L2, \dots L13)}{\text{Max}(L1, L2, \dots L13)}$$



Document Title	M133NWF2 R0 Product Information				12/31
Document No.		Issue date	2013/10/24	Revision	00

Figure 8 Measurement Locations Of 13 Points





Document Title	M133NWF2 R0 Product Information				13/31
Document No.		Issue date	2013/10/24	Revision	00

5.0 Backlight Characteristics

5.1 Parameter Guideline Of LED Backlight

Table 4 Parameter Guideline for LED Backlight

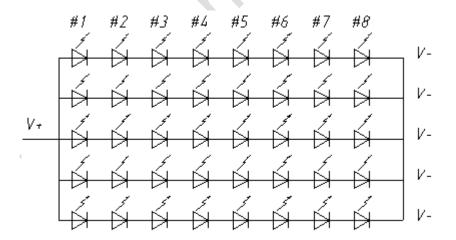
Item	Symbol		Min.	Тур.	Max.	Units	Note
LED Input Voltage	V _{LED}		21.6	23.2	24.8	V	(2),(3)
LED Power Consumption	P _{LED}	P _{LED}		2.4	2.5	W	(2),(3)
LED Forward Voltage	V_{F}		2.7	2.9	3.1	V	
LED Forward Current	I _F	I _F		20	-	mA	
PWM Signal Input		High	1.8	-	2.5	V	
Voltage	PWM_IN	Low	0	-	0.8	V	(5)
PWM Signal Output	PWM OUT	High	2.0	-	2.5		(2)
Voltage	PWW_OUT	Low	0	7/	0.5	V	
PWM Duty Ratio	-	-			100	%	
Input PWM Frequency	FPWM		200	-	2,000	Hz	
LED Life Time	LT		12,000	1	-	Hours	(1)(2)

Note (1) The LED life time define as the estimated time to 50% degradation of initial luminous.

Note (2) Operating temperature is 25 °C, humidity is 55%.

Note (3) Definition of V_{LED} and P_{LED}:

$$V_{LED} = V_F x 8$$
, $P_{LED} = V_{LED} x I_F x 5$





Document Title	M133NWF2 R0 Product Information				14/31
Document No.		Issue date	2013/10/24	Revision	00

6.0 Electrical Characteristics

6.1 Interface Connector

Input signals shall be low or Hi- resistance state when VDD is off.

Table 5 Connector Name / Designation

Manufacturer	STM
Part Number	MSAK24025P30D

Table 6 Signal Pin Assignment

Pin #	Signal Name	Description	Remarks
		Panel_ID0 (LSB), Reserve a Pull down 10K OHM	
1	Panel_ID0 (LSB)	to GND, Reserve a Pull-up 100K to LCD_VCC	-
		(3.3V)	
2	H_GND	High Speed Ground	-
3	LAN1_N	Complement Signal Link Lane 1	-
4	LAN1_P	True Signal Link Lane 1	-
5	H_GND	High Speed Ground	-
6	Lane 0 (N)	Complement Signal Link Lane 0	-
7	Lane 0 (P)	True Signal Link Line 0	-
8	H_GND	High Speed Ground	-
9	AUX_CH(P)	True Signal Auxiliary Ch.	-
10	AUX_CH(N)	Complement Signal Auxiliary Ch.	-
11	H_GND	High Speed Ground	-
12	LCD_VCC	LCD Logic and Driver Power	+3.3V
13	LCD_VCC	LCD Logic and Driver Power	+3.3V
14	LCD_Self Test	Not Connection (Reserved for IVO)	-
15	LCD_GND	LCD ground	-
16	LCD_GND	LCD ground	-
17	HPD	HPD Signal Pin	-
18	PWM_IN	System PWM Signal Input	-
19	PWM_OUT	Panel PWM Signal Output to System	-
20	Cathode 1	LED Cathode	-
21	Cathode 2	LED Cathode	-
22	Cathode 3	LED Cathode	-
23	Cathode 4	LED Cathode	-
24	Cathode 5	LED Cathode	-
25	Cathode 6	NC	-

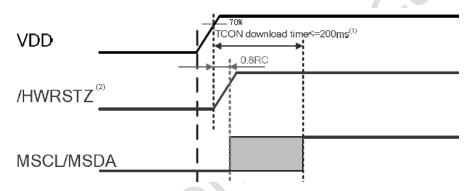


Document Title	M133NWF2 R0 Product Information			Page No.	15/31
Document No.		Issue date	2013/10/24	Revision	00

26	I2C_SCL	Reserved for I2C BUS	Note(1),(2)
27	I2C_SDA	Reserved for I2C BUS	Note(1),(2)
28	Anode	LED Anode	-
29	Anode	LED Anode	-
30	Panel_ID1 (MSB)	Panel_ID1 (MSB), Reserve a Pull down 10K OHM to GND, Reserve a Pull-up 100K to LCD_VCC (3.3V)	1

Note: (1) I2C_SCL, I2C_SDA channel should not be connected to ground capacitance, if the ground capacitance is needed that the capacitor value should be less than 68pF.

(2) The I²C channel can not be used until the TCON has been working for 200ms.



1) Condition: R=100kOhm, C=0.1uF, I²C Frequency=250~400kHz

2) /HWRSTZ: Reset Input(Low Active)



Document Title	M133NWF2 R0 Product Information			Page No.	16/31
Document No.		Issue date	2013/10/24	Revision	00

6.2 Signal Electrical Characteristics

Table 7 Display Port Main Link

Parameter	Description	Min.	Тур.	Max.	Unit
V _{CM}	Differentia Common Mode Voltage	0	-	2.0	V
V _{Diff P-P} Level 1	Differential Peak to Peak Voltage Level 1	0.34	0.40	0.46	V
V _{Diff P-P} Level 2	Differential Peak to Peak Voltage Level 2	0.51	0.60	0.68	V
V _{Diff P-P} Level 3	Differential Peak to Peak Voltage Level 3	0.69	0.80	0.92	V
V _{Diff P-P} Level 4	Differential Peak to Peak Voltage Level 4	1.02	1.20	1.38	V

Note: (1) Input signals shall be low or Hi- resistance state when VDD is off.

- (2) It is recommended to refer the specifications of VESA Display Port Standard V1.2 in detail.
- (3) Fallow as VESA display port standard V1.2 at both 1.62 and 2.7Gbps link rates.

Figure 9 Display Port Main Link Signal

Figure 10 Display Port AUX_CH Signal

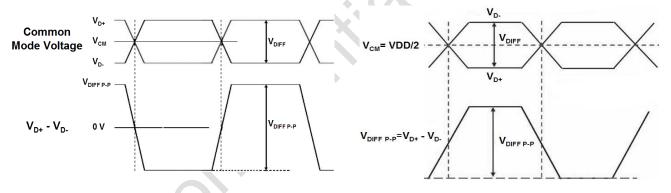


Table 8 Display Port AUX_CH

Parameter	Description	Min.	Тур.	Max.	Unit
V _{CM}	Differentia Common Mode Voltage	0	VDD/2	2	V
V _{Diff P-P}	Differential Peak to Peak Voltage	0.39	-	1.38	V

Note: Fallow as VESA display port standard V1.2.

Table 9 Display Port V_{HPD}

Parameter	Description	Min.	Тур.	Max.	Unit
V_{HPD}	HPD Voltage	2.25	-	3.60	V

Note: Fallow as VESA display port standard V1.2.



Document Title	M133NWF2 R0 Product Information			Page No.	17/31
Document No.		Issue date	2013/10/24	Revision	00

7.0 Interface Timings

7.1 Timing Characteristics

Basically, interface timings should match the $1,920 \times 1,080 / 60$ Hz manufacturing guide line timing.

Table 10 Interface Timings

Parameter	Symbol	Unit	Min.	Тур.	Max.
Signal Clock Frequency	f _{dck}	MHz	112.6	138.5	145.4
H Total Time	T_{hp}	clocks	2,040	2,080	2,120
H Active Time	HA	clocks	1,920		
H Blanking	T_{hfp}	clocks	-	160	-
V Total Time	T_{vp}	lines	1,104	1,112	1,120
V Active Time	VA	lines	1,080		
V Blanking	T _{vfp}	lines		32	-
V Frequency	f _v	Hz	50	60	65



Document Title	M133NWF2 R0 Product Information			Page No.	18/31
Document No.		Issue date	2013/10/24	Revision	00

8.0 Power Consumption

Input power specifications are as follows.

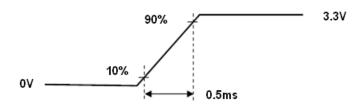
Table 11 Power Consumption

Item		Symbol	Min.	Тур.	Max.	Units	Note
Logic/LCD Drive Voltage		VDD	3.0	3.3	3.6	V	(4), (6)
VDD Current	White Pattern	IDD	-	-	(0.45)	Α	
VDD Current	Mosaic Pattern	IDD	-	-	(0.40)	Α	(4) (5) (0)
VDD Power	White Pattern	PDD	-	-	(1.50)	W	(1), (5),(6)
Consumption	Mosaic Pattern	PDD	-	-	(1.32)	W	
Rush Current		Inrush	-	-	1.5	Α	(2), (3),(6)
Allowable Logic/LCD		\/DDrn			200	m\/	(6)
Drive Ripple V	oltage	VDDrp	-	_	200	mV	(6)

Note (1) IDD measurement condition f_{dck} =138.5 MHz, f_v =60Hz, VDD=3.3V.

Note (2) Measure Condition

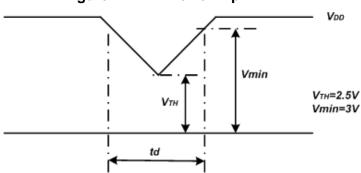
Figure 11 VDD Rising Time



Note (3) When the rush current measure condition at VDD rising time=1.5ms, the value of Inrush(Typ.)= (1A)

Note (4) VDD Power Dip Condition

Figure 12 VDD Power Dip



If V_{TH}<VDD≤V min, then td≤10ms; When the voltage return to normal our panel must revive automatically.

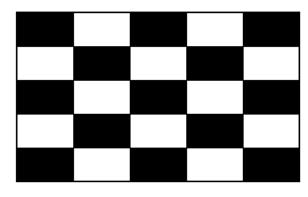
Note(5) The specified power supply current is under the condition at VDD=3.3V, DC current and f_v



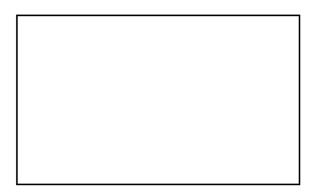
Document Title	M133NWF2 R0 Product Information			Page No.	19/31
Document No.		Issue date	2013/10/24	Revision	00

=60Hz, where as a power dissipation check pattern below is displayed.

a. Mosaic Pattern



b. White Pattern



Active Area

Active Area

Note (6) Operating temperature is 25 °C, humidity is 55%.



Document Title	M133NWF2 R0 Product Information			Page No.	20/31
Document No.		Issue date	2013/10/24	Revision	00

9.0 Power ON/OFF Sequence

VDD power on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi- resistance state or low level when VDD is off.

Logic VDD eDP Display Automatic Black Video Video form Source or Sink RFB Automatic Blad Video HPD From Sink Sink Aux CH AUX Channel Operational **T7** Link Idle or Off Valid Video Data or P&R Active Source Main-Link Data Idle Trainin

Figure 13 Power Sequence

Table 12 Power Sequencing Requirements

Parameter	Unit	Min.	Max.
T1	ms	0.5	10
T2	ms	0	200
T3	ms	0	200
T4	ms	-	-
T5	ms	-	-
T6	ms	-	-
T7	ms	0	50
T8	ms	0	500
Т9	ms	0	10
T10	ms	150	-

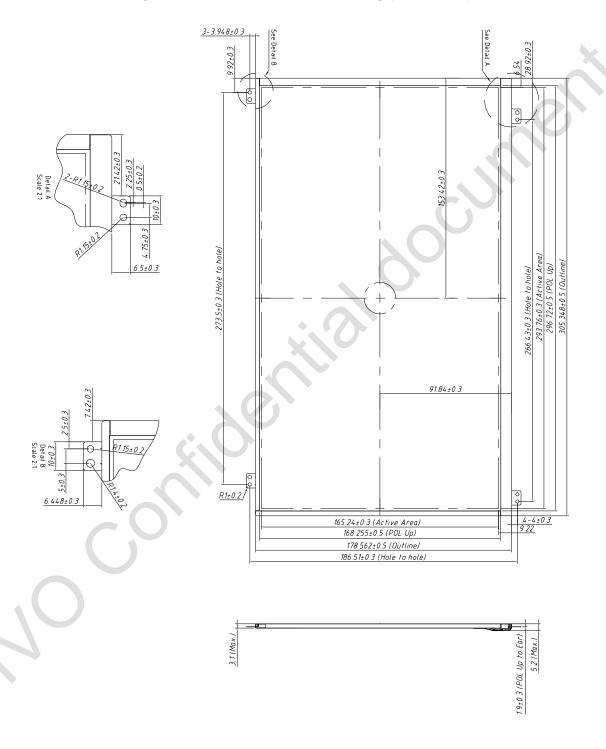


Document Title	M133NWF2 R0 Produc	Page No.	21/31		
Document No.		Issue date	2013/10/24	Revision	00

10.0 Mechanical Characteristics

10.1 Outline Drawing

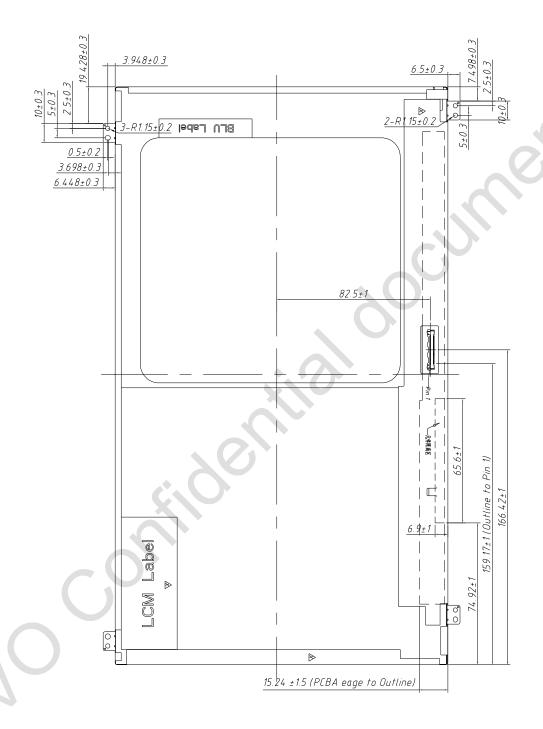
Figure 14 Reference Outline Drawing (Front Side)





Document Title	M133NWF2 R0 Produc	Page No.	22/31		
Document No.		Issue date	2013/10/24	Revision	00

Figure 15 Reference Outline Drawing (Back Side)





Document Title	M133NWF2 R0 Produc	Page No.	23/31		
Document No.		Issue date	2013/10/24	Revision	00

10.2 Dimension Specifications

Table 13 Module Outline Dimension Specifications

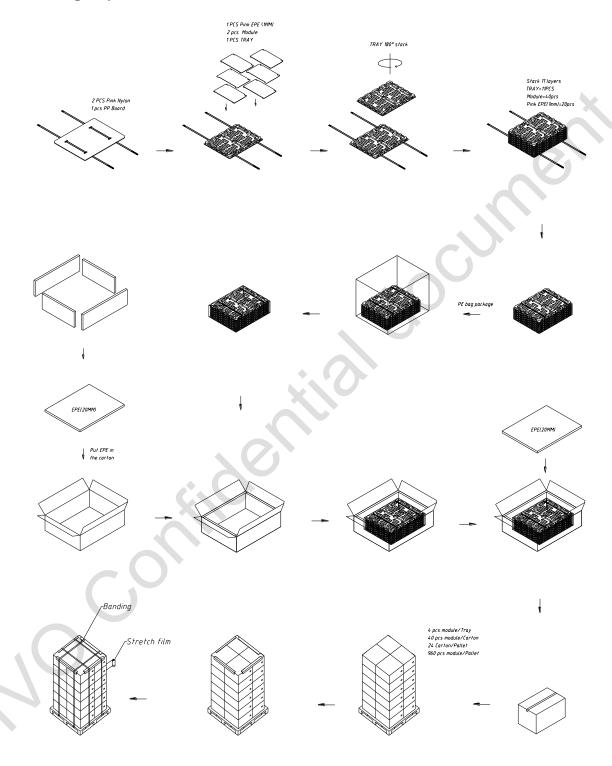
Item	Min.	Тур.	Max.	Units
Width	304.848	305.348	305.848	mm
Height	178.062	178.562	179.062	mm
Thickness	-	-	5.2	mm
Weight	-	-	320	g

Note: Measure instrument is vernier caliper.



Document Title	M133NWF2 R0 Produc	Page No.	24/31		
Document No.		Issue date	2013/10/24	Revision	00

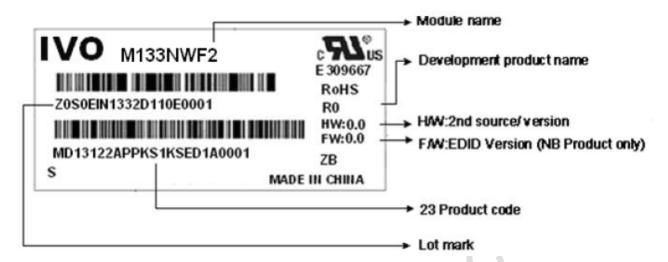
11.0 Package Specification





Document Title	M133NWF2 R0 Produc	Page No.	25/31		
Document No.		Issue date	2013/10/24	Revision	00

12.0 Lot Mark



12.1 Lot Mark

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
				l															II

code 1,2,4,5,6,7,8,9,10,11,16: IVO internal flow control code.

code 3: Production location.

code 12: Production year.

code 13: Production month.

code 14,15: Production date.

code 17,18,19,20: Serial number.

Note (1) Production Year

Year	2,006	2,007	2,008	2,009	2,010	2,011	2,012	2,013	2,014	2,015
Mark	6	7	8	9	Α	В	С	D	Ш	F

Note (2) Production Month

Month	Jan.	Feb.	Mar.	Apr.	Мау.	Jun.	Jul.	Aug.	Sep.	Oct	Nov.	Dec.
Mark	1	2	3	4	5	6	7	8	9	Α	В	С

12.2 23 Product Barcode

_																							
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

code 1,2: Manufacture District.

code 3,4,5,6,7: IVO internal module name.

code 8,9,10,13,16: IVO internal flow control code.

code 11,12: Cell location Suzhou defined as "SZ".

code 14,15: Module line kunshan defined as" KS".

code 17,18,19: Year, Month, Day Refer to Note(1) and Note(2) of Lot Mark.

code 20~23: Serial Number.



Document Title	M133NWF2 R0 Produc	Page No.	26/31		
Document No.		Issue date	2013/10/24	Revision	00

13.0 General Precaution

13.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life-threatening or otherwise catastrophic.

13.2 Handling Precaution

- (1) Please mount LCD module by using mounting holes arranged in four corners tightly.
- (2) Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. IVO does not warrant the module, if customers disassemble or modify the module.
- (3) If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystal, and do not contact liquid crystal with skin. If liquid crystal contacts mouth or eyes, rinse out with water immediately. If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.
- (4) Disconnect power supply before handling LCD module
- (5) Refrain from strong mechanical shock and /or any force to the module.
- (6) Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature; etc otherwise LCD module may be damaged. It's recommended employing protection circuit for power supply.
- (7) Do not touch, push or rub the polarizer with anything harder than HB pencil lead. Use fingerstalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.
- (8) When the surface is dusty, please wipe gently with absorbent cotton or other soft Material. When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzene or other adequate solvent.
- (9) Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may causes deformation or color fading.
- (10) Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.
- (11) Because LCD module uses CMOS-IC on circuit board and TFT-LCD panel, it is very weak to electrostatic discharge, please be careful with electrostatic discharge. Persons who handle the module should be grounded through adequate methods.
- (12) Do not adjust the variable resistor located on the module.

13.3 Storage Precaution

- (1) Please do not leave LCD module in the environment of high humidity and high temperature for a long time.
- (2) The module shall not be exposed under strong light such as direct sunlight. Otherwise, display characteristics may be changed.
- (3) The module should be stored in a dark place. It is prohibited to apply sunlight or fluorescent light in storage.

13.4 Operation Precaution

- (1) Do not connect or disconnect the module in the "Power ON" condition.
- (2) Power supply should always be turned on/off by "Power ON/OFF Sequence".
- (3) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference should be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.



Document Title	M133NWF2 R0 Produc	t Information		Page No.	27/31
Document No.		Issue date	2013/10/24	Revision	00

(4) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

13.5 Others

- (1) Ultra-violet ray filter is necessary for outdoor operation.
- (2) Avoid condensation of water which may result in improper operation or disconnection of electrode.
- (3) If the module keeps displaying the same pattern for a long period of time, the image may be "sticked" to the screen.
- (4) This module has its circuitry PCB's on the rear side and should be handled carefully in order not to be stressed.

13.6 Disposal

When disposing LCD module, obey the local environmental regulations.



Document Title	M133NWF2 R0 Product Information				28/31
Document No.		Issue date	2013/10/24	Revision	00

14.0EDID Data Structure

Table 14 EDID Table Format

Address	Address	Field Name & Comments	Value	Value	Value
(Decimal)	(HEX)	Field Name & Comments	(HEX)	(BIN)	(DEC)
0	0	Header	00	00000000	0
1	1	Header	FF	11111111	255
2	2	Header	FF	11111111	255
3	3	Header	FF	11111111	255
4	4	Header	FF	11111111	255
5	5	Header	FF	11111111	255
6	6	Header	FF	11111111	255
7	7	Header	00	00000000	0
8	8	manufacture code	26	00100110	38
9	9	manufacture code	CF	11001111	207
10	0A	Product Code	34	00110100	52
11	0B	Product Code	05	00000101	5
12	0C	LCD module Serial No –("0" if not used)	00	00000000	0
13	0D	LCD module Serial No -("0" if not used)	00	00000000	0
14	0E	LCD module Serial No -("0" if not used)	00	00000000	0
15	0F	LCD module Serial No –("0" if not used)	00	00000000	0
16	10	Week of manufacture	00	00000000	0
17	11	Year of manufacture	17	00010111	23
18	12	EDID Structure Ver # = 1	01	00000001	1
19	13	EDID revision # = 3	04	00000100	4
20	14	Video I/P definition = Digital I/P (80h)	80	10000000	128
21	15	Max H image size = (Rounded to cm)	1D	00011101	29
22	16	Max V image size = (Rounded to cm)	11	00010001	17
23	17	Display Gamma	78	01111000	120
24	18	Feature support (no DPMS, Active off, RGB, timing BLK 1)	0A	00001010	10
25	19	Red/Green Low bits (RxRy/GxGy)	DE	11011110	222
26	19 1A	Blue/White Low bits (BxBy/WxWy)	50	01010100	80
27	1B	Red X Rx	A3	101000011	163
28	1C	Red Y Ry	54	01010100	84
	1D	•	4C		
29	טו	Green X Gx	40	01001100	76



Document Title	M133NWF2 R0 Product Information				29/31
Document No.		Issue date	2013/10/24	Revision	00

30			0 40			1-0
32 20 Blue Y By 0F 00001111 15			•			
33 21 White XWx 50 01010000 80 34 22 White Y Wy 54 01010100 84 35 23 Established timings 1 (00h if not used) 00 00000000 0 36 24 Established timings 2 (00h if not used) 00 00000000 0 37 25 Manufacturer@39; timings (00h if not used) 01 00000000 0 38 26 Standard timing ID1 (01h if not used) 01 00000001 1 39 27 Standard timing ID2 (01h if not used) 01 00000001 1 40 28 Standard timing ID2 (01h if not used) 01 00000001 1 41 29 Standard timing ID3 (01h if not used) 01 00000001 1 42 2A Standard timing ID3 (01h if not used) 01 00000001 1 43 2B Standard timing ID3 (01h if not used) 01 00000001 1 44 2C Standard timing ID4 (01h if not used) 01 00000001 1 45 2D Standard timing ID4 (01h if not used) 01 00000001 1 46 2E Standard timing ID5 (01h if not used) 01 00000001 1 47 2F Standard timing ID5 (01h if not used) 01 00000001 1 48 30 Standard timing ID5 (01h if not used) 01 00000001 1 48 30 Standard timing ID6 (01h if not used) 01 00000001 1 49 31 Standard timing ID6 (01h if not used) 01 00000001 1 50 32 Standard timing ID6 (01h if not used) 01 00000001 1 51 33 Standard timing ID7 (01h if not used) 01 00000001 1 52 34 Standard timing ID7 (01h if not used) 01 00000001 1 53 35 Standard timing ID8 (01h if not used) 01 00000001 1 54 36 Pixel Clock LSB 1A 00011010 26 55 37 Pixel Clock LSB 1A 00011010 54 56 38 Horizontal Active (lower 8 bits) 80 10000000 128 57 39 Hor blanking (lower 8 bits) 80 11000000 15 58 3A Vertical active(lower 8 bits) 38 00111000 56 60 3C Vertical blanking(lower 8 bits) 20 00100000 64 62 3E Horizontal Sync Offset 32 00110010 50						
34 22 White YWy 54 01010100 84 35 23 Established timings 1 (00h if not used) 00 00000000 0 36 24 Established timing 2 (00h if not used) 00 00000000 0 37 25 Manufacturer@39:s timings (00h if not used) 00 00000000 0 38 26 Standard timing ID1 (01h if not used) 01 00000001 1 39 27 Standard timing ID2 (01h if not used) 01 00000001 1 40 28 Standard timing ID2 (01h if not used) 01 00000001 1 41 29 Standard timing ID2 (01h if not used) 01 00000001 1 42 2A Standard timing ID3 (01h if not used) 01 00000001 1 43 2B Standard timing ID3 (01h if not used) 01 00000001 1 44 2C Standard timing ID4 (01h if not used) 01 00000001 1 45 2D Standard timing ID4 (01h if not used) 01 00000001 1 46 2E Standard timing ID5 (01h if not used) 01 00000001 1 47 2F Standard timing ID5 (01h if not used) 01 00000001 1 48 30 Standard timing ID5 (01h if not used) 01 00000001 1 48 30 Standard timing ID6 (01h if not used) 01 00000001 1 49 31 Standard timing ID6 (01h if not used) 01 00000001 1 50 32 Standard timing ID6 (01h if not used) 01 00000001 1 51 33 Standard timing ID7 (01h if not used) 01 00000001 1 52 34 Standard timing ID7 (01h if not used) 01 00000001 1 53 35 Standard timing ID8 (01h if not used) 01 00000001 1 54 36 Pixel Clock LSB 1A 00011010 26 55 37 Pixel Clock LSB 1A 00011010 54 58 3A Bits) Vertical Blanking (upper4:4 bits) 40 01100000 32 61 3D Vertical Active : Vertical Blanking (upper4:4 bits) 40 01000000 64 62 3E Horizontal Active (lower 8 bits) 40 01000000 64			·			
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37	35	23	Established timings 1 (00h if not used)	00	00000000	
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39 27 Standard timing ID1 (01h if not used) 01 00000001 1 40 28 Standard timing ID2 (01h if not used) 01 00000001 1 41 29 Standard timing ID2 (01h if not used) 01 00000001 1 42 2A Standard timing ID3 (01h if not used) 01 00000001 1 43 2B Standard timing ID3 (01h if not used) 01 00000001 1 44 2C Standard timing ID4 (01h if not used) 01 00000001 1 45 2D Standard timing ID5 (01h if not used) 01 00000001 1 46 2E Standard timing ID5 (01h if not used) 01 00000001 1 47 2F Standard timing ID5 (01h if not used) 01 00000001 1 48 30 Standard timing ID6 (01h if not used) 01 00000001 1 49 31 Standard timing ID7 (01h if not used) 01 00000001 1 50 32 Standard timin	37	25	Manufacturer@39;s timings (00h if not used)	00	00000000	0
40 28 Standard timing ID2 (01h if not used) 01 00000001 1 41 29 Standard timing ID2 (01h if not used) 01 00000001 1 42 2A Standard timing ID3 (01h if not used) 01 00000001 1 43 2B Standard timing ID3 (01h if not used) 01 00000001 1 44 2C Standard timing ID4 (01h if not used) 01 00000001 1 45 2D Standard timing ID4 (01h if not used) 01 00000001 1 46 2E Standard timing ID5 (01h if not used) 01 00000001 1 47 2F Standard timing ID5 (01h if not used) 01 00000001 1 48 30 Standard timing ID5 (01h if not used) 01 00000001 1 49 31 Standard timing ID6 (01h if not used) 01 00000001 1 50 32 Standard timing ID7 (01h if not used) 01 00000001 1 51 33 Standard timing ID7 (01h if not used) 01 00000001 1 52 34 Standard timing ID8 (01h if not used) 01 00000001 1 53 35 Standard timing ID8 (01h if not used) 01 00000001 1 54 36 Pixel Clock LSB 1A 00011010 26 55 37 Pixel Clock LSB 1A 00011010 54 56 38 Horizontal Active (lower 8 bits) 80 10000000 128 57 39 Hor blanking (lower 8 bits) 80 10110000 128 58 3A Wertcal active/Horizontal blanking (upper4:4 bits) 40 01100000 32 61 3D Vertical Blanking (lower 8 bits) 20 00100000 32 61 3D Vertical Active : Vertical Blanking (upper4:4 bits) 40 01000000 64 62 3E Horizontal Sync Offset 32 00110010 50	38	26	Standard timing ID1 (01h if not used)	01	00000001	1
41 29 Standard timing ID2 (01h if not used) 01 00000001 1 42 2A Standard timing ID3 (01h if not used) 01 00000001 1 43 2B Standard timing ID3 (01h if not used) 01 00000001 1 44 2C Standard timing ID4 (01h if not used) 01 00000001 1 45 2D Standard timing ID5 (01h if not used) 01 00000001 1 46 2E Standard timing ID5 (01h if not used) 01 00000001 1 47 2F Standard timing ID5 (01h if not used) 01 00000001 1 48 30 Standard timing ID6 (01h if not used) 01 00000001 1 49 31 Standard timing ID7 (01h if not used) 01 00000001 1 50 32 Standard timing ID7 (01h if not used) 01 00000001 1 51 33 Standard timing ID8 (01h if not used) 01 00000001 1 52 34 Standard timin	39	27	Standard timing ID1 (01h if not used)	01	00000001	1
42 2A Standard timing ID3 (01h if not used) 01 00000001 1 43 2B Standard timing ID3 (01h if not used) 01 00000001 1 44 2C Standard timing ID4 (01h if not used) 01 00000001 1 45 2D Standard timing ID5 (01h if not used) 01 00000001 1 46 2E Standard timing ID5 (01h if not used) 01 00000001 1 47 2F Standard timing ID6 (01h if not used) 01 00000001 1 48 30 Standard timing ID6 (01h if not used) 01 00000001 1 49 31 Standard timing ID6 (01h if not used) 01 00000001 1 50 32 Standard timing ID7 (01h if not used) 01 00000001 1 51 33 Standard timing ID8 (01h if not used) 01 00000001 1 52 34 Standard timing ID8 (01h if not used) 01 00000001 1 53 35 Standard timin	40	28	Standard timing ID2 (01h if not used)	01	00000001	1
43 2B Standard timing ID3 (01h if not used) 01 00000001 1 44 2C Standard timing ID4 (01h if not used) 01 00000001 1 45 2D Standard timing ID4 (01h if not used) 01 00000001 1 46 2E Standard timing ID5 (01h if not used) 01 00000001 1 47 2F Standard timing ID5 (01h if not used) 01 00000001 1 48 30 Standard timing ID6 (01h if not used) 01 00000001 1 49 31 Standard timing ID6 (01h if not used) 01 00000001 1 50 32 Standard timing ID7 (01h if not used) 01 00000001 1 51 33 Standard timing ID7 (01h if not used) 01 00000001 1 52 34 Standard timing ID8 (01h if not used) 01 00000001 1 53 35 Standard timing ID8 (01h if not used) 01 00000001 1 54 36 Pixel Clock LSB 1A 00011010 26 55 37 Pixel Clock LSB 1A 00011010 54 56 38 Horizontal Active (lower 8 bits) 80 10000000 128 57 39 Hor blanking (lower 8 bits) A0 10100000 160 60 3C Vertical blanking (lower 8 bits) 38 00111000 56 60 3C Vertical blanking (lower 8 bits) 20 00100000 64 62 3E Horizontal Sync Offset 32 00110010 50	41	29	Standard timing ID2 (01h if not used)	01	00000001	1
44 2C Standard timing ID4 (01h if not used) 01 00000001 1 45 2D Standard timing ID4 (01h if not used) 01 00000001 1 46 2E Standard timing ID5 (01h if not used) 01 00000001 1 47 2F Standard timing ID5 (01h if not used) 01 00000001 1 48 30 Standard timing ID6 (01h if not used) 01 00000001 1 49 31 Standard timing ID6 (01h if not used) 01 00000001 1 50 32 Standard timing ID7 (01h if not used) 01 00000001 1 51 33 Standard timing ID8 (01h if not used) 01 00000001 1 52 34 Standard timing ID8 (01h if not used) 01 00000001 1 53 35 Standard timing ID8 (01h if not used) 01 00000001 1 54 36 Pixel Clock LSB 1A 00011010 26 55 37 Pixel Clock HSB 36	42	2A	Standard timing ID3 (01h if not used)	01	00000001	1
45 2D Standard timing ID4 (01h if not used) 01 00000001 1 46 2E Standard timing ID5 (01h if not used) 01 00000001 1 47 2F Standard timing ID5 (01h if not used) 01 00000001 1 48 30 Standard timing ID6 (01h if not used) 01 00000001 1 49 31 Standard timing ID6 (01h if not used) 01 00000001 1 50 32 Standard timing ID7 (01h if not used) 01 00000001 1 51 33 Standard timing ID8 (01h if not used) 01 00000001 1 52 34 Standard timing ID8 (01h if not used) 01 00000001 1 53 35 Standard timing ID8 (01h if not used) 01 00000001 1 54 36 Pixel Clock LSB 1A 00011010 26 55 37 Pixel Clock HSB 36 00110110 54 56 38 Horizontal Active (lower 8 bits) 80 <td>43</td> <td>2B</td> <td>Standard timing ID3 (01h if not used)</td> <td>01</td> <td>00000001</td> <td>1</td>	43	2B	Standard timing ID3 (01h if not used)	01	00000001	1
46 2E Standard timing ID5 (01h if not used) 01 00000001 1 47 2F Standard timing ID5 (01h if not used) 01 00000001 1 48 30 Standard timing ID6 (01h if not used) 01 00000001 1 49 31 Standard timing ID6 (01h if not used) 01 00000001 1 50 32 Standard timing ID7 (01h if not used) 01 00000001 1 51 33 Standard timing ID8 (01h if not used) 01 00000001 1 52 34 Standard timing ID8 (01h if not used) 01 00000001 1 53 35 Standard timing ID8 (01h if not used) 01 00000001 1 54 36 Pixel Clock LSB 1A 00011010 26 55 37 Pixel Clock HSB 36 00110110 54 56 38 Horizontal Active (lower 8 bits) 80 10000000 128 57 39 Hor blanking (lower 8 bits) A0	44	2C	Standard timing ID4 (01h if not used)	01	00000001	1
47 2F Standard timing ID5 (01h if not used) 01 00000001 1 48 30 Standard timing ID6 (01h if not used) 01 00000001 1 49 31 Standard timing ID6 (01h if not used) 01 00000001 1 50 32 Standard timing ID7 (01h if not used) 01 00000001 1 51 33 Standard timing ID8 (01h if not used) 01 00000001 1 52 34 Standard timing ID8 (01h if not used) 01 00000001 1 53 35 Standard timing ID8 (01h if not used) 01 00000001 1 54 36 Pixel Clock LSB 1A 00011010 26 55 37 Pixel Clock HSB 36 00110110 54 56 38 Horizontal Active (lower 8 bits) 80 10000000 128 57 39 Hor blanking (lower 8 bits) A0 1010000 160 58 3A bits) 38 00111000 <td< td=""><td>45</td><td>2D</td><td>Standard timing ID4 (01h if not used)</td><td>01</td><td>00000001</td><td>1</td></td<>	45	2D	Standard timing ID4 (01h if not used)	01	00000001	1
Standard timing ID6 (01h if not used)	46	2E	Standard timing ID5 (01h if not used)	01	00000001	1
49 31 Standard timing ID6 (01h if not used) 01 00000001 1 50 32 Standard timing ID7 (01h if not used) 01 00000001 1 51 33 Standard timing ID7 (01h if not used) 01 00000001 1 52 34 Standard timing ID8 (01h if not used) 01 00000001 1 53 35 Standard timing ID8 (01h if not used) 01 00000001 1 54 36 Pixel Clock LSB 1A 00011010 26 55 37 Pixel Clock HSB 36 00110110 54 56 38 Horizontal Active (lower 8 bits) 80 10000000 128 57 39 Hor blanking (lower 8 bits) A0 10100000 160 40 Horizontal Active/Horizontal blanking (upper4:4 bits) 70 01110000 112 58 3A Vertical active (lower 8 bits) 38 00111000 56 60 3C Vertical blanking (lower 8 bits) 20 00100000 32 61 3D Vertical Active : Vertical Blanking (u	47	2F	Standard timing ID5 (01h if not used)	01	00000001	1
50 32 Standard timing ID7 (01h if not used) 01 00000001 1 51 33 Standard timing ID7 (01h if not used) 01 00000001 1 52 34 Standard timing ID8 (01h if not used) 01 00000001 1 53 35 Standard timing ID8 (01h if not used) 01 00000001 1 54 36 Pixel Clock LSB 1A 00011010 26 55 37 Pixel Clock HSB 36 00110110 54 56 38 Horizontal Active (lower 8 bits) 80 10000000 128 57 39 Hor blanking (lower 8 bits) A0 10100000 160 4 Horizontal Active/Horizontal blanking (upper4:4 bits) 70 01110000 112 58 3A bits) 38 00111000 56 60 3C Vertical blanking (lower 8 bits) 20 00100000 32 61 3D Vertical Active : Vertical Blanking (upper4:4 bits) 40 01000000	48	30	Standard timing ID6 (01h if not used)	01	00000001	1
51 33 Standard timing ID7 (01h if not used) 01 00000001 1 52 34 Standard timing ID8 (01h if not used) 01 00000001 1 53 35 Standard timing ID8 (01h if not used) 01 00000001 1 54 36 Pixel Clock LSB 1A 00011010 26 55 37 Pixel Clock HSB 36 00110110 54 56 38 Horizontal Active (lower 8 bits) 80 10000000 128 57 39 Hor blanking (lower 8 bits) A0 10100000 160 4 Horizontal Active/Horizontal blanking (upper4:4 bits) 70 01110000 112 58 3A Vertical active (lower 8 bits) 38 00111000 56 60 3C Vertical blanking (lower 8 bits) 20 00100000 32 61 3D Vertical Active : Vertical Blanking (upper4:4 bits) 40 01000000 64 62 3E Horizontal Sync Offset 32 00110	49	31	Standard timing ID6 (01h if not used)	01	00000001	1
52 34 Standard timing ID8 (01h if not used) 01 00000001 1 53 35 Standard timing ID8 (01h if not used) 01 00000001 1 54 36 Pixel Clock LSB 1A 00011010 26 55 37 Pixel Clock HSB 36 00110110 54 56 38 Horizontal Active (lower 8 bits) 80 10000000 128 57 39 Hor blanking (lower 8 bits) A0 10100000 160 40 Horizontal Active/Horizontal blanking (upper4:4 bits) 70 01110000 112 58 3A bits) 38 00111000 56 60 3C Vertical active (lower 8 bits) 38 00111000 56 60 3C Vertical blanking (lower 8 bits) 20 00100000 32 61 3D Vertical Blanking (upper4:4 bits) 40 01000000 64 62 3E Horizontal Sync Offset 32 00110010 50	50	32	Standard timing ID7 (01h if not used)	01	00000001	1
53 35 Standard timing ID8 (01h if not used) 01 00000001 1 54 36 Pixel Clock LSB 1A 00011010 26 55 37 Pixel Clock HSB 36 00110110 54 56 38 Horizontal Active (lower 8 bits) 80 10000000 128 57 39 Hor blanking (lower 8 bits) A0 10100000 160 Horizontal Active/Horizontal blanking (upper4:4 bits) 70 01110000 112 58 3A Vertical active(lower 8 bits) 38 00111000 56 60 3C Vertical blanking(lower 8 bits) 20 00100000 32 61 3D Vertical Active : Vertical Blanking (upper4:4 bits) 40 01000000 64 62 3E Horizontal Sync Offset 32 00110010 50	51	33	Standard timing ID7 (01h if not used)	01	00000001	1
53 35 Standard timing ID8 (01h if not used) 01 00000001 1 54 36 Pixel Clock LSB 1A 00011010 26 55 37 Pixel Clock HSB 36 00110110 54 56 38 Horizontal Active (lower 8 bits) 80 10000000 128 57 39 Hor blanking (lower 8 bits) A0 10100000 160 Horizontal Active/Horizontal blanking (upper4:4 bits) 70 01110000 112 58 3A Dits) 38 00111000 56 60 3C Vertical active(lower 8 bits) 38 00111000 56 60 3C Vertical blanking(lower 8 bits) 20 00100000 32 61 3D Vertical Active : Vertical Blanking (upper4:4 bits) 40 01000000 64 62 3E Horizontal Sync Offset 32 00110010 50	52	34	Standard timing ID8 (01h if not used)	01	00000001	1
54 36 Pixel Clock LSB 1A 00011010 26 55 37 Pixel Clock HSB 36 00110110 54 56 38 Horizontal Active (lower 8 bits) 80 10000000 128 57 39 Hor blanking (lower 8 bits) A0 10100000 160 4 Horizontal Active/Horizontal blanking (upper4:4 bits) 70 01110000 112 58 3A Vertcal active(lower 8 bits) 38 00111000 56 60 3C Vertical blanking(lower 8 bits) 20 00100000 32 61 3D Vertical Active : Vertical Blanking (upper4:4 bits) 40 01000000 64 62 3E Horizontal Sync Offset 32 00110010 50	53	35	Standard timing ID8 (01h if not used)	01	00000001	1
55 37 Pixel Clock HSB 36 00110110 54 56 38 Horizontal Active (lower 8 bits) 80 10000000 128 57 39 Hor blanking (lower 8 bits) A0 10100000 160 Horizontal Active/Horizontal blanking (upper4:4 bits) 70 01110000 112 59 3B Vertcal active(lower 8 bits) 38 00111000 56 60 3C Vertical blanking(lower 8 bits) 20 00100000 32 61 3D Vertical Active : Vertical Blanking (upper4:4 bits) 40 01000000 64 62 3E Horizontal Sync Offset 32 00110010 50	54					26
56 38 Horizontal Active (lower 8 bits) 80 10000000 128 57 39 Hor blanking (lower 8 bits) A0 10100000 160 Horizontal Active/Horizontal blanking (upper4:4 bits) 58 3A O1110000 112 59 3B Vertcal active(lower 8 bits) 38 00111000 56 60 3C Vertical blanking(lower 8 bits) 20 00100000 32 61 3D Vertical Active : Vertical Blanking (upper4:4 bits) 40 01000000 64 62 3E Horizontal Sync Offset 32 00110010 50	55	37	Pixel Clock HSB			
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Horizontal Active/Horizontal blanking (upper4:4 bits) 70			,			
58 3A bits) 70 01110000 112 59 3B Vertcal active(lower 8 bits) 38 00111000 56 60 3C Vertical blanking(lower 8 bits) 20 00100000 32 61 3D Vertical Active : Vertical Blanking (upper4:4 bits) 40 01000000 64 62 3E Horizontal Sync Offset 32 00110010 50			<u> </u>	7 10		
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61 3D Vertical Active : Vertical Blanking (upper4:4 bits) 40 01000000 64 62 3E Horizontal Sync Offset 32 00110010 50	59	3B	Vertcal active(lower 8 bits)	38	00111000	56
62 3E Horizontal Sync Offset 32 00110010 50	60	3C	Vertical blanking(lower 8 bits)	20	00100000	32
	61	3D	Vertical Active : Vertical Blanking (upper4:4 bits)	40	01000000	64
63 3F Horizontal Sync Pulse Width 32 00110010 50	62	3E	Horizontal Sync Offset	32	00110010	50
	63	3F	Horizontal Sync Pulse Width	32	00110010	50



Document Title	M133NWF2 R0 Product Information				30/31
Document No.		Issue date	2013/10/24	Revision	00

64	40	Vertical Sync Offset , Sync Width	AA	10101010	170
		Horizontal Vertical Sync Offset/Width upper 2	00	0000000	0
65	41	bits	00	00000000	0
66	42	Horizontal Image Size	26	00100110	38
67	43	Vertical image Size	A5	10100101	165
68	44	Horizontal Image Size / Vertical image size	10	00010000	16
69	45	Horizontal Border = (0 for Notebook LCD)	00	00000000	0
70	46	Vertical Border = (0 for Notebook LCD)	00	00000000	0
71	47	Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives,	19	00011001	25
72	48	Timing Descriptor #2	00	00000000	0
73	49		00	00000000	0
74	4A		00	00000000	0
75	4B		00	00000000	0
76	4C	10	00	00000000	0
77	4D	. 0	00	00000000	0
78	4E	27.0	00	00000000	0
79	4F		00	00000000	0
80	50		00	00000000	0
81	51	70	00	00000000	0
82	52	A* ()	00	00000000	0
83	53		00	00000000	0
84	54		00	00000000	0
85	55		00	00000000	0
86	56		00	00000000	0
87	57	/	00	00000000	0
88	58		00	00000000	0
89	59		00	00000000	0
90	5A	Detailed timing/monitor descriptor#3	00	00000000	0
91	5B	Flag	00	00000000	0
92	5C	Flag	00	00000000	0
93	5D	Range limits	FE	11111110	254
94	5E	Flag	00	00000000	0
95	5F	Min. Vertical Freq	49	01001001	73



Document Title	M133NWF2 R0 Product Information				31/31
Document No.		Issue date	2013/10/24	Revision	00

06	60	May Vartical Eros	6E	01101110	110
96	60	Max. Vertical Freq			
97	61	Min. Horizontal Freq	66	01100110	102
98	62	Max.Horizontal Freq	6F	01101111	111
99	63	Max. Pixel Clock Freq	56	01010110	86
100	64		69	01101001	105
101	65		73	01110011	115
102	66		69	01101001	105
103	67		6F	01101111	111
104	68		6E	01101110	110
105	69	New line character indicates end of ASCII string	0A	00001010	10
106	6A		20	00100000	32
107	6B		20	00100000	32
108	6C	Detailed timing/monitor descriptor #4	00	00000000	0
109	6D	. 0	00	00000000	0
110	6E		00	00000000	0
111	6F	FE (hex) defines ASCII string	FE	11111110	254
112	70	Flag	00	00000000	0
113	71	Manufacture P/N	4D	01001101	77
114	72	Manufacture P/N	31	00110001	49
115	73	Manufacture P/N	33	00110011	51
116	74	Manufacture P/N	33	00110011	51
117	75	Manufacture P/N	4E	01001110	78
118	76	Manufacture P/N	57	01010111	87
119	77	Manufacture P/N	46	01000110	70
120	78	Manufacture P/N	32	00110010	50
121	79	Manufacture P/N	20	00100000	32
122	7A	Manufacture P/N	52	01010010	82
123	7B	Manufacture P/N	30	00110000	48
124	7C	New line character indicates end of ASCII string	20	00100000	32
125	7D		0A	00001010	10
126	7E	Extension Flag = 00	00	00000000	0
127	7F	Checksum	05	00000101	5