Monitor Development
Display & Development Division
IMES Co., Ltd.

TFT Color LCD Module M141-X76H Product Specifications

35.7cm(14.1inch) XGA(1024x768)

APR 27, 2001

Rev. & date		Content of change
Rev.1.0	NOV 10, 2000	Initial Release
Rev.2.0	APR 27, 2001	PDF file

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P/N:6M1476H0
EC :6V24015

Scope

M141-X76H is a High Luminance (320cd/m^2) TFT LCD color module to be designed to realize the Largest Screen TFT monitors of Personal Computer, Industry Applications (F/A), and Medical Equipments. In addition to its large screen, the characteristics of this module are light weight, slim/thin outline, low power consumption and high resolution of XGA(1024x768) capability.

Features

. 35.7cm(14.1 inch) Diagonal
. Native 262k Colors (R/G/B 6 bit each)
. XGA 1024 x 768 pixels
. Low Reflection (Black Matrix)
. Two Lamps Backlight unit
. 320 cd/m^2 typ. High Luminance
. 1.6 typ. TCO uniformity
. 298.5mm x 231.7mm x 8.0mm typ. (without inverter)
. 650 g typ.
. 1.4W typ. for LCD Logic, 7.32 W typ. for Two Lamps
. LVDS Interface
(TI SN75LVDS86DGG or Compatible)
. Side Mount type

Application

. PC Monitors
. Industry Applications
. Medical Equipments

This module does not contain an inverter card for backlight.
The LCD cell is supplied from IBM and ADT.

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1. Characteristics Summary

The following items are characteristics summary on the table under 25 degC condition.

Items	Specifications
Screen Diagonal	35.7cm (14.1")
Active Area	285.7mm(H) x 214.3mm(V)
Pixel Format	1024(x3) x 768
Pixel Pitch	0.279(per one triad) x 0.279
Pixel Arrangement	R,G,B Vertical Stripe
Display Mode	Normally White
Typical White Luminance [cd/m^2] Design Point:(Icfl=3.5mAx2) Design Point:(Icfl=6.0mAx2)	 210 typ.(Center), 190 typ.(5 points average) 320 typ.(Center), 290 typ.(5 points average)
Contrast Ratio	250 : 1 typ.
Viewing Angle [Degrees] K: Contrast Ratio	Horizontal (Right) 40 min K>=10 (Left) 40 min Vertical (Upper) 15 min K>=10 (Lower) 30 min
TCO Uniformity	1.6 typ. 1.65 max
Optical Rise Time/Fall Time	30 msec typ., 50 msec max
Nominal Input Voltage VDD	+3.3 V typ.
Logic Power Consumption (VDD line)	1.4 W typ.
Lamp Power Consumption Design Point:(Icfl=3.5mAx2) Design Point:(Icfl=6.0mAx2)	 4.76 W typ. 7.32 W typ.
Weight	650 grams typ.
Physical Size	298.5mm(W) x 231.7mm(H) x 8.0mm(D) typ.
Electrical Interface	6-bits digital video for each color R/G/B Data, 3 Sync, Clock (4 pairs LVDS)
Supported colors	Native 262k colors (RGB 6-bit data driver)
Screen Criteria	DOT defect: LIT : 9 UNLIT : - Total DOT Defect : 15 Double LIT : 2 Double UNLIT : - Distance LIT : 3 , 20mm Line defect: No Line Defect
Backlight lamp life (Luminance becomes half value of initial value.)	20,000 Hours under following condition. - Temp = 25 degC - Continuos power on
Temperature Range Operating Storage(Shipping)	 +0 to +50 degC -20 to +60 degC

2. Absolute Maximum Ratings

Electrical Absolute Maximum Ratings

Item	Symbol	Min	Max	Unit	Conditions
Supply Voltage Logic/LCD Drive Voltage	VDD	-0.3	+4.0	V	
Input Voltage of Signal	Vin	-0.3	VDD+0.3	V	
CFL Inrush Current	Ircfl	-	20	mA	With Max. duration = 50 (msec)
CFL Current	Icfl	-	7.0	mArms	Exclude inrush current
CFL Ignition Voltage	Vs	-	1,600	Vrms	
Static Electricity					Operators should be grounded in handling the TFT LCD Module

Environmental Absolute Maximum Ratings

Rating	Symbol	Value	Unit	Conditions
Operation Temperature	TOP	0 to +50	DegC	At the glass surface
Operation Humidity	HOP	8 to 95	%RH	Max wet bulb temp. should be 39 degC and No condensation
Storage Temperature	TST	-20 to +60	DegC	At the glass surface
Storage Humidity	HST	5 to 95	%RH	Max wet bulb temp. should be 39 degC and No condensation
Vibration		1.5	G	10-200Hz,X,Y,Z (Note1)
Trapezoidal Shock		50	G	18msec, +/-X,Y,Z (Note1)
Corrosive Gas		Not Acceptable		

Note 1: At testing Vibration and Shock, the fixture in holding the Module to be tested have to be hard rigid enough so that the Module would not be twisted or bent by the fixture.

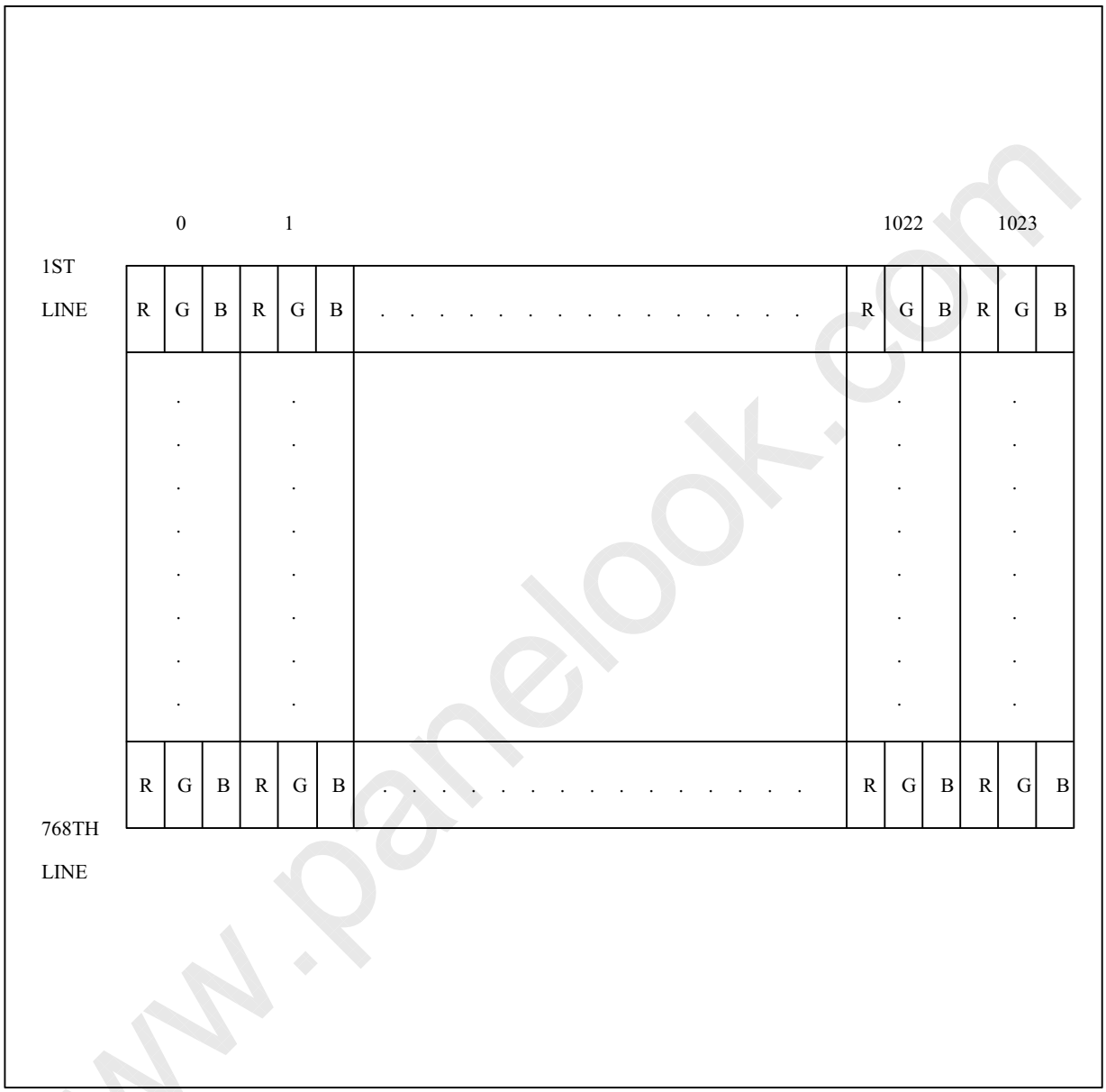
3. Optical Characteristics

The optical characteristics are measured under stable conditions as follows under 25 degC condition.

Item	Conditions	Specification	
		Typ.	Note
Viewing Angle (Degrees) K:Contrast Ratio	Horizontal (Right) K>=10 (Left) Vertical (Upper) K>=10 (lower)	40 40 15 30	- - - -
Contrast ratio		250	-
Response Time (ms)	Rising	30	50(max)
	Falling	30	50(max)
Color Chromaticity (CIE)	Red x	0.598	-
	Red y	0.333	-
	Green x	0.309	-
	Green y	0.559	-
	Blue x	0.152	-
	Blue y	0.148	-
	White x	0.321	-
	White y	0.352	
White Luminance (cd/m2) CFL 6.0mA x2		320 Center 290 5 points average	
TCO uniformity		1.6	1.65(max)

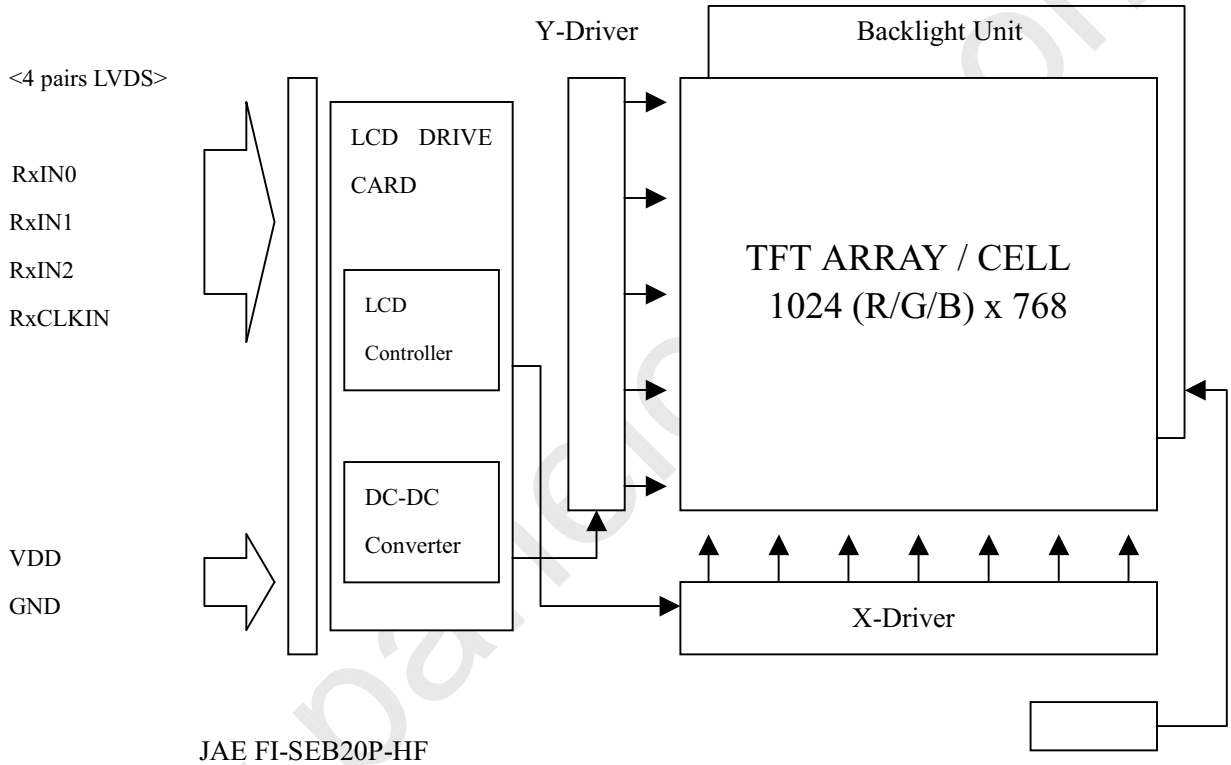
4. Color Arrangement

Following figure shows the relationship of the input signals and LCD pixel format image.



5. Functional Block Diagram

The following diagram shows the functional block of the 14.1 inches Color TFT/LCD Module:



JAE FI-SEB20P-HF
Mating JAE FI-S20S or FI-SE20M with FI-C3-A1

Lamp Connector (2pin) x2
JST BHTR-02VS
Mating JST SM02B-BHTS-B-TB

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6. Signal Interface

6.1 Connectors

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

	Supplier Name	Supplier's Part Number
LCD Signal Connector	JAE	FI-SEB20P-HF
Mating Housing	JAE	FI-S20S or FI-SE20M or FI-S20S with shell.
Mating Contact	JAE	FI-C3-A1

	Supplier Name	Supplier's Part Number
Lamp Connector	JST	BHTR-02VS
Mating Connector	JST	SM02B-BHTS-B-TB

6.2 Signal Pin

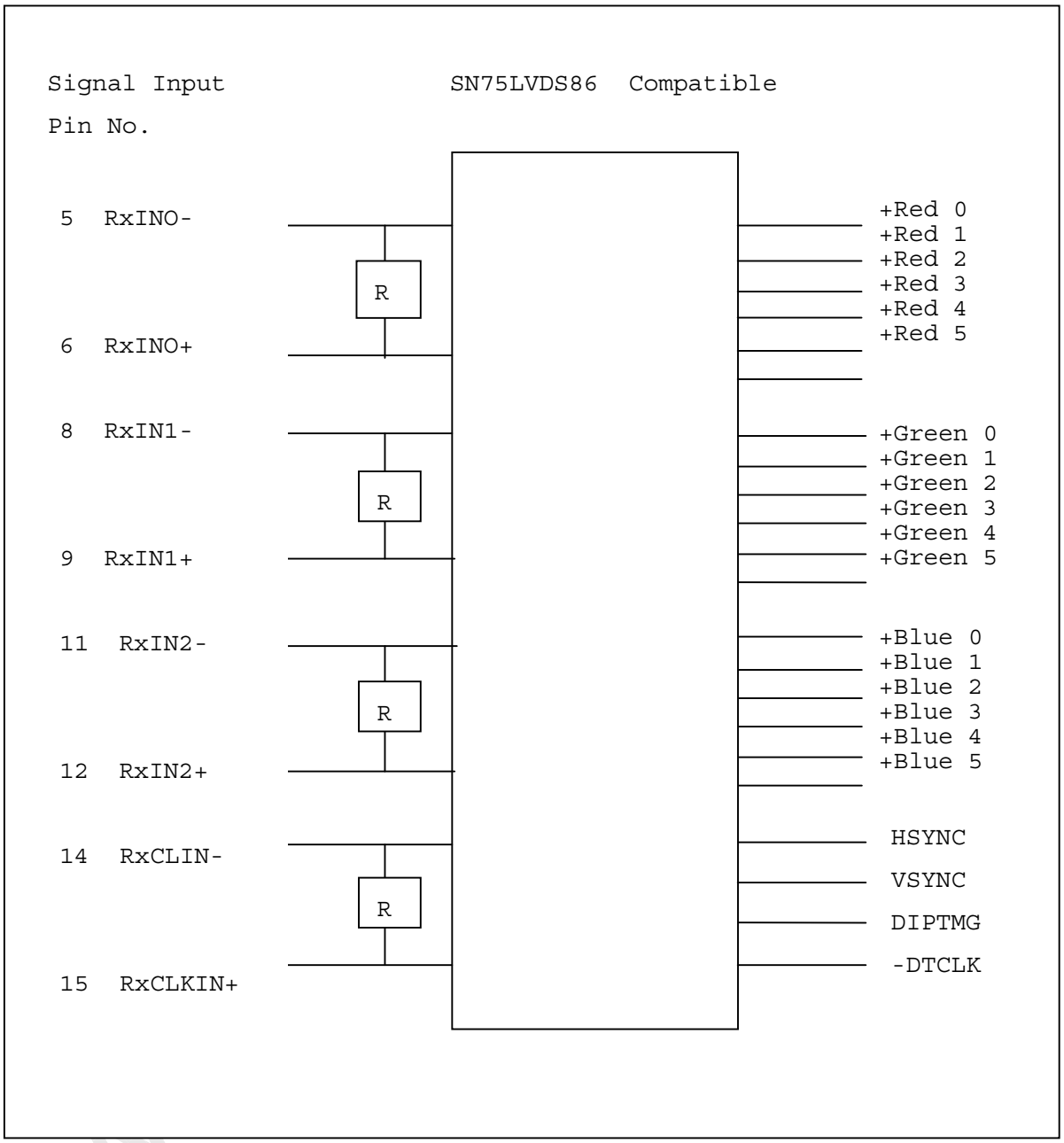
Pin#	Signal name	Pin#	Signal Name
1	VDD	11	Rxin2-
2	VDD	12	Rxin2+
3	GND	13	GND
4	GND	14	RxCLKIN-
5	RxIN0-	15	RxCLKIN+
6	RxIN0+	16	GND
7	GND	17	Reserved
8	Rxin1-	18	Reserved
9	Rxin1+	19	GND
10	GND	20	GND

6.3 Signal Description

The module using a LVDS compatible receiver. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS84 (negative edge sampling) or compatible.

Pin #	Signal Name	Description
1	VDD	+3.3V Power Supply
2	VDD	+3.3V Power Supply
3	GND	Ground
4	GND	Ground
5	RxIN0-	Negative LVDS differential data input (R0-R5,G0)
6	RxIN0+	Positive LVDS differential data input (R0-R5,G0)
7	GND	Ground
8	RxIN1-	Negative LVDS differential data input (G1-G5,B0-B1)
9	RxIN1+	Positive LVDS differential data input (G1-G5,B0-B1)
10	GND	Ground
11	RxIN2-	Negative LVDS differential data input (B2-B5,HSYNC,VSYNC, DSPTMG)
12	RxIN2+	Positive LVDS differential data input (B2-B5,HSYNC,VSYNC, DSPTMG)
13	GND	Ground
14	RxCLKIN-	Negative LVDS differential clock input
15	RxCLKIN+	Positive LVDS differential clock input
16	GND	Ground
17	Reserved	Reserved
18	Reserved	Reserved
19	GND	Ground
20	GND	Ground

Internal circuit of LVDS input are as follows.



The module uses a 100 ohms resistor between positive and negative data lines of each receiver input.

Signal Name	Description	
+RED5 +RED4 +RED3 +RED2 +RED1 +RED0	Red Data 5 Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 Red-pixel Data	(MSB) (LSB) Each red pixel's data consists of these 6 bits pixel data
+GREEN5 +GREEN4 +GREEN3 +GREEN2 +GREEN1 +GREEN0	Green Data 5 Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 Green-Pixel-Data	(MSB) (LSB) Each Green pixel's data consists of these 6 bits pixel data
+BLUE5 +BLUE4 +BLUE3 +BLUE2 +BLUE1 +BLUE0	Blue Data 5 Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 Blue-Pixel-Data	(MSB) (LSB) Each Blue pixel's data consists of these 6 bits pixel data
-DTCLK	Data Clock	The typical frequency is 65.0 MHz. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high.
DSPTMG	Display Timing	This signal strobed at falling edge of –DTCLK. When the signal is high, the pixel data shall be valid to be displayed.
VSYNC	Vertical Sync	The signal is synchronized to –DTCLK.
HSYNC	Horizontal Sync	The signal is synchronized to –DTCLK.

Note: Output signals from system shall be low or Hi-Z state when VDD is off.

6.4 Signal Electrical Characteristics

Input signals shall be low or Hi-Z state when VDD is off.

It is recommended to refer the specifications of SN75LVDS86DGG(Texas Instruments) in detail.

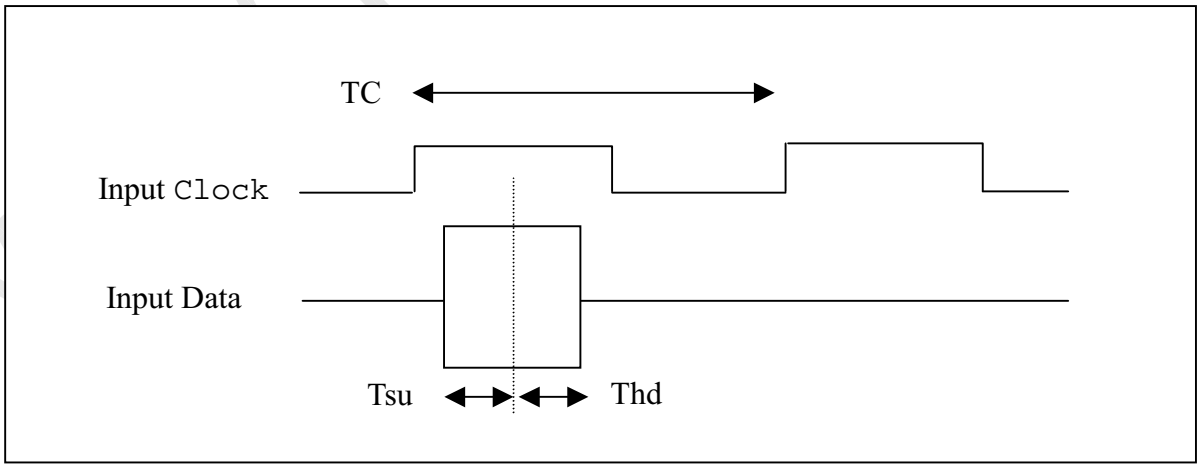
Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
Vth	Differential Input High Voltage (VCM=+1.2V)		+100	mV
Vtl	Differential Input Low Voltage (VCM=+1.2V)	-100		mV

LVDS Macro AC characteristics are as follows;

	Symbol	Min.	Typ.	Max.	Unit	Conditions
Clock Frequency	Fc	50	65	67	MHz	
Cycle Time	Tc	14.93	15.38	20.00	ns	
PLL lock time	Tpll			10	ms	
Data Setup Time	Tsu	600			ps	F=65MHz,jitter<50ps, Vth-Vtl=200mV, Vcm=1.2V,Delta Vcm=0
Data Hold Time	Thd	600			ps	
Cycle-to-cycle jitter marjin	TCCJM	-150		+150	ps	
Cycle modulation rate	TCCJavg			20	ps/clk	(*1)

(*1) This specification defines maximum average cycle modulation rate in peak-to–peak transition within any 100 clock cycles. This specification is applied only if input clock peak jitter within any 100 cycles is greater than 300ps.



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6.5 Signal for Lamp Connector

There are two connectors for two lamps.

Pin No.	Signal Name
1	Lamp high Voltage
2	Lamp Low Voltage

7. Lamp Interface Specification and Guide Line for CFL Inverter

Parameter	Symbol	Min	D.P-1 Note5	D.P-2 Note 5	Max	Units	Condition
White Luminance Center 5 points average		-	 210 190	 320 290	-	cd/m^2	(Ta=25degC) Two Lamps 2 x Icfl
CFL current (per lamp)	Icfl	3.0	3.5	6.0	6.5	mArms	(Ta=25 degC) **Note 4**
CFL Frequency	fcfl	30	40	40	60	KHz	(Ta=25 degC) **Note 1**
CFL Ignition Voltage	Vicfl	1,400				Vrms	(Ta=0 degC) **Note 3**
CFL Discharge Voltage (Reference)	Vcfl		680	610		Vrms	(Ta=25 degC) **Note 2**
CFL Power consumption (per lamp)	Pcfl		2.38	3.66		W	(Ta=25 degC) **Note 2**

Note 1: CFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 2: Calculated value for reference (Icfl x Vcfl = Pcfl).

Note 3: CFL inverter should be able to give out a power that has a generating capacity of over 1,400 voltage. Lamp units need 1,400 volts minimum for ignition.

Note 4: It should be employed the inverter which has “Duty Dimming”, if Icfl is less than 4 mA.

Note 5: DP-1 and DP-2 are IMES recommended Design Points.

*1 All of characteristics listed are measured under the condition using IMES Test inverter.

*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.

*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CFL, for instance, becomes more than 1[M ohm] when CFL is damaged.

*4 Generally, CFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [sec] until discharge.

*5 CFL discharge frequency must be carefully chosen so as to produce interfering noise stripes on the screen.

*6 Reducing CFL current increases CFL discharge voltage and generally increases CFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

8. Interface Timings

Basically, interface timings should match the VESA 1024x768 / 60 Hz (VG901101) manufacturing guide line timing.

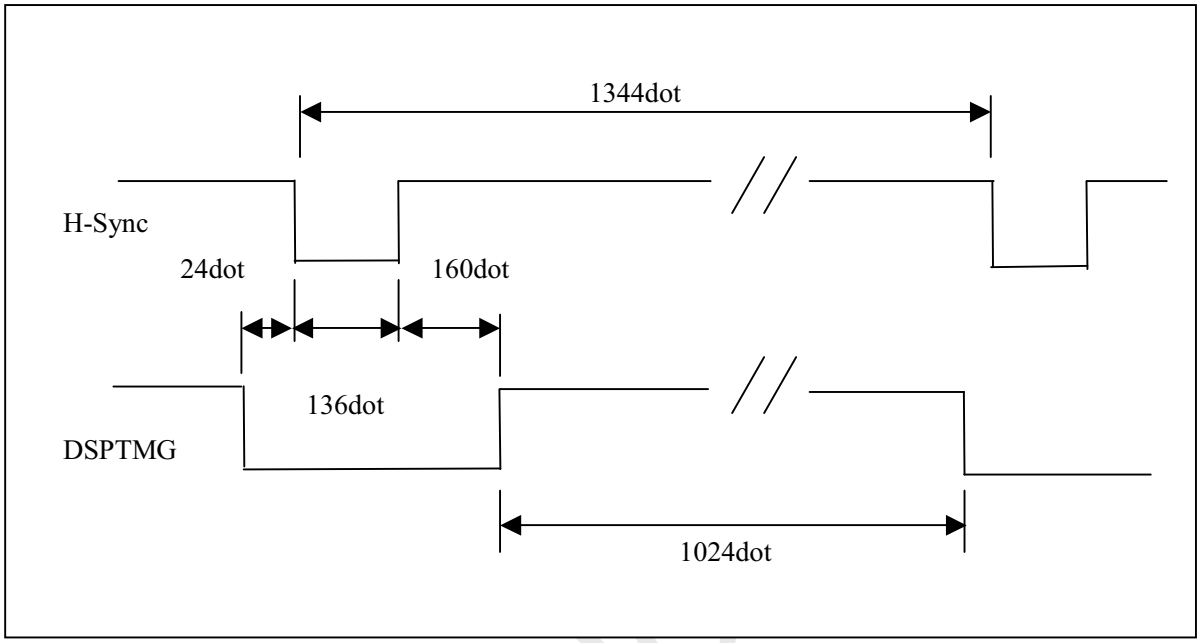
8.1 Timing Characteristics

Symbol	Signal Description	MIN	TYP	MAX	UNIT
Fdck	DTCLK frequency		65.00		MHz
Tck	DTCLK cycle time		15.38		nsec
Tx	X total time	1206	1344	2047	Tck
Tacx	X active time	1024	1024	1024	Tck
Tbkx	X blank time	90	320		Tck
Hsync	H-frequency		48.363		KHz
Hsw	H-sync width	2	136		Tck
Hbp	H-sync back porch	1	160		Tck
Hfp	H-sync front porch	0	24		Tck
Ty	Y total time	771	806	1023	Tx
Tacy	Y active time	768	768	768	Tx
Vsync	Frame rate	(55)	60	61	Hz
Vw	V-sync width	1	6		Tx
Vfp	V-sync front porch	1	3		Tx
Vbp	V-sync back porch	7	29	63	Tx

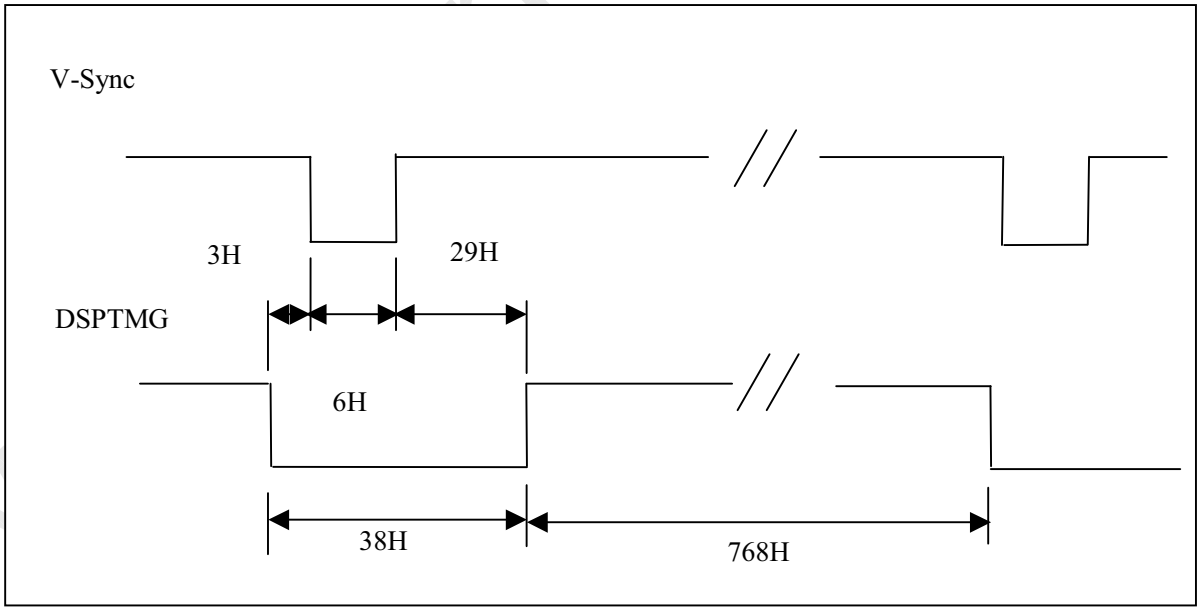
Note: Hsw(H-sync width)+Hbp(H-sync back porch) should be less than 515 Tck.

8.2 Timing Definition

Horizontal Timing



Vertical Timing



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9. Power Consumption

Input power specifications are as follows;

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITION
VDD	Logic/LCD Drive Voltage	+3.0	+3.3	+3.6	V	Load Capacitance 20uF typ
PDD	VDD Power		1.4	1.7	W	All black Pattern **Note 1**
PDDmax	VDD Power max			1.8	W	Max Pattern **Note 2**
IDD	VDD Current		420	470	mA	All black Pattern **Note 1**
IDDmax	VDD Current max			500	mA	Max Pattern **Note 2**
VDDrp	Allowable Logic/LCD Drive Ripple voltage			100	mVp-p	Max Pattern **Note 3**
VDDns	Allowable Logic/LCD Drive Ripple noise			100	mVp-p	

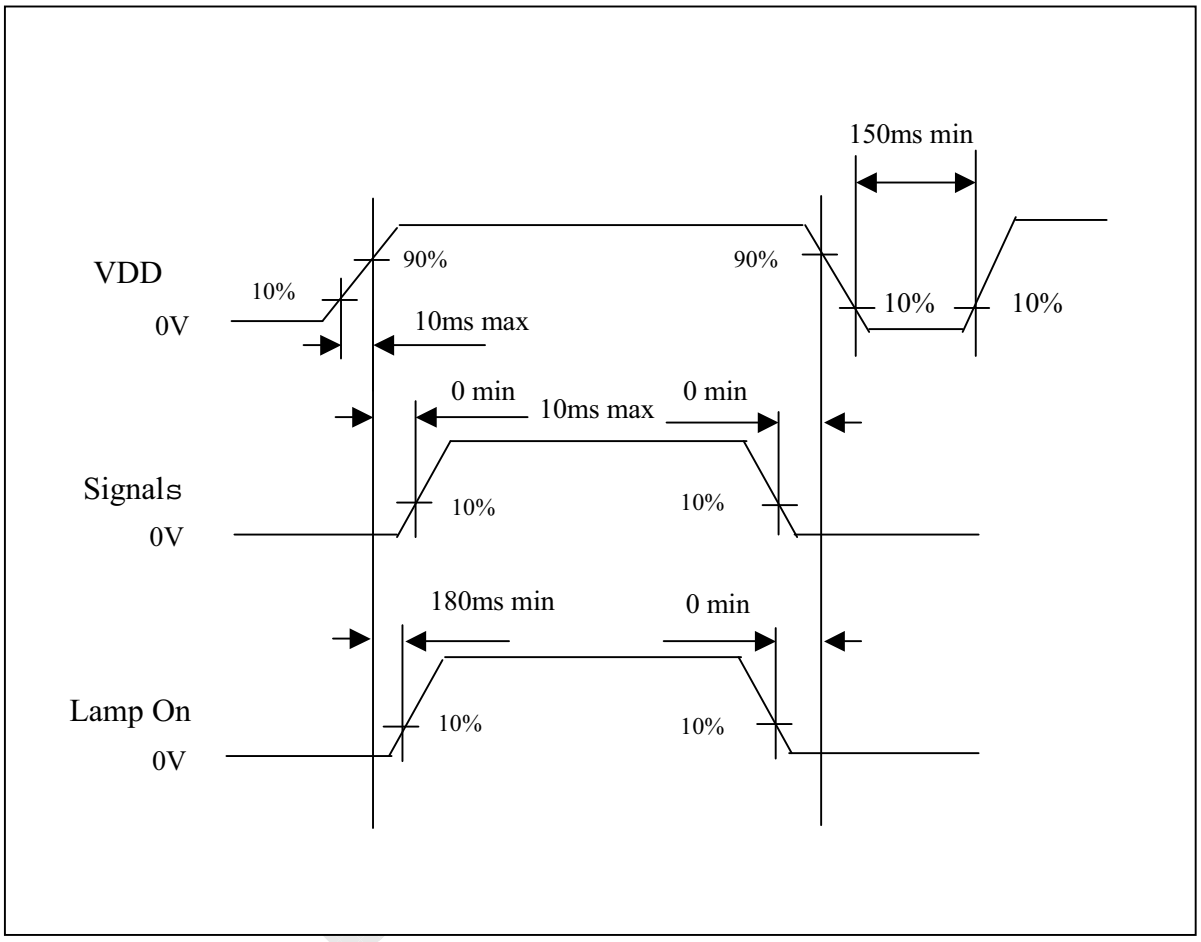
Note 1: VDD=3.0V

Note 2: VDD=3.3V

Note 3: VDD=3.6V

10. Power ON/OFF sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



11. Handling Precautions

(REFER ALSO THE FIGURES ON NEXT PAGE)

l) Since front polarizer is easily damaged, pay attention not to scratch it.

2) Be sure to turn off power supply when inserting or disconnecting from input connector.

3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots .

4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.

5) Since the panel is made of glass, it may break or creak if dropped or bumped on hard surface.

6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling .

7) Do not open nor modify the Module Assembly.

8) Do not press the reflector sheet at the back of the module to any directions.

9) In case if a Module has to be put back into the packing container slot after once it was taken out from the container, do not press the center of the CFL Reflector edge. Instead, press at the far ends of the CFL Reflector edge softly. Otherwise the TFT Module may be damaged.

10) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.

11) At and after installation of the TFT Module into an enclosure (Notebook PC Bezel, for example), do not twist nor bent the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

12) Cold cathode fluorescent (CFL) lamp in LCD contains a small amount of mercury. Please follow local ordinances or regulations for disposal.

13) Small amount of materials having no flammability grade is used in the LCD module. The LCD module should be supplied by power complied with requirements of Limited Power Source (2.11,IEC60950 or UL1950), or applied exemption conditions of flammability requirements (4.4.3.3, IEC60950 or UL1950) in an end of product.

14) The LCD module is designed so that the CFL in it is supplied by Limited Current Circuit(2.4, IEC60950 or UL1950). Do not connect the CFL in Hazardous Voltage Circuit.

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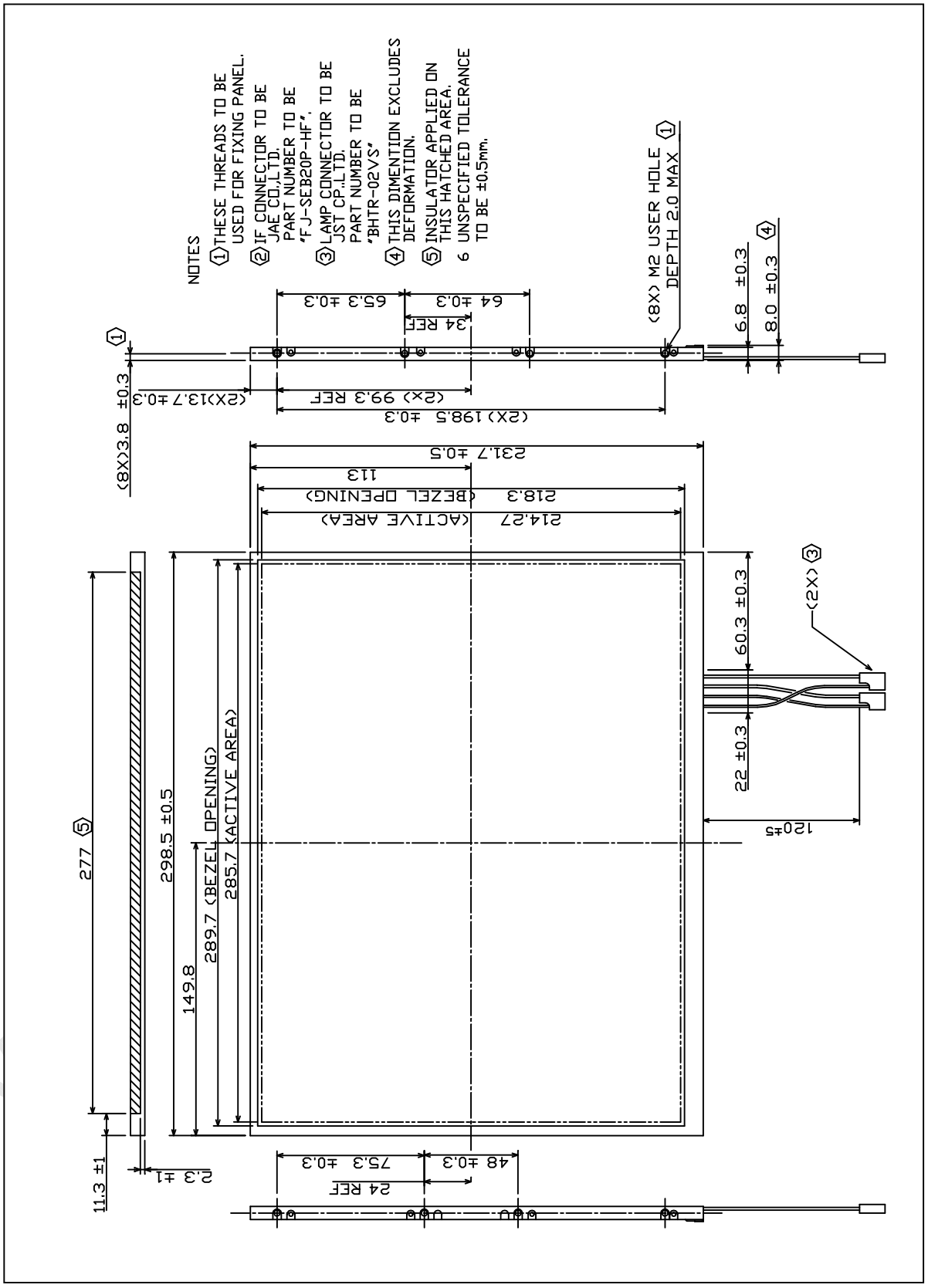
- The information contained herein may be changed without prior notice. It is therefore advisable to contact IMES before proceeding with the design of equipment incorporating this product.

12. Reference Drawing



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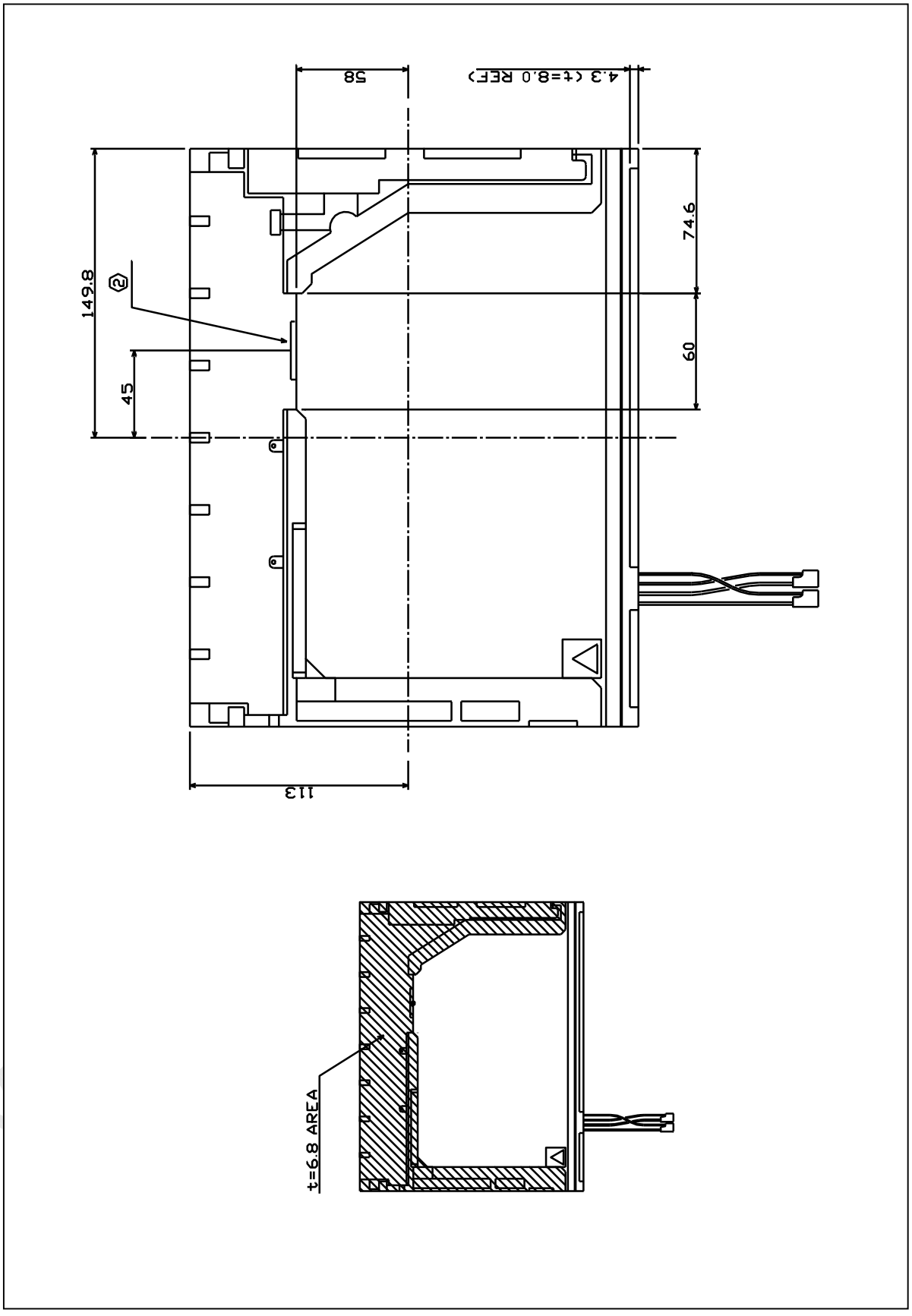

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