AU Optronics Corp.

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AU OPTRONICS CORPORATION

Product Specifications

17.0" SXGA Color TFT-LCD Module

Model Name: M170ES05
V.2

Approved by	Prepared by

DDBU Marketing Division / AU Optronics Croporation

Customer	Checked & Approved by

AU Optronics Corp.

Product Specifications

17.0” SXGA Color TFT-LCD Module
Model Name: M170ES05
V.2

(◆) Preliminary Specifications
( ) Final Specifications

Note: This Specification is subject to change without notice.

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ii Record of Revision

Version and Date	Page	Old description	New Description	Remark
0.1 2003/5/09	All	First Edition for Customer	All	

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1.0 Handling Precautions

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open nor modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT-LCD module.
10) After installation of the TFT-LCD module into an enclosure (LCD monitor housing, for example), do not twist nor bend the TFT -LCD module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT -LCD module from outside. Otherwise the TFT -LCD module may be damaged.

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General Description

This specification applies to the 17.0 inch Color TFT-LCD Module M170ES05.

The display supports the SXGA (1280(H) x 1024(V)) screen format and 262K colors (RGB 6-bits data).

All input signals are 2 Channel RSDS interface compatible.

This module does not contain an inverter card for backlight.

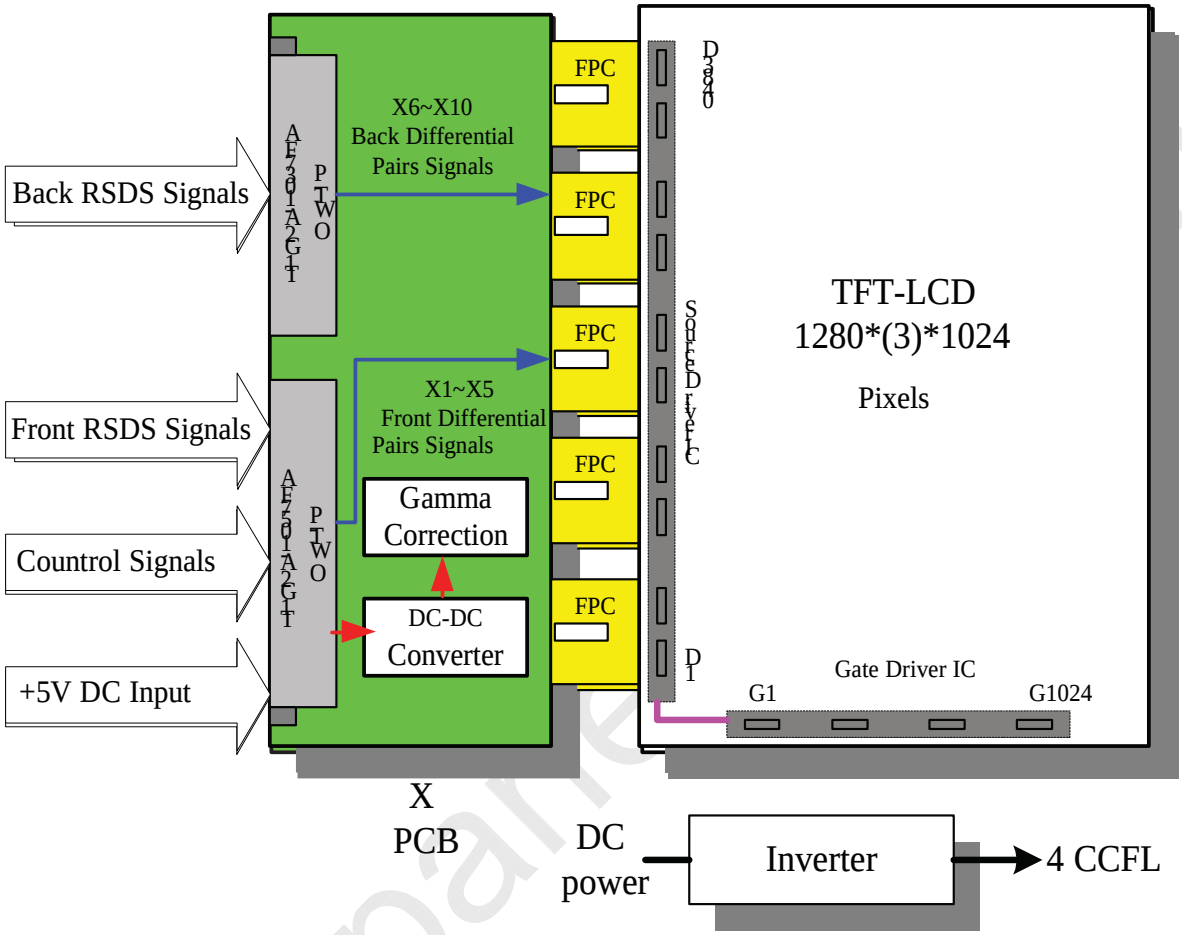
2.1 Display Characteristics

The following items are characteristics summary on the table under 25 ℃ condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	432(17.0")
Active Area	[mm]	337.920 (H) x 270.336(V)
Pixels H x V		1280(x3) x 1024
Pixel Pitch	[mm]	0.264 (per one triad) x 0.264
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
White Luminance	[cd/m^2]	300 (center) @ 7mA
Contrast Ratio		450 : 1 (Typ)
Optical Response Time	[msec]	16 (Typ.)
Color Saturation		72% NTSC
Nominal Input Voltage VDD	[Volt]	+5.0 V
Power Consumption (VDD line + CCFL line)	[Watt]	25W (w/o Inverter, All black pattern) (typ.)
Weight	[Grams]	2000 (Typ)
Physical Size	[mm]	358.5(W) x 296.5(H) x 19.0(D)
Electrical Interface		Front R/G/B data (6bits) and clock pairs Back R/G/B data (6bits) and clock pairs 7 timing control signal input 4 DC power input
Support Color		262k colors (RGB 6-bit data)
Temperature Range Operating Storage (Shipping)	 [°C] [°C]	 0 to +50 -20 to +60

2.2 Functional Block Diagram

The following diagram shows the functional block of the 17.0 inches Color TFT-LCD Module:



P-TWO AF7301-A2G1T
&
P-TWO AF7501-A2G1T

JST BHR-04VS-1

Mating Type: SM04(4.0)B-BHS-1-TB

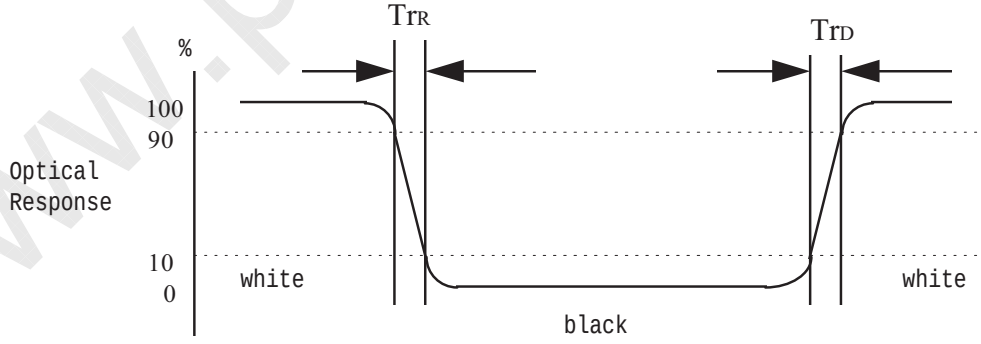
2.3 Optical Characteristics

The optical characteristics are measured under stable conditions at 25℃ (Room Temperature):

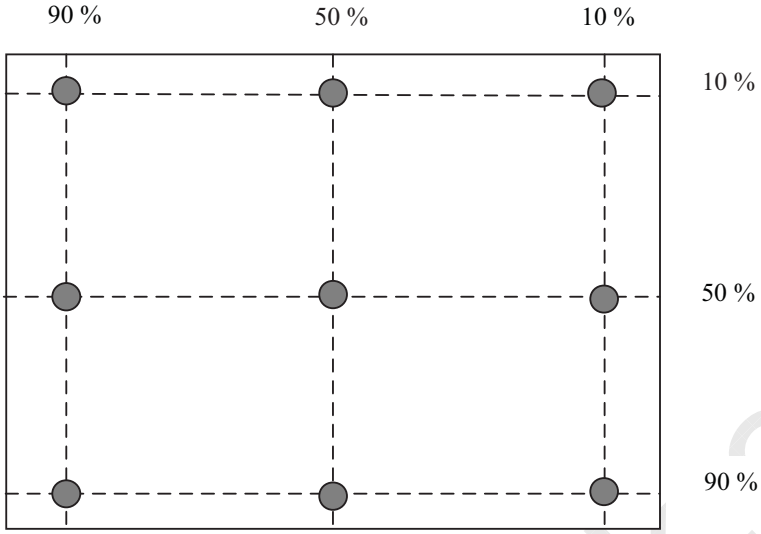
Item	Unit	Conditions	Min.	Typ.	Max.
Viewing Angle (Note 4)	[degree]	Horizontal (Right) CR = 10 (Left)	60 60	70 70	-
		Vertical (Up) CR = 10 (Down)	60 60	70 70	-
		Horizontal (Right) CR = 5 (Left)	70 70	80 80	- -
		Vertical (Up) CR = 5 (Down)	70 70	80 80	- -
Contrast ratio		Normal Direction	250	450	-
Response Time (Note 1)	[m sec]	Raising Time	-	4	5
		Falling Time	-	12	20
		Raising + Falling	-	16	25
Color / Chromaticity Coordinates (CIE)		Red x	0.61	0.64	0.67
		Red y	0.31	0.34	0.37
		Green x	0.26	0.29	0.32
		Green y	0.58	0.61	0.64
		Blue x	0.11	0.14	0.17
		Blue y	0.04	0.07	0.10
Color Coordinates (CIE) White		White x	0.28	0.31	0.34
		White y	0.30	0.33	0.36
White Luminance @ CCFL 7.0mA (center)	[cd/m^2]		230	300	-
Luminance Uniformity (Note 2)	[%]		75	80	-
Cross-talk (in 75Hz) (Note 5)	[%]				1.5

Note 1: Definition of Response time:

The output signals of photo detector are measured when the input signals are changed from " Black" to " White" (falling time), and from "White" to " Black" (rising time), respectively. The response time is interval between the 10% and 90% of amplitudes.



Note 2: Brightness uniformity of these 9 points is defined as below:



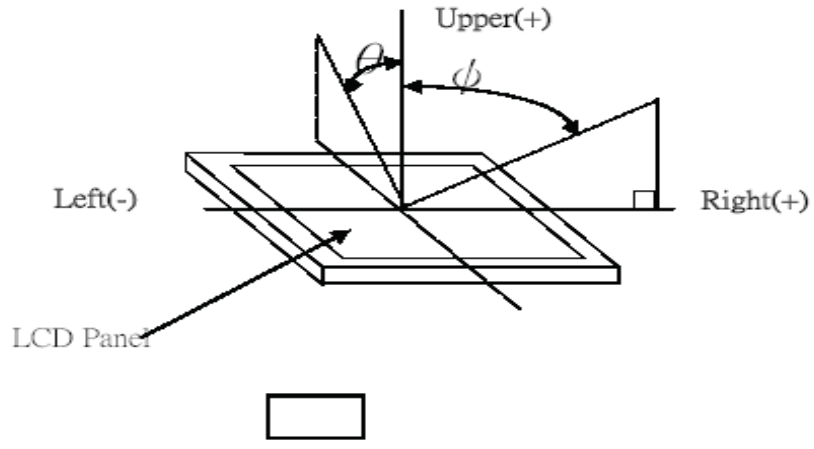
$$\text{Uniformity} = \frac{\text{Minimum Luminance in 9 Points (1-9)}}{\text{Maximum Luminance in 9 Points (1-9)}}$$

Note 3: TCO '99 Certification Requirements and test methods for environmental labeling of Display Report No. 2 defines Luminance uniformity as below:

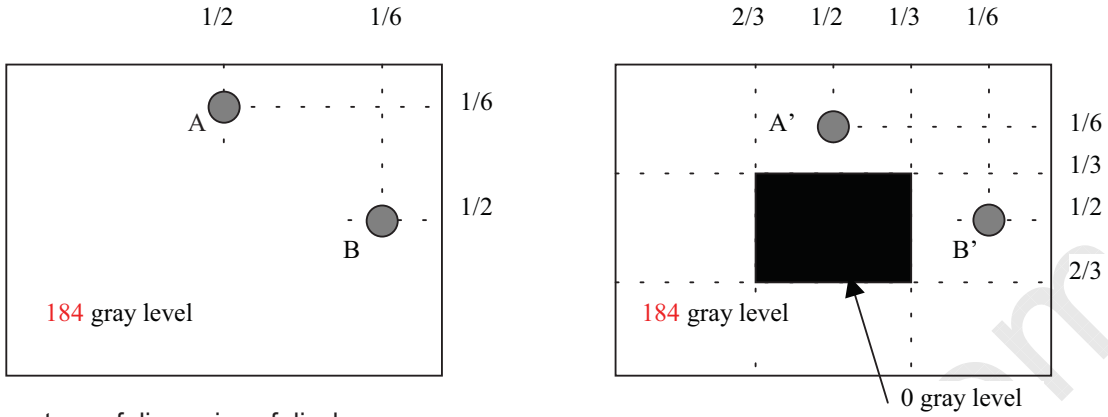
((Lmax,+30deg. / Lmin,+30deg.) + (Lmax,-30deg. / Lmin,-30deg.)) / 2

This panel is compatible with TCO99 approbation in luminance uniformity ≤1.7, luminance contrast >0.5

Note 4: Viewing angle definition



Note 5:



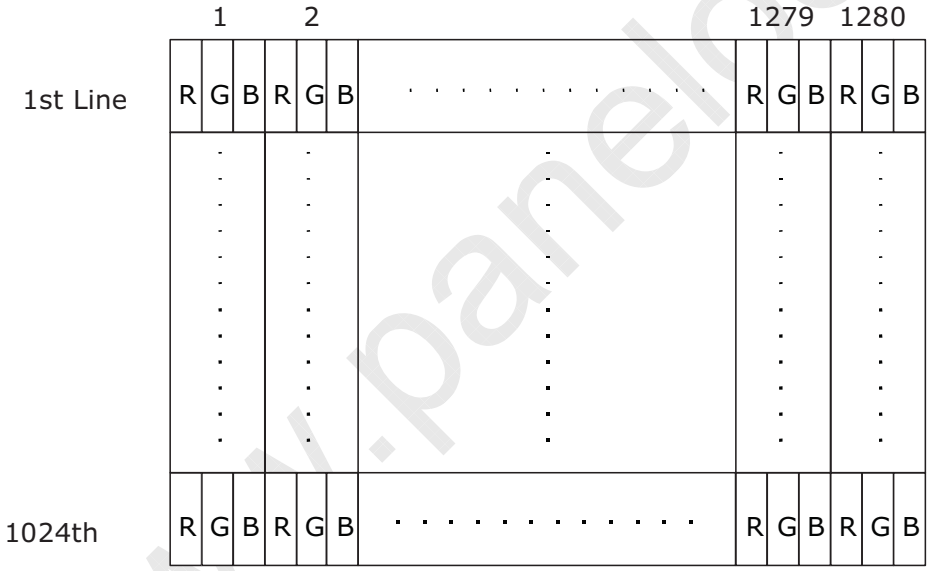
Unit: percentage of dimension of display area

I L_A-$L_{A'}$ I / L_A x 100%= 1.5% max., L_A and L_B are brightness at location A and B

I L_B-$L_{B'}$ I / L_B x 100%= 1.5% max., $L_{A'}$ and $L_{B'}$ are brightness at location A' and B'

2.4: Pixel format image

Following figure shows the relationship of the input signals and LCD pixel format.



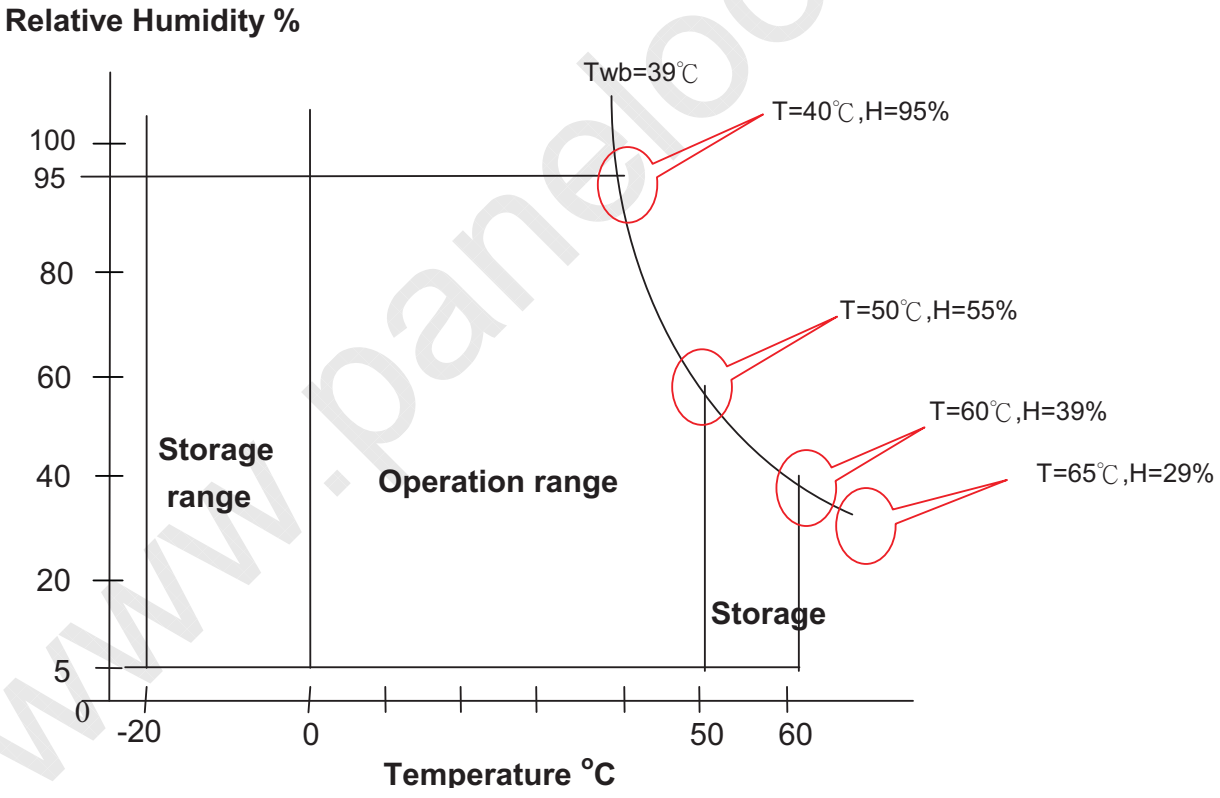
3.0 Electrical characteristics

3.1 Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	VIN	-0.3	+5.5	[Volt]	
CCFL Inrush current	ICFLL	-	38	[mA]	
CCFL Current	ICFL	-	7.6	[mA] rms	
Operating Temperature	TOP	0	+50	[°C]	Note 1
Operating Humidity	HOP	8	95	[%RH]	Note 1
Storage Temperature	TST	-20	+60	[°C]	Note 1
Storage Humidity	HST	8	95	[%RH]	Note 1

Note 1 : Maximum Wet-Bulb should be 39℃ and No condensation.



3.2 Connectors

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

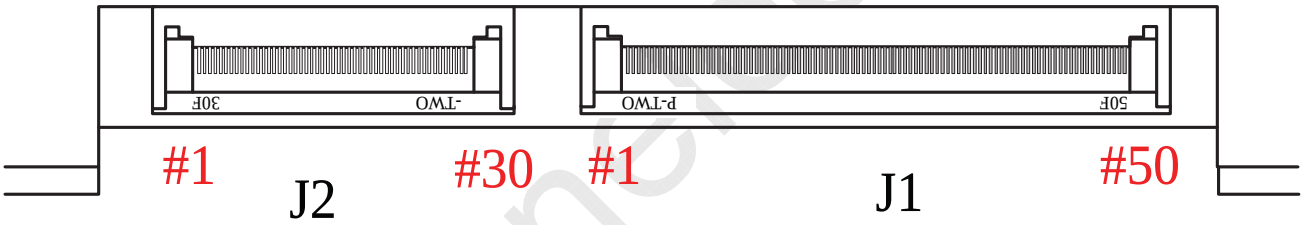
X-PCBA

Connector Name	J1	J2
Manufacture	P-TWO (禾昌) or compatible	P-TWO (禾昌) or compatible
Type Part Number	AF7501-A2G1T (FH12-50S-0.5H)	AF7301-A2G1T (FH12-30S-0.5H)

CCFL

Connector Name	Lamp Connector / Backlight lamp
Manufacturer	JST
Type Part Number	BHR-04VS-1
Mating Type Part Number	SM04(4.0)B-BHS-1-TB

Connector Diagram: Rear view of LCM



3.3 Signal Pin & Description

Connector J1

Pin NO.	Symbol	Description
1	GND	Ground
2	FB[0]N	Front side blue RSDS signal pair 0 negative data
3	FB[0]P	Front side blue RSDS signal pair 0 positive data
4	GND	Ground
5	FB[1]N	Front side blue RSDS signal pair 1 negative data
6	FB[1]P	Front side blue RSDS signal pair 1 positive data
7	GND	Ground
8	FB[2]N	Front side blue RSDS signal pair 2 negative data
9	FB[2]P	Front side blue RSDS signal pair 2 positive data
10	GND	Ground
11	FG[0]N	Front side green RSDS signal pair 0 negative data

12	FG[0]P	Front side green RSDS signal pair 0 positive data
13	GND	Ground
14	FG[1]N	Front side green RSDS signal pair 1 negative data
15	FG[1]P	Front side green RSDS signal pair 1 positive data
16	GND	Ground
17	FG[2]N	Front side green RSDS signal pair 2 negative data
18	FG[2]P	Front side green RSDS signal pair 2 positive data
19	GND	Ground
20	FCLKN	Front side RSDS clock negative
21	FCLKP	Front side RSDS clock positive
22	GND	Ground
23	FR[0]N	Front side red RSDS signal pair 0 negative data
24	FR[0]P	Front side red RSDS signal pair 0 positive data
25	GND	Ground
26	FR[1]N	Front side red RSDS signal pair 1 negative data
27	FR[1]P	Front side red RSDS signal pair 1 positive data
28	GND	Ground
29	FR[2]N	Front side red RSDS signal pair 2 negative data
30	FR[2]P	Front side red RSDS signal pair 2 positive data
31	GND	Ground
32	FXDIO	Front side source driver IC start pulse signal
33	XSTB	Latch the polarity of source outputs and switch the new data to source outputs
34	POL	Source driver IC output polarity control
35	BXDIO	Back side Source driver IC start pulse signal
36	GND	Ground
37	YCLK	Gate driver IC clock in
38	YDIO	Gate driver IC start pulse
39	YOE	Gate driver IC output enable signal
40	NC	-
41	GND	Ground
42	NC	-
43	NC	-
44	VDD	5V input Voltage
45	GND	Ground
46	VDD	5V input Voltage
47	VDD	5V input Voltage

48	VDD	5V input Voltage
49	ID1	Maker ID bit1 (Ground)
50	ID0	Maker ID bit0 (Ground)

Connector J2

Pin NO.	Symbol	Description
1	GND	Ground
2	BB[0]N	Back side blue RSDS signal pair 0 negative data
3	BB[0]P	Back side blue RSDS signal pair 0 positive data
4	GND	Ground
5	BB[1]N	Back side blue RSDS signal pair 1 negative data
6	BB[1]P	Back side blue RSDS signal pair 1 positive data
7	GND	Ground
8	BB[2]N	Back side blue RSDS signal pair 2 negative data
9	BB[2]P	Back side blue RSDS signal pair 2 positive data
10	GND	Ground
11	BG[0]N	Back side green RSDS signal pair 0 negative data
12	BG[0]P	Back side green RSDS signal pair 0 positive data
13	GND	Ground
14	BG[1]N	Back side green RSDS signal pair 1 negative data
15	BG[1]P	Back side green RSDS signal pair 1 positive data
16	GND	Ground
17	BG[2]N	Back side green RSDS signal pair 2 negative data
18	BG[2]P	Back side green RSDS signal pair 2 positive data
19	GND	Ground
20	BCLKN	Back side RSDS clock negative
21	BCLKP	Back side RSDS clock positive
22	GND	Ground
23	BR[0]N	Back side red RSDS signal pair 0 negative data
24	BR[0]P	Back side red RSDS signal pair 0 positive data
25	GND	Ground
26	BR[1]N	Back side red RSDS signal pair 1 negative data
27	BR[1]P	Back side red RSDS signal pair 1 positive data
28	GND	Ground
29	BR[2]N	Back side red RSDS signal pair 2 negative data
30	BR[2]P	Back side red RSDS signal pair 2 positive data

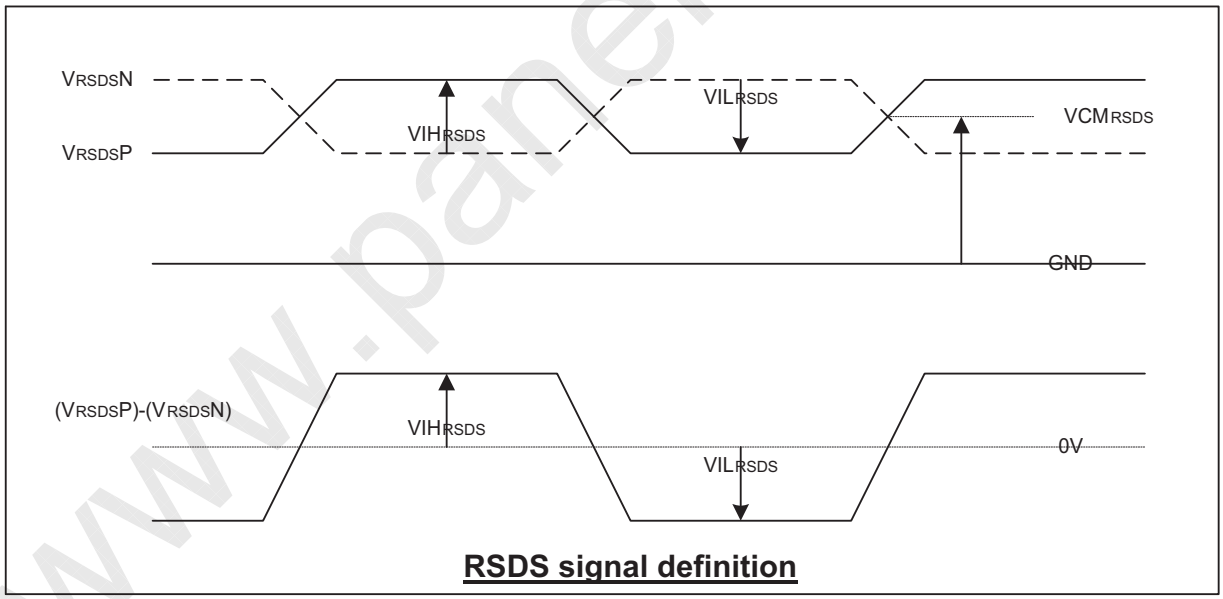
3.4 RSDS signal electrical characteristic

RSDS Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
RSDS high input voltage	VIHRSDS	100	200	-	mV	VCMRSDS = + 1.2 V
RSDS low input voltage	VILRSDS	-	- 200	- 100	mV	VCMRSDS = + 1.2 V
RSDS common mode input voltage range	VCMRSDS(1)	0.5	-	1.4	V	VDIFFRSDS (2) = 200 mV (minimum value)
RSDS input leakage current	IDL	-10	-	10	uA	DxxP,DxxN,CLKP,CLKN(3)

Notes:

1. VCMRSDS = (VCLKP + VCLKN) / 2 or VCMRSDS = (VDxxP + VDxxN) / 2
2. VDIFFRSDS = VCLKP - VCLKN or VDIFFRSDS = VDxxP - VDxxN
   The typical RSDS swing level of peak to peak is 400mV.
3. DxxP/N=Differential inputs for 6-bit RGB data
   CLKP/N= Differential inputs for clock data



RSDS signal definition

3.5 Timing Requirement

This following data describes the source and gate drivers timing requirement for 17" SXGA (1280x1024) Panel. The control timing is defined based on VESA SXGA standard(non-interlaced). The symbols and timing requirement are defined in Table 1 and Table 2. And, the timing diagrams for the source and gate drivers are shown in Figure 1 、Figure 2 and Figure 3 respectively.

Source Driver IC (Horizontal Timing)

Table 1.

Item		Symbol	-			Unit
			Min.	Typ.	Max.	
Last Data Timing		T_{LDT}	1	14	-	$CLKP_{period}$
XDIO Pulse Width		PW_{XDIO}	1	1.6	2	$CLKP_{period}$
XSTB-XDIO Time		$T_{STB-XDIO}$	5	92	-	$CLKP_{period}$
XSTB Pulse Width		PW_{STB}	5(?)	80	-	$CLKP_{period}$
POL-XSTB Time		$T_{POL-STB}$	14	(15 $CLKP_{period}$)	-	ns($CLKP_{period}$)
XSTB-XPOL Time		$T_{STB-POL}$	10	(11 $CLKP_{period}$)	-	ns($CLKP_{period}$)
XSTB-CLK Time		$T_{STB\uparrow(90\%)}$-$CLK_{P-N\downarrow(50\%)}$	4		-	ns
XDIO setup time		T_{SETUP2}	2	-	-	ns
XDIO hold time		T_{HOLD2}	4	-	-	ns
Data setup time		T_{SETUP1}	3	-	-	ns
Data hold time		T_{HOLD1}	1	-	-	ns
Clock pulse low period		PWCLK(L)	6	-	-	ns
Clock pulse high period		PWCLK(H)	6	-	-	ns
Clock Pulse width	Frequency	FCLK	40	54	67.5	MHz
	Period	PWCLK	14.81	18.52	20	ns

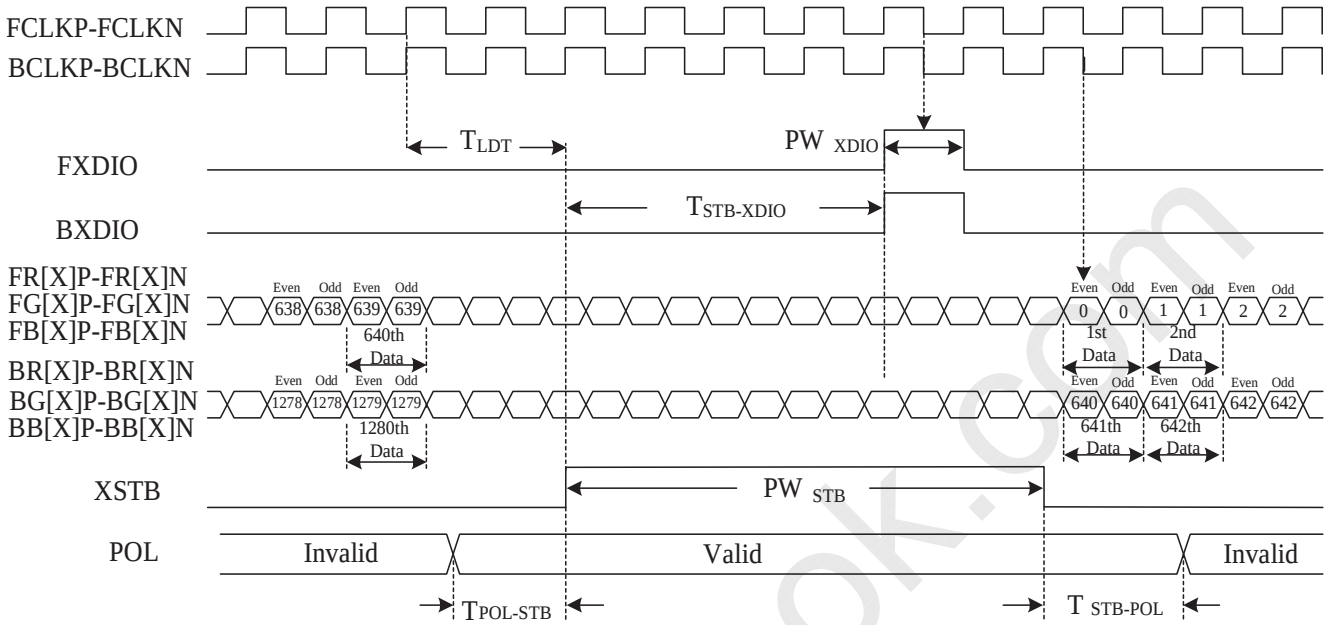


Figure 1

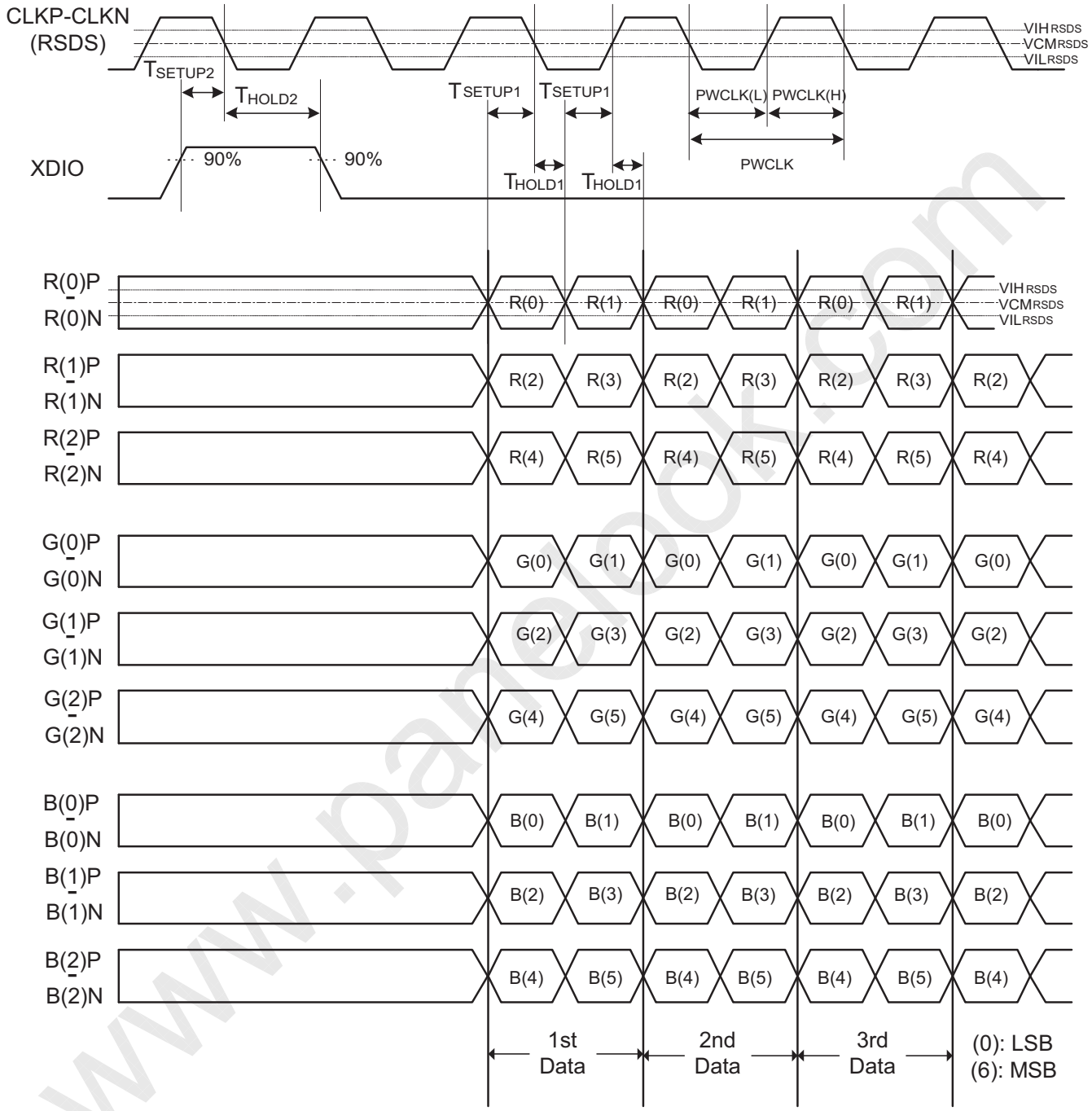


Figure 2

Gate Driver IC (Vertical Timing)

Table 2.

Item	Symbol	-						Unit
		Frame rate@60Hz			Frame rate@75Hz			
		Min.	Typ.	Max.	Min.	Typ.	Max.	
YDIO setup time	T_{SDI}	200	6640	-	200	5280	-	ns
YDIO hold time	T_{HDI}	350	9040	-	350	7200	-	ns
Gate off time	T_{GOFF}	-	1846	-	-	1470	-	ns
Gate delay time	T_{GDLY}	-	282	-	-	242	-	ns
YOE low period	$T_{GOFF}+T_{GDLY}$	1000	2128	-	1000	1712	-	ns

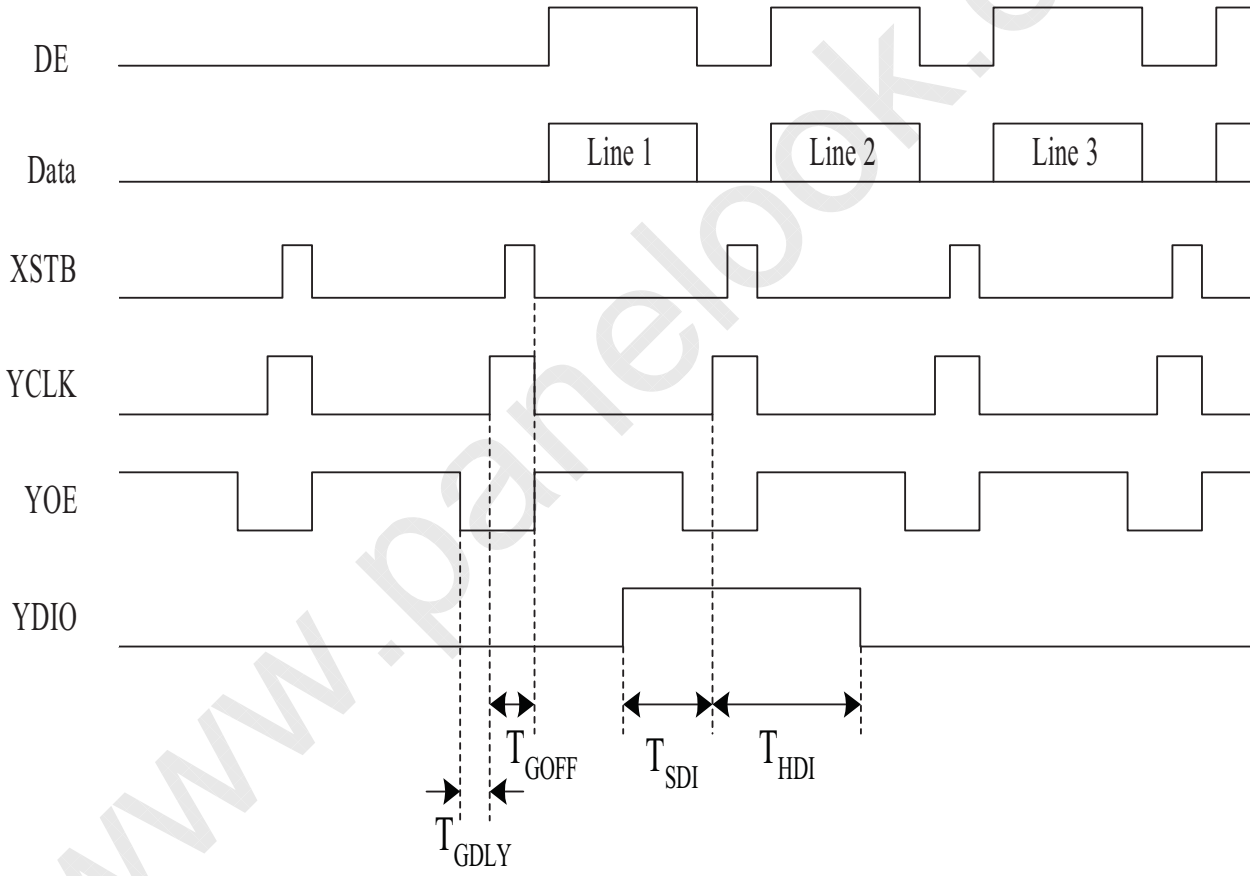


Table 3

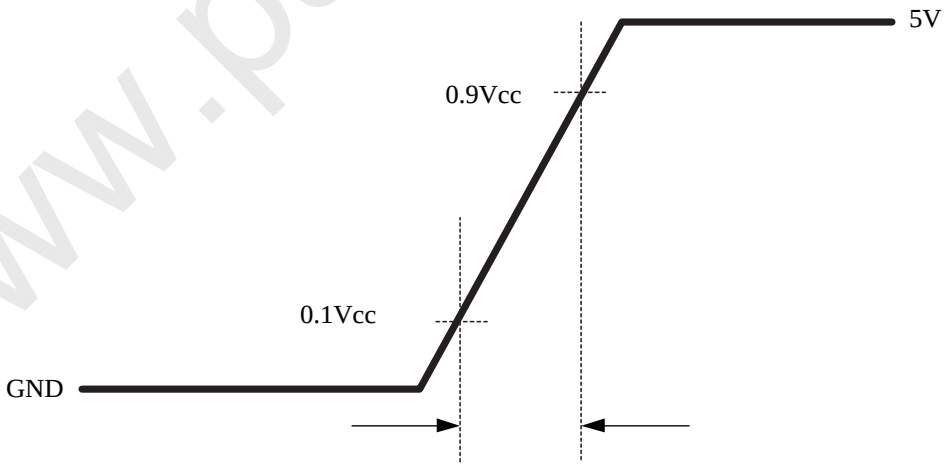
Note1 : DE is reference signal, DE means the display data valid.

3.6 Electrical Ratings

Item	Symbol	Values			Unit	Notes
		Min	Typ	Max		
Power Supply Input Voltage Voltage (1)	VDD	4.5	5	5.5	V(DC)	
Power Supply Ripple		-	-	250	mV_{p-p}	
Power Supply Input Current	Icc	-	800	1000	mA	1
Differential pair Impedance Current	Zm	90	100	110	Ohm	2
Power Consumption	Pc		4	5	W	1
Inrush current	Irush	-	-	5	A	3

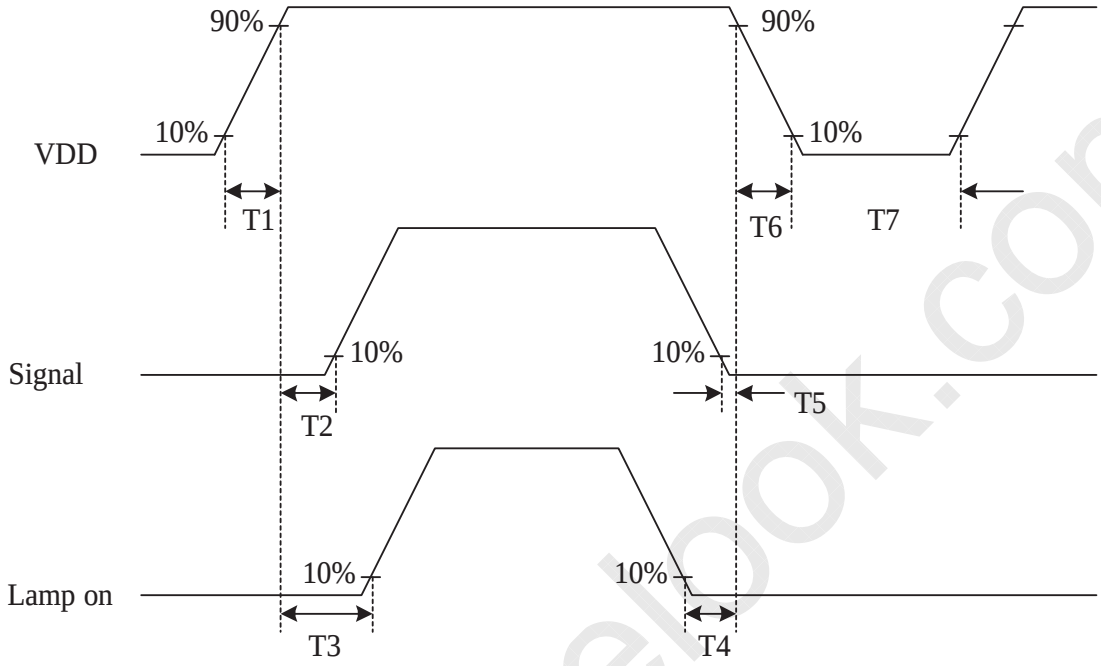
Notes:

1. **The specified current and power consumption are under the conditions (VDD=5V,T=25℃,Frame rate=75Hz,black pattern).**
2. **This value is needed to a proper signal quality and is measured from Scalar Chip output pins to its mating connector. Besides, the impedance of FPC between scalar board and LCD panel is also needed to keep.**
3. **Based on AU circuit design ,the duration of the rush current is about 1 ms, which should have the following typical condition.**



3.7 Power ON/OFF Sequence

The LCD module must be powered up and down as indicated or the device may be damaged permanently. The power-on includes both system starting and from the sleep to wake-up mode ; the power-off includes both system shunt down and the one from on to sleep. There should be no power sequence changing in the sleep to wake-up mode.



Parameter	Values		Unit
	Min	Max	
T1	0.5	10	ms
T2	0.01	30	ms
T3	170	-	ms
T4	100	-	ms
T5	0	-	ms
T6	-	-	ms
T7	1000	-	ms

4.0 Backlight Characteristics

4.1 Signal for Lamp connector

Pin #	Signal Name
1	Lamp High Voltage
2	Lamp High Voltage
3	No Connection
4	Ground

4.2 Parameter guide line for CFL Inverter

Symbol	Parameter	Min	Typ	Max	Units	Condition
(L63)	White Luminance	230	300	-	[cd/m^2]	(Ta=25°C)
ISCFL	CCFL standard current	6.5	7.0	7.5	[mA] rms	(Ta=25°C)
IRCFL	CCFL operation range	3.0	7.0	7.5	[mA] rms	(Ta=25°C)
fCFL	CCFL Frequency	40	50	80	[KHz]	(Ta=25°C) Note 1
ViCFL (0°C)	CCFL Ignition Voltage	1700			[Volt] rms	(Ta=0°C) Note 2
ViCFL (25°C)	CCFL Ignition Voltage	1200			[Volt] rms	(Ta=25°C) Note 2
VCFL	CCFL Discharge Voltage (Reference)		700	860	[Volt] rms	(Ta=25°C) Note 3
PCFL	CCFL Power consumption		19.6	25.8	[Watt]	(Ta=25°C) Note 3

Note 1: CCFL Frequency should be carefully determined to avoid interference between inverter and TFT LCD
Note 2: CCFL inverter should be able to give out a power that has a generating capacity of over 1700 voltage. Lamp units need 1700 voltage minimum for ignition
Note 3: Calculator value for reference (ICFL×VCFL=PCFL)

5.0 Vibration, Shock, and Drop

5.1 Vibration & Shock

Frequency: 10 - 200Hz
Sweep: 30 Minutes each Axis (X, Y, Z)
Acceleration: 1.5G(10~200Hz P- P)
Test method:

Acceleration (G)	1.5
Frequency (Hz)	10~200~10
Active time(min)	30

5.2 Shock Test Spec:

Acceleration (G)	50
Active time	20
Wave form	half-sin
Times	1

Direction: ±X , ±Y, ±Z

5.3 Drop test

Package test: The drop height is 60 cm.

6.0 Environment

The display module will meet the provision of this specification during operating condition or after storage or shipment condition specified below. Operation at 10% beyond the specified range will not cause physical damage to the unit.

6.1 Temperature and Humidity

6.1.1 Operating Conditions

The display module operates error free, when operated under the following conditions;

Temperature	0 ^{0}C to 50 ^{0}C
Relative Humidity	8% to 95%
Wet Bulb Temperature	39.0 ^{0}C

6.1.2 Shipping Conditions

The display module operates error free, after the following conditions;

Temperature	-20 ^{0}C to 60 ^{0}C
Relative Humidity	8% to 95%
Wet Bulb Temperature	39.0 ^{0}C

6.2 Atmospheric Pressure

The display assembly is capable of being operated without affecting its operations over the pressure range as following specified;

	Pressure	Note
Maximum Pressure	1040hPa	0m = sea level
Minimum Pressure	674hPa	3048m = 10.000 feet

Note : Non-operation attitude limit of this display module = 30,000 feet. = 9145 m.

6.3 Thermal Shock

The display module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20^{0}C to 60^{0}C, and back again.

Thermal shock cycle -20 ^{0}C for 30min
60 ^{0}C for 30min

Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before powering on.

7.0 Reliability

This display module and the packaging of that will comply following standards.

7.1 Failure Criteria

The display assembly will be considered as failing unit when it no longer meets any of the requirements stated in this specification. Only as for maximum white luminance, following criteria is applicable.

Note : Maximum white Luminance shall be 125 cd/m^{2}or more.

7.2 Failure Rate

The average failure rate of the display module (from first power-on cycle till 1,000 hours later) will not exceed 1.0%.
The average failure rate of the display module from 1,000 hours until 16,000 hours will not exceed 0.7% per 1000 hours.

7.2.1 Usage

The assumed usage for the above criteria is:

220 power-on hours per month
500 power on/off cycles per month
Maximum brightness setting
Operation to be within office environment (25^0C typical)

7.2.2 Component De-rating

All the components used in this device will be checked the load condition to meet the failure rate criteria.

7.3 CCFL Life

The assumed CCFL Life will be longer than 30,000 hours, typical value is 40,000 hours under stable condition at 25 ± 5^oC;
Standard current at 7.0 ± 0.5mA.
Definition of life: brightness becomes 50% or less than the minimum luminance value of CCFL.

7.4 ON/OFF Cycle

The display module will be capable of being operated over the following ON/OFF Cycles.

ON/OFF	Value	Cycles
+Vin and CCFL power	30,000	10 seconds on / 10 seconds off

8.0 Safety

8.1 Sharp Edge Requirements

There will be no sharp edges or comers on the display assembly that could cause injury.

8.2 Materials

8.2.1 Toxicity

There will be no carcinogenic materials used anywhere in the display module. If toxic materials are used, they will be reviewed and approved by the responsible AU Toxicologist.

8.2.2 Flammability

All components including electrical components that do not meet the flammability grade UL94-V1 in the module will complete the flammability rating exception approval process. The printed circuit board will be made from material rated 94-V1 or better. The actual UL flammability rating will be printed on the printed circuit board.

8.3 Capacitors

If any polarized capacitors are used in the display assembly, provisions will be made to keep them from being inserted backwards.

8.4 Hazardous Voltages

Any point exceeding 42.4 volts meets the requirement of the limited current circuit. The current through a 2KΩ resistance is less than 0.7 x f (kHz) mA.

9.0 Other requirements

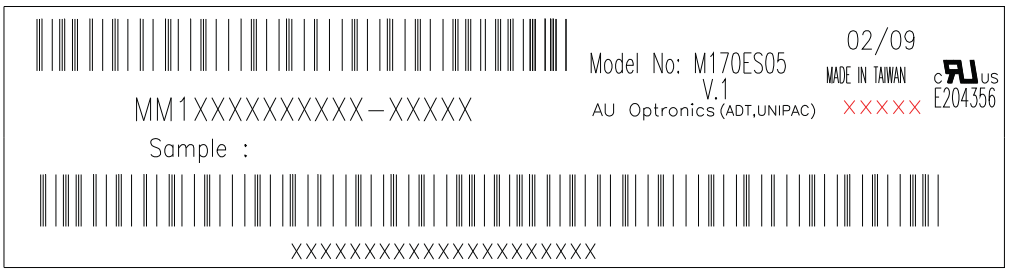
9.1 National Test Lab Requirement

The display module will satisfy all requirements for compliance to

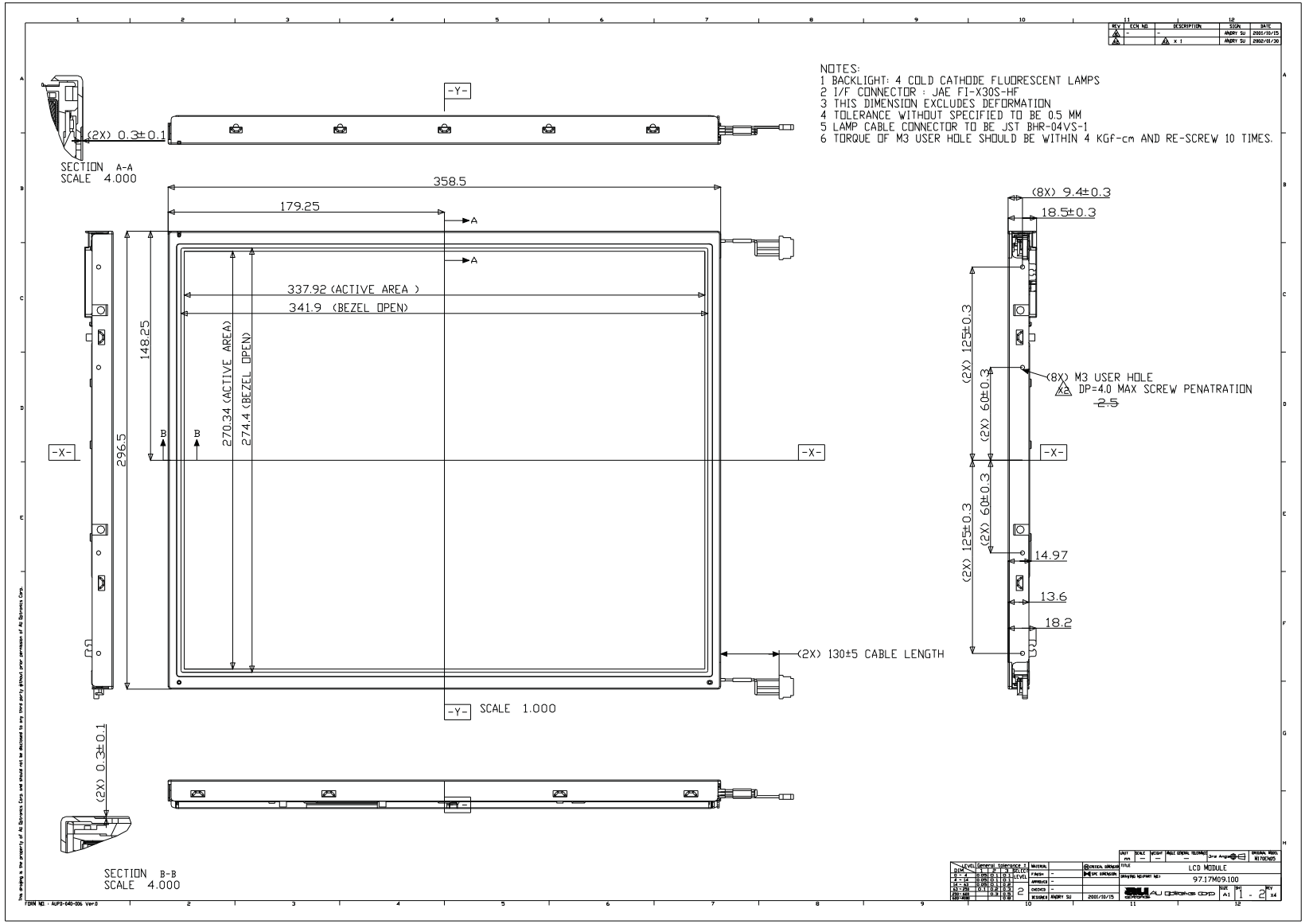
UL 1950, First Edition	U.S.A. Information Technology Equipment
CSA C22.2 No.950-M89	Canada, Information Technology Equipment
EEC 950	International, Information Technology Equipment
EN 60 950	International, Information Processing Equipment (European Norm for IEC950)

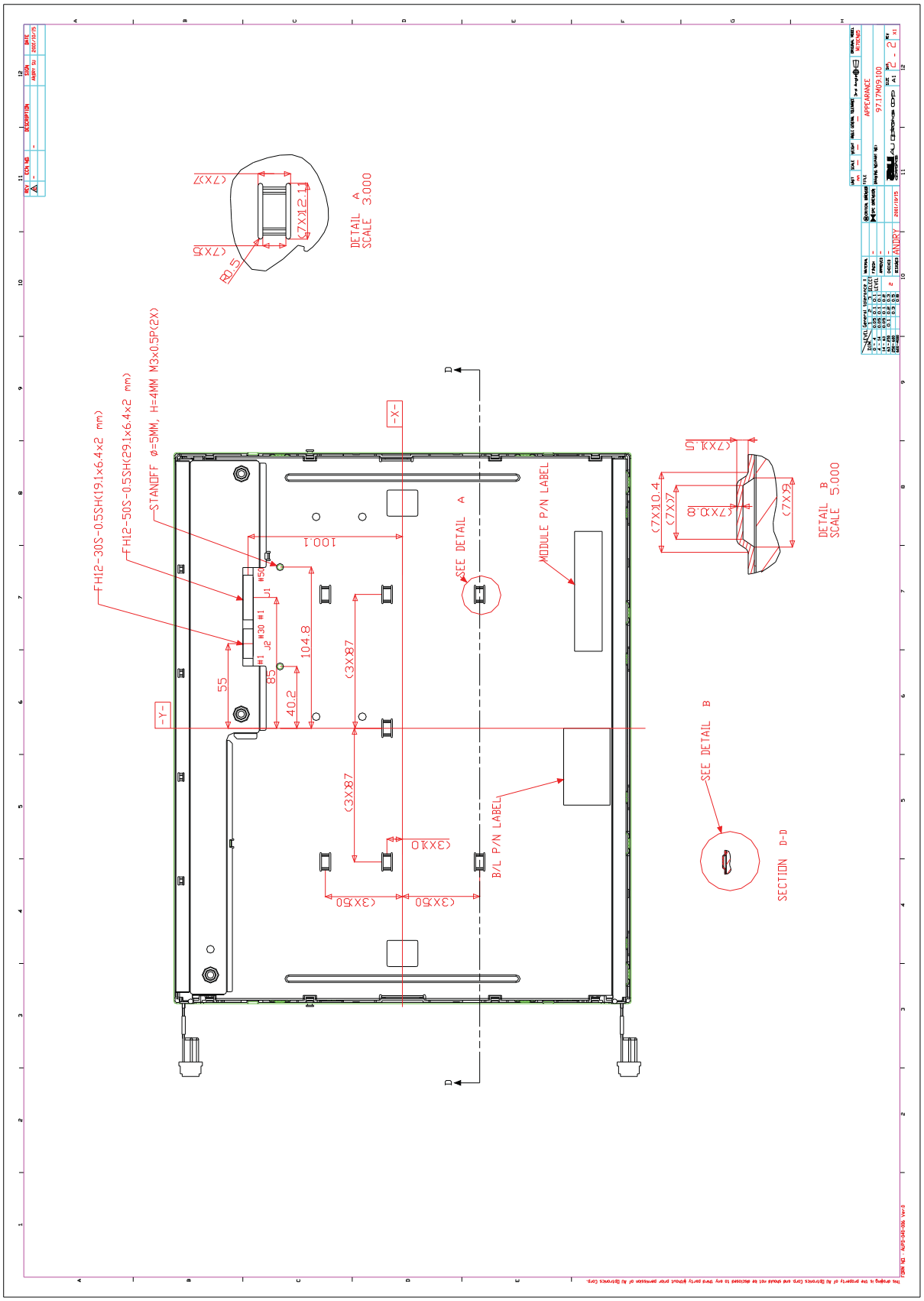
9.2 Label

9.2.1 Product label



10.0 Mechanical Characteristics





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