



WIRELESS DOOR CHIME
遙控門鈴 IC

DOOR CHIME

M1D-BL

GENERAL DESCRIPTION 功能敘述

The M1D-BL is a CMOS ASIC for wireless door bell receiver use. It will receive the RF signal from M1E (ENCODER) and give a DING-DONG output if address are checked the same..

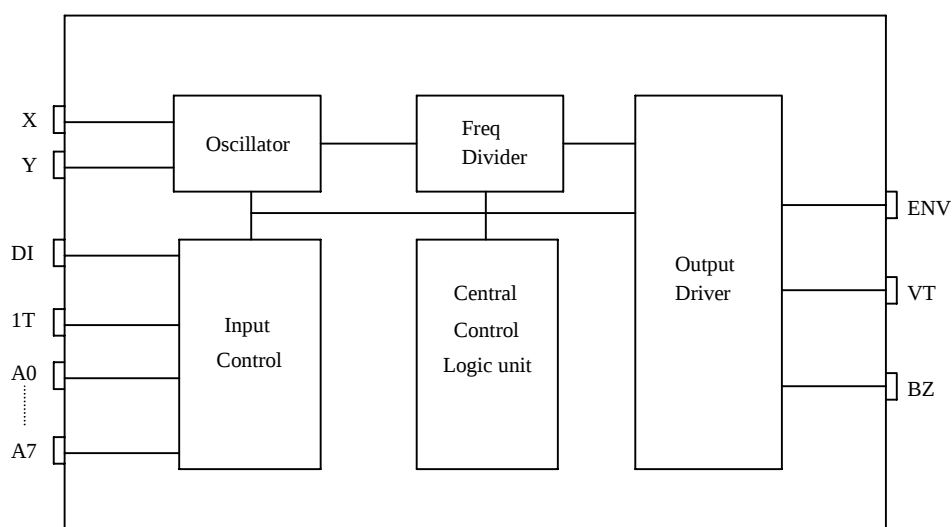
FEATURES 产品特长

- Same Rosc matched to the ENCODER M1E
- $2^8 = 256$ codes, “0”, “1” binary
- 3 cycles checked each time
- BZ : DING-DONG / DING-DING sound
- 1T : 1 time option (default 2 times)
- RC envelop

APPLICATIONS 产品应用

- Wireless door bell, visitor chime etc..

BLOCK DIAGRAM 功能方块图



*All specs and applications shown above subject to change without prior notice.
(以上电路及规格仅供参考,本公司得径行修正)



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ABSOLUTE MAXIMUM RATING

(TA=25℃)

Parameter	Rating	Unit
Supply Voltage	-0.3 to 5.0	V
Input Voltage	-0.2~V _{DD} +0.2	V
Operating Temperature	-20 to 75	℃
Storage Temperature	-50 to 125	℃

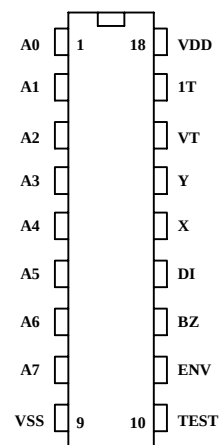
ELECTRICAL CHARACTERISTICS

Characteristics	Sym.	Min.	Typ.	Max.	Unit	Conditions
Operating Voltage	V _{DD}	2.4	3	4.5	V	
Operating Current	I _{OP}	—	0.3	1	μ A	
Quiescent Current	I _{SB}	—	1	10	mA	No load
Output Drive Current	I _O	1	—	—	mA	@V _{DS} =1.2V
Input Voltage	V _{IH}	V _{DD} -0.2	V _{DD}	V _{DD}	V	
	V _{IL}	V _{SS}	V _{SS}	V _{SS} +0.2		
Oscillator Frequency	Fosc	—	80	—	KHz	External ± 30%

PIN DESCRIPTION

No.	Name	Description
1~8	A0~A7	3 states address inputs
9	VSS	Negative power supply
10	TEST	Testing use
11	ENV	RC envelop
12	BZ	Audio output
13	DI	Data input
14	X	Oscillator input
15	Y	Oscillator output
16	VT	Valid transmit
17	1T	OPEN : 2 times VDD : 1 time
18	VDD	Positive power supply

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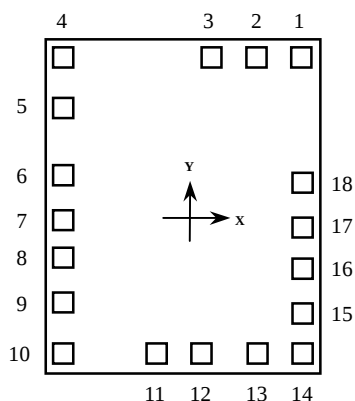


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PAD ASSIGNMENT & POSITION



UNIT : μm

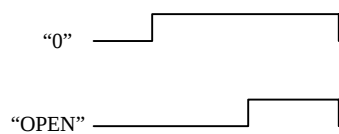
No.	NAME	X	Y
1	BZ	635	812
2	DI	425	812
3	X	192	812
4	Y	-639	812
5	VT	-639	534
6	1T	-639	178
7	VDD	-639	-55
8	A0	-639	-265
9	A1	-639	-505
10	A2	-639	-810
11	A3	-126	-810
12	A4	107	-810
13	A5	402	-810
14	A6	635	-810
15	A7	635	-600
16	VSS	635	-367
17	TEST	635	-157
18	ENV	635	76

* CHIP SIZE $\sim 1.58 \times 2.03 \text{ mm}^2$

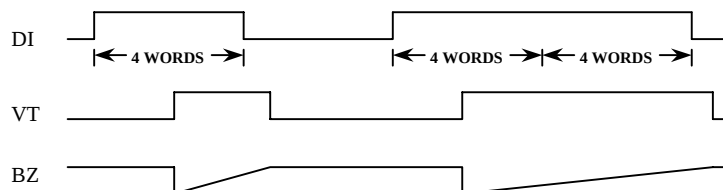
* IC substrate should be connected to VDD in PCB (PCB 上 IC 底座必須接 VDD)

TIMING WAVEFORM

(1) BIT FORMAT



(2) TIMING DIAGRAM



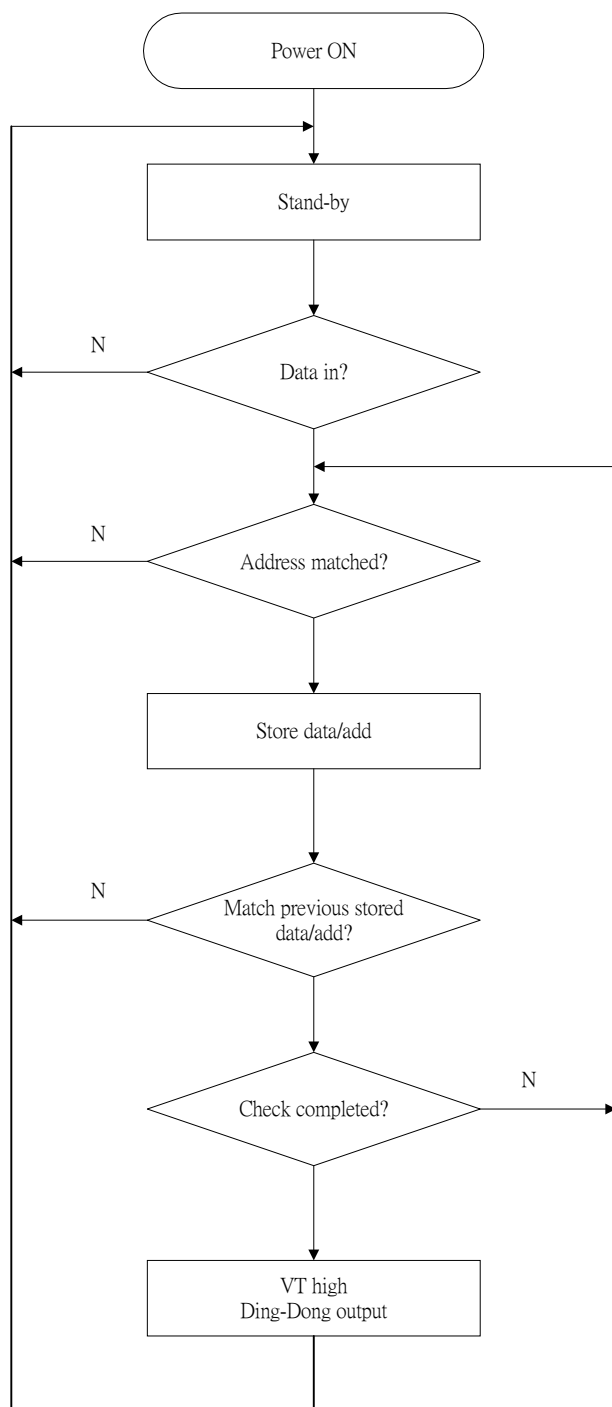


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OPERATION FLOWCHART



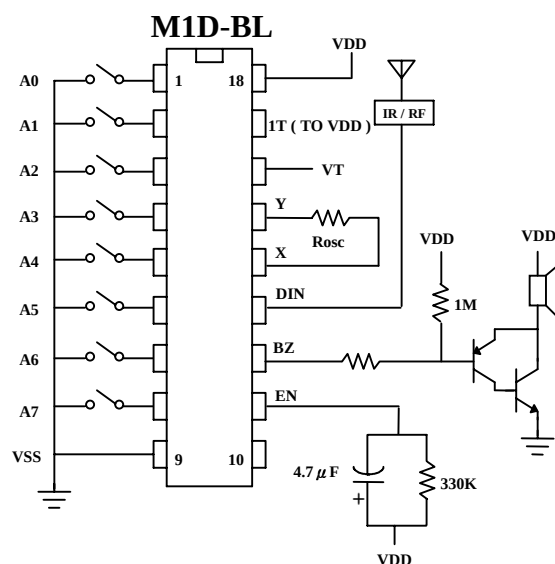
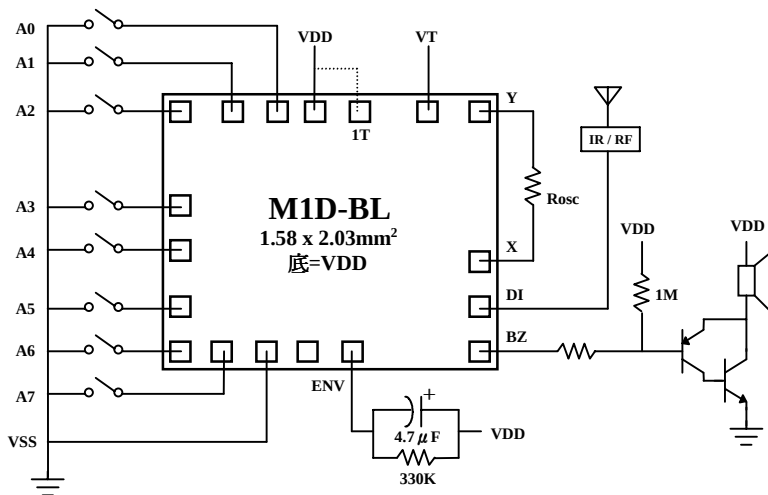
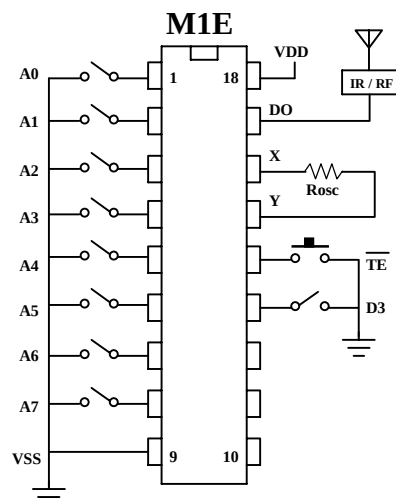
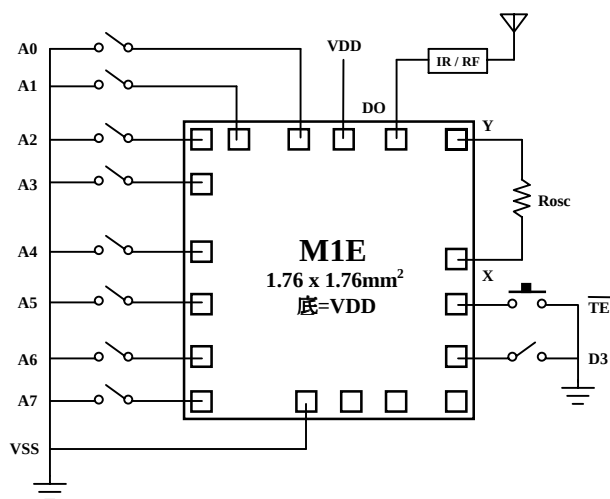


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APPLICATION DIAGRAM 參考電路圖



D3	SOUND
OPEN	DING DONG
VSS	DING DING