M2004-01

Frequency Synthesizer

FEATURES

- Output Clock Frequency up to 700MHz
- Differential LVPECL Outputs
- Internal Low-jitter SAW-based Oscillator
- Intrinsic Jitter <1ps rms (12kHz - 20MHz)
- Jitter Attenuation of Input Reference Clock
- Dual Input MUX
- Parallel Programming
- Tunable Loop Filter Response
- Differential LVPECL Outputs
- 3.3V Operation
- Small 9mm x 9mm SMT Package

APPLICATIONS

- SONET / SDH / 10GbE System Synchronization
- Add / Drop Muxes, Access and Edge Switches
- Line Card System Clock Cleaner / Translator
- Optical Module Clock Cleaner / Translator

DESCRIPTION

The M2004-01 integrates a high performance Phase Locked Loop (PLL) with a Voltage Controlled SAW Oscillator (VCSO) to provide a low jitter Frequency Translator in a 9mm x 9mm surface mount package.

The internal high “Q” SAW filter provides low jitter signal performance and determines the maximum output frequency of the VCSO. A programmable output divider can divide the VCSO frequency to achieve an output as low as 38.88MHz.

The input to the Frequency Translator is provided by selecting between one of two output reference clocks. The output frequency is an integer multiple of the input reference frequency.

Parallel and serial control of the output and feedback dividers is provided via the configuration logic. An external loop filter sets the PLL bandwidth which can be optimized to provide jitter attenuation of the input reference clock.

The M2004-01 is available at SONET/SDH and 10GbE frequencies up to 700MHz.

ABSOLUTE MAX RATINGS

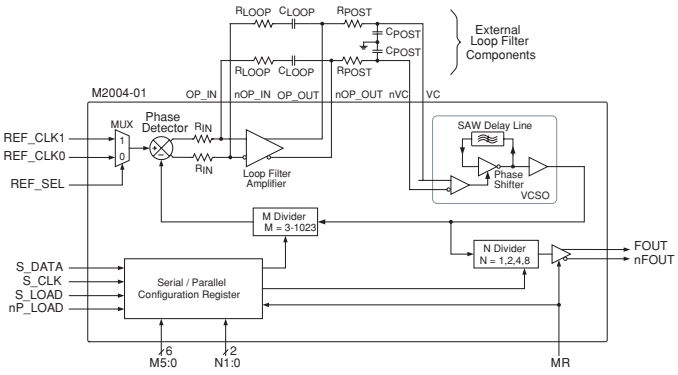
Inputs, V_I: ..... -0.5 to V_{CC}+0.5V
Output, V_O: ..... -0.5 to V_{CC}+0.5V
Supply Voltage, V_{DD}: ..... 4.6 V
Storage Temperature, T_{STO}: ..... -45°C to +100°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the DC Characteristics *or* AC Characteristics *is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.*

ISO 9001 Registered

FUNCTIONAL BLOCK DIAGRAM

The internal PLL will adjust the VCSO output frequency to be M times the selected input reference clock frequency. Note that the product of M x input frequency must be such that it falls within the “lock” range of the VCSO. The N output divider can be programmed to divide the VCSO output frequency by 1, 2, 4, or 8 and provide a 50% output duty cycle.



The M2004-01 supports both parallel and serial operating modes for programming the M divider and N output divider. Figure 1 shows the timing diagram for each mode. In the parallel mode the nP_LOAD input is initially LOW. The data on inputs M0 through M5 and N0 and N1 is passed directly to the M divider. On the LOW-to-HIGH transition of the nP_LOAD input, the data is latched and the M divider remains loaded until the next LOW transition on nP_LOAD or until a serial event occurs. As a result, the M and N bits can be hardwired to set the M divider and N output divider to a specific default state that will automatically occur during power-up.

The relationship between the VCSO frequency, the input REF_CLK , and the M divider is defined as follows:

$$F\ VCSO = F\ REF\_CLK \times M$$

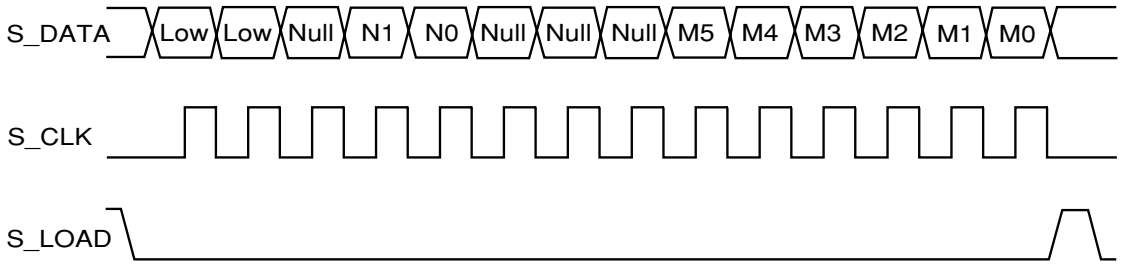
When the N output divider is included, the complete relationship for the output frequency is defined as:

$$FOUT = \frac{F\ VCSO}{N} = F\ REF\_CLK \times \frac{M}{N}$$

The M value and the required logic states of M0 through M5 are shown in Table 5B, Programmable VCSO Frequency Function Table. (i.e. For an output frequency of 622.0800MHz and an input frequency of 19.44MHz the M value would be 32 and the N value would be 1.

Similarly, for an output frequency of 311.04MHz and an input frequency of 19.44 MHz the M value would be 32 and the N value would be 2.) Serial operation occurs when nP_LOAD is HIGH and S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the M divider and N output divider when S_LOAD transitions from LOW-to-HIGH. The M divider and N output divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH, data at the S_DATA input is passed directly to the M divider and N output divider on each rising edge of S_CLOCK.

FIGURE 1



FUNCTIONAL DESCRIPTION

LOOP FILTER

The M2004-01 requires the use of an external loop filter via the provided filter pins. Due to the differential design, the implementation requires two identical RC filters as shown in Figure 2.

FIGURE 2

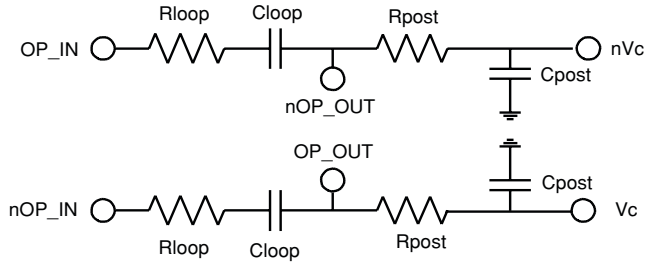


TABLE 1. RECOMMENDED LOOP FILTER VALUES

REF_CLK Frequency	VCSO Frequency	M	N	FOUT	Rloop	Cloop	Rpost	Cpost
19.44MHz	622.0800MHz	32	1	622.0800MHz	5kΩ	1MF	50kΩ	100pf

PIN DESCRIPTIONS

TABLE 2

Pin Number	Name	I/O	Configuration	Description
1, 2, 3	GND	GND		Power Supply Ground
4, 9	OP_IN, nOP_IN	Analog I/O		Used for external loop filter. See Figure 2.
5, 8	nOP_OUT, OP_OUT	Analog I/O		Used for external loop filter. See Figure 2
6, 7	nVC, VC	Input	VCSO	Differential Control Voltage Input Pair
10, 14, 26	GND	GND		Power Supply Ground
11, 19, 33	VDD	Power		Positive Supply Pins
12, 13	N0, N1	Input	Pull - down	Determines the output divider value as defined in table 3C. LVCMOS / LVTTL interface levels.
15, 16	FOUT, nFOUT	Output	Unterminated	Differential output, 3.3V LVPECL levels.
17	MR	Input	Pull - down	Logic HIGH resets the reference frequency and N output dividers. Logic LOW enables the outputs. LVCMOS / LVTTL interface levels.
18	S_CLOCK	Input	Pull - down	Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK.
20	S_DATA	Input	Pull - down	Shift register serial input. Data is sampled on the rising edge of S_CLOCK.
21	S_LOAD	Input	Pull - down	Controls transition of data from shift register into the dividers. LVCMOS / LVTTL interface levels
22	nP_LOAD	Input	Pull - down	Parallel load input. Determines when data present at M5:M0 is loaded into Mdivider, and when data present at N1:N0 sets the N output divider value. LVCMOS / LVTTL interface levels.
23	REF_ CLK 1	Input	Pull - down	Input reference clock. LVCMOS / LVTTL interface levels.
24	REF_ CLK 0	Input	Pull - down	Input reference clock. LVCMOS / LVTTL interface levels.
25	REF_SEL	Input	Pull - down	Selects between the different reference clock inputs as the PLL reference source. See table 3D. LVCMOS / LVTTL interface levels.
27, 28, 29, 30, 31	M0, M1, M2, M3, M4	Input	Pull - down	M divider inputs. Data is latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS/ LVTTL interface levels.
32	M5	Input	Pull - down	
34, 35, 36	DNC			Do not connect. Internal test pins must be left floating.

PIN CHARACTERISTICS

TABLE 4

Symbol	Parameter	Test Conditions	Min	Typical	Max	Units
C_{IN}	Input Capacitance				4	pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

PARALLEL & SERIAL MODES FUNCTION

TABLE 5A

Inputs							
MR	nP Load	M	N	S Load	S Clock	S Data	Conditions
H	X	X	X	X	X	X	Reset, Forces outputs LOW.
L	L	Data	Data	X	X	X	Data on M and N inputs passed directly to the M divider and N output divider. TEST output forced LOW.
L	↑	Data	Data	L	X	X	Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs.
L	H	X	X	L	↑	Data	Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK
L	H	X	X	↑	L	Data	Contents of the shift register are passed to the M divider and N output divider.
L	H	X	X	↓	L	Data	M divider and N output divider values are latched.
L	H	X	X	L	X	X	Parallel or serial input do not affect shift registers.
L	H	X	X	H	↑	Data	S_DATA passed directly to M divider as it is clocked.

Note: L = Low; H = High; X = Don't care; ↑ = Rising Edge Transition; ↓ = Falling Edge Transition

PROGRAMMABLE VCSO FREQUENCY FUNCTION

TABLE 5B

VCSO Frequency (MHz)	M Divide	32 M5	16 M4	8 M3	4 M2	2 M1	1 M0
325	13	0	0	1	1	0	1
350	14	0	0	1	1	1	0
375	15	0	0	1	1	1	1
400	16	0	1	0	0	0	0
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
600	24	0	1	1	0	0	0
625	25	0	1	1	0	0	1
650	26	0	1	1	0	1	0

NOTE 1: These M divide values and the resulting frequencies correspond to a reference frequency of 25MHz.

PARALLEL MODE FUNCTION

TABLE 5C

Inputs N1	Inputs N0	N Divider Value	Output Frequency (MHz) Min	Output Frequency (MHz) Max
0	0	1	311	700
0	1	2	155.5	350
1	0	4	77.75	175
1	1	8	38.875	87.5

SERIAL MODE FUNCTION

TABLE 5D

Inputs REF SEL	Inputs Reference
0	DIFF_REF
1	REF_CLK

POWER SUPPLY DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			162		mA

V_{CC}= 3.3V ±5%, T_A= 0°C to 70°C

LVCMOS/LVTTL DC CHARACTERISTICS

Symbol	Parameter		Test Conditions	Min	Max	Units
V_{IH}	Input High Voltage	REF_SEL, S_LOAD, S_ DATA, S_CLOCK nP_LOAD, N0:N1, M0:M5, MR REF_CLK0, REF_CLK1		2 2	VCC + 0.3 VCC + 0.3	V V
V_{IL}	Input Low Voltage	REF_SEL, S_LOAD, S_DATA, S_CLOCK nP_LOAD, N0:N1, M0:M5, MR		-0.3	0.8	V
		REF_CLK0, REF_CLK1		-0.3	1.3	V
I_{IH}	Input High Current	M5	$V_{DD} = V_{IN}$ = 3.465V		5	µA
		N0, N1, MR, M0:M4, S_CLOCK, S_DATA, S_LOAD, nP_LOAD, REF_SEL, REF_CLK0, REF_CLK1	$V_{DD} = V_{IN}$ = 3.465V		150	µA
I_{IL}	Input Low Current	M5	V_{DD} = 3.465, V_{IN} = 0V	-150		µA
		N0, N1, MR, M0:M4, S_CLOCK, S_DATA, S_LOAD, nP_LOAD, REF_SEL, REF_CLK0, REF_CLK1	V_{DD} = 3.465, V_{IN} = 0V	-5		µA
V_{OH}	Output High Voltage; NOTE 1			2.6		V
V_{OL}	Output Low Voltage; NOTE 1				0.5	V

Note 1: Outputs terminated with 50Ω to V_{CC}/2. See parameter Measurement section, 3.3V Output Load Test Circuit.

LVPECL DC CHARACTERISTICS

Symbol	Parameter	Signal	Min	Max	Units
V_{OH}	Output High Voltage: Note 1	FOUT, nFOUT	V_{DD} – 1.4	Vcc – 1.0	V
V_{OL}	Output Low Voltage: Note 1	FOUT, nFOUT	V_{DD} – 2.0	Vcc – 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing	FOUT, nFOUT	0.6	0.85	V

Note 1: Output terminated with 50Ω to V_{DD}–2.V

INPUT FREQUENCY CHARACTERISTICS

Symbol	Parameter	Test Conditions	Min	Max	Units
F_{IN}	Input Frequency	REF_CLK0, REF_CLK1	10	166	MHz
		S_CLOCK		50	MHz

V_{CC} = 3.3V±5%, T_A = 0°C to 70°C

AC CHARACTERISTICS

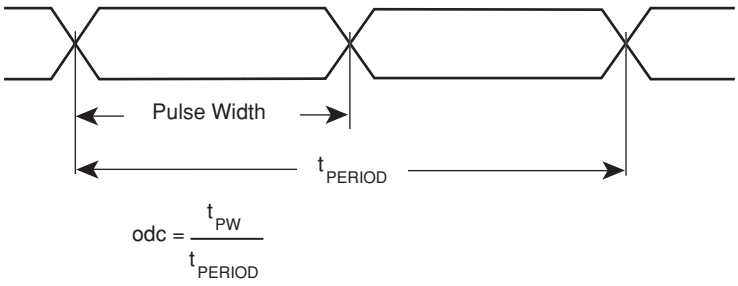
Symbol	Parameter		Test Conditions	Min	Typ	Max	Units
F_{OUT}	Output Frequency			38.88		700	MHz
ØNOISE	Single Side Band		1kHz offset		-72		dBc/Hz
	Phase Noise		10kHz offset		-94		dBc/Hz
			100kHz offset		-123		dBc/Hz
J (t)	Jitter (RMS)		12kHz to 20 MHz		0.69		ps
odc	Output Duty Cycle				50		%
t_R (Note 1)	Output Rise Time for output pairs FOUT0, nFOUT0 & FOUT1, nFOUT1	FOUT = 155MHz	20% to 80%, each output of pair measured is terminated into 50Ω load biased at Vcc-2V	350	450	550	ps
		FOUT = 311MHz		325	425	500	ps
		FOUT = 622MHz		200	275	350	ps
t_F (Note 1)	Output Fall Time for output pairs FOUT0, nFOUT0 & FOUT1, nFOUT1	FOUT = 155MHz	20% to 80%, each output of pair measured is terminated into 50Ω load biased at Vcc-2V	350	450	550	ps
		FOUT = 311MHz		325	425	500	ps
		FOUT = 622MHz		200	275	350	ps
t_S	Setup Time	M, N, to nP_LOAD		5			ns
		S_DATA to S_CLK		5			ns
		S_CLK to S_LOAD		5			ns
t_H	Hold Time	M,N, to nP_LOAD		5			ns
		S_DATA to S_CLK		5			ns
		S_CLK to S_LOAD		5			ns
t_{LOCK}	PLL Lock Time					1	ms
t_{PW}	Output Pulse Width					TBD	ns
						TBD	ns

Note: The output frequencies of 155MHz, 311MHz and 622MHz were chosen for device characterization as these are common optical network clock frequencies.

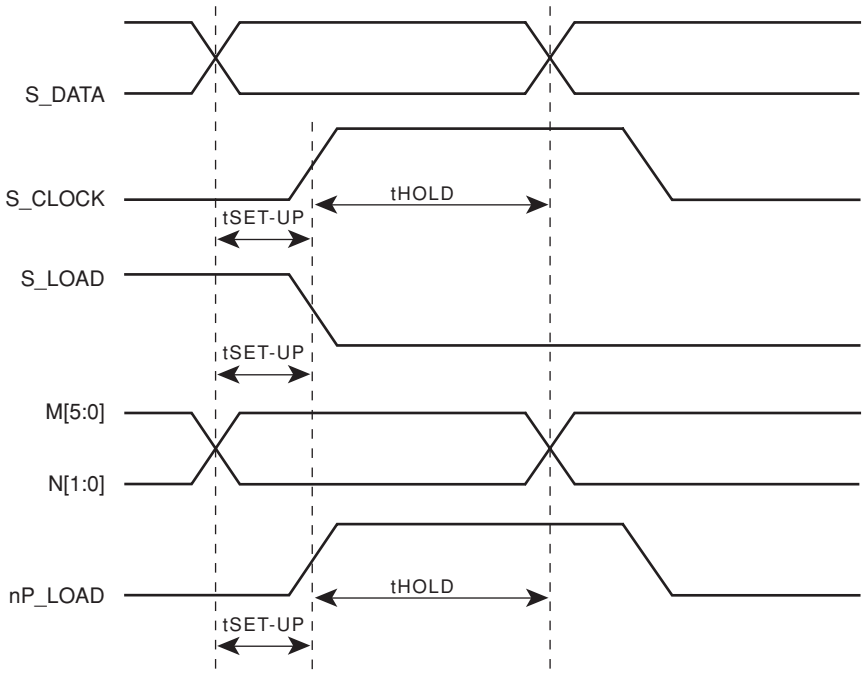
PARAMETER MEASUREMENT INFORMATION

INPUT AND OUTPUT RISE AND FALL TIME

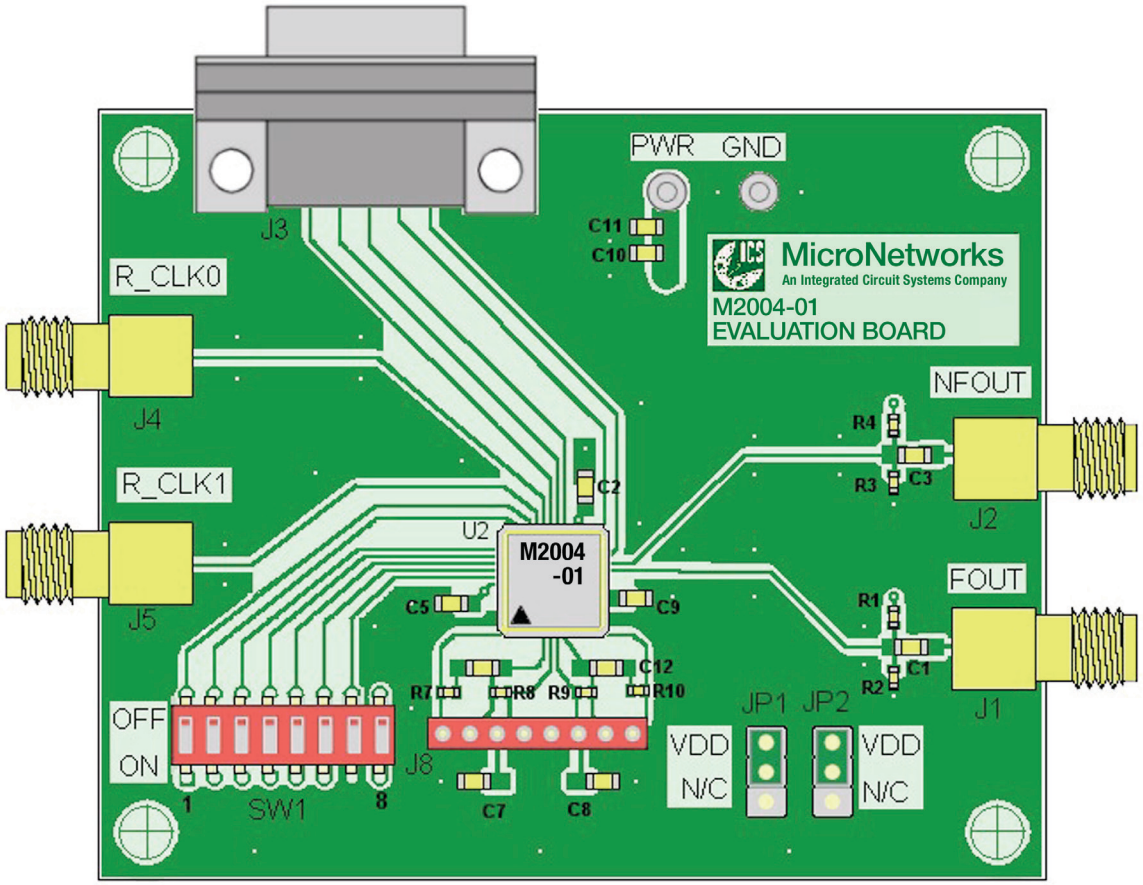
ODC & t_{PERIOD}



SETUP AND HOLD TIME



TEST EVALUATION BOARD



J3 9-PIN D CONNECTOR

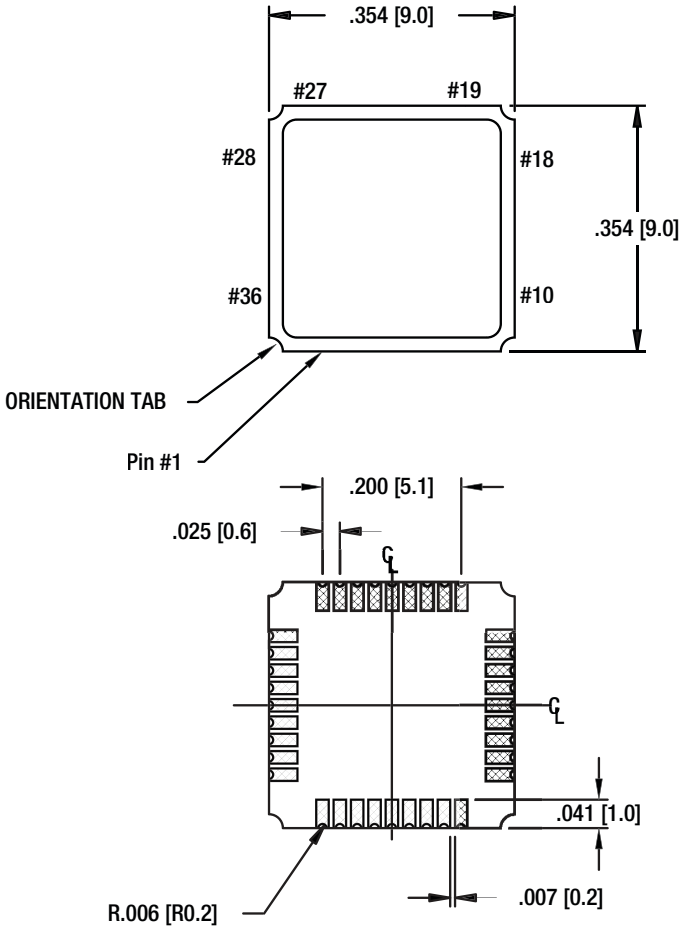
Pin	Signal
1	MR
3	S_CLOCK
5	S_DATA
7	S_LOAD
9	nP_LOAD

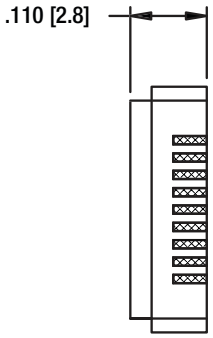
SW1

	1	2	3	4	5	6	7	8
Position	REF Select	M5	M4	M3	M2	M1	M0	N/C
Off	REF_CLK0	“1”	“0”	“0”	“0”	“0”	“0”	N/C
On	REF_CLK1	“0”	“1”	“1”	“1”	“1”	“1”	N/C

JP1: N0 Logic “1” when installed
JP2: N1 Logic “0” when installed

MECHANICAL DIMENSIONS & PIN CONFIGURATION





Pin#	Designation	Pin#	Designation
1	GND	18	S_CLOCK
2	GND	19	VDD
3	GND	20	S_DATA
4	OP_IN	21	S_LOAD
5	nOP_OUT	22	nP_LOAD
6	nVC	23	REF_CLK1
7	VC	24	REF_CLK0
8	OP_OUT	25	REF_SEL
9	nOP_IN	26	GND
10	GND	27	M0
11	VDD	28	M1
12	NO	29	M2
13	N1	30	M3
14	GND	31	M4
15	FOUT	32	M5
16	nFOUT	33	VDD
17	MR	34, 35, 36	N/C

Dimensions are in inches, (dimensions) are in mm.

ORDERING INFORMATION

PART NUMBER **M2004-01-622.0800**

Series

Model

VCSO Center Frequency
(i.e. 622.0800MHz)

Available VCSO Frequencies

622.0800	669.1281
625.0000	669.3266
627.3296	672.1600
644.5313	690.5692
666.5143	693.4830

Micro Networks
An Integrated Circuit Systems Company
324 Clark Street ■ Worcester, MA 01606 ■ tel: 508-852-5400 ■ fax: 508-852-8456
European Sales Headquarters ■ Hertogsingel 20 ■ 6214 AD Maastricht ■ The Netherlands ■ tel: +31-43-32-70912 ■ fax: +31-43-32-70715
www.micronetworks.com