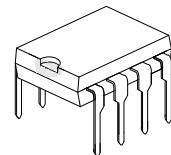


**M2073****LINEAR INTEGRATED CIRCUIT****DUAL LOW VOLTAGE POWER AMPLIFIER****■ DESCRIPTION**

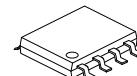
As a dual low voltage power amplifier, the UTC **M2073** has the internal circuits, such as parasitic oscillation preventing circuit and muting circuit.

Considering the fixed gain of UTC **M2073**, there's an additional voltage reducing application for the UTC **M2073**.

The normal application of **M2073** is being used as a dual audio power amplifier in lots of portable equipments.



DIP-8



SOP-8

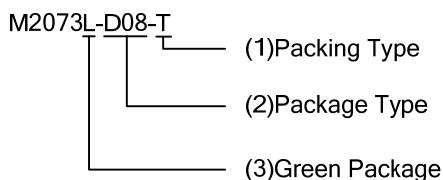
**■ FEATURES**

- \* Operating Voltage (  $V_{CC}=1.8V\sim15V$  )
- \* Low Crossover Distortion
- \* Low Operating Current
- \* Bridge or Stereo Configuration
- \* No Turn-on Noise
- \* Bipolar Technology

**■ ORDERING INFORMATION**

Ordering Number		Package	Packing
Lead Free	Halogen Free		
M2073L-D08-T	M2073G-D08-T	DIP-8	Tube
-	M2073G-S08-R	SOP-8	Tape Reel

Note: Pin Assignment: G: Gate D: Drain S: Source

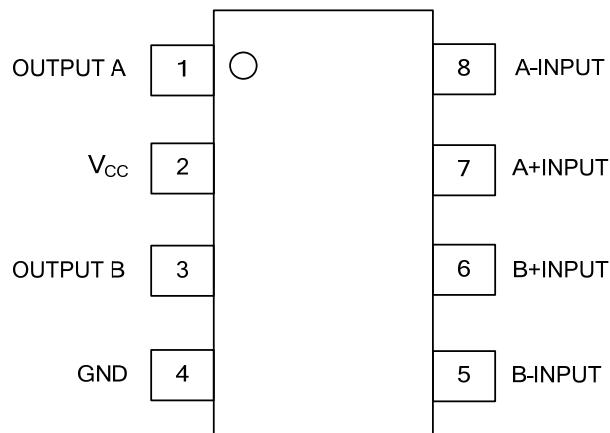


- (1) T: Tube, R: Tape Reel
- (2) D08: DIP-8, S08: SOP-8
- (3) L: Lead Free, G: Halogen Free and Lead Free

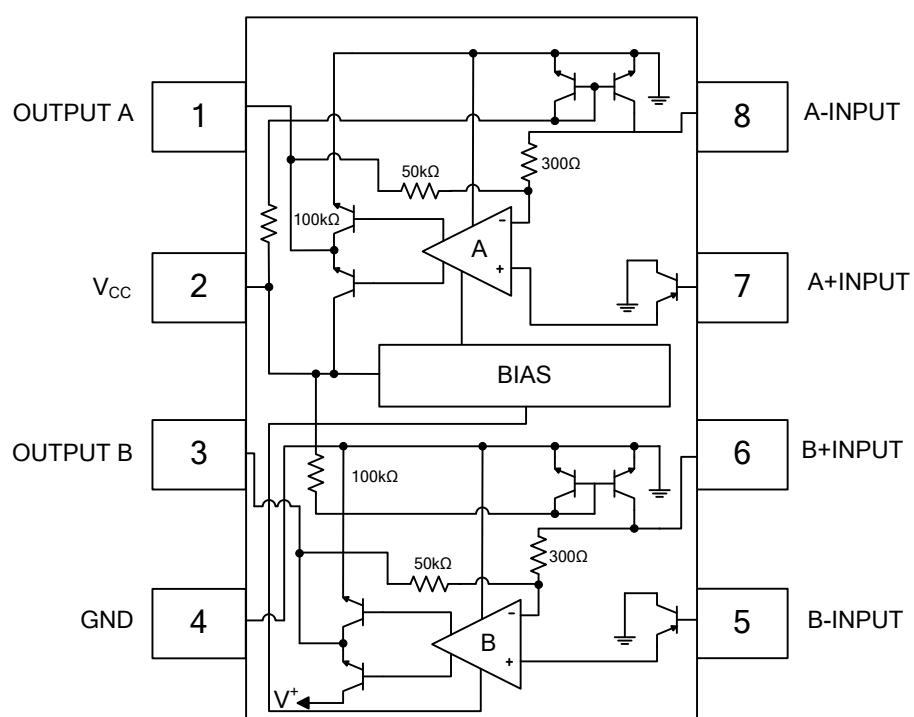
**■ MARKING**

DIP-8	SOP-8
<p>Markings on DIP-8 package:</p> <ul style="list-style-type: none"> <li>Date Code: Located at the top of the package, between pins 5 and 6.</li> <li>L: Lead Free: Located below the date code, between pins 4 and 5.</li> <li>G: Halogen Free: Located below the L mark, between pins 3 and 4.</li> <li>Lot Code: Located at the bottom of the package, between pins 1 and 2.</li> </ul>	<p>Markings on SOP-8 package:</p> <ul style="list-style-type: none"> <li>Date Code: Located at the top of the package, between pins 5 and 6.</li> <li>UTC M2073G: Located in the center of the package.</li> <li>Lot Code: Located at the bottom of the package, between pins 1 and 4.</li> </ul>

### ■ PIN CONFIGURATION



### ■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V <sub>CC</sub>	15	V
Input Voltage Range	V <sub>IN</sub>	± 0.4	V
Output Peak Current	I <sub>OP</sub>	1	A
Power Dissipation	DIP-8	700	mW
	SOP-8	300	mW
Junction Temperature	T <sub>J</sub>	125	°C
Operating Temperature	T <sub>OPR</sub>	-40 ~ +85	°C
Storage Temperature	T <sub>STG</sub>	-40 ~ +125	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS

BTL Configuration (Page 6) ( V<sub>CC</sub>=6V, Ta=25°C )

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Operating Voltage	V <sub>CC</sub>		1.8		15	V	
Operating Current	I <sub>CC</sub>	R <sub>L</sub> =∞		6	9	mA	
Output Offset Voltage ( Between the Outputs )	ΔV <sub>OUT</sub>	R <sub>L</sub> =8Ω		10	50	mV	
Input Bias Current	I <sub>I(BIAS)</sub>			100		nA	
Output Power	P <sub>OUT</sub>	THD=10% f=1kHz	V <sub>CC</sub> =9V, R <sub>L</sub> =16Ω ( Note )	DIP-8	2.0	W	
			V <sub>CC</sub> =6V, R <sub>L</sub> =8Ω ( Note )		0.9	W	
			V <sub>CC</sub> =4.5V, R <sub>L</sub> =8Ω		0.6	W	
			V <sub>CC</sub> =4.5V, R <sub>L</sub> =4Ω ( Note )		0.8	W	
			V <sub>CC</sub> =3V, R <sub>L</sub> =4Ω		200	mW	
			V <sub>CC</sub> =2V, R <sub>L</sub> =4Ω		80	mW	
			V <sub>CC</sub> =6V, R <sub>L</sub> =16Ω ( Note )	SOP-8	0.8	W	
			V <sub>CC</sub> =4V, R <sub>L</sub> =8Ω ( Note )		350	mW	
			V <sub>CC</sub> =3V, R <sub>L</sub> =4Ω ( Note )		200	mW	
			V <sub>CC</sub> =2V, R <sub>L</sub> =4Ω		80	mW	
	P <sub>OUT</sub>	THD=1% f=40Hz~15kHz	V <sub>CC</sub> =6V, R <sub>L</sub> =8Ω	DIP-8	1.0	W	
			V <sub>CC</sub> =4.5V, R <sub>L</sub> =4Ω		0.6	W	
			V <sub>CC</sub> =4V, R <sub>L</sub> =8Ω	SOP-8	380	mW	
Total Harmonic Distortion	THD	P <sub>OUT</sub> =0.5W, R <sub>L</sub> =8Ω, f=1kHz	DIP-8		0.2	%	
		V <sub>CC</sub> =4V, R <sub>L</sub> =8Ω, P <sub>OUT</sub> =200mW, R <sub>L</sub> =8Ω, f=1kHz	SOP-8		0.2	%	
Close Loop Voltage Gain	G <sub>V</sub>	f=1kHz		41	44	47	dB
Input Impedance	Z <sub>IN</sub>	f=1kHz		100			kΩ
Equivalent Input Noise Voltage	V <sub>NI1</sub>	R <sub>S</sub> =10kΩ, A Curve			2		μV
	V <sub>NI2</sub>	R <sub>S</sub> =10kΩ, B=22Hz~22kHz			2.5		μV
Ripple Rejection	RR	f=100Hz			40		dB
Cutoff Frequency	f <sub>H</sub>	G <sub>V</sub> = -3dB from f=1kHz, R <sub>L</sub> =8Ω, P <sub>OUT</sub> =1W	DIP-8		130		kHz
		G <sub>V</sub> = -3dB from f=1kHz, R <sub>L</sub> =16Ω, P <sub>OUT</sub> =0.5W	SOP-8		130		kHz

Note: At on PC Board

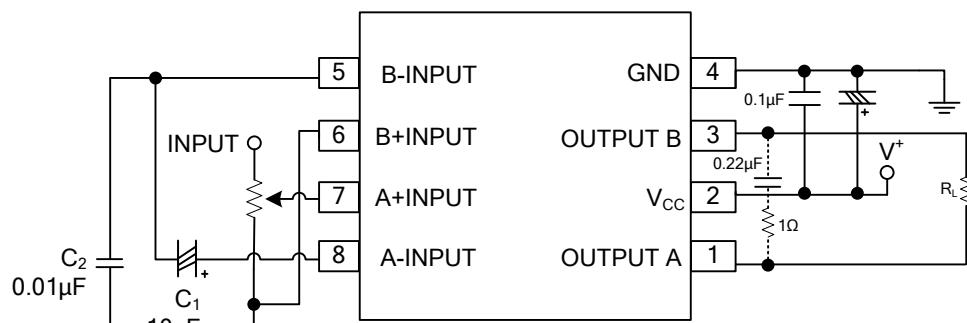
## ■ ELECTRICAL CHARACTERISTICS(Cont.)

## Stereo Configuration (Page 7)

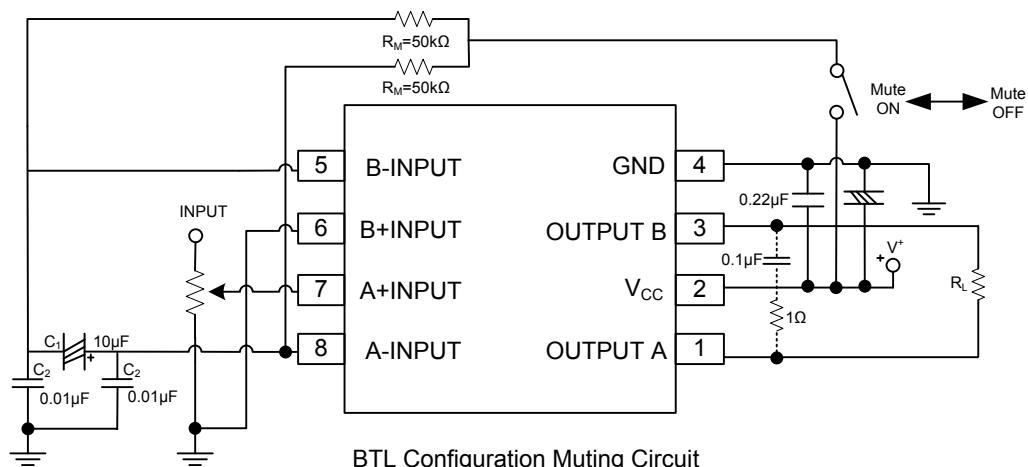
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Operating Voltage	$V_{CC}$		1.8		15	V	
Output Voltage	$V_{OUT}$			2.7		V	
Operating Current	$I_{CC}$	$R_L = \infty$		6	9	mA	
Input Bias Current	$I_{I(BIAS)}$			100		nA	
Output Power (Each Channel)	$P_{OUT}$	THD=10% $f=1\text{kHz}$	$V_{CC} = 6V, R_L = 4\Omega$ ( Note )	DIP-8	0.5	0.65	W
			$V_{CC} = 4.5V, R_L = 4\Omega$		0.32		W
			$V_{CC} = 3V, R_L = 4\Omega$		120		mW
			$V_{CC} = 2V, R_L = 4\Omega$		30		mW
			$V_{CC} = 6V, R_L = 16\Omega$	SOP-8	240		mW
			$V_{CC} = 5V, R_L = 8\Omega$ ( Note )		270		mW
			$V_{CC} = 4V, R_L = 4\Omega$ ( Note )		180	250	mW
			$V_{CC} = 3V, R_L = 4\Omega$		120		mW
		THD=1% $f=1\text{kHz}$	$V_{CC} = 2V, R_L = 4\Omega$	DIP-8	30		mW
			$V_{CC} = 6V, R_L = 4\Omega$		500		mW
			$V_{CC} = 4.5V, R_L = 4\Omega$		250		mW
			$V_{CC} = 4V, R_L = 4\Omega$	SOP-8	180		mW
Total Harmonic Distortion	THD	$P_{OUT}=0.4W, R_L=4\Omega, f=1\text{kHz}$	DIP-8		0.25		%
		$V_{CC} = 4V, R_L=4\Omega, P_{OUT}=150\text{mW}, f=1\text{kHz}$	SOP-8		0.25		%
Voltage Gain	$G_V$	$f=1\text{kHz}$		41	44	47	dB
Channel Balance	$\Delta G_V$					$\pm 1$	dB
Input Impedance	$Z_{IN}$	$f=1\text{kHz}$		100			k $\Omega$
Equivalent Input Noise Voltage	$V_{NI1}$	$R_S=10k\Omega$ , A Curve			2.5		$\mu V$
	$V_{NI2}$	$R_S=10k\Omega$ , B=22Hz~22kHz			3		$\mu V$
Ripple Rejection	RR	$f=100\text{Hz}, C_x=100\mu F$		24	30		dB
Cutoff Frequency	$f_H$	$G_V = -3\text{dB}$ from $f=1\text{kHz}, R_L=8\Omega, P_{OUT}=250\text{mW}$	DIP-8		200		kHz
		$G_V = -3\text{dB}$ from $f=1\text{kHz}, R_L=16\Omega, P_{OUT}=125\text{mW}$	SOP-8		200		kHz

Note: At on PC Board

■ APPLICATION CIRCUITS FOR BTL MODE

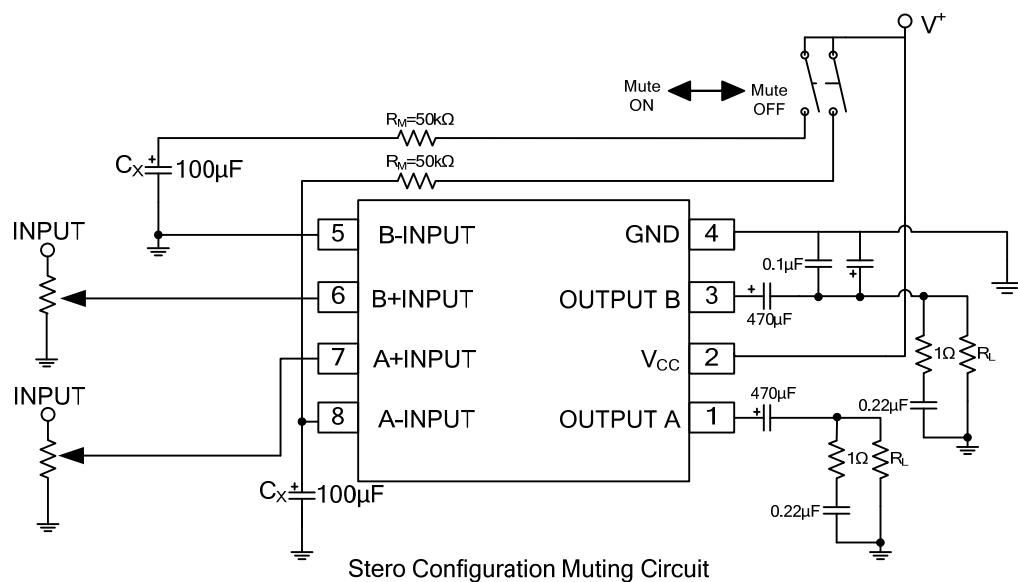
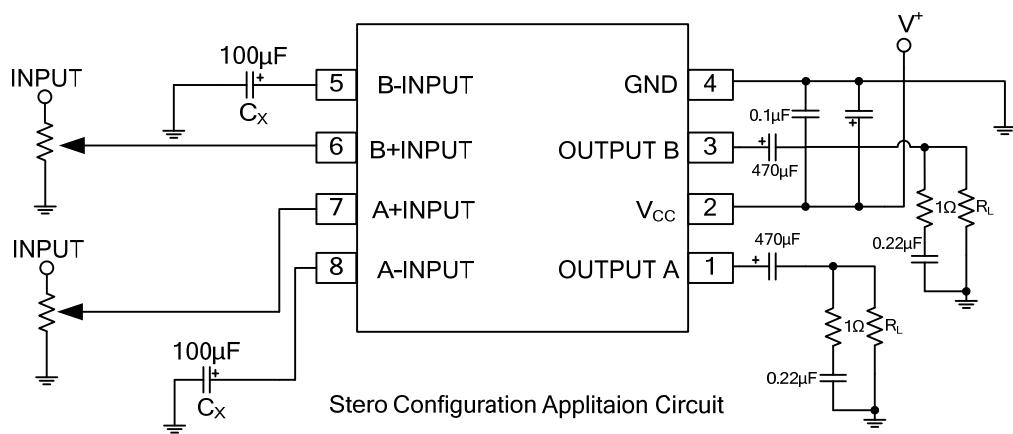


BTL Configuration Applitaion Circuit

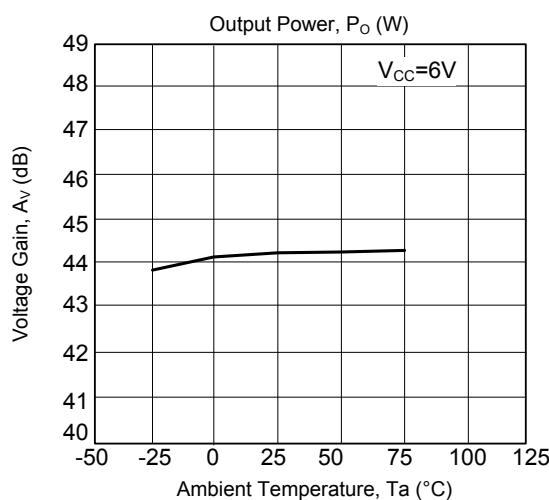
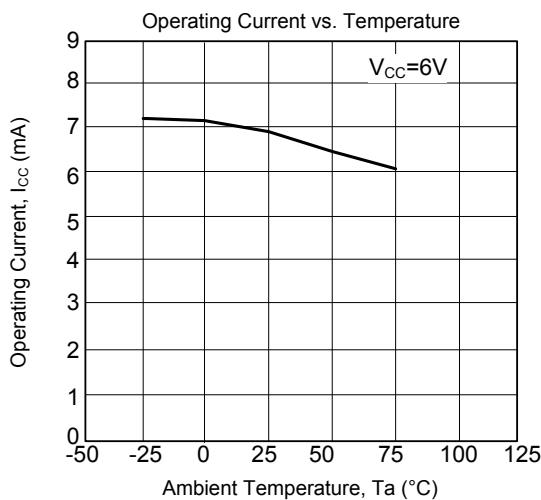
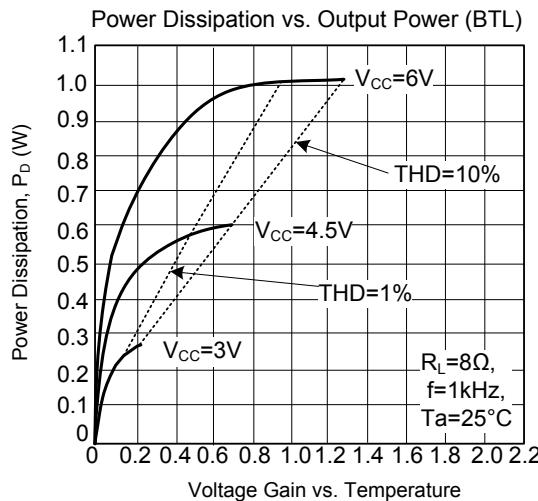
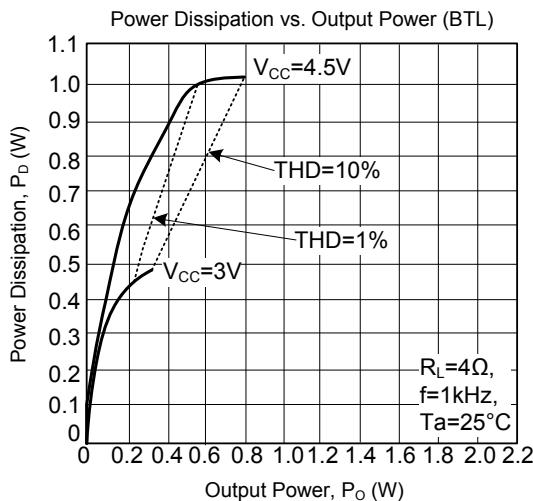
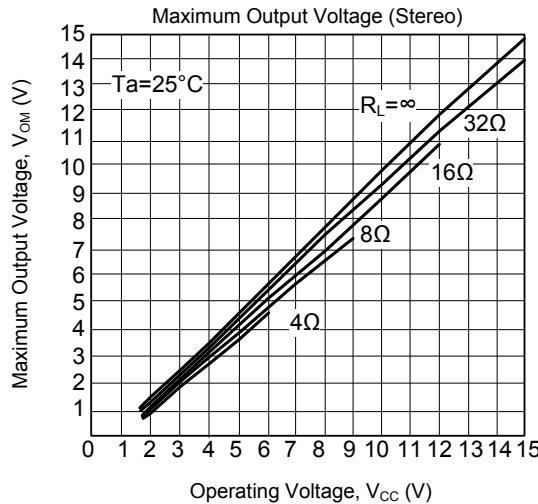
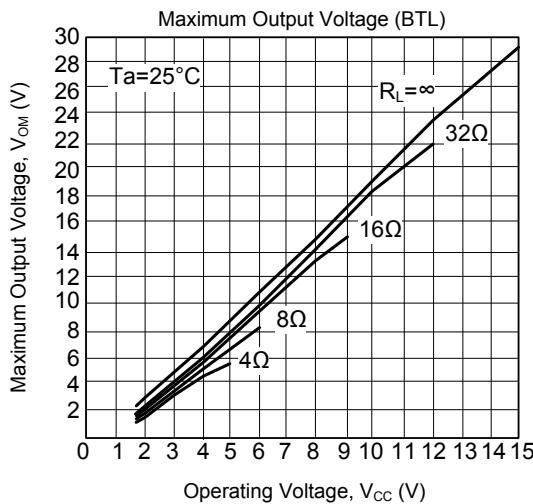


BTL Configuration Muting Circuit

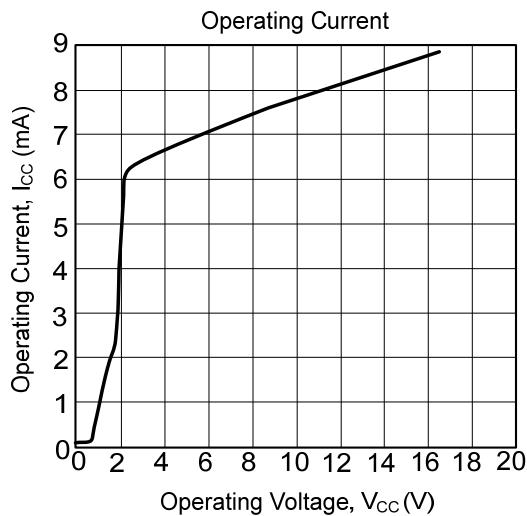
## ■ APPLICATION CIRCUITS FOR STEREO MODE



■ TYPICAL CHARACTERISTICS



### ■ TYPICAL CHARACTERISTICS (Cont.)



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