1024 - BIT STATIC RANDOM ACCESS MEMORY

POWER SUPPLY V_{CC}= 5V
TTL COMPATIBLE ALL INPUTS AND OUTPUTS
THREE-STATE OUTPUT
INPUTS PROTECTED AGAINST STATIC CHARGE
ORGANIZATION 1024 x 1 BIT IN 16 PIN STD PACKAGE

TYPE	STANDBY PWR (mW)	OPERATING PWR (mW)	ACCESS TIME (ns)
M 2102 AL - 2	42	342	250
M 2102 AL	35	174	350
M 2102 AL - 4	35	174	450
M 2102 A - 2	–	342	250
M 2102 A	–	289	350
M 2102 A - 4	–	289	450
M 2102 A - 6	–	289	650

The M 2102A is a high speed 1024 word by 1 static N-channel silicon-gate MOS RAM. The device is fully static and therefore does not require clocks or refreshing to operate. The data is read out non destructively and has the same polarity as the input data.
A low standby power version (M 2102 AL) is also available. It has all the same operating characteristics of the M 2102A with the added feature of 35 mW maximum power dissipation in standby and 174 mW in operations. The device is available in 16 lead dual in-line ceramic package, metal-seal or frit-seal and plastic package.

ABSOLUTE MAXIMUM RATINGS

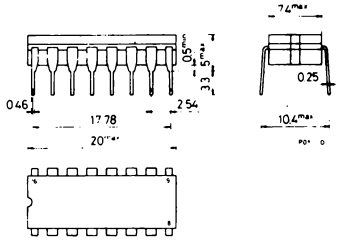
V_i*	Input voltage (at any pin)	-0.5 to 7	V
P_{tot}	Total power dissipation	1	W
T_{stg}	Storage temperature	-65 to 150	°C
T_{op}	Operating temperature under bias	0 to 70	°C

* All voltage are referred to GND pin voltage

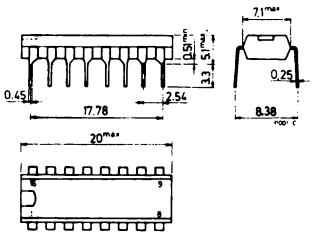
ORDERING NUMBERS:
M 2102A - B1 for dual-in-line plastic package
M 2102A - D1 for dual-in-line ceramic package, metal-seal
M 2102A - F1 for dual-in-line ceramic package, frit-seal
M 2102AL - B1 for dual-in-line plastic package
M 2102AL - D1 for dual-in-line ceramic package, metal-seal
M 2102AL - F1 for dual-in-line ceramic package, frit-seal

MECHANICAL DATA (dimensions in mm)

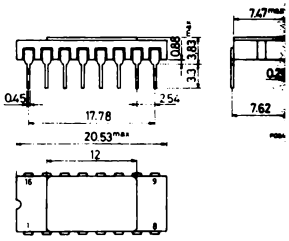
Dual in-line ceramic package frit-seal for M2102A/AL-F1



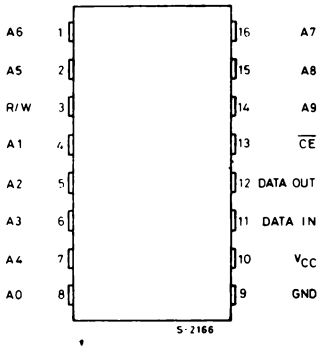
Dual in-line plastic package for M 2102A/AL-B1



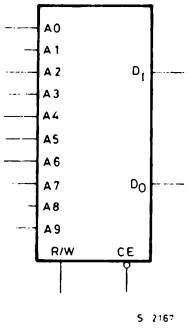
Dual in-line ceramic package metal-seal for M 2102A/AL-D



CONNECTION DIAGRAM



LOGIC DIAGRAM



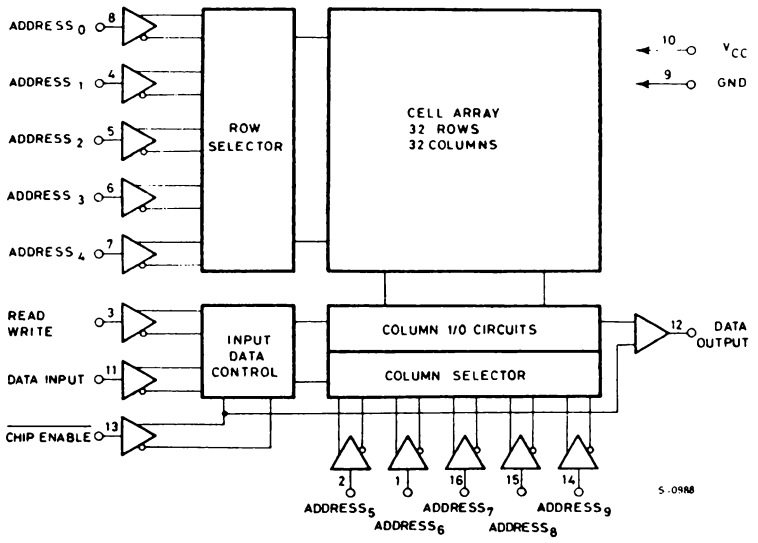
PIN NAMES

D_{IN}	DATA INPUT
A_0-A_9	ADDRESS INPUTS
R/W	READ/WRITE INPUT
$\overline{CE}$	CHIP ENABLE
D_{OUT}	DATA OUTPUT
V_{CC}	POWER (+5V)

TRUTH TABLE

$\overline{CE}$	R/W	D_{IN}	D_{OUT}	MODE
H	X	X	HIGH Z	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D_{OUT}	READ

BLOCK DIAGRAM



STATIC ELECTRICAL CHARACTERISTICS (V_{CC}= 4.75 to 5.25V, T_{amb}= 0 to 70°C unless otherwise specified)

Parameter		Test conditions	M 2102 A M 2102 AL M 2102 A -4 M 2102 AL-4			M 2102 A -2 M 2102 AL-2			M 2102 A-6			Unit
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	Min.	Typ.*	Max.	
V_{IH}	Input high voltage		2		V_{CC}	2		V_{CC}	2.2		V_{CC}	V
V_{IL}	Input low voltage		-0,5		0.8	-0.5		0.8	-0.5		0.65	V
V_{OH}	Output high voltage	I_{OH}= -100 µA	2.4			2.4			2.2			V
V_{OL}	Output low voltage	I_{OL}= 2.1 mA			0.4			0.4			0.45	V
I_{LI}	Input load current	V_I= 0 to 5.25V		1	10		1	10		1	10	µA
I_{OH}	Output leakage current	$\overline{CE}$= 2V. V_O= V_{OH}		1	5		1	5		1	5	µA
I_{OL}	Output leakage current	$\overline{CE}$= 2V V_O= 0.4V		-1	-10		-1	-10		-1	-10	µA
I_{CC}	Supply current	V_I= 5.25V T_{amb}= 0°C Data out open		33	**		45	65		33	55	mA

* Typical values for T_{amb}= 25°C and nominal supply voltage.
** The maximum I_{CC} value is 55 mA for the M 2102A and M 2102A-4, and 33 mA for the M 2102AL and M 2102AL-4.

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb}= 0 to 70°C, V_{CC}= 5V ± 5% unless otherwise specified)

Parameter		Test condition	M 2102 A -2 M 2102 AL-2		M 2102 A - M 2102 AL		M 2102 A -4 M 2102 AL-4		M 2102 A-6		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle											
t_{rc}	Read cycle	t_R, t_F= 10 ns Load = 1 TTL gate and C_L= 100 pF	250		350		450		650		ns
t_a	Access time			250		350		450		650	ns
t_E	CE to output time			130		180		230		400	ns
t_{OH1}	Previous read data valid with respect to address		40		40		40		50		ns
t_{OH2}	Previous read data valid with respect to chip enable		0		0		0		0		ns
Write Cycle											
t_{WC}	Write cycle	t_R, t_F= 10 ns Load = 1 TTL gate and C_L= 100 pF	250		350		450		650		ns
t_{AW}	Address to with setup time		20		20		20		200		ns
t_{WP}	Write pulse width		180		250		300		400		ns
t_{WR}	Write recovery time		0		0		0		50		ns
t_S	Data setup time		180		250		300		450		ns
t_h	Data hold time		0		0		0		20		ns
t_{CW}	Chip enable to write setup time		180		250		300		550		ns

CAPACITANCE (T_{amb}= 25°C, f= 1 MHz)

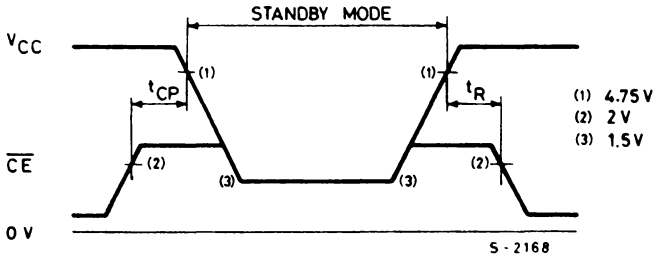
Parameter		Test conditions	Values			Unit
			Min.	Typ.	Max.	
C_I	Input capacitance	V_I = 0V		3	5	pF
C_O	Output capacitance	V_O = 0V		7	10	pF

STANDBY CHARACTERISTICS (T_{amb}= 0°C to 70°C)

Parameter		Test conditions	M 2102 AL-4 M 2102 AL			M 2102 AL-2			Unit
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
V_{PD}	V_{CC} in standby		1.5			1.5			V
V_{CES}**	CE bias in standby	$2V \leqslant V_{PD} \leqslant V_{CC}$ Max.	2			2			V
		$1.5V \leqslant V_{PD} < 2V$	V_{PD}			V_{PD}			V
I_{PD1}	Standby current	All inputs = V_{PD1} = 1.5V		15	23		20	28	mA
I_{PD2}	Standby current	All inputs = V_{PD2} = 2V		20	30		25	38	mA
t_{CP}	Chip deselect to standby time		0			0			ns
t_R***	Standby recovery time		t_{RC}			t_{RC}			ns

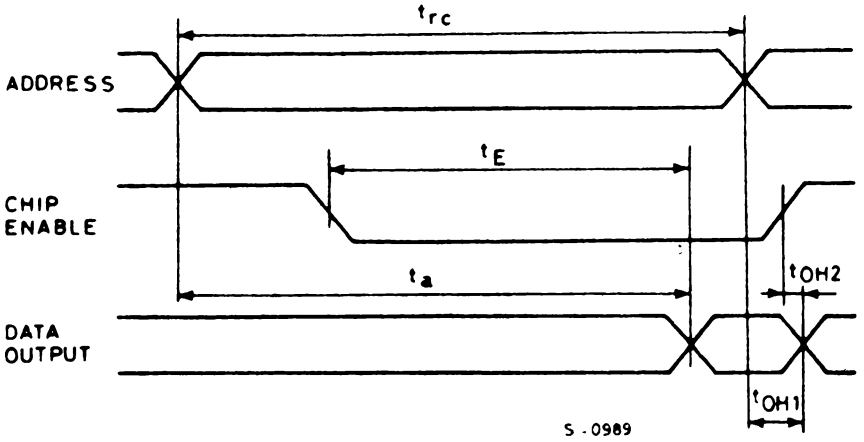
* Typical values are for T_{amb}= 25°C.
** Consider the test conditions as shown: if the standby voltage (V_{PD}) is between 5.25V (V_{CC} max) and 2V, then $\overline{CE}$ must be held at 2V Min. (V_{IH}). If the standby voltage is than 2V but greater than 1.5V (V_{PD} min), then $\overline{CE}$ and standby voltage must be at least the same value or, if they are different, $\overline{CE}$ must be the more positive of the two.
***$t_R = t_{RC}$ (READ CYCLE TIME).

STANDBY WAVEFORMS



WAVEFORMS

Read cycle



Write cycle