NuMicro® Family

Arm® 32-bit Cortex®-M23 Microcontroller

M2351/M2351SF Series Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

www.nuvoton.com

TABLE OF CONTENTS

LIST OF FIGURES

List of Tables

1 GENERAL DESCRIPTION

NuMicro® M2351 Series – *a TrustZone® empowered microcontroller series focusing on IoT security.*

The rise of the internet of things (IoT) era has increased awareness for the integration of the physical world into digital systems. While the efficiency improvements and economic benefits coming behind the digitization of our everyday lives, it has also placed pressure on system designers to deliver the innovative products capable of connecting and exchanging data incessantly. Since security and power consumption are the key requirements of IoT applications, Nuvoton NuMicro® M2351 series is excellence in supporting the proliferation of intelligent connected devices.

The NuMicro® M2351 microcontroller series is powered by Arm® Cortex®-M23 core with TrustZone® for Armv8-M architecture, which elevates the traditional firmware security to the new level of robust software security.

The low-power M2351 microcontrollers run up to 64 MHz with up to 512 Kbytes embedded Flash memory in dual bank mode, supporting secure OTA (Over-The-Air) firmware update and up to 96 Kbytes embedded SRAM. Furthermore, the M2351 series provides high-performance connectivity peripheral interfaces such as UART, SPI, I^2C, GPIOs, USB and ISO 7816-3 for smart card reader. Its secure and low-power features strengthen the innovation of IoT security.

TrustZone® for Armv8-M Empowered

The NuMicro® M2351 series is empowered by Arm® TrustZone® for Armv8-M architecture. The TrustZone® technology is a System on Chip (SoC) and CPU system-wide approach to security. In addition to the firmware-level security, the M2351 series offers a more enhanced software-level security for more robust security and greater power efficiency.

Nuvoton Security Functions Strengthened

In addition to the TrustZone® technology, the NuMicro® M2351 series is also equipped with rich functions to improve system security. The Secure Bootloader supports trusted boot feature. The hardware crypto accelerators, including ECC, support encryption and decryption operations to offload the main processor's computing power. The KPROM is a password protection mechanism to allow Flash memory write and erase. The XOM defines execute-only memory regions to protect critical program codes. The Flash lock bits are designed to disable external Flash-read/ -write and debug interface. Tamper detection pins can detect the state transition on the tamper pins.

Low-power Technology for IoT Innovation

Other than security, low power is also vital for IoT applications. Regarding the power consumption of the M2351 series, the normal run mode consumes 97 μA/MHz in LDO mode and 45 μA/MHz in DC-DC mode. The current consumption of Standby Power-down mode is 2.8 μA and the Deep Power-down mode without V_{BAT} is less than 2μA.

Arm® PSA with Nuvoton Secure Microcontroller Platform (NuSMP) Supported

The Platform Security Architecture (PSA) is a holistic set of threat models, security analysis, hardware and firmware architecture specifications, and an open source firmware reference implementation. The PSA is a contribution from Arm® to the entire IoT ecosystem, offering common ground rules and a more economical approach to building more secure devices.

Nuvoton has developed the Nuvoton Secure Microcontroller Platform (NuSMP) to support Arm® PSA. The NuSMP is a range of hardware and software mixture technologies for security requirements of general purpose and secure IoT microcontrollers. With NuSMP, developers can easily achieve the secure services with the M2351 series in coverage of: Trusted Boot (Root of Trust), Secure OTA (Over-The-Air) firmware update (including secure software download), Power Management APIs for non-secure world and PC side crypto related development software tool.

Security Features

- Arm® Cortex®-M23 TrustZone® Technology
- 8 regions MPU_NS (for non-secure world);
  8 regions MPU_S (for secure world)
- 8 regions Security Attribution Units (SAU)
- Implementation Defined Attribution Unit (IDAU)
- 2 KB OTP ROM with additional 1KB lock bits
- Hardware Crypto Accelerators
- CRC calculation unit
- Up to 6 tamper detection pins
- 96-bit Unique ID (UID), 128-bit Unique Customer ID (UCID)
- Arm® Platform Security Architecture (PSA) and Trusted Base System Architecture-M (TBSA-M) supported

Applications

- IoT Devices with Secure Connection
- Collaborative Secure Software Development Business Model
- Fingerprint Card, Fingerprint Lock
- Smart Home Appliance
- Smart City Facilities
- Wireless Sensor Node Device (WSND)
- Auto Meter Reading (AMR)
- Portable Wireless Data Collector
- Digital Currency Authentication
- Trusted Execution Environment (TEE) with Trusted Applications (TAs)

2 FEATURES

Core and System	
Arm® Cortex®-M23	• Arm® Cortex®-M23 processor, running up to 64 MHz • 64MHz at 1.8V-3.6V; 48MHz at 1.7V-3.6V • Supports Arm® TrustZone® technology Built-in PMSAv8 Memory Protection Unit (MPU) • Built-in Security Attribution Unit (SAU) • Built-in Nested Vectored Interrupt Controller (NVIC) • Built-in Embedded Trace Macrocell (ETM) • 32-bit Single-cycle hardware multiplier and 32-bit 17-cycle hardware divider • 24-bit system tick timer • Supports Programmble and maskable interrupt • Supports Low Power Sleep mode by WFI and WFE instructions • Supports single cycle I/O access
Secure Configuration Unit (SCU)	• Configures SRAM's secure attribution block by block • Configures GPIO's secure attribution port by port • Monitor secure violation incident on the chip • 24-bit non-secure state monitor timer
Brown-out Detector (BOD)	• Eight-level BOD with brown-out interrupt and reset option (3.0V/2.8V/2.6V/2.4V/2.2V/2.0V/1.8V/1.6V)
Low Voltage Reset (LVR)	• LVR with 1.5V threshold voltage level
Power Manager	• Dual voltage regulator is available for DC-DC converter or LDO • Supports 1.26v and 1.2v core voltage • Supports Power-down mode • Supports Standby Power-down mode • Supports low leakage Power-down mode • Supports ultra low leakage Power-down mode • Supports fast wake-up Power-down mode • Supports deep Power-down mode
Security	• 96-bit Unique ID (UID) • 128-bit Unique Customer ID (UCID) • One built-in temperature sensor with 1℃ resolution
Memories	
Boot Loader	• Factory pre-loaded 32 KB mask ROM for secure boot procedure • Root of Trust for Nuvoton Secure Microcontroller Platform
Flash	• Dual bank 512 KB on-chip Application ROM (APROM) for Over-

	The-Air (OTA) upgrade • 64 MHz maximum frequency, with performance at zero wait cycle in continuous address read access • 4 KB on-chip Flash memory for user-defined loader (LDROM) • 4 KB non-readbale Key Protection ROM (KPROM) for firmware programming protection • 2 KB OTP for general-purpose control use, (2 KB data + 1 KB lock bit) easy for PLM (Product Lifecycle Management) implementation • Execute Only Memory (XOM) for software intelectual property protection • 32 KB Secure Boot ROM • All on-chip Flash support 2 KB page erase • Fast Flash programming verification with CRC • On-chip Flash programming with In-Chip Programming (ICP), In-System Programming (ISP) and In-Application Programming (IAP) capabilities • Configurable boot up sources including boot loader, user-defined loader (LDROM) or Application ROM (APROM) • 2-wired ICP Flash updating through SWD interface • 32-bit/64-bit and multi-word Flash programming function
SRAM	• Up to 96 KB on-chip SRAM includes: – 32 KB SRAM located in bank 0 that supports hardware parity check; Exception (NMI) generated upon a parity check error – 64 KB SRAM located in bank 1 • Byte-, half-word- and word-access • PDMA operation
Cyclic Redundancy Calculation (CRC)	• Supports CRC-CCITT, CRC-8, CRC-16 and CRC-32 polynomials • Programmable initial value and seed value • Programmable order reverse setting and one's complement setting for input data and CRC checksum • 8-bit, 16-bit, and 32-bit data width • 8-bit write mode with 1-AHB clock cycle operation • 16-bit write mode with 2-AHB clock cycle operation • 32-bit write mode with 4-AHB clock cycle operation • Uses DMA to write data with performing CRC operation
Peripheral DMA (PDMA)	• 16 independent and configurable channels for automatic data transfer between memories and peripherals • 8 channels of PDMA1 can be configured as secure or non-secure channels • Supports time-out function when transfer time-out • Basic and Scatter-Gather transfer modes • Each channel supports circular buffer management using Scatter-Gather Transfer mode

	• Stride function for rectangle image data movement • Fixed-priority and Round-robin priorities modes • Single and burst transfer types • Byte-, half-word- and word tranfer unit with count up to 65536 • Incremental or fixed source and destination address
Clocks	
External Clock Source	• 4~24 MHz High-speed external crystal oscillator (HXT) for precise timing operation • 32.768 kHz Low-speed external crystal oscillator (LXT) for RTC function and low-power system operation • Supports clock failure detection for external crystal oscillators and exception generation (NMI)
Internal Clock Source	• 12 MHz High-speed Internal RC oscillator (HIRC) trimmed to 0.25% accuracy that can optionally be used as a system clock • 48 MHz High-speed Internal RC oscillator (HIRC48) trimmed to 0.25% accuracy that can optionally be used as a system clock • 10 kHz Low-speed Internal RC oscillator (LIRC) for watchdog timer and wakeup operation • 32 kHz Low-speed Internal RC oscillator (LIRC32) for RTC function • Up to 144 MHz on-chip PLL, sourced from HIRC or HXT, allowing for CPU operation up to the maximum CPU frequency without the need for a high-frequency crystal
Real-Time Clock (RTC)	• Real-Time Clock with a separate power domain • The RTC clock source includes Low-speed external crystal oscillator (LXT) and 32kHz Low-speed Internal RC oscillator (LIRC32) and 10kHz Low-speed Internal RC oscillator (LIRC) • The RTC block includes 80 bytes of battery-powered backup registers, which can be cleared by tamper pins • Supports 6 static and dynamic tamper pins • Able to wake up CPU from any reduced power mode • Supports Alarm registers (second, minute, hour, day, month, year) • Supports RTC Time Tick and Alarm Match interrupt • Automatic leap year recognition • Supports 1 Hz clock output for calibration • Frequency of RTC clock source compensate by RTC_FREQADJ register
Timers	
32-bit Timer	**TIMER** • Four sets of 32-bit timers with 24-bit up counter and one 8-bit pre-scale counter from independent clock source • One-shot, Periodic, Toggle and Continuous Counting operation modes • Supports event counting function to count the event from external

	pins • Supports external capture pin for interval measurement and resetting 24-bit up counter • Supports chip wake-up function, if a timer interrupt signal is generated **PWM** • Eight 16-bit PWM counters with 12-bit clock prescale with up to 64 MHz • Supports 12-bit deadband (dead time) • Up, down or up-down PWM counter type • Supports brake function • Supports mask function and tri-state output for each PWM channel
Enhanced PWM (EPWM)	• Twelve 16-bit counters with 12-bit clock prescale for twelve 64 MHz PWM output channels • Up to 12 independent input capture channels with 16-bit resolution counter • Supports dead time with maximum divided 12-bit prescale • Up, down or up-down PWM counter type • Supports complementary mode for 3 complementary paired PWM output channels • Synchronous function for phase control • Counter synchronous start function • Brake function with auto recovery mechanism • Mask function and tri-state output for each PWM channel • Able to trigger EADC or DAC to start conversion
Basic PWM (BPWM)	• Two 16-bit counters with 12-bit clock prescale for twelve 64 MHz PWM output channels • Up to 6 independent input capture channels with 16-bit resolution counter • Up, down or up-down PWM counter type • Counter synchronous start function • Mask function and tri-state output for each PWM channel • Able to trigger EADC to start conversion
Watchdog	• 18-bit free running up counter for WDT time-out interval • Supports multiple clock sources from LIRC (default selection), HCLK/2048 and LXT with 8 selectable time-out period • Able to wake up system from Power-down or Idle mode • Time-out event to trigger interrupt or reset system • Supports four WDT reset delay periods, including 1026, 130, 18 or 3 WDT_CLK reset delay period • Configured to force WDT enabled on chip power-on or reset
Window Watchdog	• Clock sourced from HCLK/2048 or LIRC; the window set by 6-bit down counter with 11-bit prescale

	• Suspended in Idle/Power-down mode
Analog Interfaces	
Enhanced Analog-to-Digital Converter (EADC)	• One 12-bit, 16-ch 3.76 MSPS SAR EADC with up to 16 single-ended input channels or 8 differential input pairs; 10-bit accuracy is guaranteed. • Three internal channels for V_{BAT}, band-gap V_{BG} input and Temperature sensor input. • Supports external VREF pin or internal reference voltage VREF: 1.6V, 2.0V, 2.5V, and 3.0V. • Two power saving modes: Power-down mode and Standby mode. • Supports calibration capability. • Analog-to-Digital conversion can be triggered by software enable, external pin, Timer 0~3 overflow pulse trigger or EPWM trigger. • Configurable EADC sampling time. • Up to 19 sample modules. • Double data buffers for sample module 0~3. • PDMA operation.
Digital-to-Analog Converter (DAC)	• Two 12-bit, 1 MSPS voltage type DAC with 8-bit mode and 8μs rail-to-rail settle time • Maximum output voltage AV_{DD} -0.2V in buffer mode. • Digital-to-Analog conversion triggered by Timer0~3, EPWM0, EPWM1, external trigger pin to start DAC conversion or software. • Supports group mode for synchronized data update of two DACs. • PDMA operation.
Analog Comparator (ACMP)	• Two rail-to-rail Analog Comparators. • Supports four multiplexed I/O pins at positive input. • Supports I/O pins, band-gap, DAC output, and 16-level Voltage divider from AV_{DD} or V_{REF} at negative input. • Supports four programmable propagation speeds for power saving. • Supports wake up from Power-down by interrput. • Supports triggers for brake events and cycle-by-cycle control for PWM. • Supports window compare mode and window latch mode. • Supports programmable hysteresis window: 0mV, 10mV, 20mV and 30mV.
Communication Interfaces	
Low-power UART	• Six sets of UARTs with up to 10.66 MHz baud rate • Auto-Baud Rate measurement and baud rate compensation function • Supports low power UART (LPUART): baud rate clock from LXT(32.768 KHz) with 9600bps in Power-down mode even system clock is stopped • 16-byte FIFOs with programmable level trigger

	• Auto flow control (nCTS and nRTS) • Supports IrDA (SIR) function • Supports LIN function on UART0 and UART1 • Supports RS-485 9-bit mode and direction control • Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in idle mode • Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction • Supports wake-up function • 8-bit receiver FIFO time-out detection function • Supports break error, frame error, parity error and receive/transmit FIFO overflow detection function • PDMA operation
Smart Card Interface	• Three sets of ISO-7816-3 which are compliant with ISO-7816-3 T=0, T=1 • Supports full duplex UART function • 4-byte FIFOs with programmable level trigger • Programmable guard time selection (11 ETU ~ 266 ETU) • One 24-bit and two 8 bit time-out counters for Answer to Request (ATR) and waiting times processing • Auto inverse convention function • Stop clock level and clock stop (clock keep) function • Transmitter and receiver error retry function • Supports hardware activation, deactivation and warm reset sequence process • Supports hardware auto deactivation sequence after card removal
I^2C	• Three sets of I^2C devices with Master/Slave mode • Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps) • Supports 10 bits mode • Programmable clocks allowing for versatile rate control • Supports multiple address recognition (four slave address with mask option) • Supports SM (Sytem Management) Bus and PM (Power Management) Bus • Supports multi-address power-down wake-up function • PDMA operation
Quad SPI	• One set of SPI Quad controller with Master/Slave mode, up to 64 MHz at 2.7V~3.6V stsyem voltage. • Supports Dual and Quad I/O Transfer mode • Supports one/two data channel half-duplex transfer • Supports receive-only mode

	• Configurable bit length of a transfer word from 8 to 32-bit • Provides separate 8-level depth transmit and receive FIFO buffers • MSB first or LSB first transfer sequence • The byte reorder function • Supports Byte or Word Suspend mode • Supports 3-wired, no slave select signal, bi-direction interface • PDMA operation.
SPI/I²S	• Up to four sets of SPI/I²S controllers with Master/Slave mode • SPI can communicate at up to 64 Mbit/s • SPI/I²S provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers **SPI** • Configurable bit length of a transfer word from 8 to 32-bit • MSB first or LSB first transfer sequence • Byte reorder function • Supports Byte or Word Suspend mode • Supports one data channel half-duplex transfer • Supports receive-only mode **I²S** • Supports mono and stereo audio data with 8-, 16-, 24- and 32-bit audio data sizes • Supports PCM mode A, PCM mode B, I2S and MSB justified data format • PDMA operation
I²S	• One set of I²S interface with Master/Slave mode • I²S audio sampling frequencies up to 192 kHz are supported • Supports mono and stereo audio data with 8-, 16-, 24- and 32-bit word sizes • Two 16-level FIFO data buffers, one for transmitting and the other for receiving • Supports I²S protocols: Philips standard, MSB-justified, and LSB-justified data format • Supports PCM protocols: PCM standard, MSB-justified, and LSB-justified data format • PCM protocol supports TDM multi-channel transmission in one audio sample; the number of data channel can be set as 2, 4, 6 or 8 • PDMA operation
Universal Serial Control Interface (USCI)	• Two sets of USCI,configured as UART, SPI or I²C function • Supports single byte TX and RX buffer mode • UART • Supports one transmit buffer and two receive buffers for data payload • Supports hardware auto flow control function and programmable

	flow control trigger level • 9-bit Data Transfer • Baud rate detection by built-in capture event of baud rate generator • Supports wake-up function • PDMA operation • SPI • Supports Master or Slave mode operation • Supports one transmit buffer and two receive buffer for data payload • Configurable bit length of a transfer word from 4 to 16-bit • Supports MSB first or LSB first transfer sequence • Supports Word Suspend function • Supports 3-wire, no slave select signal, bi-direction interface • Supports wake-up function by slave select signal in slave mode • Supports one data channel half-duplex transfer • PDMA operation • I^2C • Supports master and slave device capability • Supports one transmit buffer and two receive buffer for data payload • Communication in standard mode (100 kbps), fast mode (up to 400 kbps), and Fast mode plus (1 Mbps) • Supports 10-bit mode • Supports 10-bit bus time out capability • Supports bus monitor mode • Supports power-down wake-up by data toggle or address match • Supports multiple address recognition • Supports device address flag • Programmable setup/hold time
Controller Area Network (CAN)	• Two sets of CAN 2.0B controllers • Each supports 32 Message Objects; each Message Object has its own identifier mask • Programmable FIFO mode (concatenation of Message Object) • Disabled Automatic Re-transmission mode for Time Triggered CAN applications • Supports power-down wake-up function
Secure Digital Host Controller (SDHC)	• One set of Secure Digital Host Controller, compliant with SD Memory Card Specification Version 2.0 • Supports 50 MHz to achieve 200 Mbps at 3.3V operation • Supports dedicated DMA master with Scatter-Gather function to accelerate the data transfer between system memory and SD/SDHC/SDIO card
External Bus Interface (EBI)	• Supports up to three memory banks with individual adjustment of timing parameter

	• Each bank supports dedicated external chip select pin with polarity control and up to 1 MB addressing space • 8-/16-bit data width • Supports byte write in 16-bit data width mode • Supports variable external bus base clock (MCLK) which based on HCLK • Configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R) • Supports Address/Data multiplexed mode • Supports address bus and data bus separate mode • Supports LCD interface i80 mode • PDMA operation
GPIO	• Supports four I/O modes: Quasi bi-direction, Push-Pull output, Open-Drain output and Input only with high impendence mode • Selectable TTL/Schmitt trigger input • Configured as interrupt source with edge/level trigger setting • Supports independent pull-up/pull-down control • Supports high driver and high sink current I/O • Supports software selectable slew rate control • Supports 5V-tolerance function except analog I/O. (Except PA.8 ~ 15; PB.0 ~ 15; PD.10 ~ 12; PF.2 ~ 5; nReset.) • Improve access efficiency by using single cycle IO bus
Control Interfaces	
Quadrature Encoder Interface (QEI)	• Two QEI phase inputs (QEI_A, QEI_B) and one Index input (QEI_INDEX) • Supports 2/4 times free-counting mode and 2/4 compare-counting mode • Supports encoder pulse width measurement mode with ECAP
Enhanced Capture (ECAP)	• Input Capture Timer/Counter • Supports three input channels with independent capture counter hold register • 24-bit Input Capture up-counting timer/counter supports captured events reset and/or reload capture counter • Supports rising edge, falling edge and both edge detector options with noise filter in front of input ports • Supports compare-match function
Advanced Connectivity	
USB 2.0 Full Speed with on-chip transceiver	**USB 2.0 Full Speed OTG (On-The-Go)** • On-chip USB 2.0 full speed OTG transceiver • Compliant with USB OTG Supplement 2.0 • Configurable as host-only, device-only or ID-dependent

	USB 1.1 Host Controller • Compliant with USB Revision 1.1 Specification • Compatible with OHCI (Open Host Controller Interface) Revision 1.0 • Supports full-speed (12Mbps) and low-speed (1.5Mbps) USB devices • Supports Control, Bulk, Interrupt, Isochronous and Split transfers • Integrated a port routing logic to route full/low speed device to OHCI controller • Supports an integrated Root Hub • Supports port power control and port over current detection • Built-in DMA **USB 2.0 Full Speed Device Controller** • Compliant with USB Revision 2.0 Specification • Supports crystal-less • Supports suspend function when no bus activity existing for 3 ms • 12 configurable endpoints for configurable Isochronous, Bulk, Interrupt and Control transfer types • 1024 bytes configurable RAM for endpoint buffer • Remote wake-up capability
Cryptography Accelerator	
Elliptic Curve Cryptography (ECC)	• Hardware ECC accelerator • Supports both prime field GF(p) and binary field GF(2m) • Supports NIST P-192, P-224, P-256, P-384 and P-521 curve sizes • Supports NIST B-163, B-233, B-283, B-409 and B-571 curve sizes • Supports NIST K-163, K-233, K-283, K-409 and K-571 curve sizes • Supports point multiplication, addition and doubling operations in GF(p) and GF(2^m) • Supports modulus division, multiplication, addition and subtraction operations in GF(p)
Advanced Encryption Standard (AES)	• Hardware AES accelerator • Supports 128-bit, 192-bit and 256-bit key length and key expander, and is compliant with FIPS 197 • Supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2 and CBC-CS3 block cipher modes • Compliant with NIST SP800-38A and addendum
Data Encryption Standard (DES)	• Hardware DES accelerator • Supports ECB, CBC, CFB, OFB, and CTR block cipher mode • Compliant with FIPS 46-3
Triple Data Encryption Standard (3DES)	• Hardware Triple DES accelerator • Supports two or three different keys in each round • Supports ECB, CBC, CFB, OFB, and CTR block cipher mode

	• Implemented based on X9.52 standard and compliant with FIPS SP 800-67
Secure Hash Algorithm (SHA)	• Hardware SHA accelerator • Supports SHA-160, SHA-224, SHA-256 and SHA-384 • Compliant with FIPS 180/180-2
Pseudo Random Number Generator (PRNG)	• Supports 64-bit, 128-bit, 192-bit and 256-bit random number generation
True Randon Number Generator (TRNG)	• Up to 800 random bits per second

3 PARTS INFORMATION

3.1 Package Type

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

Part No.	QFN33	WLCSP49	LQFP64	LQFP128
M2351	M2351ZIAAE	M2351CIAAE	M2351SIAAE M2351SFSIAAP	M2351KIAAE

3.2 M2351 Series Selection Guide

PART NUMBER		M2351				
		ZIAAE	CIAAE	SIAAE	KIAAE	SFSIAAP
Flash (KB)		512	512	512	512	512
SRAM (KB)		96	96	96	96	96
ISP Loader ROM (KB)		4				
I/O		25	41	51	107	45
32-bit Timer		4				4
Tamper		-	-	1	6	1
RTC		√				
Connectivity	LPUART	6				
	ISO-7816	3				
	Quad SPI	1				-
	SPI/I²S	3	3	4	4	4
	I²S	1				
	I²C	3				
	USCI (UART/I²C/ SPI)	2				
	CAN	1				
	LIN	2				
	SDHC	1	2	2	2	2
Crypto	TRNG	√				
	DES / 3-DES / AES	√				
	ECC	√				
	SHA	√				
16-bit Enhanced PWM		12				
16-bit Basic PWM		12				
QEI		1	2	2	2	2
ECAP		-	1	1	1	1
USB 2.0 FS OTG		√				
12-bit ADC		10	16	16	16	16
12-bit DAC		2				
Analog Comparator		1	2	2	2	2
Cryptography		√				
External Bus Interface		-	√	√	√	√
Package		QFN 33	WLCSP 49	LQFP 64	LQFP 128	LQFP 64

3.3 M2351 Series Naming Rule

M23	51	SF	S	I	A	A	E
Core	**Line**	**MCP**	**Package**	**Flash**	**SRAM**	**Revision**	**Temperature**
Cortex®-M23	**51:** Base Line	SF: Secure Flash (optional letters)	**C:** WLCSP49 (2.960x2.905 mm) **Z:** QFN33 (5x5 mm) **S:** LQFP64 (7x7 mm) **K:** LQFP128 (14x14 mm)	**I:** 512 KB **G:** 256 KB **E:** 128 KB	**C:** 128 KB **A:** 96 KB **8:** 64 KB **6:** 32 KB	***M2351SF** A: 4 MB B: 2 MB C: 512 KB	**E:** -40°C ~ 105°C P: -25°C ~ 85°C

4 PIN CONFIGURATION

4.1 M2351 Series QFN33 Pin Diagram

Corresponding Part Number: M2351ZIAAE

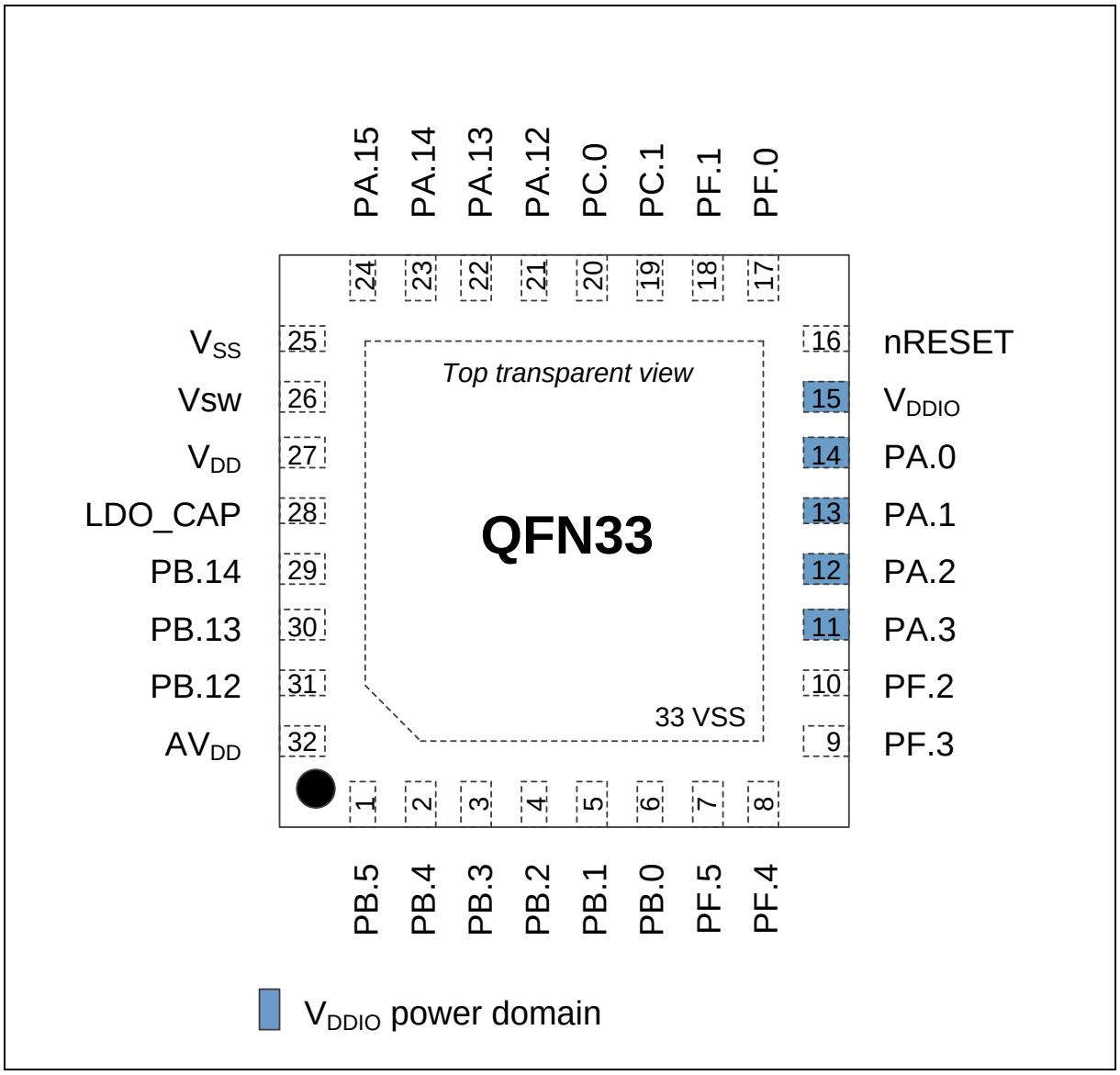


Figure 4.1-1 M2351 Series QFN 33-pin Diagram

4.2 M2351 Series WLCSP49 Pin Diagram

Corresponding Part Number: M2351CIAAE

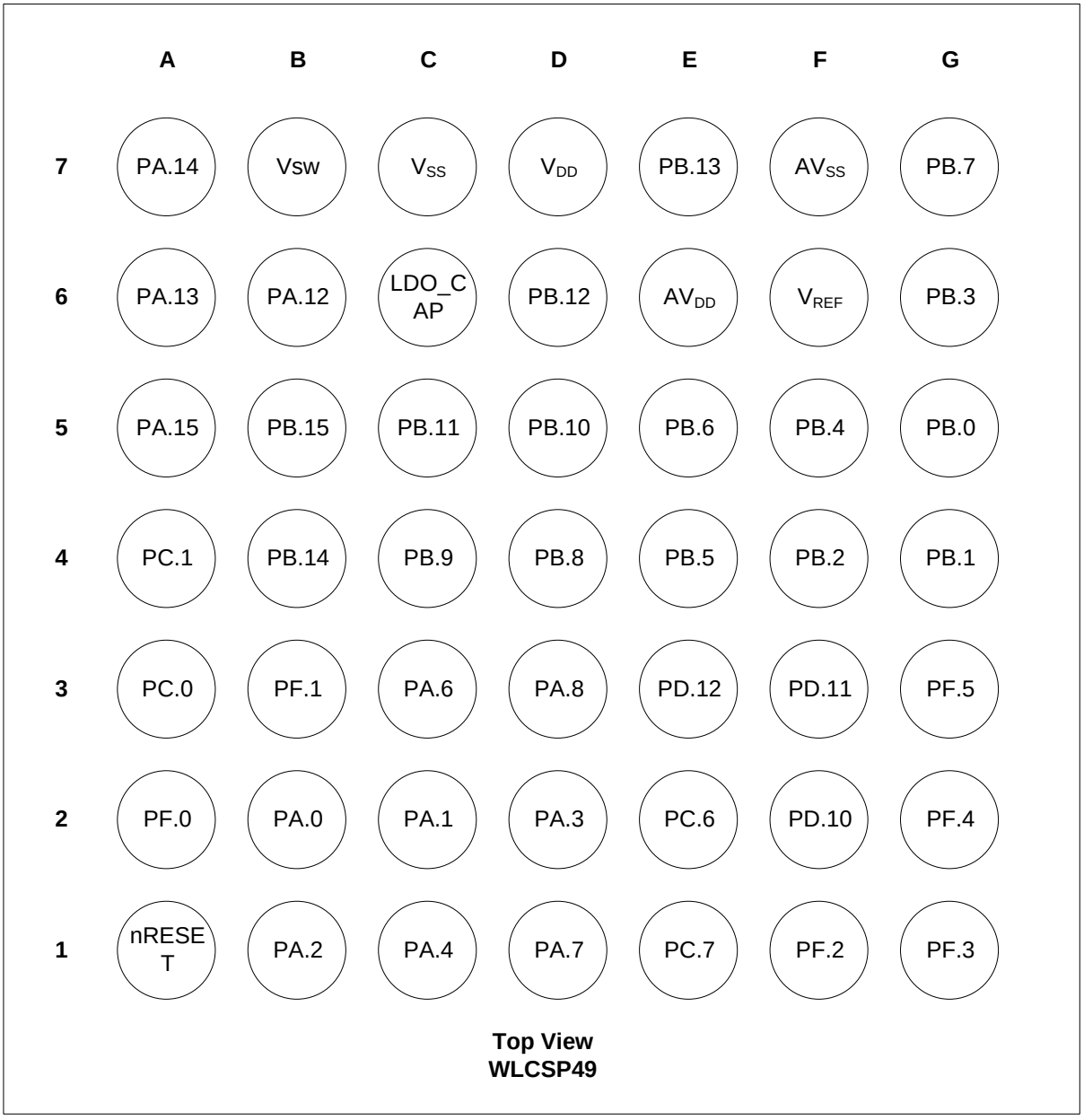


Figure 4.2-1 M2351 Series WLCSP 49-pin Diagram

4.3 M2351 Series LQFP64 Pin Diagram

Corresponding Part Number: M2351SIAAE

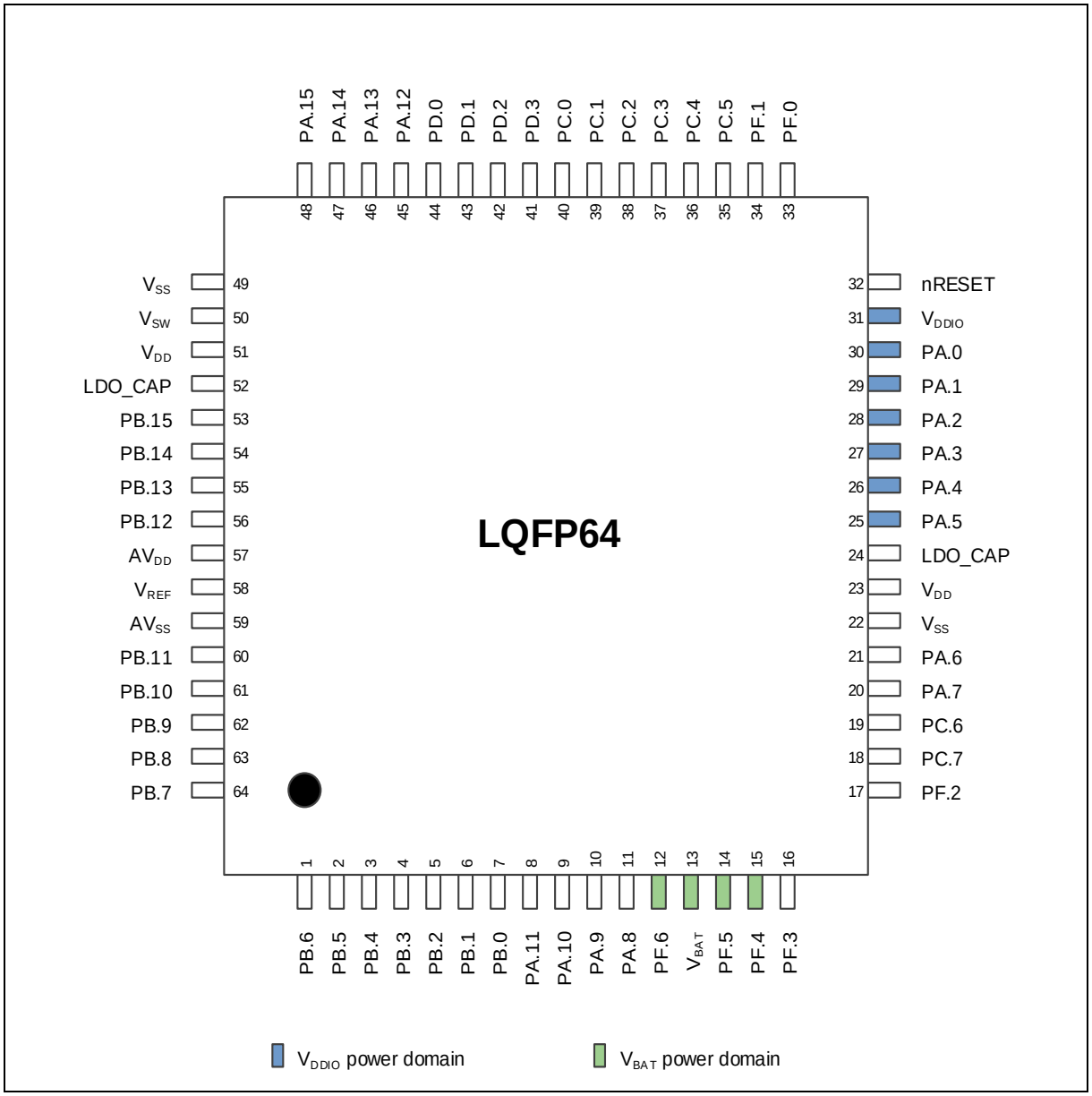


Figure 4.3-1 M2351 Series LQFP 64-pin Diagram

4.4 M2351 Series LQFP64 Pin Diagram

Corresponding Part Number: M2351SFSIAAP

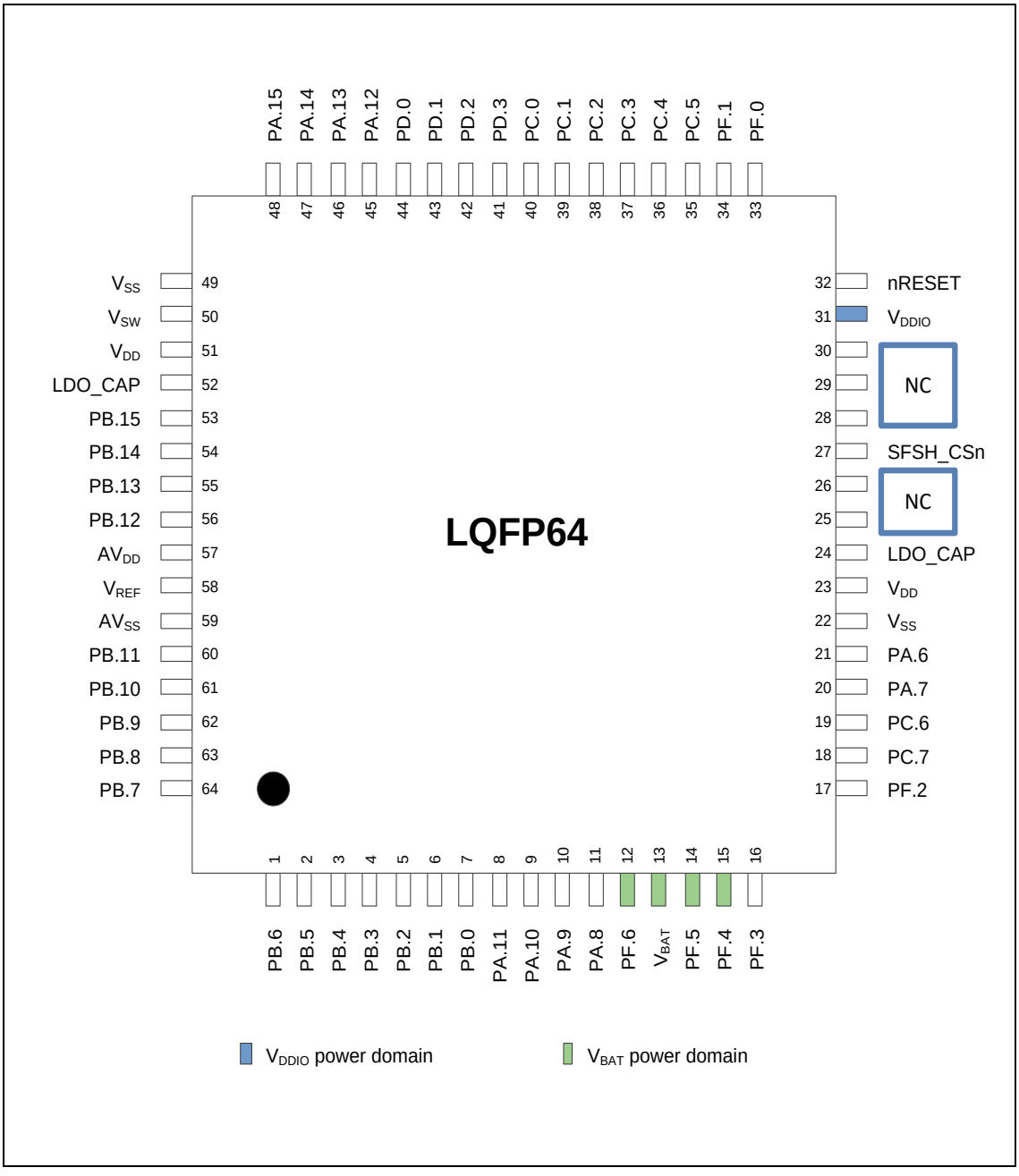


Figure 4.44-1 M2351SF Series LQFP 64-pin Diagram

4.5 M2351 Series LQFP128 Pin Diagram

Corresponding Part Number: M2351KIAAE

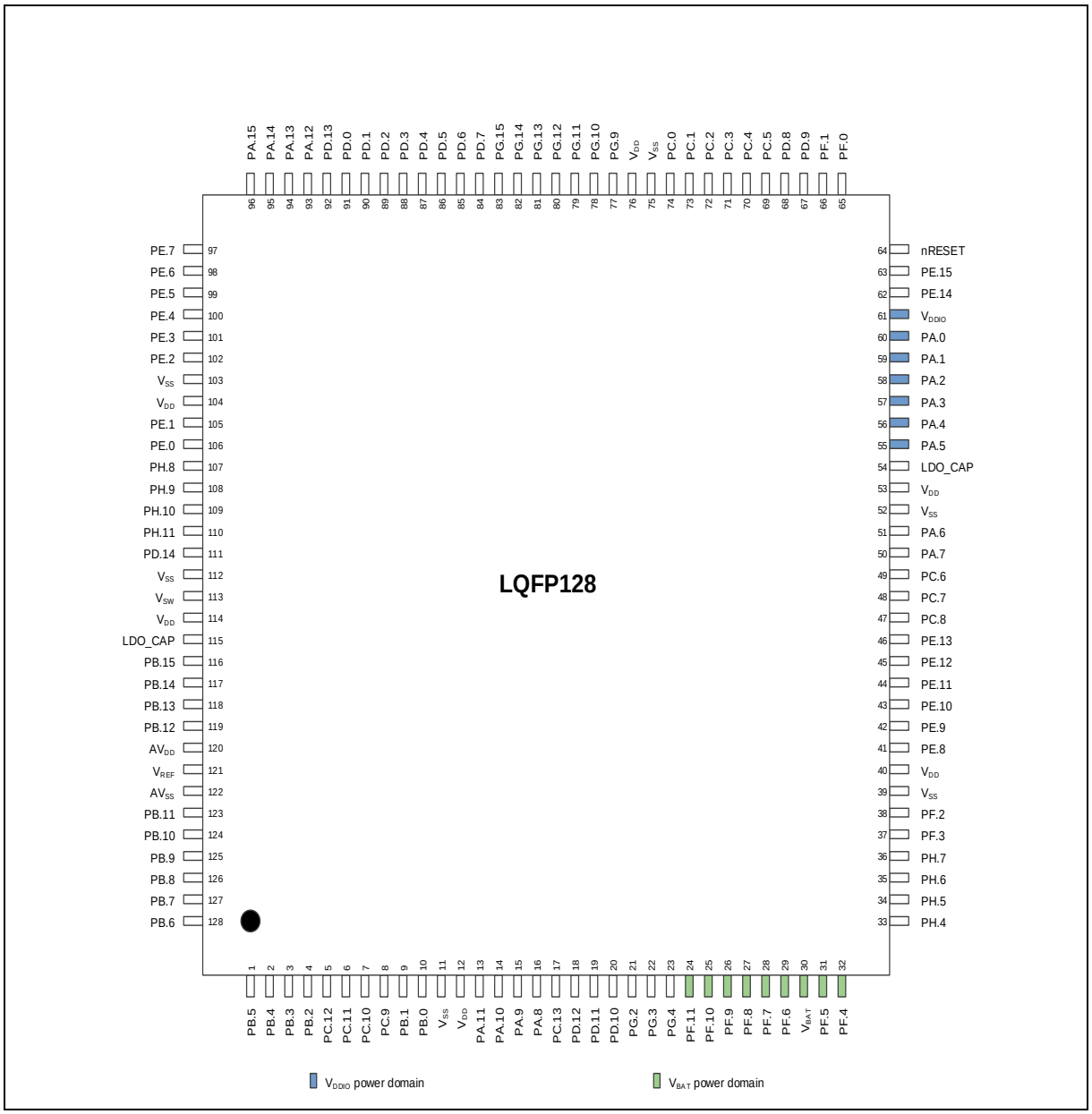


Figure 4.55-1 M2351 Series LQFP 128-pin Diagram

4.6 M2351 Performance Series Pin Description

MFP* = Multi-function pin. (Refer to section SYS_GPx_MFPL and SYS_GPx_MFPH)

PA.0 MFP0 means SYS_GPA_MFPL[3:0] = 0x0.

PA.9 MFP5 means SYS_GPA_MFPH[7:4] = 0x5.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
1	E4	2	1	PB.5	I/O	MFP0	General purpose digital I/O pin.
				EADC0_CH5	A	MFP1	EADC0 channel 5 analog input.
				ACMP1_N	A	MFP1	Analog comparator 1 negative input pin.
				EBI_ADR0	O	MFP2	EBI address bus bit 0.
				SD0_DAT3	I/O	MFP3	SD/SDIO0 data line bit 3.
				SPI1_MISO	I/O	MFP5	SPI1 MISO (Master In, Slave Out) pin.
				I2C0_SCL	I/O	MFP6	I2C0 clock pin.
				UART5_TXD	O	MFP7	UART5 data transmitter output pin.
				USCI1_CTL0	I/O	MFP8	USCI1 control 0 pin.
				SC0_CLK	O	MFP9	Smart Card 0 clock pin.
				I2S0_BCLK	O	MFP10	I2S0 bit clock output pin.
				EPWM0_CH0	I/O	MFP11	EPWM0 channel 0 output/capture input.
				TM0	I/O	MFP14	Timer0 event counter input/toggle output pin.
				INT0	I	MFP15	External interrupt 0 input pin.
2	F5	3	2	PB.4	I/O	MFP0	General purpose digital I/O pin.
				EADC0_CH4	A	MFP1	EADC0 channel 4 analog input.
				ACMP1_P1	A	MFP1	Analog comparator 1 positive input 1 pin.
				EBI_ADR1	O	MFP2	EBI address bus bit 1.
				SD0_DAT2	I/O	MFP3	SD/SDIO0 data line bit 2.
				SPI1_MOSI	I/O	MFP5	SPI1 MOSI (Master Out, Slave In) pin.
				I2C0_SDA	I/O	MFP6	I2C0 data input/output pin.
				UART5_RXD	I	MFP7	UART5 data receiver input pin.
				USCI1_CTL1	I/O	MFP8	USCI1 control 1 pin.
				SC0_DAT	I/O	MFP9	Smart Card 0 data pin.
				I2S0_MCLK	O	MFP10	I2S0 master clock output pin.
				EPWM0_CH1	I/O	MFP11	EPWM0 channel 1 output/capture input.
				TM1	I/O	MFP14	Timer1 event counter input/toggle output pin.
				INT1	I	MFP15	External interrupt 1 input pin.
3	G6	4	3	PB.3	I/O	MFP0	General purpose digital I/O pin.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
				EADC0_CH3	A	MFP1	EADC0 channel 3 analog input.
				ACMP0_N	A	MFP1	Analog comparator 0 negative input pin.
				EBI_ADR2	O	MFP2	EBI address bus bit 2.
				SD0_DAT1	I/O	MFP3	SD/SDIO0 data line bit 1.
				SPI1_CLK	I/O	MFP5	SPI1 serial clock pin.
				UART1_TXD	O	MFP6	UART1 data transmitter output pin.
				UART5_nRTS	O	MFP7	UART5 request to Send output pin.
				USCI1_DAT1	I/O	MFP8	USCI1 data 1 pin.
				SC0_RST	O	MFP9	Smart Card 0 reset pin.
				I2S0_DI	I	MFP10	I2S0 data input pin.
				EPWM0_CH2	I/O	MFP11	EPWM0 channel 2 output/capture input.
				TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
				INT2	I	MFP15	External interrupt 2 input pin.
4	F4	5	4	PB.2	I/O	MFP0	General purpose digital I/O pin.
				EADC0_CH2	A	MFP1	EADC0 channel 2 analog input.
				ACMP0_P1	A	MFP1	Analog comparator 0 positive input 1 pin.
				EBI_ADR3	O	MFP2	EBI address bus bit 3.
				SD0_DAT0	I/O	MFP3	SD/SDIO0 data line bit 0.
				SPI1_SS	I/O	MFP5	SPI1 slave select pin.
				UART1_RXD	I	MFP6	UART1 data receiver input pin.
				UART5_nCTS	I	MFP7	UART5 clear to Send input pin.
				USCI1_DAT0	I/O	MFP8	USCI1 data 0 pin.
				SC0_PWR	O	MFP9	Smart Card 0 power pin.
				I2S0_DO	O	MFP10	I2S0 data output pin.
				EPWM0_CH3	I/O	MFP11	EPWM0 channel 3 output/capture input.
				TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
				INT3	I	MFP15	External interrupt 3 input pin.
			5	PC.12	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR4	O	MFP2	EBI address bus bit 4.
				UART0_TXD	O	MFP3	UART0 data transmitter output pin.
				I2C0_SCL	I/O	MFP4	I2C0 clock pin.
				SPI3_MISO	I/O	MFP6	SPI3 MISO (Master In, Slave Out) pin.
				SC0_nCD	I	MFP9	Smart Card 0 card detect pin.
				ECAP1_IC2	I	MFP11	Enhanced capture unit 1 input 2 pin.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
				EPWM1_CH0	I/O	MFP12	EPWM1 channel 0 output/capture input.
				ACMP0_O	O	MFP14	Analog comparator 0 output pin.
			6	PC.11	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR5	O	MFP2	EBI address bus bit 5.
				UART0_RXD	I	MFP3	UART0 data receiver input pin.
				I2C0_SDA	I/O	MFP4	I2C0 data input/output pin.
				SPI3_MOSI	I/O	MFP6	SPI3 MOSI (Master Out, Slave In) pin.
				ECAP1_IC1	I	MFP11	Enhanced capture unit 1 input 1 pin.
				EPWM1_CH1	I/O	MFP12	EPWM1 channel 1 output/capture input.
				ACMP1_O	O	MFP14	Analog comparator 1 output pin.
			7	PC.10	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR6	O	MFP2	EBI address bus bit 6.
				SPI3_CLK	I/O	MFP6	SPI3 serial clock pin.
				UART3_TXD	O	MFP7	UART3 data transmitter output pin.
				ECAP1_IC0	I	MFP11	Enhanced capture unit 1 input 0 pin.
				EPWM1_CH2	I/O	MFP12	EPWM1 channel 2 output/capture input.
			8	PC.9	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR7	O	MFP2	EBI address bus bit 7.
				SPI3_SS	I/O	MFP6	SPI3 slave select pin.
				UART3_RXD	I	MFP7	UART3 data receiver input pin.
				EPWM1_CH3	I/O	MFP12	EPWM1 channel 3 output/capture input.
5	G4	6	9	PB.1	I/O	MFP0	General purpose digital I/O pin.
				EADC0_CH1	A	MFP1	EADC0 channel 1 analog input.
				EBI_ADR8	O	MFP2	EBI address bus bit 8.
				SD0_CLK	O	MFP3	SD/SDIO0 clock output pin
				SPI1_I2SMCLK	I/O	MFP5	SPI1 I2S master clock output pin
				SPI3_I2SMCLK	I/O	MFP6	SPI3 I2S master clock output pin
				UART2_TXD	O	MFP7	UART2 data transmitter output pin.
				USCI1_CLK	I/O	MFP8	USCI1 clock pin.
				I2C1_SCL	I/O	MFP9	I2C1 clock pin.
				I2S0_LRCK	O	MFP10	I2S0 left right channel clock output pin.
				EPWM0_CH4	I/O	MFP11	EPWM0 channel 4 output/capture input.
				EPWM1_CH4	I/O	MFP12	EPWM1 channel 4 output/capture input.
				EPWM0_BRAKE0	I	MFP13	EPWM0 Brake 0 input pin.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
6	G5	7	10	PB.0	I/O	MFP0	General purpose digital I/O pin.
				EADC0_CH0	A	MFP1	EADC0 channel 0 analog input.
				EBI_ADR9	O	MFP2	EBI address bus bit 9.
				SD0_CMD	I/O	MFP3	SD/SDIO0 command/response pin
				UART2_RXD	I	MFP7	UART2 data receiver input pin.
				SPI0_I2SMCLK	I/O	MFP8	SPI0 I2S master clock output pin
				I2C1_SDA	I/O	MFP9	I2C1 data input/output pin.
				EPWM0_CH5	I/O	MFP11	EPWM0 channel 5 output/capture input.
				EPWM1_CH5	I/O	MFP12	EPWM1 channel 5 output/capture input.
				EPWM0_BRAKE1	I	MFP13	EPWM0 Brake 1 input pin.
			11	V_{SS}	P	MFP0	Ground pin for digital circuit.
			12	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
		8	13	PA.11	I/O	MFP0	General purpose digital I/O pin.
				ACMP0_P0	A	MFP1	Analog comparator 0 positive input 0 pin.
				EBI_nRD	O	MFP2	EBI read enable output pin.
				SC2_PWR	O	MFP3	Smart Card 2 power pin.
				SPI2_SS	I/O	MFP4	SPI2 slave select pin.
				USCI0_CLK	I/O	MFP6	USCI0 clock pin.
				I2C2_SCL	I/O	MFP7	I2C2 clock pin.
				BPWM0_CH0	I/O	MFP9	BPWM0 channel 0 output/capture input.
				EPWM0_SYNC_OUT	O	MFP10	EPWM0 counter synchronous trigger output pin.
				TM0_EXT	I/O	MFP13	Timer0 external capture input/toggle output pin.
				DAC1_ST	I	MFP14	DAC1 external trigger input.
		9	14	PA.10	I/O	MFP0	General purpose digital I/O pin.
				ACMP1_P0	A	MFP1	Analog comparator 1 positive input 0 pin.
				EBI_nWR	O	MFP2	EBI write enable output pin.
				SC2_RST	O	MFP3	Smart Card 2 reset pin.
				SPI2_CLK	I/O	MFP4	SPI2 serial clock pin.
				USCI0_DAT0	I/O	MFP6	USCI0 data 0 pin.
				I2C2_SDA	I/O	MFP7	I2C2 data input/output pin.
				BPWM0_CH1	I/O	MFP9	BPWM0 channel 1 output/capture input.
				QEI1_INDEX	I	MFP10	Quadrature encoder 1 index input
				ECAP0_IC0	I	MFP11	Enhanced capture unit 0 input 0 pin.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
				TM1_EXT	I/O	MFP13	Timer1 external capture input/toggle output pin.
				DAC0_ST	I	MFP14	DAC0 external trigger input.
		10	15	PA.9	I/O	MFP0	General purpose digital I/O pin.
				EBI_MCLK	O	MFP2	EBI external clock output pin.
				SC2_DAT	I/O	MFP3	Smart Card 2 data pin.
				SPI2_MISO	I/O	MFP4	SPI2 MISO (Master In, Slave Out) pin.
				USCI0_DAT1	I/O	MFP6	USCI0 data 1 pin.
				UART1_TXD	O	MFP7	UART1 data transmitter output pin.
				BPWM0_CH2	I/O	MFP9	BPWM0 channel 2 output/capture input.
				QEI1_A	I	MFP10	Quadrature encoder 1 phase A input
				ECAP0_IC1	I	MFP11	Enhanced capture unit 0 input 1 pin.
				TM2_EXT	I/O	MFP13	Timer2 external capture input/toggle output pin.
	D3	11	16	PA.8	I/O	MFP0	General purpose digital I/O pin.
				EBI_ALE	O	MFP2	EBI address latch enable output pin.
				SC2_CLK	O	MFP3	Smart Card 2 clock pin.
				SPI2_MOSI	I/O	MFP4	SPI2 MOSI (Master Out, Slave In) pin.
				USCI0_CTL1	I/O	MFP6	USCI0 control 1 pin.
				UART1_RXD	I	MFP7	UART1 data receiver input pin.
				BPWM0_CH3	I/O	MFP9	BPWM0 channel 3 output/capture input.
				QEI1_B	I	MFP10	Quadrature encoder 1 phase B input
				ECAP0_IC2	I	MFP11	Enhanced capture unit 0 input 2 pin.
				TM3_EXT	I/O	MFP13	Timer3 external capture input/toggle output pin.
				INT4	I	MFP15	External interrupt 4 input pin.
			17	PC.13	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR10	O	MFP2	EBI address bus bit 10.
				SC2_nCD	I	MFP3	Smart Card 2 card detect pin.
				SPI2_I2SMCLK	I/O	MFP4	SPI2 I2S master clock output pin
				USCI0_CTL0	I/O	MFP6	USCI0 control 0 pin.
				UART2_TXD	O	MFP7	UART2 data transmitter output pin.
				BPWM0_CH4	I/O	MFP9	BPWM0 channel 4 output/capture input.
				CLKO	O	MFP13	Clock Out
				EADC0_ST	I	MFP14	EADC0 external trigger input.
	E3		18	PD.12	I/O	MFP0	General purpose digital I/O pin.
				EBI_nCS0	O	MFP2	EBI chip select 0 output pin.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
				UART2_RXD	I	MFP7	UART2 data receiver input pin.
				BPWM0_CH5	I/O	MFP9	BPWM0 channel 5 output/capture input.
				QEI0_INDEX	I	MFP10	Quadrature encoder 0 index input
				CLKO	O	MFP13	Clock Out
				EADC0_ST	I	MFP14	EADC0 external trigger input.
				INT5	I	MFP15	External interrupt 5 input pin.
	F3		19	PD.11	I/O	MFP0	General purpose digital I/O pin.
				EBI_nCS1	O	MFP2	EBI chip select 1 output pin.
				UART1_TXD	O	MFP3	UART1 data transmitter output pin.
				CAN0_TXD	O	MFP4	CAN0 bus transmitter output.
				QEI0_A	I	MFP10	Quadrature encoder 0 phase A input
				INT6	I	MFP15	External interrupt 6 input pin.
	F2		20	PD.10	I/O	MFP0	General purpose digital I/O pin.
				EBI_nCS2	O	MFP2	EBI chip select 2 output pin.
				UART1_RXD	I	MFP3	UART1 data receiver input pin.
				CAN0_RXD	I	MFP4	CAN0 bus receiver input.
				QEI0_B	I	MFP10	Quadrature encoder 0 phase B input
				INT7	I	MFP15	External interrupt 7 input pin.
			21	PG.2	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR11	O	MFP2	EBI address bus bit 11.
				SPI2_SS	I/O	MFP3	SPI2 slave select pin.
				I2C0_SMBAL	O	MFP4	I2C0 SMBus SMBALTER pin
				I2C1_SCL	I/O	MFP5	I2C1 clock pin.
				TM0	I/O	MFP13	Timer0 event counter input/toggle output pin.
			22	PG.3	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR12	O	MFP2	EBI address bus bit 12.
				SPI2_CLK	I/O	MFP3	SPI2 serial clock pin.
				I2C0_SMBSUS	O	MFP4	I2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
				I2C1_SDA	I/O	MFP5	I2C1 data input/output pin.
				TM1	I/O	MFP13	Timer1 event counter input/toggle output pin.
			23	PG.4	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR13	O	MFP2	EBI address bus bit 13.
				SPI2_MISO	I/O	MFP3	SPI2 MISO (Master In, Slave Out) pin.
				TM2	I/O	MFP13	Timer2 event counter input/toggle output pin.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
			24	PF.11	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR14	O	MFP2	EBI address bus bit 14.
				SPI2_MOSI	I/O	MFP3	SPI2 MOSI (Master Out, Slave In) pin.
				TAMPER5	I/O	MFP10	TAMPER detector loop pin 5.
				TM3	I/O	MFP13	Timer3 event counter input/toggle output pin.
			25	PF.10	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR15	O	MFP2	EBI address bus bit 15.
				SC0_nCD	I	MFP3	Smart Card 0 card detect pin.
				I2S0_BCLK	O	MFP4	I2S0 bit clock output pin.
				SPI0_I2SMCLK	I/O	MFP5	SPI0 I2S master clock output pin
				TAMPER4	I/O	MFP10	TAMPER detector loop pin 4.
			26	PF.9	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR16	O	MFP2	EBI address bus bit 16.
				SC0_PWR	O	MFP3	Smart Card 0 power pin.
				I2S0_MCLK	O	MFP4	I2S0 master clock output pin.
				SPI0_SS	I/O	MFP5	SPI0 slave select pin.
				TAMPER3	I/O	MFP10	TAMPER detector loop pin 3.
			27	PF.8	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR17	O	MFP2	EBI address bus bit 17.
				SC0_RST	O	MFP3	Smart Card 0 reset pin.
				I2S0_DI	I	MFP4	I2S0 data input pin.
				SPI0_CLK	I/O	MFP5	SPI0 serial clock pin.
				TAMPER2	I/O	MFP10	TAMPER detector loop pin 2.
			28	PF.7	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR18	O	MFP2	EBI address bus bit 18.
				SC0_DAT	I/O	MFP3	Smart Card 0 data pin.
				I2S0_DO	O	MFP4	I2S0 data output pin.
				SPI0_MISO	I/O	MFP5	SPI0 MISO (Master In, Slave Out) pin.
				UART4_TXD	O	MFP6	UART4 data transmitter output pin.
				TAMPER1	I/O	MFP10	TAMPER detector loop pin 1.
		12	29	PF.6	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR19	O	MFP2	EBI address bus bit 19.
				SC0_CLK	O	MFP3	Smart Card 0 clock pin.
				I2S0_LRCK	O	MFP4	I2S0 left right channel clock output pin.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
				SPI0_MOSI	I/O	MFP5	SPI0 MOSI (Master Out, Slave In) pin.
				UART4_RXD	I	MFP6	UART4 data receiver input pin.
				EBI_nCS0	O	MFP7	EBI chip select 0 output pin.
				TAMPER0	I/O	MFP10	TAMPER detector loop pin 0.
		13	30	V_{BAT}	P	MFP0	Power supply by batteries for RTC.
7	G3	14	31	PF.5	I/O	MFP0	General purpose digital I/O pin.
				UART2_RXD	I	MFP2	UART2 data receiver input pin.
				UART2_nCTS	I	MFP4	UART2 clear to Send input pin.
				BPWM0_CH4	I/O	MFP8	BPWM0 channel 4 output/capture input.
				EPWM0_SYNC_OUT	O	MFP9	EPWM0 counter synchronous trigger output pin.
				X32_IN	I	MFP10	External 32.768 kHz crystal input pin.
				EADC0_ST	I	MFP11	EADC0 external trigger input.
8	G2	15	32	PF.4	I/O	MFP0	General purpose digital I/O pin.
				UART2_TXD	O	MFP2	UART2 data transmitter output pin.
				UART2_nRTS	O	MFP4	UART2 request to Send output pin.
				BPWM0_CH5	I/O	MFP8	BPWM0 channel 5 output/capture input.
				X32_OUT	O	MFP10	External 32.768 kHz crystal output pin.
			33	PH.4	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR3	O	MFP2	EBI address bus bit 3.
				SPI1_MISO	I/O	MFP3	SPI1 MISO (Master In, Slave Out) pin.
			34	PH.5	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR2	O	MFP2	EBI address bus bit 2.
				SPI1_MOSI	I/O	MFP3	SPI1 MOSI (Master Out, Slave In) pin.
			35	PH.6	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR1	O	MFP2	EBI address bus bit 1.
				SPI1_CLK	I/O	MFP3	SPI1 serial clock pin.
			36	PH.7	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR0	O	MFP2	EBI address bus bit 0.
				SPI1_SS	I/O	MFP3	SPI1 slave select pin.
9	G1	16	37	PF.3	I/O	MFP0	General purpose digital I/O pin.
				EBI_nCS0	O	MFP2	EBI chip select 0 output pin.
				UART0_TXD	O	MFP3	UART0 data transmitter output pin.
				I2C0_SCL	I/O	MFP4	I2C0 clock pin.
				XT1_IN	I	MFP10	External 4~24 MHz (high speed) crystal input pin.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
				BPWM1_CH0	I/O	MFP11	BPWM1 channel 0 output/capture input.
10	F1	17	38	PF.2	I/O	MFP0	General purpose digital I/O pin.
				EBI_nCS1	O	MFP2	EBI chip select 1 output pin.
				UART0_RXD	I	MFP3	UART0 data receiver input pin.
				I2C0_SDA	I/O	MFP4	I2C0 data input/output pin.
				QSPI0_CLK	I/O	MFP5	Quad SPI0 serial clock pin.
				XT1_OUT	O	MFP10	External 4~24 MHz (high speed) crystal output pin.
				BPWM1_CH1	I/O	MFP11	BPWM1 channel 1 output/capture input.
			39	V_{SS}	P	MFP0	Ground pin for digital circuit.
			40	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
			41	PE.8	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR10	O	MFP2	EBI address bus bit 10.
				I2S0_BCLK	O	MFP4	I2S0 bit clock output pin.
				SPI2_CLK	I/O	MFP5	SPI2 serial clock pin.
				USCI1_CTL1	I/O	MFP6	USCI1 control 1 pin.
				UART2_TXD	O	MFP7	UART2 data transmitter output pin.
				EPWM0_CH0	I/O	MFP10	EPWM0 channel 0 output/capture input.
				EPWM0_BRAKE0	I	MFP11	EPWM0 Brake 0 input pin.
				ECAP0_IC0	I	MFP12	Enhanced capture unit 0 input 0 pin.
				TRACE_DATA3	O	MFP14	ETM Trace Data 3 output pin
			42	PE.9	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR11	O	MFP2	EBI address bus bit 11.
				I2S0_MCLK	O	MFP4	I2S0 master clock output pin.
				SPI2_MISO	I/O	MFP5	SPI2 MISO (Master In, Slave Out) pin.
				USCI1_CTL0	I/O	MFP6	USCI1 control 0 pin.
				UART2_RXD	I	MFP7	UART2 data receiver input pin.
				EPWM0_CH1	I/O	MFP10	EPWM0 channel 1 output/capture input.
				EPWM0_BRAKE1	I	MFP11	EPWM0 Brake 1 input pin.
				ECAP0_IC1	I	MFP12	Enhanced capture unit 0 input 1 pin.
				TRACE_DATA2	O	MFP14	ETM Trace Data 2 output pin
			43	PE.10	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR12	O	MFP2	EBI address bus bit 12.
				I2S0_DI	I	MFP4	I2S0 data input pin.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
				SPI2_MOSI	I/O	MFP5	SPI2 MOSI (Master Out, Slave In) pin.
				USCI1_DAT0	I/O	MFP6	USCI1 data 0 pin.
				UART3_TXD	O	MFP7	UART3 data transmitter output pin.
				EPWM0_CH2	I/O	MFP10	EPWM0 channel 2 output/capture input.
				EPWM1_BRAKE0	I	MFP11	EPWM1 Brake 0 input pin.
				ECAP0_IC2	I	MFP12	Enhanced capture unit 0 input 2 pin.
				TRACE_DATA1	O	MFP14	ETM Trace Data 1 output pin
			44	PE.11	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR13	O	MFP2	EBI address bus bit 13.
				I2S0_DO	O	MFP4	I2S0 data output pin.
				SPI2_SS	I/O	MFP5	SPI2 slave select pin.
				USCI1_DAT1	I/O	MFP6	USCI1 data 1 pin.
				UART3_RXD	I	MFP7	UART3 data receiver input pin.
				UART1_nCTS	I	MFP8	UART1 clear to Send input pin.
				EPWM0_CH3	I/O	MFP10	EPWM0 channel 3 output/capture input.
				EPWM1_BRAKE1	I	MFP11	EPWM1 Brake 1 input pin.
				ECAP1_IC2	I	MFP13	Enhanced capture unit 1 input 2 pin.
				TRACE_DATA0	O	MFP14	ETM Trace Data 0 output pin
			45	PE.12	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR14	O	MFP2	EBI address bus bit 14.
				I2S0_LRCK	O	MFP4	I2S0 left right channel clock output pin.
				SPI2_I2SMCLK	I/O	MFP5	SPI2 I2S master clock output pin
				USCI1_CLK	I/O	MFP6	USCI1 clock pin.
				UART1_nRTS	O	MFP8	UART1 request to Send output pin.
				EPWM0_CH4	I/O	MFP10	EPWM0 channel 4 output/capture input.
				ECAP1_IC1	I	MFP13	Enhanced capture unit 1 input 1 pin.
				TRACE_CLK	O	MFP14	ETM Trace Clock output pin
			46	PE.13	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR15	O	MFP2	EBI address bus bit 15.
				I2C0_SCL	I/O	MFP4	I2C0 clock pin.
				UART4_nRTS	O	MFP5	UART4 request to Send output pin.
				UART1_TXD	O	MFP8	UART1 data transmitter output pin.
				EPWM0_CH5	I/O	MFP10	EPWM0 channel 5 output/capture input.
				EPWM1_CH0	I/O	MFP11	EPWM1 channel 0 output/capture input.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
				BPWM1_CH5	I/O	MFP12	BPWM1 channel 5 output/capture input.
				ECAP1_IC0	I	MFP13	Enhanced capture unit 1 input 0 pin.
			47	PC.8	I/O	MFP0	General purpose digital I/O pin.
				EBI_ADR16	O	MFP2	EBI address bus bit 16.
				I2C0_SDA	I/O	MFP4	I2C0 data input/output pin.
				UART4_nCTS	I	MFP5	UART4 clear to Send input pin.
				UART1_RXD	I	MFP8	UART1 data receiver input pin.
				EPWM1_CH1	I/O	MFP11	EPWM1 channel 1 output/capture input.
				BPWM1_CH4	I/O	MFP12	BPWM1 channel 4 output/capture input.
	E1	18	48	PC.7	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD9	I/O	MFP2	EBI address/data bus bit 9.
				SPI1_MISO	I/O	MFP4	SPI1 MISO (Master In, Slave Out) pin.
				UART4_TXD	O	MFP5	UART4 data transmitter output pin.
				SC2_PWR	O	MFP6	Smart Card 2 power pin.
				UART0_nCTS	I	MFP7	UART0 clear to Send input pin.
				I2C1_SMBAL	O	MFP8	I2C1 SMBus SMBALTER pin
				EPWM1_CH2	I/O	MFP11	EPWM1 channel 2 output/capture input.
				BPWM1_CH0	I/O	MFP12	BPWM1 channel 0 output/capture input.
				TM0	I/O	MFP14	Timer0 event counter input/toggle output pin.
				INT3	I	MFP15	External interrupt 3 input pin.
	E2	19	49	PC.6	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD8	I/O	MFP2	EBI address/data bus bit 8.
				SPI1_MOSI	I/O	MFP4	SPI1 MOSI (Master Out, Slave In) pin.
				UART4_RXD	I	MFP5	UART4 data receiver input pin.
				SC2_RST	O	MFP6	Smart Card 2 reset pin.
				UART0_nRTS	O	MFP7	UART0 request to Send output pin.
				I2C1_SMBSUS	O	MFP8	I2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
				EPWM1_CH3	I/O	MFP11	EPWM1 channel 3 output/capture input.
				BPWM1_CH1	I/O	MFP12	BPWM1 channel 1 output/capture input.
				TM1	I/O	MFP14	Timer1 event counter input/toggle output pin.
				INT2	I	MFP15	External interrupt 2 input pin.
	D1	20	50	PA.7	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD7	I/O	MFP2	EBI address/data bus bit 7.
				SPI1_CLK	I/O	MFP4	SPI1 serial clock pin.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
				SC2_DAT	I/O	MFP6	Smart Card 2 data pin.
				UART0_TXD	O	MFP7	UART0 data transmitter output pin.
				I2C1_SCL	I/O	MFP8	I2C1 clock pin.
				EPWM1_CH4	I/O	MFP11	EPWM1 channel 4 output/capture input.
				BPWM1_CH2	I/O	MFP12	BPWM1 channel 2 output/capture input.
				ACMP0_WLAT	I	MFP13	Analog comparator 0 window latch input pin
				TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
				INT1	I	MFP15	External interrupt 1 input pin.
	C3	21	51	PA.6	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD6	I/O	MFP2	EBI address/data bus bit 6.
				SPI1_SS	I/O	MFP4	SPI1 slave select pin.
				SC2_CLK	O	MFP6	Smart Card 2 clock pin.
				UART0_RXD	I	MFP7	UART0 data receiver input pin.
				I2C1_SDA	I/O	MFP8	I2C1 data input/output pin.
				EPWM1_CH5	I/O	MFP11	EPWM1 channel 5 output/capture input.
				BPWM1_CH3	I/O	MFP12	BPWM1 channel 3 output/capture input.
				ACMP1_WLAT	I	MFP13	Analog comparator 1 window latch input pin
				TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
				INT0	I	MFP15	External interrupt 0 input pin.
		22	52	V_{SS}	P	MFP0	Ground pin for digital circuit.
		23	53	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
		24	54	LDO_CAP	P	MFP0	LDO output pin.
		25	55	PA.5	I/O	MFP0	General purpose digital I/O pin.
				QSPI0_MISO1	I/O	MFP3	Quad SPI0 MISO1 (Master In, Slave Out) pin.
				SPI1_I2SMCLK	I/O	MFP4	SPI1 I2S master clock output pin
				SC2_nCD	I	MFP6	Smart Card 2 card detect pin.
				UART0_nCTS	I	MFP7	UART0 clear to Send input pin.
				UART5_TXD	O	MFP8	UART5 data transmitter output pin.
				I2C0_SCL	I/O	MFP9	I2C0 clock pin.
				CAN0_TXD	O	MFP10	CAN0 bus transmitter output.
				BPWM0_CH5	I/O	MFP12	BPWM0 channel 5 output/capture input.
				EPWM0_CH0	I/O	MFP13	EPWM0 channel 0 output/capture input.
				QEI0_INDEX	I	MFP14	Quadrature encoder 0 index input

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
	C1	26	56	PA.4	I/O	MFP0	General purpose digital I/O pin.
				QSPI0_MOSI1	I/O	MFP3	Quad SPI0 MOSI1 (Master Out, Slave In) pin.
				SPI0_I2SMCLK	I/O	MFP4	SPI0 I2S master clock output pin
				SC0_nCD	I	MFP6	Smart Card 0 card detect pin.
				UART0_nRTS	O	MFP7	UART0 request to Send output pin.
				UART5_RXD	I	MFP8	UART5 data receiver input pin.
				I2C0_SDA	I/O	MFP9	I2C0 data input/output pin.
				CAN0_RXD	I	MFP10	CAN0 bus receiver input.
				BPWM0_CH4	I/O	MFP12	BPWM0 channel 4 output/capture input.
				EPWM0_CH1	I/O	MFP13	EPWM0 channel 1 output/capture input.
				QEI0_A	I	MFP14	Quadrature encoder 0 phase A input
11	D2	27	57	PA.3	I/O	MFP0	General purpose digital I/O pin.
				QSPI0_SS	I/O	MFP3	Quad SPI0 slave select pin.
				SPI0_SS	I/O	MFP4	SPI0 slave select pin.
				SC0_PWR	O	MFP6	Smart Card 0 power pin.
				UART4_TXD	O	MFP7	UART4 data transmitter output pin.
				UART1_TXD	O	MFP8	UART1 data transmitter output pin.
				I2C1_SCL	I/O	MFP9	I2C1 clock pin.
				BPWM0_CH3	I/O	MFP12	BPWM0 channel 3 output/capture input.
				EPWM0_CH2	I/O	MFP13	EPWM0 channel 2 output/capture input.
				QEI0_B	I	MFP14	Quadrature encoder 0 phase B input
12	B1	28	58	PA.2	I/O	MFP0	General purpose digital I/O pin.
				QSPI0_CLK	I/O	MFP3	Quad SPI0 serial clock pin.
				SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
				SC0_RST	O	MFP6	Smart Card 0 reset pin.
				UART4_RXD	I	MFP7	UART4 data receiver input pin.
				UART1_RXD	I	MFP8	UART1 data receiver input pin.
				I2C1_SDA	I/O	MFP9	I2C1 data input/output pin.
				BPWM0_CH2	I/O	MFP12	BPWM0 channel 2 output/capture input.
				EPWM0_CH3	I/O	MFP13	EPWM0 channel 3 output/capture input.
13	C2	29	59	PA.1	I/O	MFP0	General purpose digital I/O pin.
				QSPI0_MISO0	I/O	MFP3	Quad SPI0 MISO0 (Master In, Slave Out) pin.
				SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
				SC0_DAT	I/O	MFP6	Smart Card 0 data pin.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
				UART0_TXD	O	MFP7	UART0 data transmitter output pin.
				UART1_nCTS	I	MFP8	UART1 clear to Send input pin.
				I2C2_SCL	I/O	MFP9	I2C2 clock pin.
				BPWM0_CH1	I/O	MFP12	BPWM0 channel 1 output/capture input.
				EPWM0_CH4	I/O	MFP13	EPWM0 channel 4 output/capture input.
				DAC1_ST	I	MFP15	DAC1 external trigger input.
14	B2	30	60	PA.0	I/O	MFP0	General purpose digital I/O pin.
				QSPI0_MOSI0	I/O	MFP3	Quad SPI0 MOSI0 (Master Out, Slave In) pin.
				SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
				SC0_CLK	O	MFP6	Smart Card 0 clock pin.
				UART0_RXD	I	MFP7	UART0 data receiver input pin.
				UART1_nRTS	O	MFP8	UART1 request to Send output pin.
				I2C2_SDA	I/O	MFP9	I2C2 data input/output pin.
				BPWM0_CH0	I/O	MFP12	BPWM0 channel 0 output/capture input.
				EPWM0_CH5	I/O	MFP13	EPWM0 channel 5 output/capture input.
				DAC0_ST	I	MFP15	DAC0 external trigger input.
15		31	61	V_{DDIO}	P	MFP0	Power supply for PA.0~PA.5.
			62	PE.14	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD8	I/O	MFP2	EBI address/data bus bit 8.
				UART2_TXD	O	MFP3	UART2 data transmitter output pin.
				CAN0_TXD	O	MFP4	CAN0 bus transmitter output.
			63	PE.15	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD9	I/O	MFP2	EBI address/data bus bit 9.
				UART2_RXD	I	MFP3	UART2 data receiver input pin.
				CAN0_RXD	I	MFP4	CAN0 bus receiver input.
16	A1	32	64	nRESET	I	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
17	A2	33	65	PF.0	I/O	MFP0	General purpose digital I/O pin.
				UART1_TXD	O	MFP2	UART1 data transmitter output pin.
				I2C1_SCL	I/O	MFP3	I2C1 clock pin.
				BPWM1_CH0	I/O	MFP12	BPWM1 channel 0 output/capture input.
				ICE_DAT	O	MFP14	Serial wired debugger data pin.
18	B3	34	66	PF.1	I/O	MFP0	General purpose digital I/O pin.
				UART1_RXD	I	MFP2	UART1 data receiver input pin.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
				I2C1_SDA	I/O	MFP3	I2C1 data input/output pin.
				BPWM1_CH1	I/O	MFP12	BPWM1 channel 1 output/capture input.
				ICE_CLK	I	MFP14	Serial wired debugger clock pin.
			67	PD.9	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD7	I/O	MFP2	EBI address/data bus bit 7.
				I2C2_SCL	I/O	MFP3	I2C2 clock pin.
				UART2_nCTS	I	MFP4	UART2 clear to Send input pin.
			68	PD.8	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD6	I/O	MFP2	EBI address/data bus bit 6.
				I2C2_SDA	I/O	MFP3	I2C2 data input/output pin.
				UART2_nRTS	O	MFP4	UART2 request to Send output pin.
		35	69	PC.5	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD5	I/O	MFP2	EBI address/data bus bit 5.
				QSPI0_MISO1	I/O	MFP4	Quad SPI0 MISO1 (Master In, Slave Out) pin.
				UART2_TXD	O	MFP8	UART2 data transmitter output pin.
				I2C1_SCL	I/O	MFP9	I2C1 clock pin.
				CAN0_TXD	O	MFP10	CAN0 bus transmitter output.
				UART4_TXD	O	MFP11	UART4 data transmitter output pin.
				EPWM1_CH0	I/O	MFP12	EPWM1 channel 0 output/capture input.
		36	70	PC.4	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD4	I/O	MFP2	EBI address/data bus bit 4.
				QSPI0_MOSI1	I/O	MFP4	Quad SPI0 MOSI1 (Master Out, Slave In) pin.
				SC1_nCD	I	MFP5	Smart Card 1 card detect pin.
				I2S0_BCLK	O	MFP6	I2S0 bit clock output pin.
				SPI1_I2SMCLK	I/O	MFP7	SPI1 I2S master clock output pin
				UART2_RXD	I	MFP8	UART2 data receiver input pin.
				I2C1_SDA	I/O	MFP9	I2C1 data input/output pin.
				CAN0_RXD	I	MFP10	CAN0 bus receiver input.
				UART4_RXD	I	MFP11	UART4 data receiver input pin.
				EPWM1_CH1	I/O	MFP12	EPWM1 channel 1 output/capture input.
		37	71	PC.3	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD3	I/O	MFP2	EBI address/data bus bit 3.
				QSPI0_SS	I/O	MFP4	Quad SPI0 slave select pin.
				SC1_PWR	O	MFP5	Smart Card 1 power pin.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
				I2S0_MCLK	O	MFP6	I2S0 master clock output pin.
				SPI1_MISO	I/O	MFP7	SPI1 MISO (Master In, Slave Out) pin.
				UART2_nRTS	O	MFP8	UART2 request to Send output pin.
				I2C0_SMBAL	O	MFP9	I2C0 SMBus SMBALTER pin
				UART3_TXD	O	MFP11	UART3 data transmitter output pin.
				EPWM1_CH2	I/O	MFP12	EPWM1 channel 2 output/capture input.
		38	72	PC.2	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD2	I/O	MFP2	EBI address/data bus bit 2.
				QSPI0_CLK	I/O	MFP4	Quad SPI0 serial clock pin.
				SC1_RST	O	MFP5	Smart Card 1 reset pin.
				I2S0_DI	I	MFP6	I2S0 data input pin.
				SPI1_MOSI	I/O	MFP7	SPI1 MOSI (Master Out, Slave In) pin.
				UART2_nCTS	I	MFP8	UART2 clear to Send input pin.
				I2C0_SMBSUS	O	MFP9	I2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
				UART3_RXD	I	MFP11	UART3 data receiver input pin.
				EPWM1_CH3	I/O	MFP12	EPWM1 channel 3 output/capture input.
19	A4	39	73	PC.1	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD1	I/O	MFP2	EBI address/data bus bit 1.
				QSPI0_MISO0	I/O	MFP4	Quad SPI0 MISO0 (Master In, Slave Out) pin.
				SC1_DAT	I/O	MFP5	Smart Card 1 data pin.
				I2S0_DO	O	MFP6	I2S0 data output pin.
				SPI1_CLK	I/O	MFP7	SPI1 serial clock pin.
				UART2_TXD	O	MFP8	UART2 data transmitter output pin.
				I2C0_SCL	I/O	MFP9	I2C0 clock pin.
				EPWM1_CH4	I/O	MFP12	EPWM1 channel 4 output/capture input.
				ACMP0_O	O	MFP14	Analog comparator 0 output pin.
20	A3	40	74	PC.0	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD0	I/O	MFP2	EBI address/data bus bit 0.
				QSPI0_MOSI0	I/O	MFP4	Quad SPI0 MOSI0 (Master Out, Slave In) pin.
				SC1_CLK	O	MFP5	Smart Card 1 clock pin.
				I2S0_LRCK	O	MFP6	I2S0 left right channel clock output pin.
				SPI1_SS	I/O	MFP7	SPI1 slave select pin.
				UART2_RXD	I	MFP8	UART2 data receiver input pin.
				I2C0_SDA	I/O	MFP9	I2C0 data input/output pin.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
				EPWM1_CH5	I/O	MFP12	EPWM1 channel 5 output/capture input.
				ACMP1_O	O	MFP14	Analog comparator 1 output pin.
			75	V_{SS}	P	MFP0	Ground pin for digital circuit.
			76	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
			77	PG.9	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD0	I/O	MFP2	EBI address/data bus bit 0.
				BPWM0_CH5	I/O	MFP12	BPWM0 channel 5 output/capture input.
			78	PG.10	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD1	I/O	MFP2	EBI address/data bus bit 1.
				BPWM0_CH4	I/O	MFP12	BPWM0 channel 4 output/capture input.
			79	PG.11	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD2	I/O	MFP2	EBI address/data bus bit 2.
				BPWM0_CH3	I/O	MFP12	BPWM0 channel 3 output/capture input.
			80	PG.12	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD3	I/O	MFP2	EBI address/data bus bit 3.
				BPWM0_CH2	I/O	MFP12	BPWM0 channel 2 output/capture input.
			81	PG.13	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD4	I/O	MFP2	EBI address/data bus bit 4.
				BPWM0_CH1	I/O	MFP12	BPWM0 channel 1 output/capture input.
			82	PG.14	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD5	I/O	MFP2	EBI address/data bus bit 5.
				BPWM0_CH0	I/O	MFP12	BPWM0 channel 0 output/capture input.
			83	PG.15	I/O	MFP0	General purpose digital I/O pin.
				CLKO	O	MFP14	Clock Out
				EADC0_ST	I	MFP15	EADC0 external trigger input.
			84	PD.7	I/O	MFP0	General purpose digital I/O pin.
				UART1_TXD	O	MFP3	UART1 data transmitter output pin.
				I2C0_SCL	I/O	MFP4	I2C0 clock pin.
				SPI1_MISO	I/O	MFP5	SPI1 MISO (Master In, Slave Out) pin.
				USCI1_CLK	I/O	MFP6	USCI1 clock pin.
				SC1_PWR	O	MFP8	Smart Card 1 power pin.
			85	PD.6	I/O	MFP0	General purpose digital I/O pin.
				UART1_RXD	I	MFP3	UART1 data receiver input pin.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
				I2C0_SDA	I/O	MFP4	I2C0 data input/output pin.
				SPI1_MOSI	I/O	MFP5	SPI1 MOSI (Master Out, Slave In) pin.
				USCI1_DAT1	I/O	MFP6	USCI1 data 1 pin.
				SC1_RST	O	MFP8	Smart Card 1 reset pin.
			86	PD.5	I/O	MFP0	General purpose digital I/O pin.
				I2C1_SCL	I/O	MFP4	I2C1 clock pin.
				SPI1_CLK	I/O	MFP5	SPI1 serial clock pin.
				USCI1_DAT0	I/O	MFP6	USCI1 data 0 pin.
				SC1_DAT	I/O	MFP8	Smart Card 1 data pin.
			87	PD.4	I/O	MFP0	General purpose digital I/O pin.
				USCI0_CTL0	I/O	MFP3	USCI0 control 0 pin.
				I2C1_SDA	I/O	MFP4	I2C1 data input/output pin.
				SPI1_SS	I/O	MFP5	SPI1 slave select pin.
				USCI1_CTL1	I/O	MFP6	USCI1 control 1 pin.
				SC1_CLK	O	MFP8	Smart Card 1 clock pin.
				USB_VBUS_ST	I	MFP14	USB external VBUS regulator status pin.
		41	88	PD.3	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD10	I/O	MFP2	EBI address/data bus bit 10.
				USCI0_CTL1	I/O	MFP3	USCI0 control 1 pin.
				SPI0_SS	I/O	MFP4	SPI0 slave select pin.
				UART3_nRTS	O	MFP5	UART3 request to Send output pin.
				USCI1_CTL0	I/O	MFP6	USCI1 control 0 pin.
				SC2_PWR	O	MFP7	Smart Card 2 power pin.
				SC1_nCD	I	MFP8	Smart Card 1 card detect pin.
				UART0_TXD	O	MFP9	UART0 data transmitter output pin.
		42	89	PD.2	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD11	I/O	MFP2	EBI address/data bus bit 11.
				USCI0_DAT1	I/O	MFP3	USCI0 data 1 pin.
				SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
				UART3_nCTS	I	MFP5	UART3 clear to Send input pin.
				SC2_RST	O	MFP7	Smart Card 2 reset pin.
				UART0_RXD	I	MFP9	UART0 data receiver input pin.
		43	90	PD.1	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD12	I/O	MFP2	EBI address/data bus bit 12.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
				USCI0_DAT0	I/O	MFP3	USCI0 data 0 pin.
				SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
				UART3_TXD	O	MFP5	UART3 data transmitter output pin.
				I2C2_SCL	I/O	MFP6	I2C2 clock pin.
				SC2_DAT	I/O	MFP7	Smart Card 2 data pin.
		44	91	PD.0	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD13	I/O	MFP2	EBI address/data bus bit 13.
				USCI0_CLK	I/O	MFP3	USCI0 clock pin.
				SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
				UART3_RXD	I	MFP5	UART3 data receiver input pin.
				I2C2_SDA	I/O	MFP6	I2C2 data input/output pin.
				SC2_CLK	O	MFP7	Smart Card 2 clock pin.
				TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
			92	PD.13	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD10	I/O	MFP2	EBI address/data bus bit 10.
				SD0_nCD	I	MFP3	SD/SDIO0 card detect input pin
				SPI0_I2SMCLK	I/O	MFP4	SPI0 I2S master clock output pin
				SPI1_I2SMCLK	I/O	MFP5	SPI1 I2S master clock output pin
				SC2_nCD	I	MFP7	Smart Card 2 card detect pin.
21	B6	45	93	PA.12	I/O	MFP0	General purpose digital I/O pin.
				I2S0_BCLK	O	MFP2	I2S0 bit clock output pin.
				UART4_TXD	O	MFP3	UART4 data transmitter output pin.
				I2C1_SCL	I/O	MFP4	I2C1 clock pin.
				SPI2_SS	I/O	MFP5	SPI2 slave select pin.
				CAN0_TXD	O	MFP6	CAN0 bus transmitter output.
				SC2_PWR	O	MFP7	Smart Card 2 power pin.
				BPWM1_CH2	I/O	MFP11	BPWM1 channel 2 output/capture input.
				QEI1_INDEX	I	MFP12	Quadrature encoder 1 index input
				USB_VBUS	P	MFP14	Power supply from USB host or HUB.
22	A6	46	94	PA.13	I/O	MFP0	General purpose digital I/O pin.
				I2S0_MCLK	O	MFP2	I2S0 master clock output pin.
				UART4_RXD	I	MFP3	UART4 data receiver input pin.
				I2C1_SDA	I/O	MFP4	I2C1 data input/output pin.
				SPI2_CLK	I/O	MFP5	SPI2 serial clock pin.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
				CAN0_RXD	I	MFP6	CAN0 bus receiver input.
				SC2_RST	O	MFP7	Smart Card 2 reset pin.
				BPWM1_CH3	I/O	MFP11	BPWM1 channel 3 output/capture input.
				QEI1_A	I	MFP12	Quadrature encoder 1 phase A input
				USB_D-	A	MFP14	USB differential signal D-.
23	A7	47	95	PA.14	I/O	MFP0	General purpose digital I/O pin.
				I2S0_DI	I	MFP2	I2S0 data input pin.
				UART0_TXD	O	MFP3	UART0 data transmitter output pin.
				SPI2_MISO	I/O	MFP5	SPI2 MISO (Master In, Slave Out) pin.
				I2C2_SCL	I/O	MFP6	I2C2 clock pin.
				SC2_DAT	I/O	MFP7	Smart Card 2 data pin.
				BPWM1_CH4	I/O	MFP11	BPWM1 channel 4 output/capture input.
				QEI1_B	I	MFP12	Quadrature encoder 1 phase B input
				USB_D+	A	MFP14	USB differential signal D+.
24	A5	48	96	PA.15	I/O	MFP0	General purpose digital I/O pin.
				I2S0_DO	O	MFP2	I2S0 data output pin.
				UART0_RXD	I	MFP3	UART0 data receiver input pin.
				SPI2_MOSI	I/O	MFP5	SPI2 MOSI (Master Out, Slave In) pin.
				I2C2_SDA	I/O	MFP6	I2C2 data input/output pin.
				SC2_CLK	O	MFP7	Smart Card 2 clock pin.
				BPWM1_CH5	I/O	MFP11	BPWM1 channel 5 output/capture input.
				EPWM0_SYNC_IN	I	MFP12	EPWM0 counter synchronous trigger input pin.
				USB_OTG_ID	I	MFP14	USB_ identification.
			97	PE.7	I/O	MFP0	General purpose digital I/O pin.
				SD0_CMD	I/O	MFP3	SD/SDIO0 command/response pin
				UART5_TXD	O	MFP8	UART5 data transmitter output pin.
				QEI1_INDEX	I	MFP11	Quadrature encoder 1 index input
				EPWM0_CH0	I/O	MFP12	EPWM0 channel 0 output/capture input.
				BPWM0_CH5	I/O	MFP13	BPWM0 channel 5 output/capture input.
			98	PE.6	I/O	MFP0	General purpose digital I/O pin.
				SD0_CLK	O	MFP3	SD/SDIO0 clock output pin
				SPI3_I2SMCLK	I/O	MFP5	SPI3 I2S master clock output pin
				SC0_nCD	I	MFP6	Smart Card 0 card detect pin.
				USCI0_CTL0	I/O	MFP7	USCI0 control 0 pin.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
				UART5_RXD	I	MFP8	UART5 data receiver input pin.
				QEI1_A	I	MFP11	Quadrature encoder 1 phase A input
				EPWM0_CH1	I/O	MFP12	EPWM0 channel 1 output/capture input.
				BPWM0_CH4	I/O	MFP13	BPWM0 channel 4 output/capture input.
			99	PE.5	I/O	MFP0	General purpose digital I/O pin.
				EBI_nRD	O	MFP2	EBI read enable output pin.
				SD0_DAT3	I/O	MFP3	SD/SDIO0 data line bit 3.
				SPI3_SS	I/O	MFP5	SPI3 slave select pin.
				SC0_PWR	O	MFP6	Smart Card 0 power pin.
				USCI0_CTL1	I/O	MFP7	USCI0 control 1 pin.
				QEI1_B	I	MFP11	Quadrature encoder 1 phase B input
				EPWM0_CH2	I/O	MFP12	EPWM0 channel 2 output/capture input.
				BPWM0_CH3	I/O	MFP13	BPWM0 channel 3 output/capture input.
			100	PE.4	I/O	MFP0	General purpose digital I/O pin.
				EBI_nWR	O	MFP2	EBI write enable output pin.
				SD0_DAT2	I/O	MFP3	SD/SDIO0 data line bit 2.
				SPI3_CLK	I/O	MFP5	SPI3 serial clock pin.
				SC0_RST	O	MFP6	Smart Card 0 reset pin.
				USCI0_DAT1	I/O	MFP7	USCI0 data 1 pin.
				QEI0_INDEX	I	MFP11	Quadrature encoder 0 index input
				EPWM0_CH3	I/O	MFP12	EPWM0 channel 3 output/capture input.
				BPWM0_CH2	I/O	MFP13	BPWM0 channel 2 output/capture input.
			101	PE.3	I/O	MFP0	General purpose digital I/O pin.
				EBI_MCLK	O	MFP2	EBI external clock output pin.
				SD0_DAT1	I/O	MFP3	SD/SDIO0 data line bit 1.
				SPI3_MISO	I/O	MFP5	SPI3 MISO (Master In, Slave Out) pin.
				SC0_DAT	I/O	MFP6	Smart Card 0 data pin.
				USCI0_DAT0	I/O	MFP7	USCI0 data 0 pin.
				QEI0_A	I	MFP11	Quadrature encoder 0 phase A input
				EPWM0_CH4	I/O	MFP12	EPWM0 channel 4 output/capture input.
				BPWM0_CH1	I/O	MFP13	BPWM0 channel 1 output/capture input.
			102	PE.2	I/O	MFP0	General purpose digital I/O pin.
				EBI_ALE	O	MFP2	EBI address latch enable output pin.
				SD0_DAT0	I/O	MFP3	SD/SDIO0 data line bit 0.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
				SPI3_MOSI	I/O	MFP5	SPI3 MOSI (Master Out, Slave In) pin.
				SC0_CLK	O	MFP6	Smart Card 0 clock pin.
				USCI0_CLK	I/O	MFP7	USCI0 clock pin.
				QEI0_B	I	MFP11	Quadrature encoder 0 phase B input
				EPWM0_CH5	I/O	MFP12	EPWM0 channel 5 output/capture input.
				BPWM0_CH0	I/O	MFP13	BPWM0 channel 0 output/capture input.
			103	V_{SS}	P	MFP0	Ground pin for digital circuit.
			104	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
			105	PE.1	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD10	I/O	MFP2	EBI address/data bus bit 10.
				QSPI0_MISO0	I/O	MFP3	Quad SPI0 MISO0 (Master In, Slave Out) pin.
				SC2_DAT	I/O	MFP4	Smart Card 2 data pin.
				I2S0_BCLK	O	MFP5	I2S0 bit clock output pin.
				SPI1_MISO	I/O	MFP6	SPI1 MISO (Master In, Slave Out) pin.
				UART3_TXD	O	MFP7	UART3 data transmitter output pin.
				I2C1_SCL	I/O	MFP8	I2C1 clock pin.
				UART4_nCTS	I	MFP9	UART4 clear to Send input pin.
			106	PE.0	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD11	I/O	MFP2	EBI address/data bus bit 11.
				QSPI0_MOSI0	I/O	MFP3	Quad SPI0 MOSI0 (Master Out, Slave In) pin.
				SC2_CLK	O	MFP4	Smart Card 2 clock pin.
				I2S0_MCLK	O	MFP5	I2S0 master clock output pin.
				SPI1_MOSI	I/O	MFP6	SPI1 MOSI (Master Out, Slave In) pin.
				UART3_RXD	I	MFP7	UART3 data receiver input pin.
				I2C1_SDA	I/O	MFP8	I2C1 data input/output pin.
				UART4_nRTS	O	MFP9	UART4 request to Send output pin.
			107	PH.8	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD12	I/O	MFP2	EBI address/data bus bit 12.
				QSPI0_CLK	I/O	MFP3	Quad SPI0 serial clock pin.
				SC2_PWR	O	MFP4	Smart Card 2 power pin.
				I2S0_DI	I	MFP5	I2S0 data input pin.
				SPI1_CLK	I/O	MFP6	SPI1 serial clock pin.
				UART3_nRTS	O	MFP7	UART3 request to Send output pin.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
				I2C1_SMBAL	O	MFP8	I2C1 SMBus SMBALTER pin
				I2C2_SCL	I/O	MFP9	I2C2 clock pin.
				UART1_TXD	O	MFP10	UART1 data transmitter output pin.
			108	PH.9	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD13	I/O	MFP2	EBI address/data bus bit 13.
				QSPI0_SS	I/O	MFP3	Quad SPI0 slave select pin.
				SC2_RST	O	MFP4	Smart Card 2 reset pin.
				I2S0_DO	O	MFP5	I2S0 data output pin.
				SPI1_SS	I/O	MFP6	SPI1 slave select pin.
				UART3_nCTS	I	MFP7	UART3 clear to Send input pin.
				I2C1_SMBSUS	O	MFP8	I2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
				I2C2_SDA	I/O	MFP9	I2C2 data input/output pin.
				UART1_RXD	I	MFP10	UART1 data receiver input pin.
			109	PH.10	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD14	I/O	MFP2	EBI address/data bus bit 14.
				QSPI0_MISO1	I/O	MFP3	Quad SPI0 MISO1 (Master In, Slave Out) pin.
				SC2_nCD	I	MFP4	Smart Card 2 card detect pin.
				I2S0_LRCK	O	MFP5	I2S0 left right channel clock output pin.
				SPI1_I2SMCLK	I/O	MFP6	SPI1 I2S master clock output pin
				UART4_TXD	O	MFP7	UART4 data transmitter output pin.
				UART0_TXD	O	MFP8	UART0 data transmitter output pin.
			110	PH.11	I/O	MFP0	General purpose digital I/O pin.
				EBI_AD15	I/O	MFP2	EBI address/data bus bit 15.
				QSPI0_MOSI1	I/O	MFP3	Quad SPI0 MOSI1 (Master Out, Slave In) pin.
				UART4_RXD	I	MFP7	UART4 data receiver input pin.
				UART0_RXD	I	MFP8	UART0 data receiver input pin.
				EPWM0_CH5	I/O	MFP11	EPWM0 channel 5 output/capture input.
			111	PD.14	I/O	MFP0	General purpose digital I/O pin.
				EBI_nCS0	O	MFP2	EBI chip select 0 output pin.
				SPI3_I2SMCLK	I/O	MFP3	SPI3 I2S master clock output pin
				SC1_nCD	I	MFP4	Smart Card 1 card detect pin.
				USCI0_CTL0	I/O	MFP5	USCI0 control 0 pin.
				SPI0_I2SMCLK	I/O	MFP6	SPI0 I2S master clock output pin
				EPWM0_CH4	I/O	MFP11	EPWM0 channel 4 output/capture input.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
25	C7	49	112	V_{SS}	P	MFP0	Ground pin for digital circuit.
26	B7	50	113	Vsw		MFP0	
27	D7	51	114	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
28	C6	52	115	LDO_CAP	A	MFP0	LDO output pin.
	B5	53	116	PB.15	I/O	MFP0	General purpose digital I/O pin.
				EADC0_CH15	A	MFP1	EADC0 channel 15 analog input.
				EBI_AD12	I/O	MFP2	EBI address/data bus bit 12.
				SC1_PWR	O	MFP3	Smart Card 1 power pin.
				SPI0_SS	I/O	MFP4	SPI0 slave select pin.
				USCI0_CTL1	I/O	MFP5	USCI0 control 1 pin.
				UART0_nCTS	I	MFP6	UART0 clear to Send input pin.
				UART3_TXD	O	MFP7	UART3 data transmitter output pin.
				I2C2_SMBAL	O	MFP8	I2C2 SMBus SMBALTER pin
				EPWM1_CH0	I/O	MFP11	EPWM1 channel 0 output/capture input.
				TM0_EXT	I/O	MFP13	Timer0 external capture input/toggle output pin.
				USB_VBUS_EN	O	MFP14	USB external VBUS regulator enable pin.
29	B4	54	117	PB.14	I/O	MFP0	General purpose digital I/O pin.
				EADC0_CH14	A	MFP1	EADC0 channel 14 analog input.
				EBI_AD13	I/O	MFP2	EBI address/data bus bit 13.
				SC1_RST	O	MFP3	Smart Card 1 reset pin.
				SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
				USCI0_DAT1	I/O	MFP5	USCI0 data 1 pin.
				UART0_nRTS	O	MFP6	UART0 request to Send output pin.
				UART3_RXD	I	MFP7	UART3 data receiver input pin.
				I2C2_SMBSUS	O	MFP8	I2C2 SMBus SMBSUS pin (PMBus CONTROL pin)
				EPWM1_CH1	I/O	MFP11	EPWM1 channel 1 output/capture input.
				TM1_EXT	I/O	MFP13	Timer1 external capture input/toggle output pin.
				CLKO	O	MFP14	Clock Out
				USB_VBUS_ST	I	MFP15	USB external VBUS regulator status pin.
30	E7	55	118	PB.13	I/O	MFP0	General purpose digital I/O pin.
				EADC0_CH13	A	MFP1	EADC0 channel 13 analog input.
				DAC1_OUT	A	MFP1	DAC1 channel analog output.
				ACMP0_P3	A	MFP1	Analog comparator 0 positive input 3 pin.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
				ACMP1_P3	A	MFP1	Analog comparator 1 positive input 3 pin.
				EBI_AD14	I/O	MFP2	EBI address/data bus bit 14.
				SC1_DAT	I/O	MFP3	Smart Card 1 data pin.
				SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
				USCI0_DAT0	I/O	MFP5	USCI0 data 0 pin.
				UART0_TXD	O	MFP6	UART0 data transmitter output pin.
				UART3_nRTS	O	MFP7	UART3 request to Send output pin.
				I2C2_SCL	I/O	MFP8	I2C2 clock pin.
				EPWM1_CH2	I/O	MFP11	EPWM1 channel 2 output/capture input.
				TM2_EXT	I/O	MFP13	Timer2 external capture input/toggle output pin.
31	D6	56	119	PB.12	I/O	MFP0	General purpose digital I/O pin.
				EADC0_CH12	A	MFP1	EADC0 channel 12 analog input.
				DAC0_OUT	A	MFP1	DAC0 channel analog output.
				ACMP0_P2	A	MFP1	Analog comparator 0 positive input 2 pin.
				ACMP1_P2	A	MFP1	Analog comparator 1 positive input 2 pin.
				EBI_AD15	I/O	MFP2	EBI address/data bus bit 15.
				SC1_CLK	O	MFP3	Smart Card 1 clock pin.
				SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
				USCI0_CLK	I/O	MFP5	USCI0 clock pin.
				UART0_RXD	I	MFP6	UART0 data receiver input pin.
				UART3_nCTS	I	MFP7	UART3 clear to Send input pin.
				I2C2_SDA	I/O	MFP8	I2C2 data input/output pin.
				SD0_nCD	I	MFP9	SD/SDIO0 card detect input pin
				EPWM1_CH3	I/O	MFP11	EPWM1 channel 3 output/capture input.
				TM3_EXT	I/O	MFP13	Timer3 external capture input/toggle output pin.
32	E6	57	120	AV_{DD}	P	MFP0	Power supply for internal analog circuit.
	F6	58	121	V_{REF}	A	MFP0	ADC reference voltage input. Note: This pin needs to be connected with a 1uF capacitor.
	F7	59	122	AV_{SS}	P	MFP0	Ground pin for analog circuit.
	C5	60	123	PB.11	I/O	MFP0	General purpose digital I/O pin.
				EADC0_CH11	A	MFP1	EADC0 channel 11 analog input.
				EBI_ADR16	O	MFP2	EBI address bus bit 16.
				UART0_nCTS	I	MFP5	UART0 clear to Send input pin.
				UART4_TXD	O	MFP6	UART4 data transmitter output pin.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
				I2C1_SCL	I/O	MFP7	I2C1 clock pin.
				CAN0_TXD	O	MFP8	CAN0 bus transmitter output.
				SPI0_I2SMCLK	I/O	MFP9	SPI0 I2S master clock output pin
				BPWM1_CH0	I/O	MFP10	BPWM1 channel 0 output/capture input.
				SPI3_CLK	I/O	MFP11	SPI3 serial clock pin.
	D5	61	124	PB.10	I/O	MFP0	General purpose digital I/O pin.
				EADC0_CH10	A	MFP1	EADC0 channel 10 analog input.
				EBI_ADR17	O	MFP2	EBI address bus bit 17.
				USCI1_CTL0	I/O	MFP4	USCI1 control 0 pin.
				UART0_nRTS	O	MFP5	UART0 request to Send output pin.
				UART4_RXD	I	MFP6	UART4 data receiver input pin.
				I2C1_SDA	I/O	MFP7	I2C1 data input/output pin.
				CAN0_RXD	I	MFP8	CAN0 bus receiver input.
				BPWM1_CH1	I/O	MFP10	BPWM1 channel 1 output/capture input.
				SPI3_SS	I/O	MFP11	SPI3 slave select pin.
	C4	62	125	PB.9	I/O	MFP0	General purpose digital I/O pin.
				EADC0_CH9	A	MFP1	EADC0 channel 9 analog input.
				EBI_ADR18	O	MFP2	EBI address bus bit 18.
				USCI1_CTL1	I/O	MFP4	USCI1 control 1 pin.
				UART0_TXD	O	MFP5	UART0 data transmitter output pin.
				UART1_nCTS	I	MFP6	UART1 clear to Send input pin.
				I2C1_SMBAL	O	MFP7	I2C1 SMBus SMBALTER pin
				BPWM1_CH2	I/O	MFP10	BPWM1 channel 2 output/capture input.
				SPI3_MISO	I/O	MFP11	SPI3 MISO (Master In, Slave Out) pin.
				INT7	I	MFP13	External interrupt 7 input pin.
	D4	63	126	PB.8	I/O	MFP0	General purpose digital I/O pin.
				EADC0_CH8	A	MFP1	EADC0 channel 8 analog input.
				EBI_ADR19	O	MFP2	EBI address bus bit 19.
				USCI1_CLK	I/O	MFP4	USCI1 clock pin.
				UART0_RXD	I	MFP5	UART0 data receiver input pin.
				UART1_nRTS	O	MFP6	UART1 request to Send output pin.
				I2C1_SMBSUS	O	MFP7	I2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
				BPWM1_CH3	I/O	MFP10	BPWM1 channel 3 output/capture input.
				SPI3_MOSI	I/O	MFP11	SPI3 MOSI (Master Out, Slave In) pin.

33 Pin	49 Pin	64 Pin	128 Pin	Pin Name	Type	MFP	Description
				INT6	I	MFP13	External interrupt 6 input pin.
	G7	64	127	PB.7	I/O	MFP0	General purpose digital I/O pin.
				EADC0_CH7	A	MFP1	EADC0 channel 7 analog input.
				EBI_nWRL	O	MFP2	EBI low byte write enable output pin.
				USCI1_DAT0	I/O	MFP4	USCI1 data 0 pin.
				UART1_TXD	O	MFP6	UART1 data transmitter output pin.
				EBI_nCS0	O	MFP8	EBI chip select 0 output pin.
				BPWM1_CH4	I/O	MFP10	BPWM1 channel 4 output/capture input.
				EPWM1_BRAKE0	I	MFP11	EPWM1 Brake 0 input pin.
				EPWM1_CH4	I/O	MFP12	EPWM1 channel 4 output/capture input.
				INT5	I	MFP13	External interrupt 5 input pin.
				USB_VBUS_ST	I	MFP14	USB external VBUS regulator status pin.
				ACMP0_O	O	MFP15	Analog comparator 0 output pin.
	E5	1	128	PB.6	I/O	MFP0	General purpose digital I/O pin.
				EADC0_CH6	A	MFP1	EADC0 channel 6 analog input.
				EBI_nWRH	O	MFP2	EBI high byte write enable output pin
				USCI1_DAT1	I/O	MFP4	USCI1 data 1 pin.
				UART1_RXD	I	MFP6	UART1 data receiver input pin.
				EBI_nCS1	O	MFP8	EBI chip select 1 output pin.
				BPWM1_CH5	I/O	MFP10	BPWM1 channel 5 output/capture input.
				EPWM1_BRAKE1	I	MFP11	EPWM1 Brake 1 input pin.
				EPWM1_CH5	I/O	MFP12	EPWM1 channel 5 output/capture input.
				INT4	I	MFP13	External interrupt 4 input pin.
				USB_VBUS_EN	O	MFP14	USB external VBUS regulator enable pin.
				ACMP1_O	O	MFP15	Analog comparator 1 output pin.

M2351 Multi-function Summary Table

Group	Pin Name	GPIO	MFP	Type	Description
ACMP0	ACMP0_N	PB.3	MFP1	A	Analog comparator 0 negative input pin.
	ACMP0_O	PC.12	MFP14	O	Analog comparator 0 output pin.
		PC.1	MFP14	O	
		PB.7	MFP15	O	
	ACMP0_P0	PA.11	MFP1	A	Analog comparator 0 positive input 0 pin.
	ACMP0_P1	PB.2	MFP1	A	Analog comparator 0 positive input 1 pin.

Group	Pin Name	GPIO	MFP	Type	Description
	ACMP0_P2	PB.12	MFP1	A	Analog comparator 0 positive input 2 pin.
	ACMP0_P3	PB.13	MFP1	A	Analog comparator 0 positive input 3 pin.
	ACMP0_WLAT	PA.7	MFP13	I	Analog comparator 0 window latch input pin
ACMP1	ACMP1_N	PB.5	MFP1	A	Analog comparator 1 negative input pin.
	ACMP1_O	PB.6	MFP15	O	Analog comparator 1 output pin.
		PC.11	MFP14	O	
		PC.0	MFP14	O	
	ACMP1_P0	PA.10	MFP1	A	Analog comparator 1 positive input 0 pin.
	ACMP1_P1	PB.4	MFP1	A	Analog comparator 1 positive input 1 pin.
	ACMP1_P2	PB.12	MFP1	A	Analog comparator 1 positive input 2 pin.
	ACMP1_P3	PB.13	MFP1	A	Analog comparator 1 positive input 3 pin.
	ACMP1_WLAT	PA.6	MFP13	I	Analog comparator 1 window latch input pin
BPWM0	BPWM0_CH0	PA.11	MFP9	I/O	BPWM0 channel 0 output/capture input.
		PA.0	MFP12	I/O	
		PG.14	MFP12	I/O	
		PE.2	MFP13	I/O	
	BPWM0_CH1	PA.10	MFP9	I/O	BPWM0 channel 1 output/capture input.
		PA.1	MFP12	I/O	
		PG.13	MFP12	I/O	
		PE.3	MFP13	I/O	
	BPWM0_CH2	PA.9	MFP9	I/O	BPWM0 channel 2 output/capture input.
		PA.2	MFP12	I/O	
		PG.12	MFP12	I/O	
		PE.4	MFP13	I/O	
	BPWM0_CH3	PA.8	MFP9	I/O	BPWM0 channel 3 output/capture input.
		PA.3	MFP12	I/O	
		PG.11	MFP12	I/O	
		PE.5	MFP13	I/O	
	BPWM0_CH4	PC.13	MFP9	I/O	BPWM0 channel 4 output/capture input.
		PF.5	MFP8	I/O	
		PA.4	MFP12	I/O	
		PG.10	MFP12	I/O	
		PE.6	MFP13	I/O	
	BPWM0_CH5	PD.12	MFP9	I/O	BPWM0 channel 5 output/capture input.

Group	Pin Name	GPIO	MFP	Type	Description
		PF.4	MFP8	I/O	
		PA.5	MFP12	I/O	
		PG.9	MFP12	I/O	
		PE.7	MFP13	I/O	
BPWM1	BPWM1_CH0	PF.3	MFP11	I/O	BPWM1 channel 0 output/capture input.
		PC.7	MFP12	I/O	
		PF.0	MFP12	I/O	
		PB.11	MFP10	I/O	
	BPWM1_CH1	PF.2	MFP11	I/O	BPWM1 channel 1 output/capture input.
		PC.6	MFP12	I/O	
		PF.1	MFP12	I/O	
		PB.10	MFP10	I/O	
	BPWM1_CH2	PA.7	MFP12	I/O	BPWM1 channel 2 output/capture input.
		PA.12	MFP11	I/O	
		PB.9	MFP10	I/O	
	BPWM1_CH3	PA.6	MFP12	I/O	BPWM1 channel 3 output/capture input.
		PA.13	MFP11	I/O	
		PB.8	MFP10	I/O	
	BPWM1_CH4	PC.8	MFP12	I/O	BPWM1 channel 4 output/capture input.
		PA.14	MFP11	I/O	
		PB.7	MFP10	I/O	
	BPWM1_CH5	PB.6	MFP10	I/O	BPWM1 channel 5 output/capture input.
		PE.13	MFP12	I/O	
		PA.15	MFP11	I/O	
CAN0	CAN0_RXD	PD.10	MFP4	I	CAN0 bus receiver input.
		PA.4	MFP10	I	
		PE.15	MFP4	I	
		PC.4	MFP10	I	
		PA.13	MFP6	I	
		PB.10	MFP8	I	
	CAN0_TXD	PD.11	MFP4	O	CAN0 bus transmitter output.
		PA.5	MFP10	O	
		PE.14	MFP4	O	
		PC.5	MFP10	O	

Group	Pin Name	GPIO	MFP	Type	Description
		PA.12	MFP6	O	
		PB.11	MFP8	O	
CLKO	CLKO	PC.13	MFP13	O	Clock Out
		PD.12	MFP13	O	
		PG.15	MFP14	O	
		PB.14	MFP14	O	
DAC0	DAC0_OUT	PB.12	MFP1	A	DAC0 channel analog output.
	DAC0_ST	PA.10	MFP14	I	DAC0 external trigger input.
		PA.0	MFP15	I	
DAC1	DAC1_OUT	PB.13	MFP1	A	DAC1 channel analog output.
	DAC1_ST	PA.11	MFP14	I	DAC1 external trigger input.
		PA.1	MFP15	I	
EADC0	EADC0_CH0	PB.0	MFP1	A	EADC0 channel 0 analog input.
	EADC0_CH1	PB.1	MFP1	A	EADC0 channel 1 analog input.
	EADC0_CH2	PB.2	MFP1	A	EADC0 channel 2 analog input.
	EADC0_CH3	PB.3	MFP1	A	EADC0 channel 3 analog input.
	EADC0_CH4	PB.4	MFP1	A	EADC0 channel 4 analog input.
	EADC0_CH5	PB.5	MFP1	A	EADC0 channel 5 analog input.
	EADC0_CH6	PB.6	MFP1	A	EADC0 channel 6 analog input.
	EADC0_CH7	PB.7	MFP1	A	EADC0 channel 7 analog input.
	EADC0_CH8	PB.8	MFP1	A	EADC0 channel 8 analog input.
	EADC0_CH9	PB.9	MFP1	A	EADC0 channel 9 analog input.
	EADC0_CH10	PB.10	MFP1	A	EADC0 channel 10 analog input.
	EADC0_CH11	PB.11	MFP1	A	EADC0 channel 11 analog input.
	EADC0_CH12	PB.12	MFP1	A	EADC0 channel 12 analog input.
	EADC0_CH13	PB.13	MFP1	A	EADC0 channel 13 analog input.
	EADC0_CH14	PB.14	MFP1	A	EADC0 channel 14 analog input.
	EADC0_CH15	PB.15	MFP1	A	EADC0 channel 15 analog input.
	EADC0_ST	PC.13	MFP14	I	EADC0 external trigger input.
		PD.12	MFP14	I	
		PF.5	MFP11	I	
		PG.15	MFP15	I	
EBI	EBI_AD0	PC.0	MFP2	I/O	EBI address/data bus bit 0.
		PG.9	MFP2	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
	EBI_AD1	PC.1	MFP2	I/O	EBI address/data bus bit 1.
		PG.10	MFP2	I/O	
	EBI_AD2	PC.2	MFP2	I/O	EBI address/data bus bit 2.
		PG.11	MFP2	I/O	
	EBI_AD3	PC.3	MFP2	I/O	EBI address/data bus bit 3.
		PG.12	MFP2	I/O	
	EBI_AD4	PC.4	MFP2	I/O	EBI address/data bus bit 4.
		PG.13	MFP2	I/O	
	EBI_AD5	PC.5	MFP2	I/O	EBI address/data bus bit 5.
		PG.14	MFP2	I/O	
	EBI_AD6	PA.6	MFP2	I/O	EBI address/data bus bit 6.
		PD.8	MFP2	I/O	
	EBI_AD7	PA.7	MFP2	I/O	EBI address/data bus bit 7.
		PD.9	MFP2	I/O	
	EBI_AD8	PC.6	MFP2	I/O	EBI address/data bus bit 8.
		PE.14	MFP2	I/O	
	EBI_AD9	PC.7	MFP2	I/O	EBI address/data bus bit 9.
		PE.15	MFP2	I/O	
	EBI_AD10	PD.3	MFP2	I/O	EBI address/data bus bit 10.
		PD.13	MFP2	I/O	
		PE.1	MFP2	I/O	
	EBI_AD11	PD.2	MFP2	I/O	EBI address/data bus bit 11.
		PE.0	MFP2	I/O	
	EBI_AD12	PD.1	MFP2	I/O	EBI address/data bus bit 12.
		PH.8	MFP2	I/O	
		PB.15	MFP2	I/O	
	EBI_AD13	PD.0	MFP2	I/O	EBI address/data bus bit 13.
		PH.9	MFP2	I/O	
		PB.14	MFP2	I/O	
	EBI_AD14	PH.10	MFP2	I/O	EBI address/data bus bit 14.
		PB.13	MFP2	I/O	
	EBI_AD15	PH.11	MFP2	I/O	EBI address/data bus bit 15.
		PB.12	MFP2	I/O	
	EBI_ADR0	PB.5	MFP2	O	EBI address bus bit 0.

Group	Pin Name	GPIO	MFP	Type	Description
		PH.7	MFP2	O	
	EBI_ADR1	PB.4	MFP2	O	EBI address bus bit 1.
		PH.6	MFP2	O	
	EBI_ADR2	PB.3	MFP2	O	EBI address bus bit 2.
		PH.5	MFP2	O	
	EBI_ADR3	PB.2	MFP2	O	EBI address bus bit 3.
		PH.4	MFP2	O	
	EBI_ADR4	PC.12	MFP2	O	EBI address bus bit 4.
	EBI_ADR5	PC.11	MFP2	O	EBI address bus bit 5.
	EBI_ADR6	PC.10	MFP2	O	EBI address bus bit 6.
	EBI_ADR7	PC.9	MFP2	O	EBI address bus bit 7.
	EBI_ADR8	PB.1	MFP2	O	EBI address bus bit 8.
	EBI_ADR9	PB.0	MFP2	O	EBI address bus bit 9.
	EBI_ADR10	PC.13	MFP2	O	EBI address bus bit 10.
		PE.8	MFP2	O	
	EBI_ADR11	PG.2	MFP2	O	EBI address bus bit 11.
		PE.9	MFP2	O	
	EBI_ADR12	PG.3	MFP2	O	EBI address bus bit 12.
		PE.10	MFP2	O	
	EBI_ADR13	PG.4	MFP2	O	EBI address bus bit 13.
		PE.11	MFP2	O	
	EBI_ADR14	PF.11	MFP2	O	EBI address bus bit 14.
		PE.12	MFP2	O	
	EBI_ADR15	PF.10	MFP2	O	EBI address bus bit 15.
		PE.13	MFP2	O	
	EBI_ADR16	PF.9	MFP2	O	EBI address bus bit 16.
		PC.8	MFP2	O	
		PB.11	MFP2	O	
	EBI_ADR17	PF.8	MFP2	O	EBI address bus bit 17.
		PB.10	MFP2	O	
	EBI_ADR18	PF.7	MFP2	O	EBI address bus bit 18.
		PB.9	MFP2	O	
	EBI_ADR19	PF.6	MFP2	O	EBI address bus bit 19.
		PB.8	MFP2	O	

Group	Pin Name	GPIO	MFP	Type	Description
	EBI_ALE	PA.8	MFP2	O	EBI address latch enable output pin.
		PE.2	MFP2	O	
	EBI_MCLK	PA.9	MFP2	O	EBI external clock output pin.
		PE.3	MFP2	O	
	EBI_nCS0	PD.12	MFP2	O	EBI chip select 0 output pin.
		PF.6	MFP7	O	
		PF.3	MFP2	O	
		PD.14	MFP2	O	
		PB.7	MFP8	O	
	EBI_nCS1	PB.6	MFP8	O	EBI chip select 1 output pin.
		PD.11	MFP2	O	
		PF.2	MFP2	O	
	EBI_nCS2	PD.10	MFP2	O	EBI chip select 2 output pin.
	EBI_nRD	PA.11	MFP2	O	EBI read enable output pin.
		PE.5	MFP2	O	
	EBI_nWR	PA.10	MFP2	O	EBI write enable output pin.
		PE.4	MFP2	O	
	EBI_nWRH	PB.6	MFP2	O	EBI high byte write enable output pin
	EBI_nWRL	PB.7	MFP2	O	EBI low byte write enable output pin.
ECAP0	ECAP0_IC0	PA.10	MFP11	I	Enhanced capture unit 0 input 0 pin.
		PE.8	MFP12	I	
	ECAP0_IC1	PA.9	MFP11	I	Enhanced capture unit 0 input 1 pin.
		PE.9	MFP12	I	
	ECAP0_IC2	PA.8	MFP11	I	Enhanced capture unit 0 input 2 pin.
		PE.10	MFP12	I	
ECAP1	ECAP1_IC0	PC.10	MFP11	I	Enhanced capture unit 1 input 0 pin.
		PE.13	MFP13	I	
	ECAP1_IC1	PC.11	MFP11	I	Enhanced capture unit 1 input 1 pin.
		PE.12	MFP13	I	
	ECAP1_IC2	PC.12	MFP11	I	Enhanced capture unit 1 input 2 pin.
		PE.11	MFP13	I	
I2C0	I2C0_SCL	PB.5	MFP6	I/O	I2C0 clock pin.
		PC.12	MFP4	I/O	
		PF.3	MFP4	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PE.13	MFP4	I/O	
		PA.5	MFP9	I/O	
		PC.1	MFP9	I/O	
		PD.7	MFP4	I/O	
	I2C0_SDA	PB.4	MFP6	I/O	I2C0 data input/output pin.
		PC.11	MFP4	I/O	
		PF.2	MFP4	I/O	
		PC.8	MFP4	I/O	
		PA.4	MFP9	I/O	
		PC.0	MFP9	I/O	
		PD.6	MFP4	I/O	
	I2C0_SMBAL	PG.2	MFP4	O	I2C0 SMBus SMBALTER pin
		PC.3	MFP9	O	
	I2C0_SMBSUS	PG.3	MFP4	O	I2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
		PC.2	MFP9	O	
I2C1	I2C1_SCL	PB.1	MFP9	I/O	I2C1 clock pin.
		PG.2	MFP5	I/O	
		PA.7	MFP8	I/O	
		PA.3	MFP9	I/O	
		PF.0	MFP3	I/O	
		PC.5	MFP9	I/O	
		PD.5	MFP4	I/O	
		PA.12	MFP4	I/O	
		PE.1	MFP8	I/O	
		PB.11	MFP7	I/O	
	I2C1_SDA	PB.0	MFP9	I/O	I2C1 data input/output pin.
		PG.3	MFP5	I/O	
		PA.6	MFP8	I/O	
		PA.2	MFP9	I/O	
		PF.1	MFP3	I/O	
		PC.4	MFP9	I/O	
		PD.4	MFP4	I/O	
		PA.13	MFP4	I/O	
		PE.0	MFP8	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PB.10	MFP7	I/O	
	I2C1_SMBAL	PC.7	MFP8	O	I2C1 SMBus SMBALTER pin
		PH.8	MFP8	O	
		PB.9	MFP7	O	
	I2C1_SMBSUS	PC.6	MFP8	O	I2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
		PH.9	MFP8	O	
		PB.8	MFP7	O	
I2C2	I2C2_SCL	PA.11	MFP7	I/O	I2C2 clock pin.
		PA.1	MFP9	I/O	
		PD.9	MFP3	I/O	
		PD.1	MFP6	I/O	
		PA.14	MFP6	I/O	
		PH.8	MFP9	I/O	
		PB.13	MFP8	I/O	
	I2C2_SDA	PA.10	MFP7	I/O	I2C2 data input/output pin.
		PA.0	MFP9	I/O	
		PD.8	MFP3	I/O	
		PD.0	MFP6	I/O	
		PA.15	MFP6	I/O	
		PH.9	MFP9	I/O	
		PB.12	MFP8	I/O	
	I2C2_SMBAL	PB.15	MFP8	O	I2C2 SMBus SMBALTER pin
	I2C2_SMBSUS	PB.14	MFP8	O	I2C2 SMBus SMBSUS pin (PMBus CONTROL pin)
I2S0	I2S0_BCLK	PB.5	MFP10	O	I2S0 bit clock output pin.
		PF.10	MFP4	O	
		PE.8	MFP4	O	
		PC.4	MFP6	O	
		PA.12	MFP2	O	
		PE.1	MFP5	O	
	I2S0_DI	PB.3	MFP10	I	I2S0 data input pin.
		PF.8	MFP4	I	
		PE.10	MFP4	I	
		PC.2	MFP6	I	
		PA.14	MFP2	I	

Group	Pin Name	GPIO	MFP	Type	Description
		PH.8	MFP5	I	
	I2S0_DO	PB.2	MFP10	O	I2S0 data output pin.
		PF.7	MFP4	O	
		PE.11	MFP4	O	
		PC.1	MFP6	O	
		PA.15	MFP2	O	
		PH.9	MFP5	O	
	I2S0_LRCK	PB.1	MFP10	O	I2S0 left right channel clock output pin.
		PF.6	MFP4	O	
		PE.12	MFP4	O	
		PC.0	MFP6	O	
		PH.10	MFP5	O	
	I2S0_MCLK	PB.4	MFP10	O	I2S0 master clock output pin.
		PF.9	MFP4	O	
		PE.9	MFP4	O	
		PC.3	MFP6	O	
		PA.13	MFP2	O	
		PE.0	MFP5	O	
ICE	ICE_CLK	PF.1	MFP14	I	Serial wired debugger clock pin.
	ICE_DAT	PF.0	MFP14	O	Serial wired debugger data pin.
INT0	INT0	PB.5	MFP15	I	External interrupt 0 input pin.
		PA.6	MFP15	I	
INT1	INT1	PB.4	MFP15	I	External interrupt 1 input pin.
		PA.7	MFP15	I	
INT2	INT2	PB.3	MFP15	I	External interrupt 2 input pin.
		PC.6	MFP15	I	
INT3	INT3	PB.2	MFP15	I	External interrupt 3 input pin.
		PC.7	MFP15	I	
INT4	INT4	PB.6	MFP13	I	External interrupt 4 input pin.
		PA.8	MFP15	I	
INT5	INT5	PD.12	MFP15	I	External interrupt 5 input pin.
		PB.7	MFP13	I	
INT6	INT6	PD.11	MFP15	I	External interrupt 6 input pin.
		PB.8	MFP13	I	

Group	Pin Name	GPIO	MFP	Type	Description
INT7	INT7	PD.10	MFP15	I	External interrupt 7 input pin.
		PB.9	MFP13	I	
EPWM0	EPWM0_BRAKE0	PB.1	MFP13	I	EPWM0 Brake 0 input pin.
		PE.8	MFP11	I	
	EPWM0_BRAKE1	PB.0	MFP13	I	EPWM0 Brake 1 input pin.
		PE.9	MFP11	I	
	EPWM0_CH0	PB.5	MFP11	I/O	EPWM0 channel 0 output/capture input.
		PE.8	MFP10	I/O	
		PA.5	MFP13	I/O	
		PE.7	MFP12	I/O	
	EPWM0_CH1	PB.4	MFP11	I/O	EPWM0 channel 1 output/capture input.
		PE.9	MFP10	I/O	
		PA.4	MFP13	I/O	
		PE.6	MFP12	I/O	
	EPWM0_CH2	PB.3	MFP11	I/O	EPWM0 channel 2 output/capture input.
		PE.10	MFP10	I/O	
		PA.3	MFP13	I/O	
		PE.5	MFP12	I/O	
	EPWM0_CH3	PB.2	MFP11	I/O	EPWM0 channel 3 output/capture input.
		PE.11	MFP10	I/O	
		PA.2	MFP13	I/O	
		PE.4	MFP12	I/O	
	EPWM0_CH4	PB.1	MFP11	I/O	PWM0 channel 4 output/capture input.
		PE.12	MFP10	I/O	
		PA.1	MFP13	I/O	
		PE.3	MFP12	I/O	
		PD.14	MFP11	I/O	
	EPWM0_CH5	PB.0	MFP11	I/O	EPWM0 channel 5 output/capture input.
		PE.13	MFP10	I/O	
		PA.0	MFP13	I/O	
		PE.2	MFP12	I/O	
		PH.11	MFP11	I/O	
	EPWM0_SYNC_IN	PA.15	MFP12	I	EPWM0 counter synchronous trigger input pin.
	EPWM0_SYNC_OUT	PA.11	MFP10	O	EPWM0 counter synchronous trigger output

Group	Pin Name	GPIO	MFP	Type	Description
		PF.5	MFP9	O	pin.
PWM1	EPWM1_BRAKE0	PE.10	MFP11	I	EPWM1 Brake 0 input pin.
		PB.7	MFP11	I	
	EPWM1_BRAKE1	PB.6	MFP11	I	EPWM1 Brake 1 input pin.
		PE.11	MFP11	I	
	PWM1_CH0	PC.12	MFP12	I/O	EPWM1 channel 0 output/capture input.
		PE.13	MFP11	I/O	
		PC.5	MFP12	I/O	
		PB.15	MFP11	I/O	
	EPWM1_CH1	PC.11	MFP12	I/O	PWM1 channel 1 output/capture input.
		PC.8	MFP11	I/O	
		PC.4	MFP12	I/O	
		PB.14	MFP11	I/O	
	EPWM1_CH2	PC.10	MFP12	I/O	EPWM1 channel 2 output/capture input.
		PC.7	MFP11	I/O	
		PC.3	MFP12	I/O	
		PB.13	MFP11	I/O	
	EPWM1_CH3	PC.9	MFP12	I/O	EPWM1 channel 3 output/capture input.
		PC.6	MFP11	I/O	
		PC.2	MFP12	I/O	
		PB.12	MFP11	I/O	
	EPWM1_CH4	PB.1	MFP12	I/O	EPWM1 channel 4 output/capture input.
		PA.7	MFP11	I/O	
		PC.1	MFP12	I/O	
		PB.7	MFP12	I/O	
	EPWM1_CH5	PB.6	MFP12	I/O	EPWM1 channel 5 output/capture input.
		PB.0	MFP12	I/O	
		PA.6	MFP11	I/O	
		PC.0	MFP12	I/O	
QEI0	QEI0_A	PD.11	MFP10	I	Quadrature encoder 0 phase A input
		PA.4	MFP14	I	
		PE.3	MFP11	I	
	QEI0_B	PD.10	MFP10	I	Quadrature encoder 0 phase B input
		PA.3	MFP14	I	

Group	Pin Name	GPIO	MFP	Type	Description
		PE.2	MFP11	I	
	QEI0_INDEX	PD.12	MFP10	I	Quadrature encoder 0 index input
		PA.5	MFP14	I	
		PE.4	MFP11	I	
QEI1	QEI1_A	PA.9	MFP10	I	Quadrature encoder 1 phase A input
		PA.13	MFP12	I	
		PE.6	MFP11	I	
	QEI1_B	PA.8	MFP10	I	Quadrature encoder 1 phase B input
		PA.14	MFP12	I	
		PE.5	MFP11	I	
	QEI1_INDEX	PA.10	MFP10	I	Quadrature encoder 1 index input
		PA.12	MFP12	I	
		PE.7	MFP11	I	
SC0	SC0_CLK	PB.5	MFP9	O	Smart Card 0 clock pin.
		PF.6	MFP3	O	
		PA.0	MFP6	O	
		PE.2	MFP6	O	
	SC0_DAT	PB.4	MFP9	I/O	Smart Card 0 data pin.
		PF.7	MFP3	I/O	
		PA.1	MFP6	I/O	
		PE.3	MFP6	I/O	
	SC0_PWR	PB.2	MFP9	O	Smart Card 0 power pin.
		PF.9	MFP3	O	
		PA.3	MFP6	O	
		PE.5	MFP6	O	
	SC0_RST	PB.3	MFP9	O	Smart Card 0 reset pin.
		PF.8	MFP3	O	
		PA.2	MFP6	O	
		PE.4	MFP6	O	
	SC0_nCD	PC.12	MFP9	I	Smart Card 0 card detect pin.
		PF.10	MFP3	I	
		PA.4	MFP6	I	
		PE.6	MFP6	I	
SC1	SC1_CLK	PC.0	MFP5	O	Smart Card 1 clock pin.

Group	Pin Name	GPIO	MFP	Type	Description
		PD.4	MFP8	O	
		PB.12	MFP3	O	
	SC1_DAT	PC.1	MFP5	I/O	Smart Card 1 data pin.
		PD.5	MFP8	I/O	
		PB.13	MFP3	I/O	
	SC1_PWR	PC.3	MFP5	O	Smart Card 1 power pin.
		PD.7	MFP8	O	
		PB.15	MFP3	O	
	SC1_RST	PC.2	MFP5	O	Smart Card 1 reset pin.
		PD.6	MFP8	O	
		PB.14	MFP3	O	
	SC1_nCD	PC.4	MFP5	I	Smart Card 1 card detect pin.
		PD.3	MFP8	I	
		PD.14	MFP4	I	
SC2	SC2_CLK	PA.8	MFP3	O	Smart Card 2 clock pin.
		PA.6	MFP6	O	
		PD.0	MFP7	O	
		PA.15	MFP7	O	
		PE.0	MFP4	O	
	SC2_DAT	PA.9	MFP3	I/O	Smart Card 2 data pin.
		PA.7	MFP6	I/O	
		PD.1	MFP7	I/O	
		PA.14	MFP7	I/O	
		PE.1	MFP4	I/O	
	SC2_PWR	PA.11	MFP3	O	Smart Card 2 power pin.
		PC.7	MFP6	O	
		PD.3	MFP7	O	
		PA.12	MFP7	O	
		PH.8	MFP4	O	
	SC2_RST	PA.10	MFP3	O	Smart Card 2 reset pin.
		PC.6	MFP6	O	
		PD.2	MFP7	O	
		PA.13	MFP7	O	
		PH.9	MFP4	O	

Group	Pin Name	GPIO	MFP	Type	Description
	SC2_nCD	PC.13	MFP3	I	Smart Card 2 card detect pin.
		PA.5	MFP6	I	
		PD.13	MFP7	I	
		PH.10	MFP4	I	
SD0	SD0_CLK	PB.1	MFP3	O	SD/SDIO0 clock output pin
		PE.6	MFP3	O	
	SD0_CMD	PB.0	MFP3	I/O	SD/SDIO0 command/response pin
		PE.7	MFP3	I/O	
	SD0_DAT0	PB.2	MFP3	I/O	SD/SDIO0 data line bit 0.
		PE.2	MFP3	I/O	
	SD0_DAT1	PB.3	MFP3	I/O	SD/SDIO0 data line bit 1.
		PE.3	MFP3	I/O	
	SD0_DAT2	PB.4	MFP3	I/O	SD/SDIO0 data line bit 2.
		PE.4	MFP3	I/O	
	SD0_DAT3	PB.5	MFP3	I/O	SD/SDIO0 data line bit 3.
		PE.5	MFP3	I/O	
	SD0_nCD	PD.13	MFP3	I	SD/SDIO0 card detect input pin
		PB.12	MFP9	I	
QSPI0	QSPI0_CLK	PF.2	MFP5	I/O	Quad SPI0 serial clock pin.
		PA.2	MFP3	I/O	
		PC.2	MFP4	I/O	
		PH.8	MFP3	I/O	
	QSPI0_MISO0	PA.1	MFP3	I/O	Quad SPI0 MISO0 (Master In, Slave Out) pin.
		PC.1	MFP4	I/O	
		PE.1	MFP3	I/O	
	QSPI0_MISO1	PA.5	MFP3	I/O	Quad SPI0 MISO1 (Master In, Slave Out) pin.
		PC.5	MFP4	I/O	
		PH.10	MFP3	I/O	
	QSPI0_MOSI0	PA.0	MFP3	I/O	Quad SPI0 MOSI0 (Master Out, Slave In) pin.
		PC.0	MFP4	I/O	
		PE.0	MFP3	I/O	
	QSPI0_MOSI1	PA.4	MFP3	I/O	Quad SPI0 MOSI1 (Master Out, Slave In) pin.
		PC.4	MFP4	I/O	
		PH.11	MFP3	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
	QSPI0_SS	PA.3	MFP3	I/O	Quad SPI0 slave select pin.
		PC.3	MFP4	I/O	
		PH.9	MFP3	I/O	
SPI0	SPI0_CLK	PF.8	MFP5	I/O	SPI0 serial clock pin.
		PA.2	MFP4	I/O	
		PD.2	MFP4	I/O	
		PB.14	MFP4	I/O	
	SPI0_I2SMCLK	PB.0	MFP8	I/O	SPI0 I2S master clock output pin
		PF.10	MFP5	I/O	
		PA.4	MFP4	I/O	
		PD.13	MFP4	I/O	
		PD.14	MFP6	I/O	
		PB.11	MFP9	I/O	
	SPI0_MISO	PF.7	MFP5	I/O	SPI0 MISO (Master In, Slave Out) pin.
		PA.1	MFP4	I/O	
		PD.1	MFP4	I/O	
		PB.13	MFP4	I/O	
	SPI0 _MOSI	PF.6	MFP5	I/O	SPI0 MOSI (Master Out, Slave In) pin.
		PA.0	MFP4	I/O	
		PD.0	MFP4	I/O	
		PB.12	MFP4	I/O	
	SPI0_SS	PF.9	MFP5	I/O	SPI0 slave select pin.
		PA.3	MFP4	I/O	
		PD.3	MFP4	I/O	
		PB.15	MFP4	I/O	
SPI1	SPI1_CLK	PB.3	MFP5	I/O	SPI1 serial clock pin.
		PH.6	MFP3	I/O	
		PA.7	MFP4	I/O	
		PC.1	MFP7	I/O	
		PD.5	MFP5	I/O	
		PH.8	MFP6	I/O	
	SPI1_I2SMCLK	PB.1	MFP5	I/O	SPI1 I2S master clock output pin
		PA.5	MFP4	I/O	
		PC.4	MFP7	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PD.13	MFP5	I/O	
		PH.10	MFP6	I/O	
	SPI1_MISO	PB.5	MFP5	I/O	SPI1 MISO (Master In, Slave Out) pin.
		PH.4	MFP3	I/O	
		PC.7	MFP4	I/O	
		PC.3	MFP7	I/O	
		PD.7	MFP5	I/O	
		PE.1	MFP6	I/O	
	SPI1_MOSI	PB.4	MFP5	I/O	SPI1 MOSI (Master Out, Slave In) pin.
		PH.5	MFP3	I/O	
		PC.6	MFP4	I/O	
		PC.2	MFP7	I/O	
		PD.6	MFP5	I/O	
		PE.0	MFP6	I/O	
	SPI1_SS	PB.2	MFP5	I/O	SPI1 slave select pin.
		PH.7	MFP3	I/O	
		PA.6	MFP4	I/O	
		PC.0	MFP7	I/O	
		PD.4	MFP5	I/O	
		PH.9	MFP6	I/O	
SPI2	SPI2_CLK	PA.10	MFP4	I/O	SPI2 serial clock pin.
		PG.3	MFP3	I/O	
		PE.8	MFP5	I/O	
		PA.13	MFP5	I/O	
	SPI2_I2SMCLK	PC.13	MFP4	I/O	SPI2 I2S master clock output pin
		PE.12	MFP5	I/O	
	SPI2_MISO	PA.9	MFP4	I/O	SPI2 MISO (Master In, Slave Out) pin.
		PG.4	MFP3	I/O	
		PE.9	MFP5	I/O	
		PA.14	MFP5	I/O	
	SPI2_MOSI	PA.8	MFP4	I/O	SPI2 MOSI (Master Out, Slave In) pin.
		PF.11	MFP3	I/O	
		PE.10	MFP5	I/O	
		PA.15	MFP5	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
	SPI2_SS	PA.11	MFP4	I/O	SPI2 slave select pin.
		PG.2	MFP3	I/O	
		PE.11	MFP5	I/O	
		PA.12	MFP5	I/O	
SPI3	SPI3_CLK	PC.10	MFP6	I/O	SPI3 serial clock pin.
		PE.4	MFP5	I/O	
		PB.11	MFP11	I/O	
	SPI3_I2SMCLK	PB.1	MFP6	I/O	SPI3 I2S master clock output pin
		PE.6	MFP5	I/O	
		PD.14	MFP3	I/O	
	SPI3_MISO	PC.12	MFP6	I/O	SPI3 MISO (Master In, Slave Out) pin.
		PE.3	MFP5	I/O	
		PB.9	MFP11	I/O	
	SPI3_MOSI	PC.11	MFP6	I/O	SPI3 MOSI (Master Out, Slave In) pin.
		PE.2	MFP5	I/O	
		PB.8	MFP11	I/O	
	SPI3_SS	PC.9	MFP6	I/O	SPI3 slave select pin.
		PE.5	MFP5	I/O	
		PB.10	MFP11	I/O	
TAMPER0	TAMPER0	PF.6	MFP10	I/O	TAMPER detector loop pin 0.
TAMPER1	TAMPER1	PF.7	MFP10	I/O	TAMPER detector loop pin 1.
TAMPER2	TAMPER2	PF.8	MFP10	I/O	TAMPER detector loop pin 2.
TAMPER3	TAMPER3	PF.9	MFP10	I/O	TAMPER detector loop pin 3.
TAMPER4	TAMPER4	PF.10	MFP10	I/O	TAMPER detector loop pin 4.
TAMPER5	TAMPER5	PF.11	MFP10	I/O	TAMPER detector loop pin 5.
TM0	TM0	PB.5	MFP14	I/O	Timer0 event counter input/toggle output pin.
		PG.2	MFP13	I/O	
		PC.7	MFP14	I/O	
	TM0_EXT	PA.11	MFP13	I/O	Timer0 external capture input/toggle output pin.
		PB.15	MFP13	I/O	
TM1	TM1	PB.4	MFP14	I/O	Timer1 event counter input/toggle output pin.
		PG.3	MFP13	I/O	
		PC.6	MFP14	I/O	
	TM1_EXT	PA.10	MFP13	I/O	Timer1 external capture input/toggle output

Group	Pin Name	GPIO	MFP	Type	Description
		PB.14	MFP13	I/O	pin.
TM2	TM2	PB.3	MFP14	I/O	Timer2 event counter input/toggle output pin.
		PG.4	MFP13	I/O	
		PA.7	MFP14	I/O	
		PD.0	MFP14	I/O	
	TM2_EXT	PA.9	MFP13	I/O	Timer2 external capture input/toggle output pin.
		PB.13	MFP13	I/O	
TM3	TM3	PB.2	MFP14	I/O	Timer3 event counter input/toggle output pin.
		PF.11	MFP13	I/O	
		PA.6	MFP14	I/O	
	TM3_EXT	PA.8	MFP13	I/O	Timer3 external capture input/toggle output pin.
		PB.12	MFP13	I/O	
TRACE	TRACE_CLK	PE.12	MFP14	O	ETM Trace Clock output pin
	TRACE_DATA0	PE.11	MFP14	O	ETM Trace Data 0 output pin
	TRACE_DATA1	PE.10	MFP14	O	ETM Trace Data 1 output pin
	TRACE_DATA2	PE.9	MFP14	O	ETM Trace Data 2 output pin
	TRACE_DATA3	PE.8	MFP14	O	ETM Trace Data 3 output pin
UART0	UART0_RXD	PC.11	MFP3	I	UART0 data receiver input pin.
		PF.2	MFP3	I	
		PA.6	MFP7	I	
		PA.0	MFP7	I	
		PD.2	MFP9	I	
		PA.15	MFP3	I	
		PH.11	MFP8	I	
		PB.12	MFP6	I	
		PB.8	MFP5	I	
	UART0_TXD	PC.12	MFP3	O	UART0 data transmitter output pin.
		PF.3	MFP3	O	
		PA.7	MFP7	O	
		PA.1	MFP7	O	
		PD.3	MFP9	O	
		PA.14	MFP3	O	
		PH.10	MFP8	O	
		PB.13	MFP6	O	

Group	Pin Name	GPIO	MFP	Type	Description
		PB.9	MFP5	O	
	UART0_nCTS	PC.7	MFP7	I	UART0 clear to Send input pin.
		PA.5	MFP7	I	
		PB.15	MFP6	I	
		PB.11	MFP5	I	
	UART0_nRTS	PC.6	MFP7	O	UART0 request to Send output pin.
		PA.4	MFP7	O	
		PB.14	MFP6	O	
		PB.10	MFP5	O	
UART1	UART1_RXD	PB.6	MFP6	I	UART1 data receiver input pin.
		PB.2	MFP6	I	
		PA.8	MFP7	I	
		PD.10	MFP3	I	
		PC.8	MFP8	I	
		PA.2	MFP8	I	
		PF.1	MFP2	I	
		PD.6	MFP3	I	
		PH.9	MFP10	I	
	UART1_TXD	PB.3	MFP6	O	UART1 data transmitter output pin.
		PA.9	MFP7	O	
		PD.11	MFP3	O	
		PE.13	MFP8	O	
		PA.3	MFP8	O	
		PF.0	MFP2	O	
		PD.7	MFP3	O	
		PH.8	MFP10	O	
		PB.7	MFP6	O	
	UART1_nCTS	PE.11	MFP8	I	UART1 clear to Send input pin.
		PA.1	MFP8	I	
		PB.9	MFP6	I	
	UART1_nRTS	PE.12	MFP8	O	UART1 request to Send output pin.
		PA.0	MFP8	O	
		PB.8	MFP6	O	
UART2	UART2_RXD	PB.0	MFP7	I	UART2 data receiver input pin.

Group	Pin Name	GPIO	MFP	Type	Description
		PD.12	MFP7	I	
		PF.5	MFP2	I	
		PE.9	MFP7	I	
		PE.15	MFP3	I	
		PC.4	MFP8	I	
		PC.0	MFP8	I	
	UART2_TXD	PB.1	MFP7	O	UART2 data transmitter output pin.
		PC.13	MFP7	O	
		PF.4	MFP2	O	
		PE.8	MFP7	O	
		PE.14	MFP3	O	
		PC.5	MFP8	O	
		PC.1	MFP8	O	
	UART2_nCTS	PF.5	MFP4	I	UART2 clear to Send input pin.
		PD.9	MFP4	I	
		PC.2	MFP8	I	
	UART2_nRTS	PF.4	MFP4	O	UART2 request to Send output pin.
		PD.8	MFP4	O	
		PC.3	MFP8	O	
UART3	UART3_RXD	PC.9	MFP7	I	UART3 data receiver input pin.
		PE.11	MFP7	I	
		PC.2	MFP11	I	
		PD.0	MFP5	I	
		PE.0	MFP7	I	
		PB.14	MFP7	I	
	UART3_TXD	PC.10	MFP7	O	UART3 data transmitter output pin.
		PE.10	MFP7	O	
		PC.3	MFP11	O	
		PD.1	MFP5	O	
		PE.1	MFP7	O	
		PB.15	MFP7	O	
	UART3_nCTS	PD.2	MFP5	I	UART3 clear to Send input pin.
		PH.9	MFP7	I	
		PB.12	MFP7	I	

Group	Pin Name	GPIO	MFP	Type	Description
	UART3_nRTS	PD.3	MFP5	O	UART3 request to Send output pin.
		PH.8	MFP7	O	
		PB.13	MFP7	O	
UART4	UART4_RXD	PF.6	MFP6	I	UART4 data receiver input pin.
		PC.6	MFP5	I	
		PA.2	MFP7	I	
		PC.4	MFP11	I	
		PA.13	MFP3	I	
		PH.11	MFP7	I	
		PB.10	MFP6	I	
	UART4_TXD	PF.7	MFP6	O	UART4 data transmitter output pin.
		PC.7	MFP5	O	
		PA.3	MFP7	O	
		PC.5	MFP11	O	
		PA.12	MFP3	O	
		PH.10	MFP7	O	
		PB.11	MFP6	O	
	UART4_nCTS	PC.8	MFP5	I	UART4 clear to Send input pin.
		PE.1	MFP9	I	
	UART4_nRTS	PE.13	MFP5	O	UART4 request to Send output pin.
		PE.0	MFP9	O	
UART5	UART5_RXD	PB.4	MFP7	I	UART5 data receiver input pin.
		PA.4	MFP8	I	
		PE.6	MFP8	I	
	UART5_TXD	PB.5	MFP7	O	UART5 data transmitter output pin.
		PA.5	MFP8	O	
		PE.7	MFP8	O	
	UART5_nCTS	PB.2	MFP7	I	UART5 clear to Send input pin.
	UART5_nRTS	PB.3	MFP7	O	UART5 request to Send output pin.
USB	USB_D+	PA.14	MFP14	A	USB differential signal D+.
	USB_D-	PA.13	MFP14	A	USB differential signal D-.
	USB_OTG_ID	PA.15	MFP14	I	USB_ identification.
	USB_VBUS	PA.12	MFP14	P	Power supply from USB host or HUB.
	USB_VBUS_EN	PB.6	MFP14	O	USB external VBUS regulator enable pin.

Group	Pin Name	GPIO	MFP	Type	Description
		PB.15	MFP14	O	
	USB_VBUS_ST	PD.4	MFP14	I	USB external VBUS regulator status pin.
		PB.14	MFP15	I	
		PB.7	MFP14	I	
USCI0	USCI0_CLK	PA.11	MFP6	I/O	USCI0 clock pin.
		PD.0	MFP3	I/O	
		PE.2	MFP7	I/O	
		PB.12	MFP5	I/O	
	USCI0_CTL0	PC.13	MFP6	I/O	USCI0 control 0 pin.
		PD.4	MFP3	I/O	
		PE.6	MFP7	I/O	
		PD.14	MFP5	I/O	
	USCI0_CTL1	PA.8	MFP6	I/O	USCI0 control 1 pin.
		PD.3	MFP3	I/O	
		PE.5	MFP7	I/O	
		PB.15	MFP5	I/O	
	USCI0_DAT0	PA.10	MFP6	I/O	USCI0 data 0 pin.
		PD.1	MFP3	I/O	
		PE.3	MFP7	I/O	
		PB.13	MFP5	I/O	
	USCI0_DAT1	PA.9	MFP6	I/O	USCI0 data 1 pin.
		PD.2	MFP3	I/O	
		PE.4	MFP7	I/O	
		PB.14	MFP5	I/O	
USCI1	USCI1_CLK	PB.1	MFP8	I/O	USCI1 clock pin.
		PE.12	MFP6	I/O	
		PD.7	MFP6	I/O	
		PB.8	MFP4	I/O	
	USCI1_CTL0	PB.5	MFP8	I/O	USCI1 control 0 pin.
		PE.9	MFP6	I/O	
		PD.3	MFP6	I/O	
		PB.10	MFP4	I/O	
	USCI1_CTL1	PB.4	MFP8	I/O	USCI1 control 1 pin.
		PE.8	MFP6	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PD.4	MFP6	I/O	
		PB.9	MFP4	I/O	
	USCI1_DAT0	PB.2	MFP8	I/O	USCI1 data 0 pin.
		PE.10	MFP6	I/O	
		PD.5	MFP6	I/O	
		PB.7	MFP4	I/O	
	USCI1_DAT1	PB.6	MFP4	I/O	USCI1 data 1 pin.
		PB.3	MFP8	I/O	
		PE.11	MFP6	I/O	
		PD.6	MFP6	I/O	
X32	X32_IN	PF.5	MFP10	I	External 32.768 kHz crystal input pin.
	X32_OUT	PF.4	MFP10	O	External 32.768 kHz crystal output pin.
XT1	XT1_IN	PF.3	MFP10	I	External 4~24 MHz (high speed) crystal input pin.
	XT1_OUT	PF.2	MFP10	O	External 4~24 MHz (high speed) crystal output pin.

4.7 M2351 Multi-function Summary Table Sorted by GPIO

	Pin Name	Type	MFP	Description
PA.0	PA.0	I/O	MFP0	General purpose digital I/O pin.
	QSPI0_MOSI0	I/O	MFP3	Quad SPI0 MOSI0 (Master Out, Slave In) pin.
	SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
	SC0_CLK	O	MFP6	Smart Card 0 clock pin.
	UART0_RXD	I	MFP7	UART0 data receiver input pin.
	UART1_nRTS	O	MFP8	UART1 request to Send output pin.
	I2C2_SDA	I/O	MFP9	I2C2 data input/output pin.
	BPWM0_CH0	I/O	MFP12	BPWM0 channel 0 output/capture input.
	EPWM0_CH5	I/O	MFP13	EPWM0 channel 5 output/capture input.
	DAC0_ST	I	MFP15	DAC0 external trigger input.
PA.1	PA.1	I/O	MFP0	General purpose digital I/O pin.
	QSPI0_MISO0	I/O	MFP3	Quad SPI0 MISO0 (Master In, Slave Out) pin.
	SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
	SC0_DAT	I/O	MFP6	Smart Card 0 data pin.
	UART0_TXD	O	MFP7	UART0 data transmitter output pin.
	UART1_nCTS	I	MFP8	UART1 clear to Send input pin.
	I2C2_SCL	I/O	MFP9	I2C2 clock pin.
	BPWM0_CH1	I/O	MFP12	BPWM0 channel 1 output/capture input.
	EPWM0_CH4	I/O	MFP13	EPWM0 channel 4 output/capture input.
	DAC1_ST	I	MFP15	DAC1 external trigger input.
PA.2	PA.2	I/O	MFP0	General purpose digital I/O pin.
	QSPI0_CLK	I/O	MFP3	Quad SPI0 serial clock pin.
	SPI0_CLK	I/O	MFP4	SPI serial clock pin.
	SC0_RST	O	MFP6	Smart Card 0 reset pin.
	UART4_RXD	I	MFP7	UART4 data receiver input pin.
	UART1_RXD	I	MFP8	UART1 data receiver input pin.
	I2C1_SDA	I/O	MFP9	I2C1 data input/output pin.
	BPWM0_CH2	I/O	MFP12	BPWM0 channel 2 output/capture input.
	EPWM0_CH3	I/O	MFP13	EPWM0 channel 3 output/capture input.
PA.3	PA.3	I/O	MFP0	General purpose digital I/O pin.
	QSPI0_SS	I/O	MFP3	Quad SPI0 slave select pin.
	SPI0_SS	I/O	MFP4	SPI0 slave select pin.
	SC0_PWR	O	MFP6	Smart Card 0 power pin.

	Pin Name	Type	MFP	Description
	UART4_TXD	O	MFP7	UART4 data transmitter output pin.
	UART1_TXD	O	MFP8	UART1 data transmitter output pin.
	I2C1_SCL	I/O	MFP9	I2C1 clock pin.
	BPWM0_CH3	I/O	MFP12	BPWM0 channel 3 output/capture input.
	EPWM0_CH2	I/O	MFP13	EPWM0 channel 2 output/capture input.
	QEI0_B	I	MFP14	Quadrature encoder 0 phase B input
PA.4	PA.4	I/O	MFP0	General purpose digital I/O pin.
	QSPI0_MOSI1	I/O	MFP3	Quad SPI0 MOSI1 (Master Out, Slave In) pin.
	SPI0_I2SMCLK	I/O	MFP4	SPI0 I2S master clock output pin
	SC0_nCD	I	MFP6	Smart Card 0 card detect pin.
	UART0_nRTS	O	MFP7	UART0 request to Send output pin.
	UART5_RXD	I	MFP8	UART5 data receiver input pin.
	I2C0_SDA	I/O	MFP9	I2C0 data input/output pin.
	CAN0_RXD	I	MFP10	CAN0 bus receiver input.
	BPWM0_CH4	I/O	MFP12	BPWM0 channel 4 output/capture input.
	EPWM0_CH1	I/O	MFP13	EPWM0 channel 1 output/capture input.
	QEI0_A	I	MFP14	Quadrature encoder 0 phase A input
PA.5	PA.5	I/O	MFP0	General purpose digital I/O pin.
	QSPI0_MISO1	I/O	MFP3	Quad SPI0 MISO1 (Master In, Slave Out) pin.
	SPI1_I2SMCLK	I/O	MFP4	SPI1 I2S master clock output pin
	SC2_nCD	I	MFP6	Smart Card 2 card detect pin.
	UART0_nCTS	I	MFP7	UART0 clear to Send input pin.
	UART5_TXD	O	MFP8	UART5 data transmitter output pin.
	I2C0_SCL	I/O	MFP9	I2C0 clock pin.
	CAN0_TXD	O	MFP10	CAN0 bus transmitter output.
	BPWM0_CH5	I/O	MFP12	BPWM0 channel 5 output/capture input.
	EPWM0_CH0	I/O	MFP13	EPWM0 channel 0 output/capture input.
	QEI0_INDEX	I	MFP14	Quadrature encoder 0 index input
PA.6	PA.6	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD6	I/O	MFP2	EBI address/data bus bit 6.
	SPI1_SS	I/O	MFP4	SPI1 slave select pin.
	SC2_CLK	O	MFP6	Smart Card 2 clock pin.
	UART0_RXD	I	MFP7	UART0 data receiver input pin.
	I2C1_SDA	I/O	MFP8	I2C1 data input/output pin.

	Pin Name	Type	MFP	Description
	EPWM1_CH5	I/O	MFP11	EPWM1 channel 5 output/capture input.
	BPWM1_CH3	I/O	MFP12	BPWM1 channel 3 output/capture input.
	ACMP1_WLAT	I	MFP13	Analog comparator 1 window latch input pin
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	INT0	I	MFP15	External interrupt 0 input pin.
PA.7	PA.7	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD7	I/O	MFP2	EBI address/data bus bit 7.
	SPI1_CLK	I/O	MFP4	SPI1 serial clock pin.
	SC2_DAT	I/O	MFP6	Smart Card 2 data pin.
	UART0_TXD	O	MFP7	UART0 data transmitter output pin.
	I2C1_SCL	I/O	MFP8	I2C1 clock pin.
	EPWM1_CH4	I/O	MFP11	EPWM1 channel 4 output/capture input.
	BPWM1_CH2	I/O	MFP12	BPWM1 channel 2 output/capture input.
	ACMP0_WLAT	I	MFP13	Analog comparator 0 window latch input pin
	TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
	INT1	I	MFP15	External interrupt 1 input pin.
PA.8	PA.8	I/O	MFP0	General purpose digital I/O pin.
	EBI_ALE	O	MFP2	EBI address latch enable output pin.
	SC2_CLK	O	MFP3	Smart Card 2 clock pin.
	SPI2_MOSI	I/O	MFP4	SPI2 MOSI (Master Out, Slave In) pin.
	USCI0_CTL1	I/O	MFP6	USCI0 control 1 pin.
	UART1_RXD	I	MFP7	UART1 data receiver input pin.
	BPWM0_CH3	I/O	MFP9	BPWM0 channel 3 output/capture input.
	QEI1_B	I	MFP10	Quadrature encoder 1 phase B input
	ECAP0_IC2	I	MFP11	Enhanced capture unit 0 input 2 pin.
	TM3_EXT	I/O	MFP13	Timer3 external capture input/toggle output pin.
	INT4	I	MFP15	External interrupt 4 input pin.
PA.9	PA.9	I/O	MFP0	General purpose digital I/O pin.
	EBI_MCLK	O	MFP2	EBI external clock output pin.
	SC2_DAT	I/O	MFP3	Smart Card 2 data pin.
	SPI2_MISO	I/O	MFP4	SPI2 MISO (Master In, Slave Out) pin.
	USCI0_DAT1	I/O	MFP6	USCI0 data 1 pin.
	UART1_TXD	O	MFP7	UART1 data transmitter output pin.
	BPWM0_CH2	I/O	MFP9	BPWM0 channel 2 output/capture input.

	Pin Name	Type	MFP	Description
	QEI1_A	I	MFP10	Quadrature encoder 1 phase A input
	ECAP0_IC1	I	MFP11	Enhanced capture unit 0 input 1 pin.
	TM2_EXT	I/O	MFP13	Timer2 external capture input/toggle output pin.
PA.10	PA.10	I/O	MFP0	General purpose digital I/O pin.
	ACMP1_P0	A	MFP1	Analog comparator 1 positive input 0 pin.
	EBI_nWR	O	MFP2	EBI write enable output pin.
	SC2_RST	O	MFP3	Smart Card 2 reset pin.
	SPI2_CLK	I/O	MFP4	SPI2 serial clock pin.
	USCI0_DAT0	I/O	MFP6	USCI0 data 0 pin.
	I2C2_SDA	I/O	MFP7	I2C2 data input/output pin.
	BPWM0_CH1	I/O	MFP9	BPWM0 channel 1 output/capture input.
	QEI1_INDEX	I	MFP10	Quadrature encoder 1 index input
	ECAP0_IC0	I	MFP11	Enhanced capture unit 0 input 0 pin.
	TM1_EXT	I/O	MFP13	Timer1 external capture input/toggle output pin.
	DAC0_ST	I	MFP14	DAC0 external trigger input.
PA.11	PA.11	I/O	MFP0	General purpose digital I/O pin.
	ACMP0_P0	A	MFP1	Analog comparator 0 positive input 0 pin.
	EBI_nRD	O	MFP2	EBI read enable output pin.
	SC2_PWR	O	MFP3	Smart Card 2 power pin.
	SPI2_SS	I/O	MFP4	SPI2 slave select pin.
	USCI0_CLK	I/O	MFP6	USCI0 clock pin.
	I2C2_SCL	I/O	MFP7	I2C2 clock pin.
	BPWM0_CH0	I/O	MFP9	BPWM0 channel 0 output/capture input.
	EPWM0_SYNC_OUT	O	MFP10	EPWM0 counter synchronous trigger output pin.
	TM0_EXT	I/O	MFP13	Timer0 external capture input/toggle output pin.
	DAC1_ST	I	MFP14	DAC1 external trigger input.
PA.12	PA.12	I/O	MFP0	General purpose digital I/O pin.
	I2S0_BCLK	O	MFP2	I2S0 bit clock output pin.
	UART4_TXD	O	MFP3	UART4 data transmitter output pin.
	I2C1_SCL	I/O	MFP4	I2C1 clock pin.
	SPI2_SS	I/O	MFP5	SPI2 slave select pin.
	CAN0_TXD	O	MFP6	CAN0 bus transmitter output.
	SC2_PWR	O	MFP7	Smart Card 2 power pin.
	BPWM1_CH2	I/O	MFP11	BPWM1 channel 2 output/capture input.

	Pin Name	Type	MFP	Description
	QEI1_INDEX	I	MFP12	Quadrature encoder 1 index input
	USB_VBUS	P	MFP14	Power supply from USB host or HUB.
PA.13	PA.13	I/O	MFP0	General purpose digital I/O pin.
	I2S0_MCLK	O	MFP2	I2S0 master clock output pin.
	UART4_RXD	I	MFP3	UART4 data receiver input pin.
	I2C1_SDA	I/O	MFP4	I2C1 data input/output pin.
	SPI2_CLK	I/O	MFP5	SPI2 serial clock pin.
	CAN0_RXD	I	MFP6	CAN0 bus receiver input.
	SC2_RST	O	MFP7	Smart Card 2 reset pin.
	BPWM1_CH3	I/O	MFP11	BPWM1 channel 3 output/capture input.
	QEI1_A	I	MFP12	Quadrature encoder 1 phase A input
	USB_D-	A	MFP14	USB differential signal D-.
PA.14	PA.14	I/O	MFP0	General purpose digital I/O pin.
	I2S0_DI	I	MFP2	I2S0 data input pin.
	UART0_TXD	O	MFP3	UART0 data transmitter output pin.
	SPI2_MISO	I/O	MFP5	SPI2 MISO (Master In, Slave Out) pin.
	I2C2_SCL	I/O	MFP6	I2C2 clock pin.
	SC2_DAT	I/O	MFP7	Smart Card 2 data pin.
	BPWM1_CH4	I/O	MFP11	BPWM1 channel 4 output/capture input.
	QEI1_B	I	MFP12	Quadrature encoder 1 phase B input
	USB_D+	A	MFP14	USB differential signal D+.
PA.15	PA.15	I/O	MFP0	General purpose digital I/O pin.
	I2S0_DO	O	MFP2	I2S0 data output pin.
	UART0_RXD	I	MFP3	UART0 data receiver input pin.
	SPI2_MOSI	I/O	MFP5	SPI2 MOSI (Master Out, Slave In) pin.
	I2C2_SDA	I/O	MFP6	I2C2 data input/output pin.
	SC2_CLK	O	MFP7	Smart Card 2 clock pin.
	BPWM1_CH5	I/O	MFP11	BPWM1 channel 5 output/capture input.
	EPWM0_SYNC_IN	I	MFP12	EPWM0 counter synchronous trigger input pin.
	USB_OTG_ID	I	MFP14	USB_ identification.
PB.0	PB.0	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH0	A	MFP1	EADC0 channel 0 analog input.
	EBI_ADR9	O	MFP2	EBI address bus bit 9.
	SD0_CMD	I/O	MFP3	SD/SDIO0 command/response pin

	Pin Name	Type	MFP	Description
	UART2_RXD	I	MFP7	UART2 data receiver input pin.
	SPI0_I2SMCLK	I/O	MFP8	SPI0 I2S master clock output pin
	I2C1_SDA	I/O	MFP9	I2C1 data input/output pin.
	EPWM0_CH5	I/O	MFP11	EPWM0 channel 5 output/capture input.
	EPWM1_CH5	I/O	MFP12	EPWM1 channel 5 output/capture input.
	EPWM0_BRAKE1	I	MFP13	EPWM0 Brake 1 input pin.
PB.1	PB.1	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH1	A	MFP1	EADC0 channel 1 analog input.
	EBI_ADR8	O	MFP2	EBI address bus bit 8.
	SD0_CLK	O	MFP3	SD/SDIO0 clock output pin
	SPI1_I2SMCLK	I/O	MFP5	SPI1 I2S master clock output pin
	SPI3_I2SMCLK	I/O	MFP6	SPI3 I2S master clock output pin
	UART2_TXD	O	MFP7	UART2 data transmitter output pin.
	USCI1_CLK	I/O	MFP8	USCI1 clock pin.
	I2C1_SCL	I/O	MFP9	I2C1 clock pin.
	I2S0_LRCK	O	MFP10	I2S0 left right channel clock output pin.
	EPWM0_CH4	I/O	MFP11	EPWM0 channel 4 output/capture input.
	EPWM1_CH4	I/O	MFP12	EPWM1 channel 4 output/capture input.
	EPWM0_BRAKE0	I	MFP13	EPWM0 Brake 0 input pin.
PB.2	PB.2	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH2	A	MFP1	EADC0 channel 2 analog input.
	ACMP0_P1	A	MFP1	Analog comparator 0 positive input 1 pin.
	EBI_ADR3	O	MFP2	EBI address bus bit 3.
	SD0_DAT0	I/O	MFP3	SD/SDIO0 data line bit 0.
	SPI1_SS	I/O	MFP5	SPI1 slave select pin.
	UART1_RXD	I	MFP6	UART1 data receiver input pin.
	UART5_nCTS	I	MFP7	UART5 clear to Send input pin.
	USCI1_DAT0	I/O	MFP8	USCI1 data 0 pin.
	SC0_PWR	O	MFP9	Smart Card 0 power pin.
	I2S0_DO	O	MFP10	I2S0 data output pin.
	EPWM0_CH3	I/O	MFP11	EPWM0 channel 3 output/capture input.
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	INT3	I	MFP15	External interrupt 3 input pin.
PB.3	PB.3	I/O	MFP0	General purpose digital I/O pin.

	Pin Name	Type	MFP	Description
	EADC0_CH3	A	MFP1	EADC0 channel 3 analog input.
	ACMP0_N	A	MFP1	Analog comparator 0 negative input pin.
	EBI_ADR2	O	MFP2	EBI address bus bit 2.
	SD0_DAT1	I/O	MFP3	SD/SDIO0 data line bit 1.
	SPI1_CLK	I/O	MFP5	SPI1 serial clock pin.
	UART1_TXD	O	MFP6	UART1 data transmitter output pin.
	UART5_nRTS	O	MFP7	UART5 request to Send output pin.
	USCI1_DAT1	I/O	MFP8	USCI1 data 1 pin.
	SC0_RST	O	MFP9	Smart Card 0 reset pin.
	I2S0_DI	I	MFP10	I2S0 data input pin.
	EPWM0_CH2	I/O	MFP11	EPWM0 channel 2 output/capture input.
	TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
	INT2	I	MFP15	External interrupt 2 input pin.
PB.4	PB.4	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH4	A	MFP1	EADC0 channel 4 analog input.
	ACMP1_P1	A	MFP1	Analog comparator 1 positive input 1 pin.
	EBI_ADR1	O	MFP2	EBI address bus bit 1.
	SD0_DAT2	I/O	MFP3	SD/SDIO0 data line bit 2.
	SPI1_MOSI	I/O	MFP5	SPI1 MOSI (Master Out, Slave In) pin.
	I2C0_SDA	I/O	MFP6	I2C0 data input/output pin.
	UART5_RXD	I	MFP7	UART5 data receiver input pin.
	USCI1_CTL1	I/O	MFP8	USCI1 control 1 pin.
	SC0_DAT	I/O	MFP9	Smart Card 0 data pin.
	I2S0_MCLK	O	MFP10	I2S0 master clock output pin.
	EPWM0_CH1	I/O	MFP11	EPWM0 channel 1 output/capture input.
	TM1	I/O	MFP14	Timer1 event counter input/toggle output pin.
	INT1	I	MFP15	External interrupt 1 input pin.
PB.5	PB.5	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH5	A	MFP1	EADC0 channel 5 analog input.
	ACMP1_N	A	MFP1	Analog comparator 1 negative input pin.
	EBI_ADR0	O	MFP2	EBI address bus bit 0.
	SD0_DAT3	I/O	MFP3	SD/SDIO0 data line bit 3.
	SPI1_MISO	I/O	MFP5	SPI1 MISO (Master In, Slave Out) pin.
	I2C0_SCL	I/O	MFP6	I2C0 clock pin.

	Pin Name	Type	MFP	Description
	UART5_TXD	O	MFP7	UART5 data transmitter output pin.
	USCI1_CTL0	I/O	MFP8	USCI1 control 0 pin.
	SC0_CLK	O	MFP9	Smart Card 0 clock pin.
	I2S0_BCLK	O	MFP10	I2S0 bit clock output pin.
	EPWM0_CH0	I/O	MFP11	EPWM0 channel 0 output/capture input.
	TM0	I/O	MFP14	Timer0 event counter input/toggle output pin.
	INT0	I	MFP15	External interrupt 0 input pin.
PB.6	PB.6	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH6	A	MFP1	EADC0 channel 6 analog input.
	EBI_nWRH	O	MFP2	EBI high byte write enable output pin
	USCI1_DAT1	I/O	MFP4	USCI1 data 1 pin.
	UART1_RXD	I	MFP6	UART1 data receiver input pin.
	EBI_nCS1	O	MFP8	EBI chip select 1 output pin.
	BPWM1_CH5	I/O	MFP10	BPWM1 channel 5 output/capture input.
	EPWM1_BRAKE1	I	MFP11	EPWM1 Brake 1 input pin.
	EPWM1_CH5	I/O	MFP12	EPWM1 channel 5 output/capture input.
	INT4	I	MFP13	External interrupt 4 input pin.
	USB_VBUS_EN	O	MFP14	USB external VBUS regulator enable pin.
	ACMP1_O	O	MFP15	Analog comparator 1 output pin.
PB.7	PB.7	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH7	A	MFP1	EADC0 channel 7 analog input.
	EBI_nWRL	O	MFP2	EBI low byte write enable output pin.
	USCI1_DAT0	I/O	MFP4	USCI1 data 0 pin.
	UART1_TXD	O	MFP6	UART1 data transmitter output pin.
	EBI_nCS0	O	MFP8	EBI chip select 0 output pin.
	BPWM1_CH4	I/O	MFP10	BPWM1 channel 4 output/capture input.
	EPWM1_BRAKE0	I	MFP11	EPWM1 Brake 0 input pin.
	EPWM1_CH4	I/O	MFP12	EPWM1 channel 4 output/capture input.
	INT5	I	MFP13	External interrupt 5 input pin.
	USB_VBUS_ST	I	MFP14	USB external VBUS regulator status pin.
	ACMP0_O	O	MFP15	Analog comparator 0 output pin.
PB.8	PB.8	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH8	A	MFP1	EADC0 channel 8 analog input.
	EBI_ADR19	O	MFP2	EBI address bus bit 19.

	Pin Name	Type	MFP	Description
	USCI1_CLK	I/O	MFP4	USCI1 clock pin.
	UART0_RXD	I	MFP5	UART0 data receiver input pin.
	UART1_nRTS	O	MFP6	UART1 request to Send output pin.
	I2C1_SMBSUS	O	MFP7	I2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
	BPWM1_CH3	I/O	MFP10	BPWM1 channel 3 output/capture input.
	SPI3_MOSI	I/O	MFP11	SPI3 MOSI (Master Out, Slave In) pin.
	INT6	I	MFP13	External interrupt 6 input pin.
PB.9	PB.9	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH9	A	MFP1	EADC0 channel 9 analog input.
	EBI_ADR18	O	MFP2	EBI address bus bit 18.
	USCI1_CTL1	I/O	MFP4	USCI1 control 1 pin.
	UART0_TXD	O	MFP5	UART0 data transmitter output pin.
	UART1_nCTS	I	MFP6	UART1 clear to Send input pin.
	I2C1_SMBAL	O	MFP7	I2C1 SMBus SMBALTER pin
	BPWM1_CH2	I/O	MFP10	BPWM1 channel 2 output/capture input.
	SPI3_MISO	I/O	MFP11	SPI3 MISO (Master In, Slave Out) pin.
	INT7	I	MFP13	External interrupt 7 input pin.
PB.10	PB.10	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH10	A	MFP1	EADC0 channel 10 analog input.
	EBI_ADR17	O	MFP2	EBI address bus bit 17.
	USCI1_CTL0	I/O	MFP4	USCI1 control 0 pin.
	UART0_nRTS	O	MFP5	UART0 request to Send output pin.
	UART4_RXD	I	MFP6	UART4 data receiver input pin.
	I2C1_SDA	I/O	MFP7	I2C1 data input/output pin.
	CAN0_RXD	I	MFP8	CAN0 bus receiver input.
	BPWM1_CH1	I/O	MFP10	BPWM1 channel 1 output/capture input.
	SPI3_SS	I/O	MFP11	SPI3 slave select pin.
PB.11	PB.11	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH11	A	MFP1	EADC0 channel 11 analog input.
	EBI_ADR16	O	MFP2	EBI address bus bit 16.
	UART0_nCTS	I	MFP5	UART0 clear to Send input pin.
	UART4_TXD	O	MFP6	UART4 data transmitter output pin.
	I2C1_SCL	I/O	MFP7	I2C1 clock pin.
	CAN0_TXD	O	MFP8	CAN0 bus transmitter output.

	Pin Name	Type	MFP	Description
	SPI0_I2SMCLK	I/O	MFP9	SPI0 I2S master clock output pin
	BPWM1_CH0	I/O	MFP10	BPWM1 channel 0 output/capture input.
	SPI3_CLK	I/O	MFP11	SPI3 serial clock pin.
PB.12	PB.12	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH12	A	MFP1	EADC0 channel 12 analog input.
	DAC0_OUT	A	MFP1	DAC0 channel analog output.
	ACMP0_P2	A	MFP1	Analog comparator 0 positive input 2 pin.
	ACMP1_P2	A	MFP1	Analog comparator 1 positive input 2 pin.
	EBI_AD15	I/O	MFP2	EBI address/data bus bit 15.
	SC1_CLK	O	MFP3	Smart Card 1 clock pin.
	SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
	USCI0_CLK	I/O	MFP5	USCI0 clock pin.
	UART0_RXD	I	MFP6	UART0 data receiver input pin.
	UART3_nCTS	I	MFP7	UART3 clear to Send input pin.
	I2C2_SDA	I/O	MFP8	I2C2 data input/output pin.
	SD0_nCD	I	MFP9	SD/SDIO0 card detect input pin
	EPWM1_CH3	I/O	MFP11	EPWM1 channel 3 output/capture input.
	TM3_EXT	I/O	MFP13	Timer3 external capture input/toggle output pin.
PB.13	PB.13	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH13	A	MFP1	EADC0 channel 13 analog input.
	DAC1_OUT	A	MFP1	DAC1 channel analog output.
	ACMP0_P3	A	MFP1	Analog comparator 0 positive input 3 pin.
	ACMP1_P3	A	MFP1	Analog comparator 1 positive input 3 pin.
	EBI_AD14	I/O	MFP2	EBI address/data bus bit 14.
	SC1_DAT	I/O	MFP3	Smart Card 1 data pin.
	SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
	USCI0_DAT0	I/O	MFP5	USCI0 data 0 pin.
	UART0_TXD	O	MFP6	UART0 data transmitter output pin.
	UART3_nRTS	O	MFP7	UART3 request to Send output pin.
	I2C2_SCL	I/O	MFP8	I2C2 clock pin.
	EPWM1_CH2	I/O	MFP11	EPWM1 channel 2 output/capture input.
	TM2_EXT	I/O	MFP13	Timer2 external capture input/toggle output pin.
PB.14	PB.14	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH14	A	MFP1	EADC0 channel 14 analog input.

	Pin Name	Type	MFP	Description
	EBI_AD13	I/O	MFP2	EBI address/data bus bit 13.
	SC1_RST	O	MFP3	Smart Card 1 reset pin.
	SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
	USCI0_DAT1	I/O	MFP5	USCI0 data 1 pin.
	UART0_nRTS	O	MFP6	UART0 request to Send output pin.
	UART3_RXD	I	MFP7	UART3 data receiver input pin.
	I2C2_SMBSUS	O	MFP8	I2C2 SMBus SMBSUS pin (PMBus CONTROL pin)
	EPWM1_CH1	I/O	MFP11	EPWM1 channel 1 output/capture input.
	TM1_EXT	I/O	MFP13	Timer1 external capture input/toggle output pin.
	CLKO	O	MFP14	Clock Out
	USB_VBUS_ST	I	MFP15	USB external VBUS regulator status pin.
PB.15	PB.15	I/O	MFP0	General purpose digital I/O pin.
	EADC0_CH15	A	MFP1	EADC0 channel 15 analog input.
	EBI_AD12	I/O	MFP2	EBI address/data bus bit 12.
	SC1_PWR	O	MFP3	Smart Card 1 power pin.
	SPI0_SS	I/O	MFP4	SPI0 slave select pin.
	USCI0_CTL1	I/O	MFP5	USCI0 control 1 pin.
	UART0_nCTS	I	MFP6	UART0 clear to Send input pin.
	UART3_TXD	O	MFP7	UART3 data transmitter output pin.
	I2C2_SMBAL	O	MFP8	I2C2 SMBus SMBALTER pin
	EPWM1_CH0	I/O	MFP11	EPWM1 channel 0 output/capture input.
	TM0_EXT	I/O	MFP13	Timer0 external capture input/toggle output pin.
	USB_VBUS_EN	O	MFP14	USB external VBUS regulator enable pin.
PC.0	PC.0	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD0	I/O	MFP2	EBI address/data bus bit 0.
	QSPI0_MOSI0	I/O	MFP4	Quad SPI0 MOSI0 (Master Out, Slave In) pin.
	SC1_CLK	O	MFP5	Smart Card 1 clock pin.
	I2S0_LRCK	O	MFP6	I2S0 left right channel clock output pin.
	SPI1_SS	I/O	MFP7	SPI1 slave select pin.
	UART2_RXD	I	MFP8	UART2 data receiver input pin.
	I2C0_SDA	I/O	MFP9	I2C0 data input/output pin.
	EPWM1_CH5	I/O	MFP12	EPWM1 channel 5 output/capture input.
	ACMP1_O	O	MFP14	Analog comparator 1 output pin.
PC.1	PC.1	I/O	MFP0	General purpose digital I/O pin.

	Pin Name	Type	MFP	Description
	EBI_AD1	I/O	MFP2	EBI address/data bus bit 1.
	QSPI0_MISO0	I/O	MFP4	Quad SPI0 MISO0 (Master In, Slave Out) pin.
	SC1_DAT	I/O	MFP5	Smart Card 1 data pin.
	I2S0_DO	O	MFP6	I2S0 data output pin.
	SPI1_CLK	I/O	MFP7	SPI1 serial clock pin.
	UART2_TXD	O	MFP8	UART2 data transmitter output pin.
	I2C0_SCL	I/O	MFP9	I2C0 clock pin.
	EPWM1_CH4	I/O	MFP12	EPWM1 channel 4 output/capture input.
	ACMP0_O	O	MFP14	Analog comparator 0 output pin.
PC.2	PC.2	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD2	I/O	MFP2	EBI address/data bus bit 2.
	QSPI0_CLK	I/O	MFP4	Quad SPI0 serial clock pin.
	SC1_RST	O	MFP5	Smart Card 1 reset pin.
	I2S0_DI	I	MFP6	I2S0 data input pin.
	SPI1_MOSI	I/O	MFP7	SPI1 MOSI (Master Out, Slave In) pin.
	UART2_nCTS	I	MFP8	UART2 clear to Send input pin.
	I2C0_SMBSUS	O	MFP9	I2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
	UART3_RXD	I	MFP11	UART3 data receiver input pin.
	EPWM1_CH3	I/O	MFP12	EPWM1 channel 3 output/capture input.
PC.3	PC.3	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD3	I/O	MFP2	EBI address/data bus bit 3.
	QSPI0_SS	I/O	MFP4	Quad SPI0 slave select pin.
	SC1_PWR	O	MFP5	Smart Card 1 power pin.
	I2S0_MCLK	O	MFP6	I2S0 master clock output pin.
	SPI1_MISO	I/O	MFP7	SPI1 MISO (Master In, Slave Out) pin.
	UART2_nRTS	O	MFP8	UART2 request to Send output pin.
	I2C0_SMBAL	O	MFP9	I2C0 SMBus SMBALTER pin
	UART3_TXD	O	MFP11	UART3 data transmitter output pin.
	EPWM1_CH2	I/O	MFP12	EPWM1 channel 2 output/capture input.
PC.4	PC.4	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD4	I/O	MFP2	EBI address/data bus bit 4.
	QSPI0_MOSI1	I/O	MFP4	Quad SPI0 MOSI1 (Master Out, Slave In) pin.
	SC1_nCD	I	MFP5	Smart Card 1 card detect pin.
	I2S0_BCLK	O	MFP6	I2S0 bit clock output pin.

	Pin Name	Type	MFP	Description
	SPI1_I2SMCLK	I/O	MFP7	SPI1 I2S master clock output pin
	UART2_RXD	I	MFP8	UART2 data receiver input pin.
	I2C1_SDA	I/O	MFP9	I2C1 data input/output pin.
	CAN0_RXD	I	MFP10	CAN0 bus receiver input.
	UART4_RXD	I	MFP11	UART4 data receiver input pin.
	EPWM1_CH1	I/O	MFP12	EPWM1 channel 1 output/capture input.
PC.5	PC.5	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD5	I/O	MFP2	EBI address/data bus bit 5.
	QSPI0_MISO1	I/O	MFP4	Quad SPI0 MISO1 (Master In, Slave Out) pin.
	UART2_TXD	O	MFP8	UART2 data transmitter output pin.
	I2C1_SCL	I/O	MFP9	I2C1 clock pin.
	CAN0_TXD	O	MFP10	CAN0 bus transmitter output.
	UART4_TXD	O	MFP11	UART4 data transmitter output pin.
	EPWM1_CH0	I/O	MFP12	EPWM1 channel 0 output/capture input.
PC.6	PC.6	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD8	I/O	MFP2	EBI address/data bus bit 8.
	SPI1_MOSI	I/O	MFP4	SPI1 MOSI (Master Out, Slave In) pin.
	UART4_RXD	I	MFP5	UART4 data receiver input pin.
	SC2_RST	O	MFP6	Smart Card 2 reset pin.
	UART0_nRTS	O	MFP7	UART0 request to Send output pin.
	I2C1_SMBSUS	O	MFP8	I2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
	EPWM1_CH3	I/O	MFP11	EPWM1 channel 3 output/capture input.
	BPWM1_CH1	I/O	MFP12	BPWM1 channel 1 output/capture input.
	TM1	I/O	MFP14	Timer1 event counter input/toggle output pin.
	INT2	I	MFP15	External interrupt 2 input pin.
PC.7	PC.7	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD9	I/O	MFP2	EBI address/data bus bit 9.
	SPI1_MISO	I/O	MFP4	SPI1 MISO (Master In, Slave Out) pin.
	UART4_TXD	O	MFP5	UART4 data transmitter output pin.
	SC2_PWR	O	MFP6	Smart Card 2 power pin.
	UART0_nCTS	I	MFP7	UART0 clear to Send input pin.
	I2C1_SMBAL	O	MFP8	I2C1 SMBus SMBALTER pin
	EPWM1_CH2	I/O	MFP11	EPWM1 channel 2 output/capture input.
	BPWM1_CH0	I/O	MFP12	BPWM1 channel 0 output/capture input.

	Pin Name	Type	MFP	Description
	TM0	I/O	MFP14	Timer0 event counter input/toggle output pin.
	INT3	I	MFP15	External interrupt 3 input pin.
PC.8	PC.8	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR16	O	MFP2	EBI address bus bit 16.
	I2C0_SDA	I/O	MFP4	I2C0 data input/output pin.
	UART4_nCTS	I	MFP5	UART4 clear to Send input pin.
	UART1_RXD	I	MFP8	UART1 data receiver input pin.
	EPWM1_CH1	I/O	MFP11	EPWM1 channel 1 output/capture input.
	BPWM1_CH4	I/O	MFP12	BPWM1 channel 4 output/capture input.
PC.9	PC.9	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR7	O	MFP2	EBI address bus bit 7.
	SPI3_SS	I/O	MFP6	SPI3 slave select pin.
	UART3_RXD	I	MFP7	UART3 data receiver input pin.
	EPWM1_CH3	I/O	MFP12	EPWM1 channel 3 output/capture input.
PC.10	PC.10	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR6	O	MFP2	EBI address bus bit 6.
	SPI3_CLK	I/O	MFP6	SPI3 serial clock pin.
	UART3_TXD	O	MFP7	UART3 data transmitter output pin.
	ECAP1_IC0	I	MFP11	Enhanced capture unit 1 input 0 pin.
	EPWM1_CH2	I/O	MFP12	EPWM1 channel 2 output/capture input.
PC.11	PC.11	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR5	O	MFP2	EBI address bus bit 5.
	UART0_RXD	I	MFP3	UART0 data receiver input pin.
	I2C0_SDA	I/O	MFP4	I2C0 data input/output pin.
	SPI3_MOSI	I/O	MFP6	SPI3 MOSI (Master Out, Slave In) pin.
	ECAP1_IC1	I	MFP11	Enhanced capture unit 1 input 1 pin.
	EPWM1_CH1	I/O	MFP12	EPWM1 channel 1 output/capture input.
	ACMP1_O	O	MFP14	Analog comparator 1 output pin.
PC.12	PC.12	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR4	O	MFP2	EBI address bus bit 4.
	UART0_TXD	O	MFP3	UART0 data transmitter output pin.
	I2C0_SCL	I/O	MFP4	I2C0 clock pin.
	SPI3_MISO	I/O	MFP6	SPI3 MISO (Master In, Slave Out) pin.
	SC0_nCD	I	MFP9	Smart Card 0 card detect pin.

	Pin Name	Type	MFP	Description
	ECAP1_IC2	I	MFP11	Enhanced capture unit 1 input 2 pin.
	EPWM1_CH0	I/O	MFP12	EPWM1 channel 0 output/capture input.
	ACMP0_O	O	MFP14	Analog comparator 0 output pin.
PC.13	PC.13	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR10	O	MFP2	EBI address bus bit 10.
	SC2_nCD	I	MFP3	Smart Card 2 card detect pin.
	SPI2_I2SMCLK	I/O	MFP4	SPI2 I2S master clock output pin
	USCI0_CTL0	I/O	MFP6	USCI0 control 0 pin.
	UART2_TXD	O	MFP7	UART2 data transmitter output pin.
	BPWM0_CH4	I/O	MFP9	BPWM0 channel 4 output/capture input.
	CLKO	O	MFP13	Clock Out
	EADC0_ST	I	MFP14	EADC0 external trigger input.
PD.0	PD.0	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD13	I/O	MFP2	EBI address/data bus bit 13.
	USCI0_CLK	I/O	MFP3	USCI0 clock pin.
	SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
	UART3_RXD	I	MFP5	UART3 data receiver input pin.
	I2C2_SDA	I/O	MFP6	I2C2 data input/output pin.
	SC2_CLK	O	MFP7	Smart Card 2 clock pin.
	TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
PD.1	PD.1	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD12	I/O	MFP2	EBI address/data bus bit 12.
	USCI0_DAT0	I/O	MFP3	USCI0 data 0 pin.
	SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
	UART3_TXD	O	MFP5	UART3 data transmitter output pin.
	I2C2_SCL	I/O	MFP6	I2C2 clock pin.
	SC2_DAT	I/O	MFP7	Smart Card 2 data pin.
PD.2	PD.2	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD11	I/O	MFP2	EBI address/data bus bit 11.
	USCI0_DAT1	I/O	MFP3	USCI0 data 1 pin.
	SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
	UART3_nCTS	I	MFP5	UART3 clear to Send input pin.
	SC2_RST	O	MFP7	Smart Card 2 reset pin.
	UART0_RXD	I	MFP9	UART0 data receiver input pin.

	Pin Name	Type	MFP	Description
PD.3	PD.3	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD10	I/O	MFP2	EBI address/data bus bit 10.
	USCI0_CTL1	I/O	MFP3	USCI0 control 1 pin.
	SPI0_SS	I/O	MFP4	SPI0 slave select pin.
	UART3_nRTS	O	MFP5	UART3 request to Send output pin.
	USCI1_CTL0	I/O	MFP6	USCI1 control 0 pin.
	SC2_PWR	O	MFP7	Smart Card 2 power pin.
	SC1_nCD	I	MFP8	Smart Card 1 card detect pin.
	UART0_TXD	O	MFP9	UART0 data transmitter output pin.
PD.4	PD.4	I/O	MFP0	General purpose digital I/O pin.
	USCI0_CTL0	I/O	MFP3	USCI0 control 0 pin.
	I2C1_SDA	I/O	MFP4	I2C1 data input/output pin.
	SPI1_SS	I/O	MFP5	SPI1 slave select pin.
	USCI1_CTL1	I/O	MFP6	USCI1 control 1 pin.
	SC1_CLK	O	MFP8	Smart Card 1 clock pin.
	USB_VBUS_ST	I	MFP14	USB external VBUS regulator status pin.
PD.5	PD.5	I/O	MFP0	General purpose digital I/O pin.
	I2C1_SCL	I/O	MFP4	I2C1 clock pin.
	SPI1_CLK	I/O	MFP5	SPI1 serial clock pin.
	USCI1_DAT0	I/O	MFP6	USCI1 data 0 pin.
	SC1_DAT	I/O	MFP8	Smart Card 1 data pin.
PD.6	PD.6	I/O	MFP0	General purpose digital I/O pin.
	UART1_RXD	I	MFP3	UART1 data receiver input pin.
	I2C0_SDA	I/O	MFP4	I2C0 data input/output pin.
	SPI1_MOSI	I/O	MFP5	SPI1 MOSI (Master Out, Slave In) pin.
	USCI1_DAT1	I/O	MFP6	USCI1 data 1 pin.
	SC1_RST	O	MFP8	Smart Card 1 reset pin.
PD.7	PD.7	I/O	MFP0	General purpose digital I/O pin.
	UART1_TXD	O	MFP3	UART1 data transmitter output pin.
	I2C0_SCL	I/O	MFP4	I2C0 clock pin.
	SPI1_MISO	I/O	MFP5	SPI1 MISO (Master In, Slave Out) pin.
	USCI1_CLK	I/O	MFP6	USCI1 clock pin.
	SC1_PWR	O	MFP8	Smart Card 1 power pin.
PD.8	PD.8	I/O	MFP0	General purpose digital I/O pin.

	Pin Name	Type	MFP	Description
	EBI_AD6	I/O	MFP2	EBI address/data bus bit 6.
	I2C2_SDA	I/O	MFP3	I2C2 data input/output pin.
	UART2_nRTS	O	MFP4	UART2 request to Send output pin.
PD.9	PD.9	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD7	I/O	MFP2	EBI address/data bus bit 7.
	I2C2_SCL	I/O	MFP3	I2C2 clock pin.
	UART2_nCTS	I	MFP4	UART2 clear to Send input pin.
PD.10	PD.10	I/O	MFP0	General purpose digital I/O pin.
	EBI_nCS2	O	MFP2	EBI chip select 2 output pin.
	UART1_RXD	I	MFP3	UART1 data receiver input pin.
	CAN0_RXD	I	MFP4	CAN0 bus receiver input.
	QEI0_B	I	MFP10	Quadrature encoder 0 phase B input
	INT7	I	MFP15	External interrupt 7 input pin.
PD.11	PD.11	I/O	MFP0	General purpose digital I/O pin.
	EBI_nCS1	O	MFP2	EBI chip select 1 output pin.
	UART1_TXD	O	MFP3	UART1 data transmitter output pin.
	CAN0_TXD	O	MFP4	CAN0 bus transmitter output.
	QEI0_A	I	MFP10	Quadrature encoder 0 phase A input
	INT6	I	MFP15	External interrupt 6 input pin.
PD.12	PD.12	I/O	MFP0	General purpose digital I/O pin.
	EBI_nCS0	O	MFP2	EBI chip select 0 output pin.
	UART2_RXD	I	MFP7	UART2 data receiver input pin.
	BPWM0_CH5	I/O	MFP9	BPWM0 channel 5 output/capture input.
	QEI0_INDEX	I	MFP10	Quadrature encoder 0 index input
	CLKO	O	MFP13	Clock Out
	EADC0_ST	I	MFP14	EADC0 external trigger input.
	INT5	I	MFP15	External interrupt 5 input pin.
PD.13	PD.13	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD10	I/O	MFP2	EBI address/data bus bit 10.
	SD0_nCD	I	MFP3	SD/SDIO0 card detect input pin
	SPI0_I2SMCLK	I/O	MFP4	SPI0 I2S master clock output pin
	SPI1_I2SMCLK	I/O	MFP5	SPI1 I2S master clock output pin
	SC2_nCD	I	MFP7	Smart Card 2 card detect pin.
PD.14	PD.14	I/O	MFP0	General purpose digital I/O pin.

	Pin Name	Type	MFP	Description
	EBI_nCS0	O	MFP2	EBI chip select 0 output pin.
	SPI3_I2SMCLK	I/O	MFP3	SPI3 I2S master clock output pin
	SC1_nCD	I	MFP4	Smart Card 1 card detect pin.
	USCI0_CTL0	I/O	MFP5	USCI0 control 0 pin.
	SPI0_I2SMCLK	I/O	MFP6	SPI0 I2S master clock output pin
	EPWM0_CH4	I/O	MFP11	EPWM0 channel 4 output/capture input.
PE.0	PE.0	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD11	I/O	MFP2	EBI address/data bus bit 11.
	QSPI0_MOSI0	I/O	MFP3	Quad SPI0 MOSI0 (Master Out, Slave In) pin.
	SC2_CLK	O	MFP4	Smart Card 2 clock pin.
	I2S0_MCLK	O	MFP5	I2S0 master clock output pin.
	SPI1_MOSI	I/O	MFP6	SPI1 MOSI (Master Out, Slave In) pin.
	UART3_RXD	I	MFP7	UART3 data receiver input pin.
	I2C1_SDA	I/O	MFP8	I2C1 data input/output pin.
	UART4_nRTS	O	MFP9	UART4 request to Send output pin.
PE.1	PE.1	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD10	I/O	MFP2	EBI address/data bus bit 10.
	QSPI0_MISO0	I/O	MFP3	Quad SPI0 MISO0 (Master In, Slave Out) pin.
	SC2_DAT	I/O	MFP4	Smart Card 2 data pin.
	I2S0_BCLK	O	MFP5	I2S0 bit clock output pin.
	SPI1_MISO	I/O	MFP6	SPI1 MISO (Master In, Slave Out) pin.
	UART3_TXD	O	MFP7	UART3 data transmitter output pin.
	I2C1_SCL	I/O	MFP8	I2C1 clock pin.
	UART4_nCTS	I	MFP9	UART4 clear to Send input pin.
PE.2	PE.2	I/O	MFP0	General purpose digital I/O pin.
	EBI_ALE	O	MFP2	EBI address latch enable output pin.
	SD0_DAT0	I/O	MFP3	SD/SDIO0 data line bit 0.
	SPI3_MOSI	I/O	MFP5	SPI3 MOSI (Master Out, Slave In) pin.
	SC0_CLK	O	MFP6	Smart Card 0 clock pin.
	USCI0_CLK	I/O	MFP7	USCI0 clock pin.
	QEI0_B	I	MFP11	Quadrature encoder 0 phase B input
	EPWM0_CH5	I/O	MFP12	EPWM0 channel 5 output/capture input.
	BPWM0_CH0	I/O	MFP13	BPWM0 channel 0 output/capture input.
PE.3	PE.3	I/O	MFP0	General purpose digital I/O pin.

	Pin Name	Type	MFP	Description
	EBI_MCLK	O	MFP2	EBI external clock output pin.
	SD0_DAT1	I/O	MFP3	SD/SDIO0 data line bit 1.
	SPI3_MISO	I/O	MFP5	SPI3 MISO (Master In, Slave Out) pin.
	SC0_DAT	I/O	MFP6	Smart Card 0 data pin.
	USCI0_DAT0	I/O	MFP7	USCI0 data 0 pin.
	QEI0_A	I	MFP11	Quadrature encoder 0 phase A input
	EPWM0_CH4	I/O	MFP12	EPWM0 channel 4 output/capture input.
	BPWM0_CH1	I/O	MFP13	BPWM0 channel 1 output/capture input.
PE.4	PE.4	I/O	MFP0	General purpose digital I/O pin.
	EBI_nWR	O	MFP2	EBI write enable output pin.
	SD0_DAT2	I/O	MFP3	SD/SDIO0 data line bit 2.
	SPI3_CLK	I/O	MFP5	SPI3 serial clock pin.
	SC0_RST	O	MFP6	Smart Card 0 reset pin.
	USCI0_DAT1	I/O	MFP7	USCI0 data 1 pin.
	QEI0_INDEX	I	MFP11	Quadrature encoder 0 index input
	EPWM0_CH3	I/O	MFP12	EPWM0 channel 3 output/capture input.
	BPWM0_CH2	I/O	MFP13	BPWM0 channel 2 output/capture input.
PE.5	PE.5	I/O	MFP0	General purpose digital I/O pin.
	EBI_nRD	O	MFP2	EBI read enable output pin.
	SD0_DAT3	I/O	MFP3	SD/SDIO0 data line bit 3.
	SPI3_SS	I/O	MFP5	SPI3 slave select pin.
	SC0_PWR	O	MFP6	Smart Card 0 power pin.
	USCI0_CTL1	I/O	MFP7	USCI0 control 1 pin.
	QEI1_B	I	MFP11	Quadrature encoder 1 phase B input
	EPWM0_CH2	I/O	MFP12	EPWM0 channel 2 output/capture input.
	BPWM0_CH3	I/O	MFP13	BPWM0 channel 3 output/capture input.
PE.6	PE.6	I/O	MFP0	General purpose digital I/O pin.
	SD0_CLK	O	MFP3	SD/SDIO0 clock output pin
	SPI3_I2SMCLK	I/O	MFP5	SPI3 I2S master clock output pin
	SC0_nCD	I	MFP6	Smart Card 0 card detect pin.
	USCI0_CTL0	I/O	MFP7	USCI0 control 0 pin.
	UART5_RXD	I	MFP8	UART5 data receiver input pin.
	QEI1_A	I	MFP11	Quadrature encoder 1 phase A input
	EPWM0_CH1	I/O	MFP12	EPWM0 channel 1 output/capture input.

	Pin Name	Type	MFP	Description
	BPWM0_CH4	I/O	MFP13	BPWM0 channel 4 output/capture input.
PE.7	PE.7	I/O	MFP0	General purpose digital I/O pin.
	SD0_CMD	I/O	MFP3	SD/SDIO0 command/response pin
	UART5_TXD	O	MFP8	UART5 data transmitter output pin.
	QEI1_INDEX	I	MFP11	Quadrature encoder 1 index input
	EPWM0_CH0	I/O	MFP12	EPWM0 channel 0 output/capture input.
	BPWM0_CH5	I/O	MFP13	BPWM0 channel 5 output/capture input.
PE.8	PE.8	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR10	O	MFP2	EBI address bus bit 10.
	I2S0_BCLK	O	MFP4	I2S0 bit clock output pin.
	SPI2_CLK	I/O	MFP5	SPI2 serial clock pin.
	USCI1_CTL1	I/O	MFP6	USCI1 control 1 pin.
	UART2_TXD	O	MFP7	UART2 data transmitter output pin.
	EPWM0_CH0	I/O	MFP10	EPWM0 channel 0 output/capture input.
	EPWM0_BRAKE0	I	MFP11	EPWM0 Brake 0 input pin.
	ECAP0_IC0	I	MFP12	Enhanced capture unit 0 input 0 pin.
	TRACE_DATA3	O	MFP14	ETM Trace Data 3 output pin
PE.9	PE.9	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR11	O	MFP2	EBI address bus bit 11.
	I2S0_MCLK	O	MFP4	I2S0 master clock output pin.
	SPI2_MISO	I/O	MFP5	SPI2 MISO (Master In, Slave Out) pin.
	USCI1_CTL0	I/O	MFP6	USCI1 control 0 pin.
	UART2_RXD	I	MFP7	UART2 data receiver input pin.
	EPWM0_CH1	I/O	MFP10	EPWM0 channel 1 output/capture input.
	EPWM0_BRAKE1	I	MFP11	EPWM0 Brake 1 input pin.
	ECAP0_IC1	I	MFP12	Enhanced capture unit 0 input 1 pin.
	TRACE_DATA2	O	MFP14	ETM Trace Data 2 output pin
PE.10	PE.10	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR12	O	MFP2	EBI address bus bit 12.
	I2S0_DI	I	MFP4	I2S0 data input pin.
	SPI2_MOSI	I/O	MFP5	SPI2 MOSI (Master Out, Slave In) pin.
	USCI1_DAT0	I/O	MFP6	USCI1 data 0 pin.
	UART3_TXD	O	MFP7	UART3 data transmitter output pin.
	EPWM0_CH2	I/O	MFP10	EPWM0 channel 2 output/capture input.

	Pin Name	Type	MFP	Description
	EPWM1_BRAKE0	I	MFP11	EPWM1 Brake 0 input pin.
	ECAP0_IC2	I	MFP12	Enhanced capture unit 0 input 2 pin.
	TRACE_DATA1	O	MFP14	ETM Trace Data 1 output pin
PE.11	PE.11	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR13	O	MFP2	EBI address bus bit 13.
	I2S0_DO	O	MFP4	I2S0 data output pin.
	SPI2_SS	I/O	MFP5	SPI2 slave select pin.
	USCI1_DAT1	I/O	MFP6	USCI1 data 1 pin.
	UART3_RXD	I	MFP7	UART3 data receiver input pin.
	UART1_nCTS	I	MFP8	UART1 clear to Send input pin.
	EPWM0_CH3	I/O	MFP10	EPWM0 channel 3 output/capture input.
	EPWM1_BRAKE1	I	MFP11	EPWM1 Brake 1 input pin.
	ECAP1_IC2	I	MFP13	Enhanced capture unit 1 input 2 pin.
	TRACE_DATA0	O	MFP14	ETM Trace Data 0 output pin
PE.12	PE.12	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR14	O	MFP2	EBI address bus bit 14.
	I2S0_LRCK	O	MFP4	I2S0 left right channel clock output pin.
	SPI2_I2SMCLK	I/O	MFP5	SPI2 I2S master clock output pin
	USCI1_CLK	I/O	MFP6	USCI1 clock pin.
	UART1_nRTS	O	MFP8	UART1 request to Send output pin.
	EPWM0_CH4	I/O	MFP10	EPWM0 channel 4 output/capture input.
	ECAP1_IC1	I	MFP13	Enhanced capture unit 1 input 1 pin.
	TRACE_CLK	O	MFP14	ETM Trace Clock output pin
PE.13	PE.13	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR15	O	MFP2	EBI address bus bit 15.
	I2C0_SCL	I/O	MFP4	I2C0 clock pin.
	UART4_nRTS	O	MFP5	UART4 request to Send output pin.
	UART1_TXD	O	MFP8	UART1 data transmitter output pin.
	EPWM0_CH5	I/O	MFP10	EPWM0 channel 5 output/capture input.
	EPWM1_CH0	I/O	MFP11	EPWM1 channel 0 output/capture input.
	BPWM1_CH5	I/O	MFP12	BPWM1 channel 5 output/capture input.
	ECAP1_IC0	I	MFP13	Enhanced capture unit 1 input 0 pin.
PE.14	PE.14	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD8	I/O	MFP2	EBI address/data bus bit 8.

	Pin Name	Type	MFP	Description
	UART2_TXD	O	MFP3	UART2 data transmitter output pin.
	CAN0_TXD	O	MFP4	CAN0 bus transmitter output.
PE.15	PE.15	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD9	I/O	MFP2	EBI address/data bus bit 9.
	UART2_RXD	I	MFP3	UART2 data receiver input pin.
	CAN0_RXD	I	MFP4	CAN0 bus receiver input.
PF.0	PF.0	I/O	MFP0	General purpose digital I/O pin.
	UART1_TXD	O	MFP2	UART1 data transmitter output pin.
	I2C1_SCL	I/O	MFP3	I2C1 clock pin.
	BPWM1_CH0	I/O	MFP12	BPWM1 channel 0 output/capture input.
	ICE_DAT	O	MFP14	Serial wired debugger data pin.
PF.1	PF.1	I/O	MFP0	General purpose digital I/O pin.
	UART1_RXD	I	MFP2	UART1 data receiver input pin.
	I2C1_SDA	I/O	MFP3	I2C1 data input/output pin.
	BPWM1_CH1	I/O	MFP12	BPWM1 channel 1 output/capture input.
	ICE_CLK	I	MFP14	Serial wired debugger clock pin.
PF.2	PF.2	I/O	MFP0	General purpose digital I/O pin.
	EBI_nCS1	O	MFP2	EBI chip select 1 output pin.
	UART0_RXD	I	MFP3	UART0 data receiver input pin.
	I2C0_SDA	I/O	MFP4	I2C0 data input/output pin.
	QSPI0_CLK	I/O	MFP5	Quad SPI0 serial clock pin.
	XT1_OUT	O	MFP10	External 4~24 MHz (high speed) crystal output pin.
	BPWM1_CH1	I/O	MFP11	BPWM1 channel 1 output/capture input.
PF.3	PF.3	I/O	MFP0	General purpose digital I/O pin.
	EBI_nCS0	O	MFP2	EBI chip select 0 output pin.
	UART0_TXD	O	MFP3	UART0 data transmitter output pin.
	I2C0_SCL	I/O	MFP4	I2C0 clock pin.
	XT1_IN	I	MFP10	External 4~24 MHz (high speed) crystal input pin.
	BPWM1_CH0	I/O	MFP11	BPWM1 channel 0 output/capture input.
PF.4	PF.4	I/O	MFP0	General purpose digital I/O pin.
	UART2_TXD	O	MFP2	UART2 data transmitter output pin.
	UART2_nRTS	O	MFP4	UART2 request to Send output pin.
	BPWM0_CH5	I/O	MFP8	BPWM0 channel 5 output/capture input.
	X32_OUT	O	MFP10	External 32.768 kHz crystal output pin.

	Pin Name	Type	MFP	Description
PF.5	PF.5	I/O	MFP0	General purpose digital I/O pin.
	UART2_RXD	I	MFP2	UART2 data receiver input pin.
	UART2_nCTS	I	MFP4	UART2 clear to Send input pin.
	BPWM0_CH4	I/O	MFP8	BPWM0 channel 4 output/capture input.
	EPWM0_SYNC_OUT	O	MFP9	EPWM0 counter synchronous trigger output pin.
	X32_IN	I	MFP10	External 32.768 kHz crystal input pin.
	EADC0_ST	I	MFP11	EADC0 external trigger input.
PF.6	PF.6	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR19	O	MFP2	EBI address bus bit 19.
	SC0_CLK	O	MFP3	Smart Card 0 clock pin.
	I2S0_LRCK	O	MFP4	I2S0 left right channel clock output pin.
	SPI0_MOSI	I/O	MFP5	SPI0 MOSI (Master Out, Slave In) pin.
	UART4_RXD	I	MFP6	UART4 data receiver input pin.
	EBI_nCS0	O	MFP7	EBI chip select 0 output pin.
	TAMPER0	I/O	MFP10	TAMPER detector loop pin 0.
PF.7	PF.7	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR18	O	MFP2	EBI address bus bit 18.
	SC0_DAT	I/O	MFP3	Smart Card 0 data pin.
	I2S0_DO	O	MFP4	I2S0 data output pin.
	SPI0_MISO	I/O	MFP5	SPI0 MISO (Master In, Slave Out) pin.
	UART4_TXD	O	MFP6	UART4 data transmitter output pin.
	TAMPER1	I/O	MFP10	TAMPER detector loop pin 1.
PF.8	PF.8	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR17	O	MFP2	EBI address bus bit 17.
	SC0_RST	O	MFP3	Smart Card 0 reset pin.
	I2S0_DI	I	MFP4	I2S0 data input pin.
	SPI0_CLK	I/O	MFP5	SPI0 serial clock pin.
	TAMPER2	I/O	MFP10	TAMPER detector loop pin 2.
PF.9	PF.9	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR16	O	MFP2	EBI address bus bit 16.
	SC0_PWR	O	MFP3	Smart Card 0 power pin.
	I2S0_MCLK	O	MFP4	I2S0 master clock output pin.
	SPI0_SS	I/O	MFP5	SPI0 slave select pin.
	TAMPER3	I/O	MFP10	TAMPER detector loop pin 3.

	Pin Name	Type	MFP	Description
PF.10	PF.10	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR15	O	MFP2	EBI address bus bit 15.
	SC0_nCD	I	MFP3	Smart Card 0 card detect pin.
	I2S0_BCLK	O	MFP4	I2S0 bit clock output pin.
	SPI0_I2SMCLK	I/O	MFP5	SPI0 I2S master clock output pin
	TAMPER4	I/O	MFP10	TAMPER detector loop pin 4.
PF.11	PF.11	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR14	O	MFP2	EBI address bus bit 14.
	SPI2_MOSI	I/O	MFP3	SPI2 MOSI (Master Out, Slave In) pin.
	TAMPER5	I/O	MFP10	TAMPER detector loop pin 5.
	TM3	I/O	MFP13	Timer3 event counter input/toggle output pin.
PG.2	PG.2	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR11	O	MFP2	EBI address bus bit 11.
	SPI2_SS	I/O	MFP3	SPI2 slave select pin.
	I2C0_SMBAL	O	MFP4	I2C0 SMBus SMBALTER pin
	I2C1_SCL	I/O	MFP5	I2C1 clock pin.
	TM0	I/O	MFP13	Timer0 event counter input/toggle output pin.
PG.3	PG.3	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR12	O	MFP2	EBI address bus bit 12.
	SPI2_CLK	I/O	MFP3	SPI2 serial clock pin.
	I2C0_SMBSUS	O	MFP4	I2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
	I2C1_SDA	I/O	MFP5	I2C1 data input/output pin.
	TM1	I/O	MFP13	Timer1 event counter input/toggle output pin.
PG.4	PG.4	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR13	O	MFP2	EBI address bus bit 13.
	SPI2_MISO	I/O	MFP3	SPI2 MISO (Master In, Slave Out) pin.
	TM2	I/O	MFP13	Timer2 event counter input/toggle output pin.
PG.9	PG.9	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD0	I/O	MFP2	EBI address/data bus bit 0.
	BPWM0_CH5	I/O	MFP12	BPWM0 channel 5 output/capture input.
PG.10	PG.10	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD1	I/O	MFP2	EBI address/data bus bit 1.
	BPWM0_CH4	I/O	MFP12	BPWM0 channel 4 output/capture input.
PG.11	PG.11	I/O	MFP0	General purpose digital I/O pin.

	Pin Name	Type	MFP	Description
	EBI_AD2	I/O	MFP2	EBI address/data bus bit 2.
	BPWM0_CH3	I/O	MFP12	BPWM0 channel 3 output/capture input.
PG.12	PG.12	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD3	I/O	MFP2	EBI address/data bus bit 3.
	BPWM0_CH2	I/O	MFP12	BPWM0 channel 2 output/capture input.
PG.13	PG.13	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD4	I/O	MFP2	EBI address/data bus bit 4.
	BPWM0_CH1	I/O	MFP12	BPWM0 channel 1 output/capture input.
PG.14	PG.14	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD5	I/O	MFP2	EBI address/data bus bit 5.
	BPWM0_CH0	I/O	MFP12	BPWM0 channel 0 output/capture input.
PG.15	PG.15	I/O	MFP0	General purpose digital I/O pin.
	CLKO	O	MFP14	Clock Out
	EADC0_ST	I	MFP15	EADC0 external trigger input.
PH.4	PH.4	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR3	O	MFP2	EBI address bus bit 3.
	SPI1_MISO	I/O	MFP3	SPI1 MISO (Master In, Slave Out) pin.
PH.5	PH.5	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR2	O	MFP2	EBI address bus bit 2.
	SPI1_MOSI	I/O	MFP3	SPI1 MOSI (Master Out, Slave In) pin.
PH.6	PH.6	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR1	O	MFP2	EBI address bus bit 1.
	SPI1_CLK	I/O	MFP3	SPI1 serial clock pin.
PH.7	PH.7	I/O	MFP0	General purpose digital I/O pin.
	EBI_ADR0	O	MFP2	EBI address bus bit 0.
	SPI1_SS	I/O	MFP3	SPI1 slave select pin.
PH.8	PH.8	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD12	I/O	MFP2	EBI address/data bus bit 12.
	QSPI0_CLK	I/O	MFP3	Quad SPI0 serial clock pin.
	SC2_PWR	O	MFP4	Smart Card 2 power pin.
	I2S0_DI	I	MFP5	I2S0 data input pin.
	SPI1_CLK	I/O	MFP6	SPI1 serial clock pin.
	UART3_nRTS	O	MFP7	UART3 request to Send output pin.
	I2C1_SMBAL	O	MFP8	I2C1 SMBus SMBALTER pin

	Pin Name	Type	MFP	Description
	I2C2_SCL	I/O	MFP9	I2C2 clock pin.
	UART1_TXD	O	MFP10	UART1 data transmitter output pin.
PH.9	PH.9	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD13	I/O	MFP2	EBI address/data bus bit 13.
	QSPI0_SS	I/O	MFP3	Quad SPI0 slave select pin.
	SC2_RST	O	MFP4	Smart Card 2 reset pin.
	I2S0_DO	O	MFP5	I2S0 data output pin.
	SPI1_SS	I/O	MFP6	SPI1 slave select pin.
	UART3_nCTS	I	MFP7	UART3 clear to Send input pin.
	I2C1_SMBSUS	O	MFP8	I2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
	I2C2_SDA	I/O	MFP9	I2C2 data input/output pin.
	UART1_RXD	I	MFP10	UART1 data receiver input pin.
PH.10	PH.10	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD14	I/O	MFP2	EBI address/data bus bit 14.
	QSPI0_MISO1	I/O	MFP3	Quad SPI0 MISO1 (Master In, Slave Out) pin.
	SC2_nCD	I	MFP4	Smart Card 2 card detect pin.
	I2S0_LRCK	O	MFP5	I2S0 left right channel clock output pin.
	SPI1_I2SMCLK	I/O	MFP6	SPI1 I2S master clock output pin
	UART4_TXD	O	MFP7	UART4 data transmitter output pin.
	UART0_TXD	O	MFP8	UART0 data transmitter output pin.
PH.11	PH.11	I/O	MFP0	General purpose digital I/O pin.
	EBI_AD15	I/O	MFP2	EBI address/data bus bit 15.
	QSPI0_MOSI1	I/O	MFP3	Quad SPI0 MOSI1 (Master Out, Slave In) pin.
	UART4_RXD	I	MFP7	UART4 data receiver input pin.
	UART0_RXD	I	MFP8	UART0 data receiver input pin.
	EPWM0_CH5	I/O	MFP11	EPWM0 channel 5 output/capture input.

5 BLOCK DIAGRAM

5.1 NuMicro® M2351 Series Block Diagram

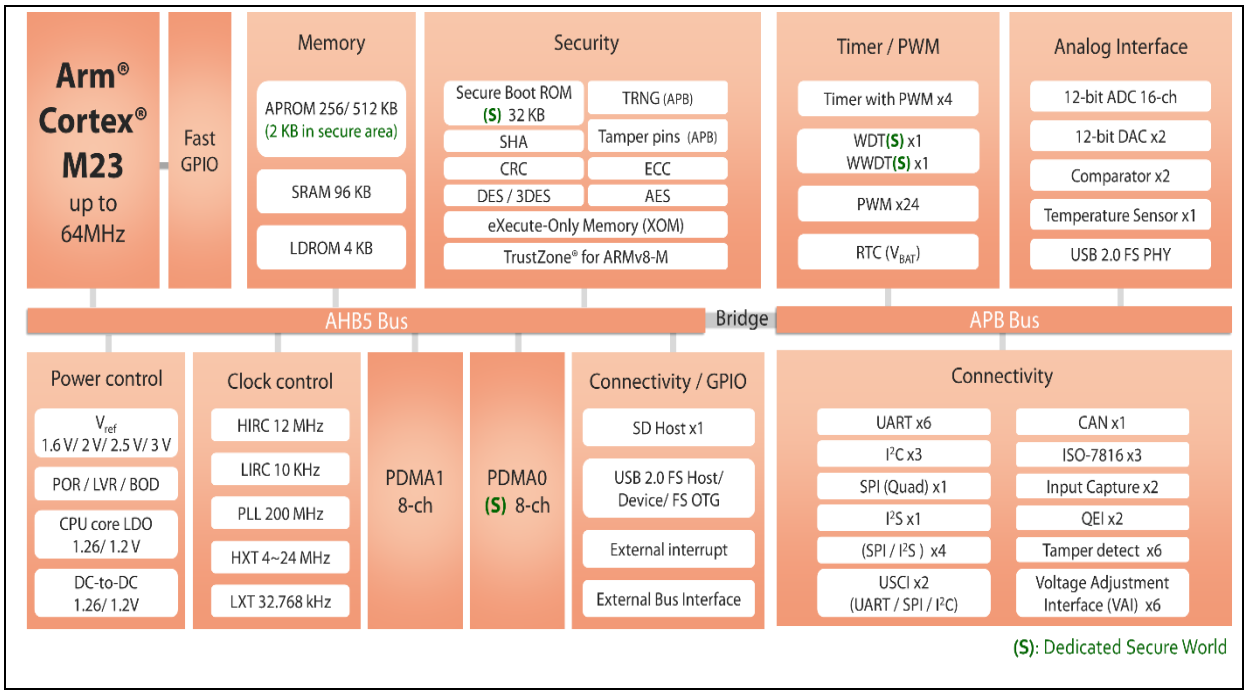


Figure 5.1-1 NuMicro® M2351 Block Diagram

5.2 NuMicro® M2351 Series TrustZone® Architecture

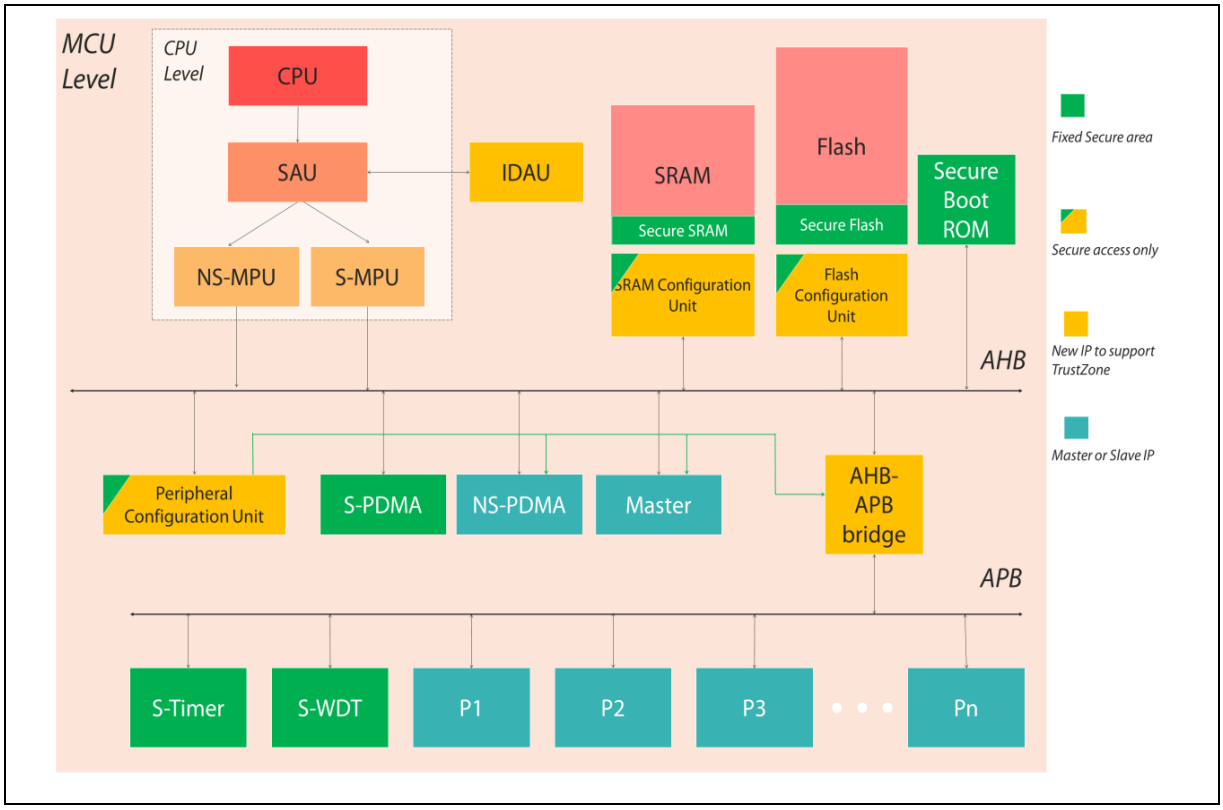


Figure 5.2-1 NuMicro® M2351 Series Cortex®-M23 Architecture

6 FUNCTIONAL DESCRIPTION

6.1 Arm® Cortex®-M23 Core

The NuMicro® M2351 series is embedded with the Cortex®-M23 processor. The Cortex®-M23 processor is a low gate count, two-stage, and highly energy efficient 32-bit RISC processor, which has an AMBA AHB5 interface supporting Arm® TrustZone® technology, a debug access port supporting serial wire debug and single-cycle I/O ports. It has an NVIC component and MPU for memory-protection functionality. The processor also supports Security Extension. Figure 6.1-1 shows the functional controller of the processor.

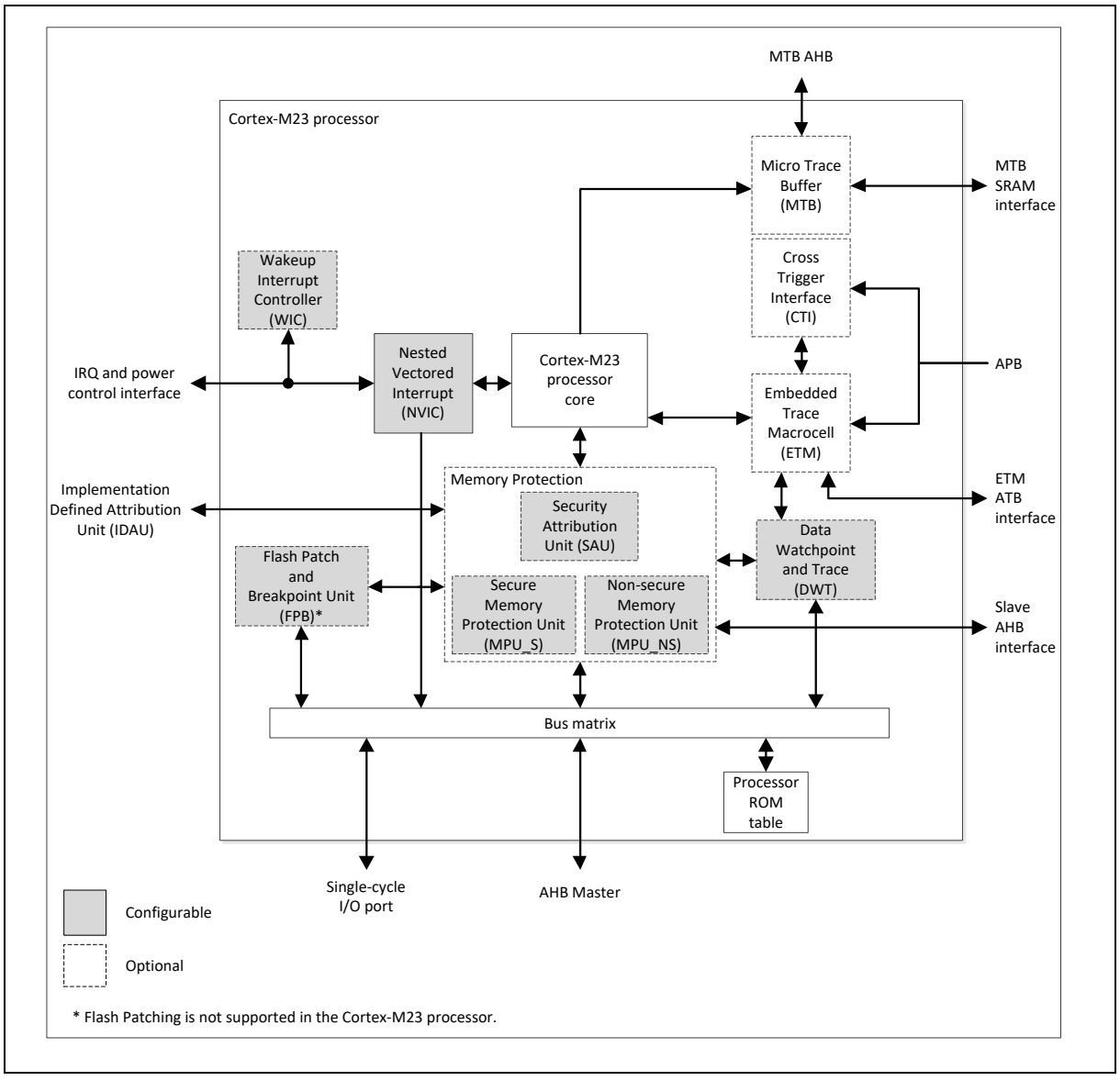


Figure 6.1-1 Cortex®-M23 Block Diagram

Cortex®-M23 processor features:

- Arm®v8-M Baseline architecture.
- Arm®v8-M Baseline Thumb®-2 instruction set that combines high code density with 32-bit performance.
- Support for single-cycle I/O access.
- Power control optimization of system components.
- Integrated sleep modes for low power consumption.
- Optimized code fetching for reduced Flash and ROM power consumption.
- 32-bit Single cycle Hardware multiplier.
- 32-bit Hardware divider.
- Deterministic, high-performance interrupt handling for time-critical applications.
- Deterministic instruction cycle timing.
- Support for system level debug authentication.
- Support for Arm® Debug Interface Architecture ADIv5.1 Serial Wire Debug (SWD).
- ETM for instruction trace.
- Separated privileged and unprivileged modes.
- Security Extension supporting a Secure and a Non-secure state.
- Protected Memory System Architecture (PMSAv8) Memory Protection Units (MPUs) for both Secure and Non-secure states.
- Security Attribution Unit (SAU).
- SysTick timers for both Secure and Non-secure states.
- A Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor with up to 240 interrupts.

6.2 Arm® TrustZone®

The Arm® TrustZone® can be considered as a physical partition that divides the microcontroller into **Secure** (Trusted) and **Non-secure** (Non-trusted) worlds according to memory address. The secure world is an isolated execution environment, code and data loaded inside are protected and cannot be accessed from Non-secure world. Code running at secure world is called secure code that can access both secure and non-secure memories and peripherals; while code running at non-secure world is called non-secure code that can only access non-secure memories and peripherals.

Figure 6.2-1 shows an example of a system divided into the secure world and non-secure world. Green blocks indicate secure components, Red blocks indicate non-secure components and white ones are both/either secure and/or non-secure accessible. When the core processor is in secure state (left side of the figure), it belongs to secure world, which has its own MSP, PSP and VTOR registers and can access the green, red, white blocks. Contrarily, when the core processor is in non-secure state (right side of the figure), it belongs to non-secure world, which also has its own MSP, PSP and VTOR registers, but, it can only access red and white blocks so that non-secure world components are not able to impact secure world.

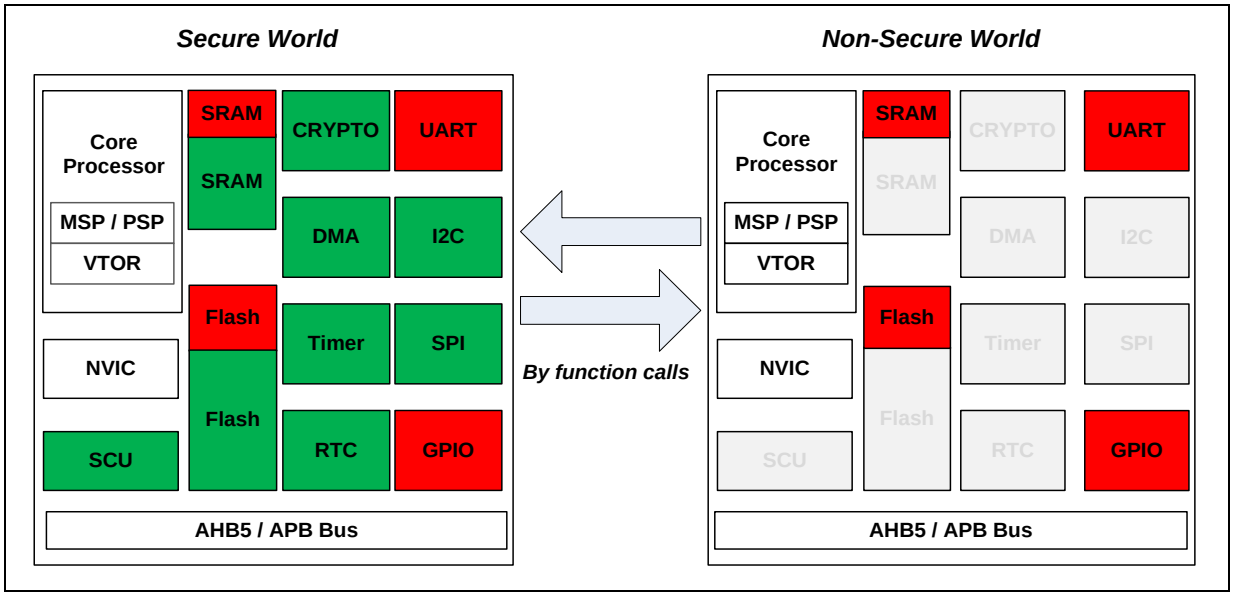


Figure 6.2-1 Secure World View and Non-secure World View on a Chip

In order to support TrustZone® to set up both secure world and non-secure world, Cortex®-M23 provides three security attributes. Each memory address is assigned with one of the security attributes. These security attributes are listed below.

- Non-secure (NS)

  Addresses used for non-secure memory or non-secure peripheral's registers.

- Secure (S)

  Addresses used for secure memory or secure peripheral's registers.

- Non-secure Callable (NSC)

  A special type of secure memory region which can contain SG instructions. The SG instruction allows a non-secure function calls to a secure function.

The address space partitioning is completed by Implementation Define Attribution Unit (IDAU) and Security Attribution Unit (SAU) together. The IDAU is non-programmable, which defines static partition of address space. The static partition specifies the default security attribute of a memory region. In contrast with IDAU, the SAU is programmable which provides dynamic partition of address space. The

dynamic partition is given by software programmer to specify the security attribute of a memory region. The core processor is in secure state when executing instructions from secure memory. Otherwise, the core processor is in non-secure state when executing instructions from non-secure memory. For setting IDAU and SAU, refer to sections “Implementation Defined Attribution Unit (IDAU)” and “Security Attribution Unit (SAU)” in “System Manager” chapter for more details.

The security attribute of Flash, SRAM and peripherals are assigned by TrustZone® related control units. The NSCBA register in FMC is used to divide the APROM into two parts, one is secure and the other is non-secure. The security attribute of SRAM and peripherals are assigned by programming Secure Configuration Unit (SCU).

Whenever being reset, the M2351 is in secure state, that is, the core processor, Flash, SRAM and peripherals are all in secure state. Therefore, the system boots in secure state. The boot code is responsible to set up TrustZone® related control units in M2351 to partition address space and assign non-secure resources that can be directly accessed from non-secure world.

6.2.1 Address Space Partition

The SAU and IDAU are the control units used to define security attribute of memory addresses. The IDAU defines default partition of secure and non-secure addresses, while the SAU is programmable to change the security attribute defined by IDAU.

6.2.1.1 Implementation Define Attribution Unit (IDAU)

The IDAU uses address bit 28 to distinguish between secure and non-secure world, i.e. the bit 28 of a secure address is always 0, and the bit 28 of a non-secure address is always 1, except regions above 0xE000_0000.

The partition of 4GB address space is shown as Figure 6.2-2. Each region consists of a secure (bit 28 is 0) and a non-secure (bit 28 is 1) sub-regions, the size of a sub-region is 256MB. In order to store entry functions for non-secure code, the security attribute of secure SRAM region is assigned as non-secure callable (**NSC**). Similarly, the secure “Code” region is assigned as NSC but has an exception at first 2 KB area. This first 2 KB area is defined as secure only to avoid accidental **SG** instruction after power on.

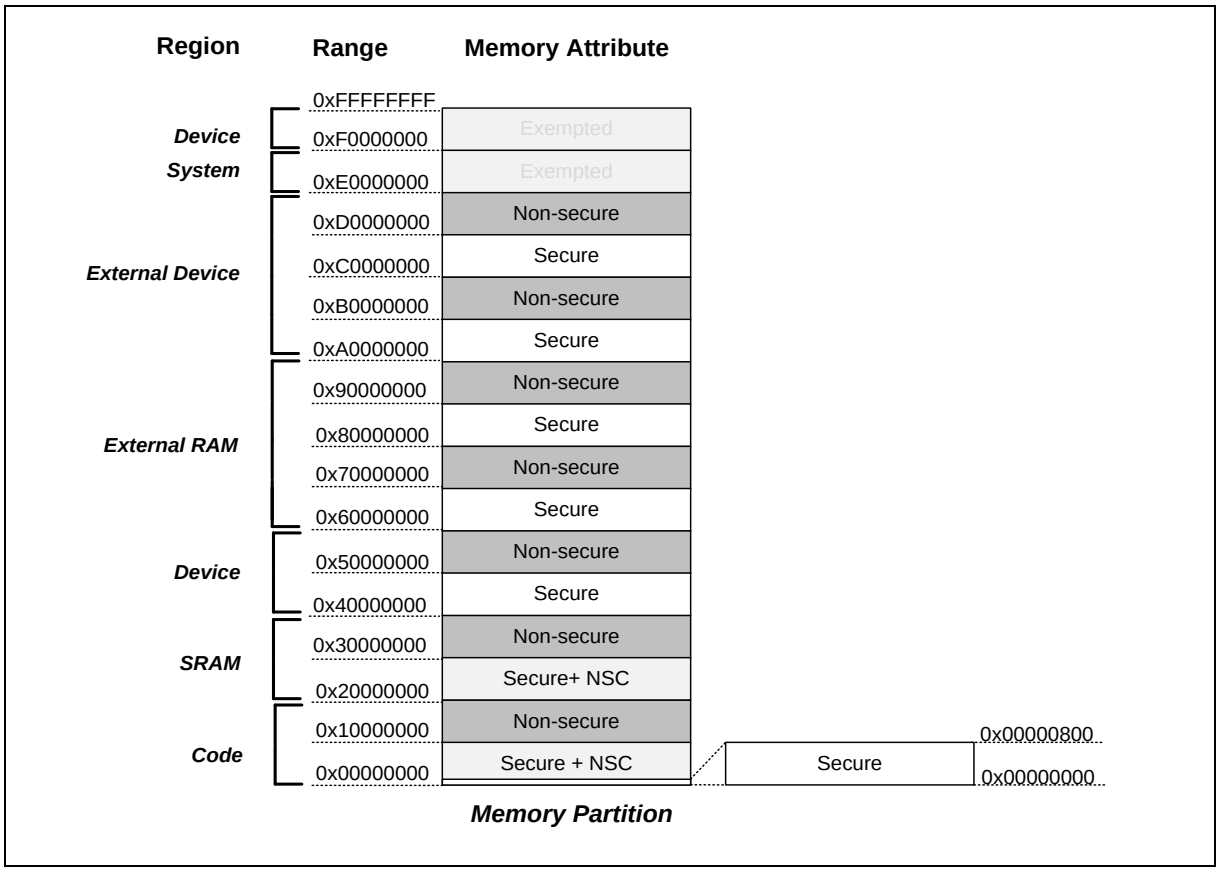


Figure 6.2-2 The 4 GB Memory Map Divided Into Secure and Non-secure Regions by IDAU

6.2.1.2 Security Attribution Unit (SAU)

The SAU is a MPU-like function unit inside Cortex®-M23. Up to 8 memory regions can be defined by programming control registers of SAU.

Memory regions are enabled individually by programming SAU_RNR, SAU_RBAR and SAU_RLAR. The memory region is enabled once RENABLE (SAU_RLAR[0]) is set to 1, and the security attribute is defined by NSC (SAU_RLAR[1]):

- NSC = 0, the memory region is Non-secure (NS).
- NSC = 1, the memory region is Secure and Non-secure callable (NSC).

The security attribute of each memory region defined by SAU is either NS or NSC. Those memory addresses not defined by SAU regions are treated as Secure. After all memory regions are set, SAU_CTRL[0] should be set to 1 to enable SAU.

Both IDAU and SAU define the security attribute of a memory address. If the definitions are different, the more secure attribute will be used for the memory address. The priority of the security attribute from high to low is Secure > NSC > NS.

When the core processor attempts to access a target, e.g. a memory or peripheral register, the security attribute of the target is decided by checking IDAU and SAU. If the core processor is non-secure but the target is secure, a HardFault exception will be generated. Because non-specified memory addresses are treated as secure, non-secure memory regions need to be defined for the core processor to access non-secure memory and non-secure peripheral registers. Besides, whole secure code and SRAM regions are defined as NSC by IDAU. The size of NSC regions can be changed according to the NSC entry functions included in application code. The example usage of SAU regions

is shown as Figure 6.2-3.

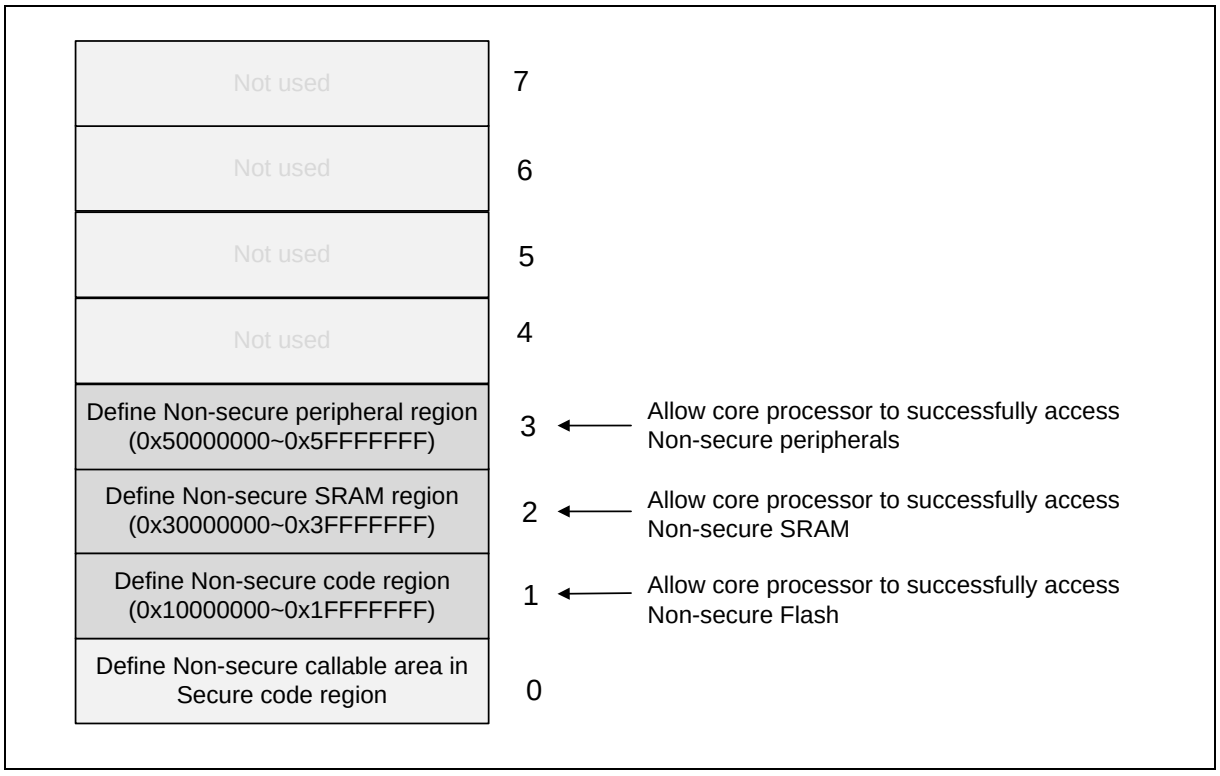


Figure 6.2-3 Typical Setting of SAU

6.2.2 Security Attribute Configuration

The previous section describes how to divide the address space of core processor view into secure world and non-secure world. For M2351, the memory and peripherals can be assigned to either secure or non-secure world during system initialization. The M2351 is designed to start execution in secure state after reset. In other words, core processor and all system resources including Flash, SRAM and peripherals are secure after reset. Then, the system initialization code may change some parts of the system resources to be non-secure.

6.2.2.1 Security Attribute Configuration of Flash

The M2351 Flash memory is split into a number of different regions such as LDROM, APROM and others. Most of the Flash regions are always secure and cannot be changed. The only one can be changed is the APROM region. Non-secure APROM region is set by programming a special control register, NSCBA (Non-secure base address). The NSCBA[23:0] indicates the starting address of non-secure APROM and its value should be aligned with a Flash page size. The secure APROM region starts from address 0x0 and ends at NSCBA[23:0] – 1, while the non-secure APROM region ranges from NSCBA[23:0] to the end of APROM. For setting NSCBA, refer to FMC section for more details.

6.2.2.2 Security Attribute Configuration of SRAM and Peripherals

The secure state of SRAM blocks and all peripherals can be configured by Security Configuration Unit (SCU), which contains a set of control registers used to assign the security attribute. Besides, the SCU monitors bus transfers to detect unsecure access. The unsecure access is one of the following conditions.

- Non-secure master peripheral tries to access a secure address (address bit 28 = 0).
- Secure code or secure master peripheral uses non-secure address (address bit 28 = 1) to access secure SRAM or peripheral.

When an unsecure access is detected, SCU blocks the access operation and generates a secure alarm interrupt.

For more details, refer to the Security Configuration Unit (SCU) chapter.

6.2.3 System Address Map and Access Scheme

In the M2351 series, the Flash, SRAM and most peripherals can be assigned to be Secure or Non-secure, but each of them can be accessed through either Secure address or Non-secure address depending on its security attribute configuration. Core processor and master peripherals should use correct address to access resources, i.e. the secure resource should be accessed by using secure address. Similarly, the non-secure resource should be accessed by using non-secure address.

6.2.3.1 Permanent Secure Peripherals

The security attribute of some peripherals are always secure and cannot be changed for safety and security. If necessary, the secure code should manage and provide functions for non-secure code to access these peripherals. Table 6.2-1 lists these secure peripherals.

Peripheral	Function	Address
SYS	System Control Registers	0x4000_0000 – 0x4000_01FF
CLK	Clock Control Registers	0x4000_0200 – 0x4000_02FF
NMI	NMI Control Registers	0x4000_0300 – 0x4000_03FF
PDMA0	Peripheral DMA 0 Control Registers	0x4000_8000 – 0x4000_8FFF
FMC	Flash Memory Control Registers	0x4000_C000 – 0x4000_CFFF
SCU	Security Configuration Unit Registers	0x4002_F000 – 0x4002_FFFF
WDT	Watchdog Timer Control Registers	0x4004_0000 – 0x4004_0FFF
TMR01	Timer0/Timer1 Control Registers	0x4005_0000 – 0x4005_0FFF

Table 6.2-1 Peripherals and Regions that are Always Secure

6.2.3.2 Secure Address vs. Non-secure Address

A memory or a peripheral register may have secure and non-secure address in system address map, but the memory or register only responds to the address that is consistent with its security attribute. The different access modes of secure and non-secure target are illustrated in Figure 6.2-4.

Suppose that SRAM block 0, 2, and 4 are in secure state, they will respond to an access when address bit 28 is 0 (secure address), but will not respond to an access with address bit 28 is 1 (non-secure address). In this example, SRAM block 1 and 3 are in non-secure state. Hence, these blocks will only respond to an access when the address bit 28 is 1.

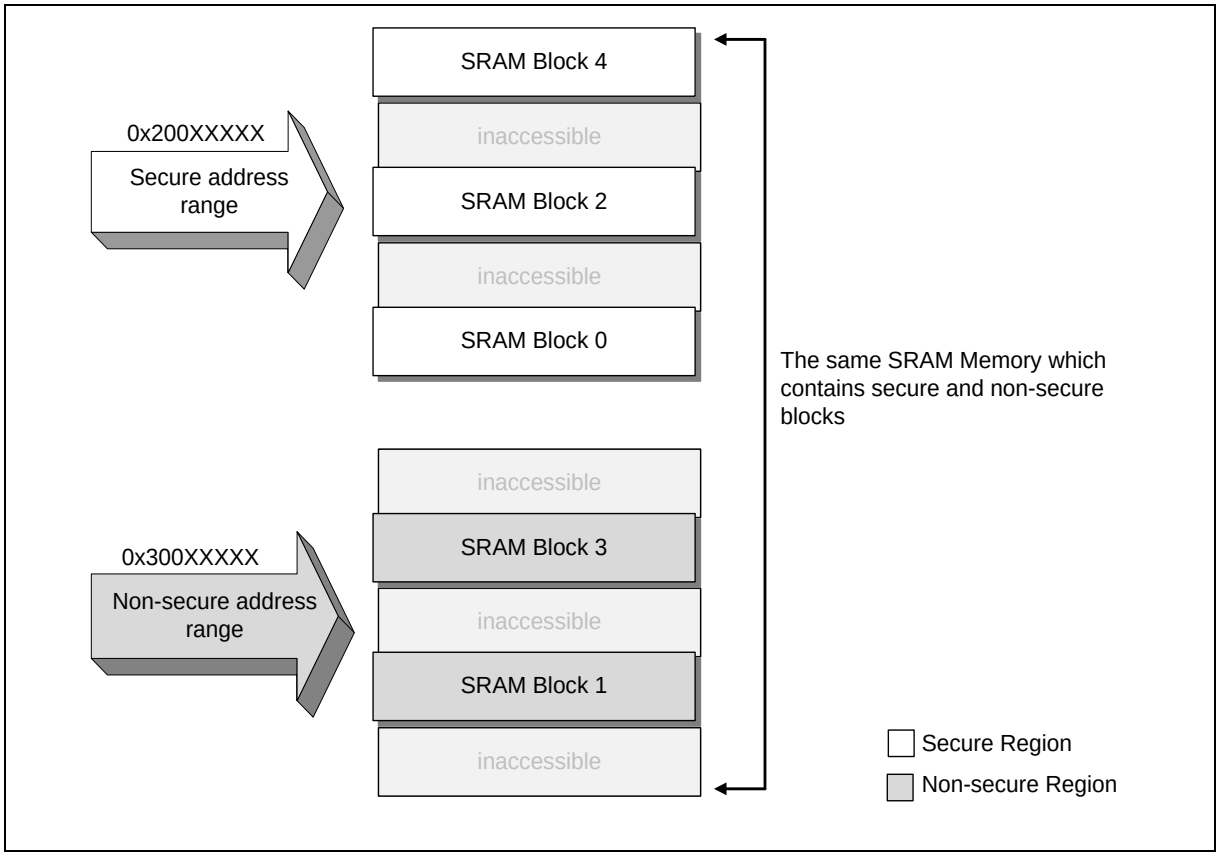


Figure 6.2-4 Example of SRAM Divided Into Secure Block and Non-secure Block

6.2.3.3 Valid Access vs. Invalid Access

When core processor or a master peripheral is trying to access (read or write) a memory or register, the result depends on the following conditions.

- Non-secure code or master peripheral is not allowed to access a secure memory or register.
- A memory or register only responds to the related address which is consistent with its security attribute.

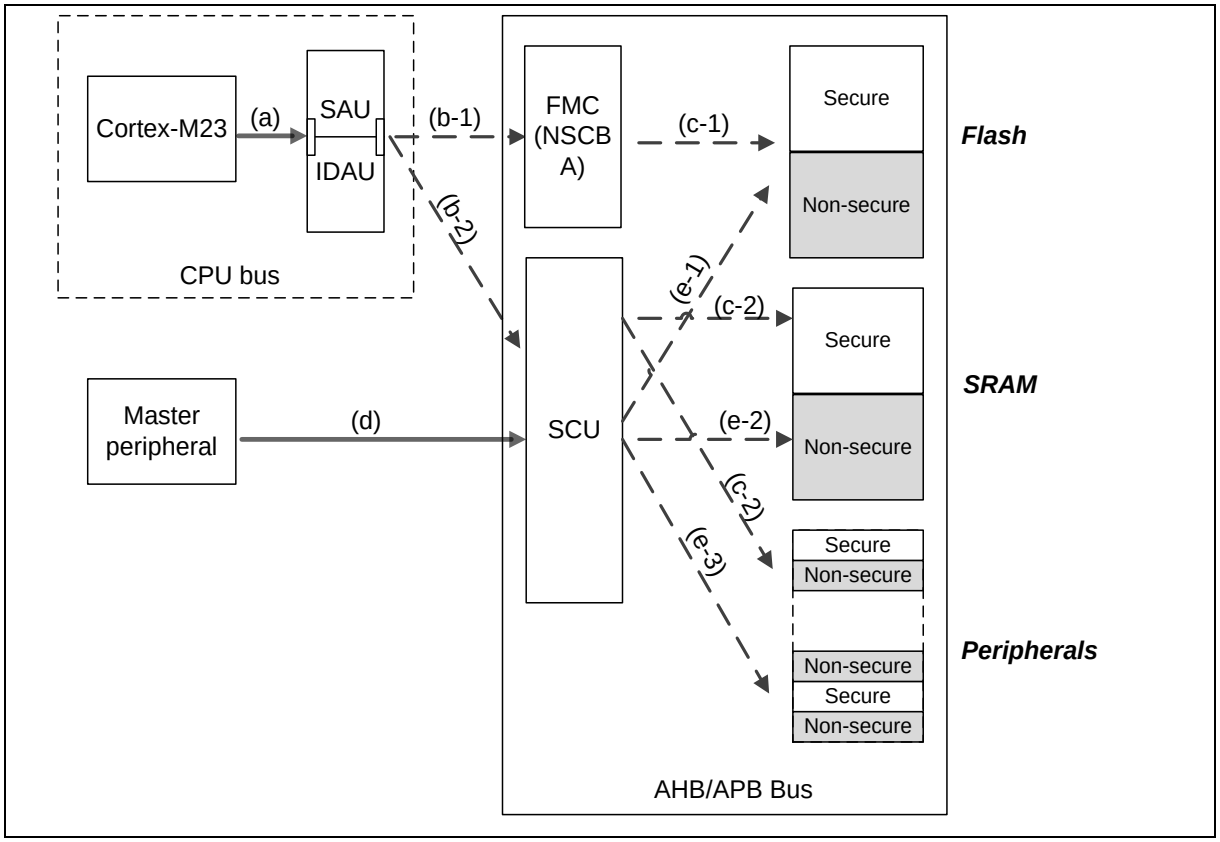


Figure 6.2-5 Checking Point of Accesses

Figure 6.2-5 illustrates how the above conditions are checked by TrustZone® related control units.

When the core processsor tries to fetch instructions or access data, the security attribute of the core processor and target address are verified by SAU and IDAU (refer to (a)). If the core processor is in non-secure state and target address is secure, a hard fault exception will be generated. The other cases will go to next checkpoints (refer to (b-1) and (b-2)). If the non-secure code tries to read/write a secure memory or register, the access will be blocked and a secure violation interrupt (SCU interrupt) can be generated. If a secure code uses non-secure address to access a secure memory or register, the operation has no effect. (refer to (c-1) and (c-2))

When a master peripheral tries to read/write a memory or register, the SCU will verify the access (refer to (d)). When a non-secure master peripheral wants to access a secure memory or register, the access will be blocked and a secure violation interrupt (SCU interrupt) can be generated. If a secure master peripheral uses non-secure address to read/write a secure memory or register, the operation has no effect.

The responses of the accesses from the core processor and master peripherals follow the rule called memory access policy, which is described in the “Memory Access Policy (MAP)” section of “Security Configuration Unit (SCU)” chapter.

6.3 System Manager

6.3.1 Overview

System management includes the following sections:

- System Reset
- System Power Distribution
- SRAM Memory Orginization
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

6.3.2 Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset sourcces are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset (POR)
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - System Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex®-M23 core only by writing 1 to CPURST (SYS_IPRST0[1])

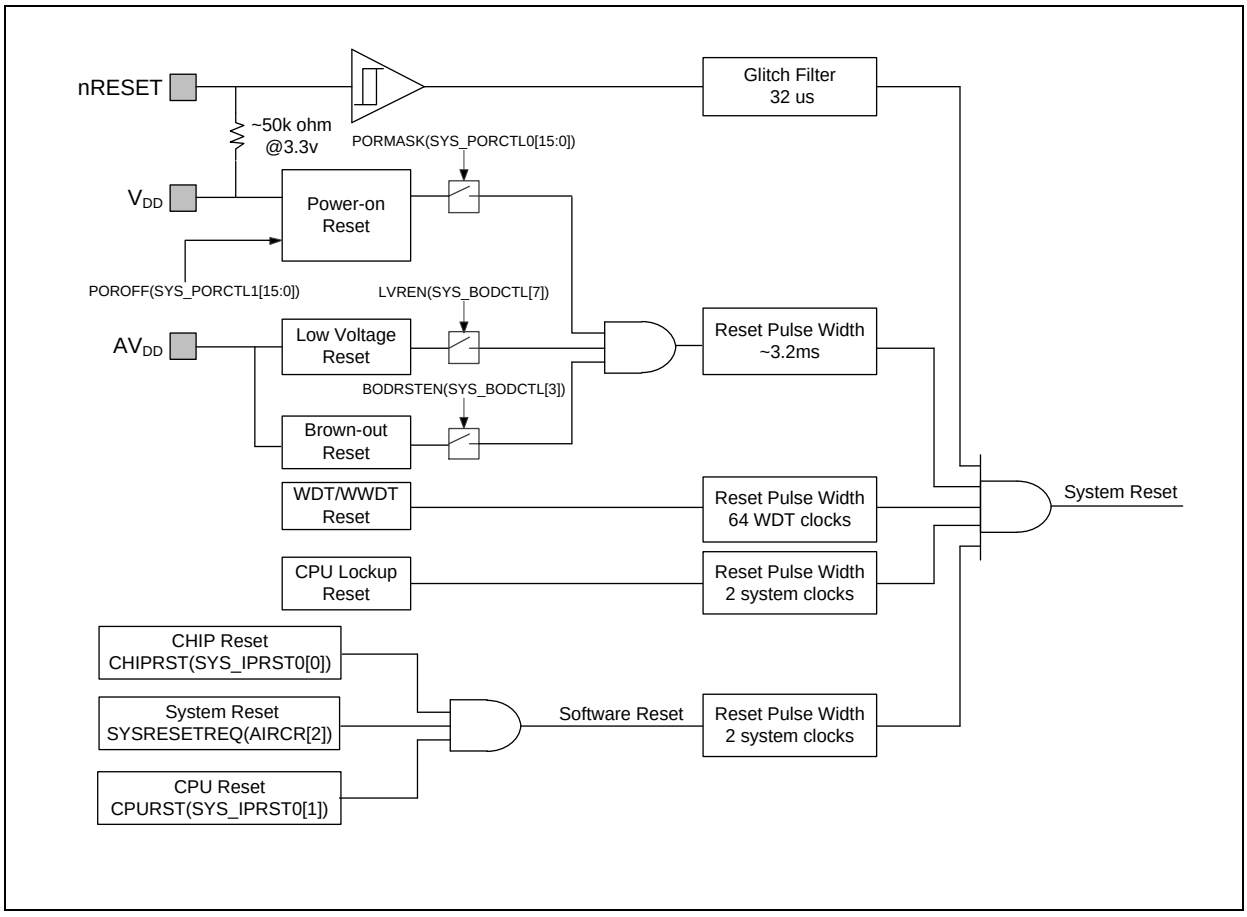


Figure 6.3-1 System Reset Sources

There are a total of 9 reset sources in the NuMicro® family. In general, CPU reset is used to reset Cortex®-M23 only; the other reset sources will reset Cortex®-M23 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.3-1.

Reset Sources Register	POR	NRESET	WDT	LVR	BOD	Lockup	CHIP	SYSTEM	CPU
SYS_RSTSTS	Bit 0 = 1	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 8 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-	-
BODEN (SYS_BODCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
BODVL (SYS_BODCTL[18:16])									
BODRSTEN (SYS_BODCTL[3])									
SYS_SRAMPCTL	0x0	-	-	-	-	-	-	-	-
SYS_SRAMPPCT	0x0	-	-	-	-	-	-	-	-

LXTEN (CLK_PWRCTL[1])	0x0	-	-	-	-	-	-	-	-
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	-	0x1	-	-
WDTSEL (CLK_CLKSEL1[1:0])	0x3	0x3	-	-	-	-	-	-	-
HXTSTB (CLK_STATUS[0])	0x0	-	-	-	-	-	-	-	-
LXTSTB (CLK_STATUS[1])	0x0	-	-	-	-	-	-	-	-
PLLSTB (CLK_STATUS[2])	0x0	-	-	-	-	-	-	-	-
HIRCSTB (CLK_STATUS[4])	0x0	-	-	-	-	-	-	-	-
CLKSFAIL (CLK_STATUS[7])	0x0	0x0	-	-	-	-	-	-	-
CLK_PLLCTL	0x000D_440A	-	-	-	-	-	-	-	-
PDMSEL (CLK_PMUCTL [2:0])	0x0	-	-	-	-	-	-	-	-
RSTEN (WDT_CTL[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
WDTEN (WDT_CTL[7])									
WDT_CTL except bit 1 and bit 7.	0x0700	0x0700	0x0700	0x0700	0x0700	-	0x0700	-	-
WDT_ALTCTL	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_RLDCNT	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CTL	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-	0x3F0800	-	-
WWDT_STATUS	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CNT	0x3F	0x3F	0x3F	0x3F	0x3F	-	0x3F	-	-
BS (FMC_ISPCTL[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
BL (FMC_ISPCTL[16])									
CBS (FMC_ISPSTS[2])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
VECMAP (FMC_ISPSTS[23:9])	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	-	Reload base on CONFIG0	-	-

Other Peripheral Registers	Reset Value	-
FMC Registers	Reset Value	
Note: '-' means that the value of register keeps original setting.		

Table 6.3-1 Reset Value of Registers

6.3.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 V_{DD} and the state keeps longer than 32 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 V_{DD} and the state keeps longer than 32 us (glitch filter). The PINRF(SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6.3-2 shows the nRESET reset waveform.

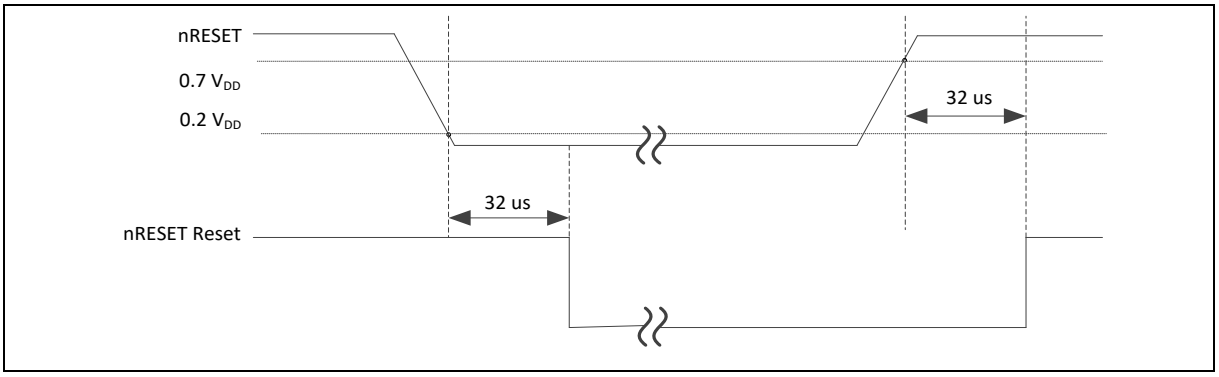


Figure 6.3-2 nRESET Reset Waveform

6.3.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.3-3 shows the power-on reset waveform.

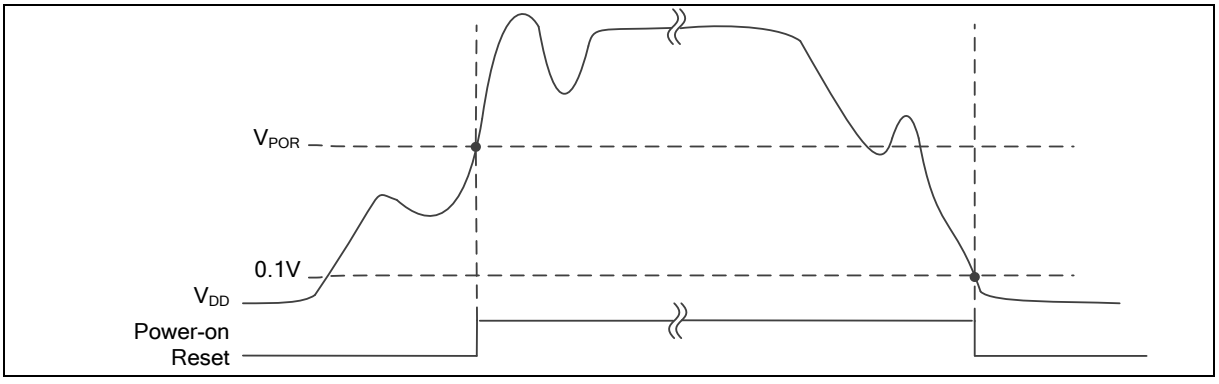


Figure 6.3-3 Power-on Reset (POR) Waveform

6.3.2.3 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, after 200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.3-4 shows the Low Voltage Reset waveform.

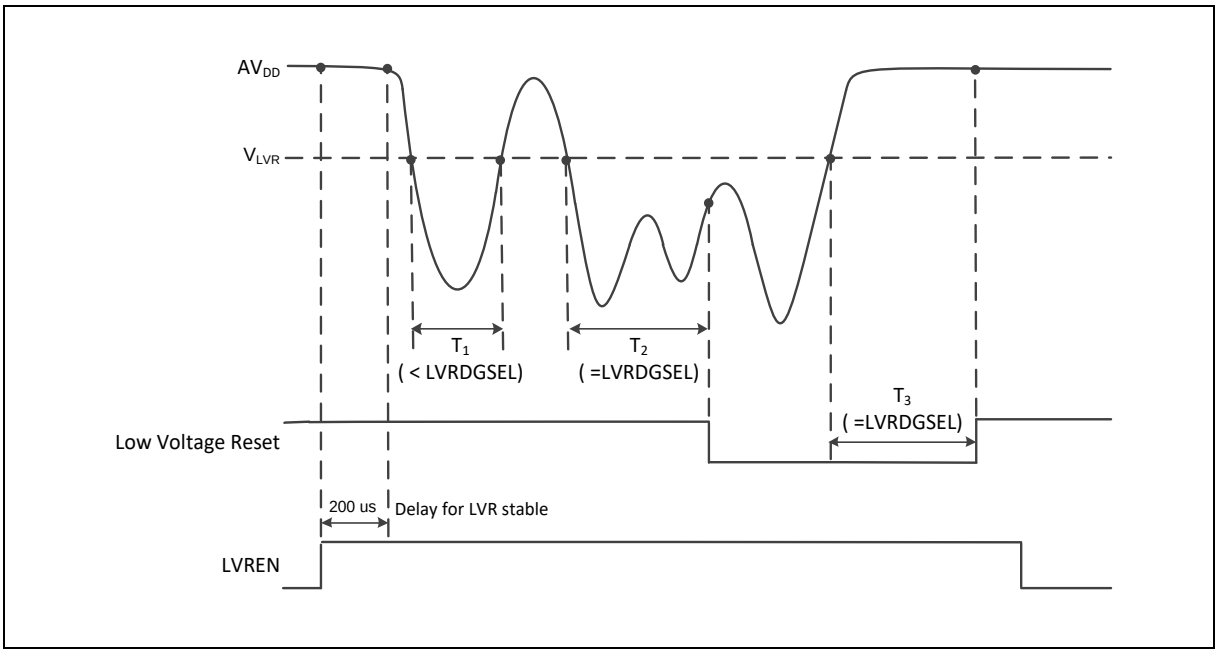


Figure 6.3-4 Low Voltage Reset (LVR) Waveform

6.3.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BODEN and BODVL (SYS_BODCTL[18:16]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time set by BODDGSEL. The default value of BODEN, BODVL and BODRSTEN (SYS_BODCTL[3]) is set by Flash controller user configuration register CBODEN (CONFIG0 [19]), CBOV (CONFIG0 [23:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.3-5 shows the Brown-out Detector waveform.

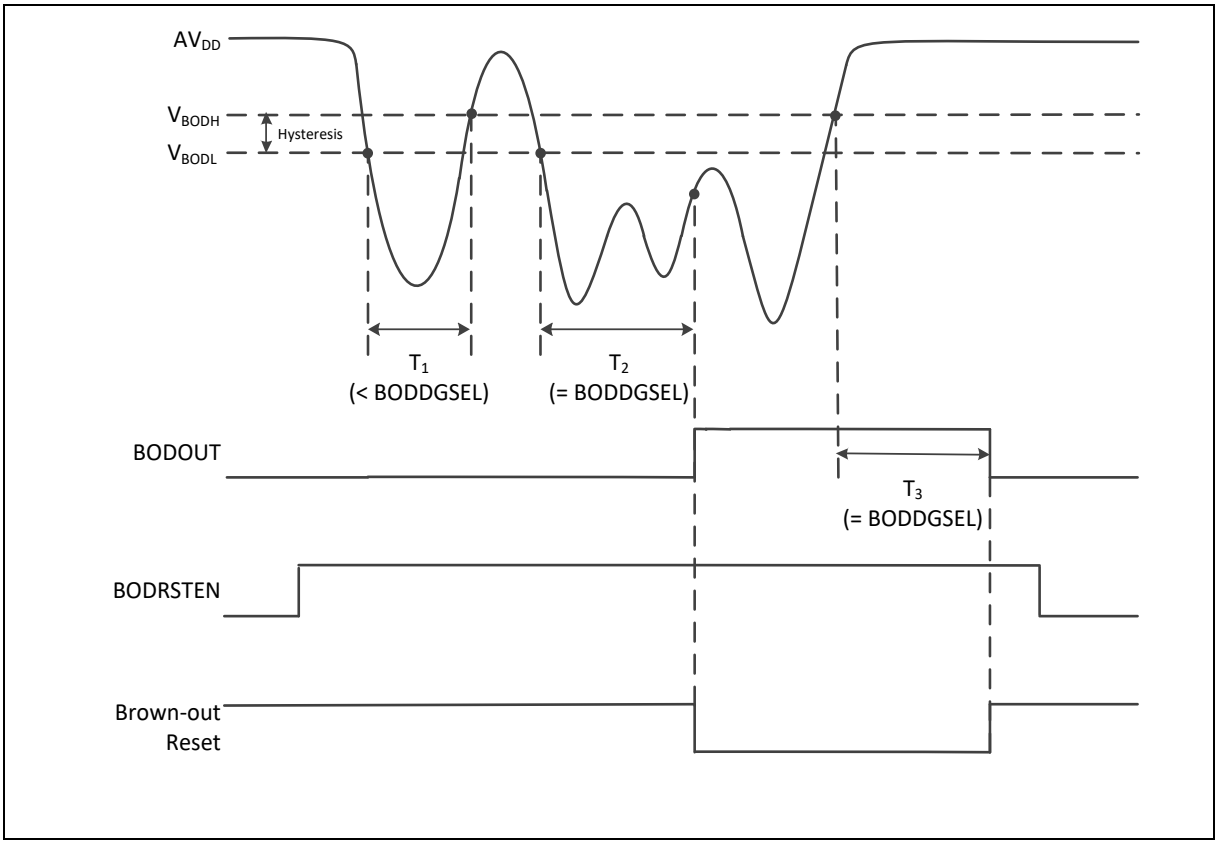


Figure 6.3-5 Brown-out Detector (BOD) Waveform

6.3.2.5 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

6.3.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

6.3.2.7 CPU Reset, CHIP Reset and System Reset

The CPU Reset means only Cortex®-M23 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-on Reset. The CPU and all peripherals are reset and BS(FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIPRST(SYS_IPRST0[1]) to 1 to assert the CHIP Reset signal.

The System Reset is similar with CHIP Reset. The difference is that BS(FMC_ISPCTL[1]) will not be reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or

LDROM. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the System Reset.

6.3.3 Power Modes and Wake-up Sources

The NuMicro® M2351 series has power manager unit to support several operating modes for saving power. Table 6.3-2 lists all power modes in the NuMicro® M2351 series.

Mode	CPU Operating Maximum Speed (MHz)	LDO_CAP (V)	Clock Disable
Normal mode	48MHz	1.20	All clocks are disabled by control register. CLK_AHBCLK, CLK_APBCLK0 and CLK_APBCLK1.
Turbo mode	64MHz	1.26	All clocks are disabled by control register. CLK_AHBCLK, CLK_APBCLK0 and CLK_APBCLK1.
Idle mode	CPU enter Sleep mode	keep	Only CPU clock is disabled.
Power-down mode (PD)	CPU enters Deep Sleep mode	keep	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Fast Wake-up Power-down mode (FWPD)	CPU enters Deep Sleep mode	keep	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Low leakage Power-down mode (LLPD)	CPU enters Deep Sleep mode	0.96	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Ultra Low leakage Power-down mode (ULLPD)	CPU enters Deep Sleep mode	0.9	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Standby Power-down mode (SPD)	Power off	Floating	Only LIRC/LXT still enable for RTC function and wake-up timer usage.
Deep Power-down mode (DPD)	Power off	Floating	Only LIRC/LXT still enable for RTC function and wake-up timer usage.

Table 6.3-2 Power Mode Table

Each power mode has different entry setting and leaving condition. Table 6.3-3 shows the entry setting for each power mode. When chip power-on, chip is running in normal mode. User can enter each mode by setting SLEEPDEEP (SCR[2]), PDEN (CLK_PWRCT[7]) and PDMSEL (CLK_PMUCTL[2:0]) and execute WFI instruction.

Register/Instruction Mode	SLEEPDEEP (SCR[2])	PDEN (CLK_PWRCTL[7])	PDMSEL (CLK_PMUCTL[2:0])	CPU Run WFI Instruction
Normal mode	0	0	0	NO
Idle mode	0	0	0	YES
Power-down mode	1	1	0	YES

Low leakage Power-down mode	1	1	1	YES
Ultra Low leakage Power-down mode	1	1	3	YES
Fast Wake-up Power-down mode	1	1	2	YES
Standby Power-down mode	1	1	4	YES
Deep Power-down mode	1	1	6	YES

Table 6.3-3 Power Mode Entry Setting Table

There are several wake-up sources in Idle mode and Power-down mode. Table 6.3-4 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-Down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content be retained by setting SYS_SRAMPCTL and SYS_SRAMPPCT.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	EINT, GPIO, UART, USBD, USBH, OTG, CAN, BOD, WDT, SDH, Timer, I²C, USCI, RTC and ACMP.
Available Clocks	All	All except CPU clock	LXT and LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6.3-4 Power Mode Difference Table

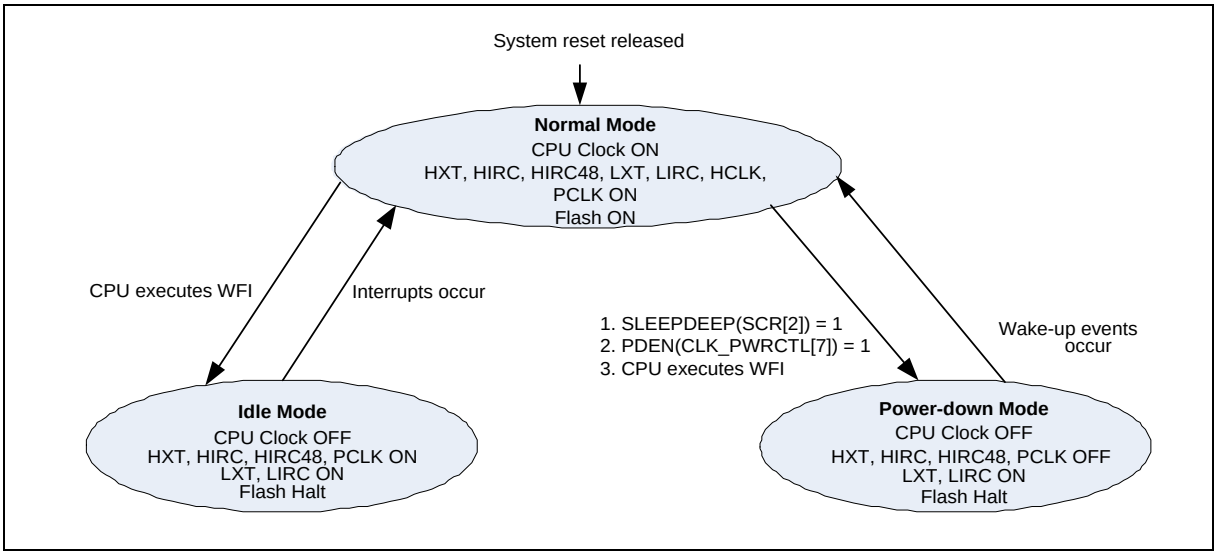


Figure 6.3-6 Power Mode State Machine

1. LXT ON or OFF depends on software setting in normal mode.

2. LIRC ON or OFF depends on software setting in normal mode.

3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.

4. If WDT clock source is selected as LIRC and LIRC is on.

5. If RTC clock source is selected as LXT and LXT is on.

6. If UART clock source is selected as LXT and LXT is on.

	Normal Mode	Idle Mode	Power-Down Mode (PD/FWPD/LLPD/ULLPD)	Power-Down Mode (SPD/DPD)
HXT	ON	ON	Halt	Halt
HIRC	ON	ON	Halt	Halt
HIRC48	ON	ON	Halt	Halt
LXT	ON	ON	ON/OFF[1]	ON/OFF[1]
LIRC	ON	ON	ON/OFF[2]	ON/OFF[2]
PLL	ON	ON	Halt	Halt
CPU	ON	Halt	Halt	Halt
HCLK/PCLK	ON	ON	Halt	Halt
FLASH	ON	ON	Halt	Halt
TIMER	ON	ON	ON/OFF[3]	Halt
WDT	ON	ON	ON/OFF[4]	Halt
RTC	ON	ON	ON/OFF[5]	ON/OFF[5]
UART	ON	ON	ON/OFF[6]	Halt
Others	ON	ON	Halt	Halt

Table 6.3-5 Clocks in Power Modes

Wake-up sources in Power-down mode:

EINT, GPIO, UART, USBD, USBH, OTG, CAN, BOD, ACMP, WDT, SDH, Timer, I²C, USCI, , , RTC.

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.3-6 lists the condition about how to enter Power-down mode again for each peripheral.

*User needs to wait this condition before setting PDEN(CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

Wake-Up Source	Wake-Up Condition	Power-down mode			System Can Enter Power-Down Mode Again Condition*
		PD LLPD ULLPD FWPD	SPD	DPD	
BOD	Brown-out Detector Reset / Interrupt	√	-	-	After software writes 1 to clear BODIF (SYS_BODCTL[4]).
	Brown-out Detector Reset	-	√	-	After software writes 1 to clear BODWK (CLK_PMUSTS[13]) when SPD mode is entered.

LVR	LVR Reset	√	-	-	After software writes 1 to clear LVRF (SYS_RSTSTS[3])
		-	√	-	After software writes 1 to clear LVRWK (CLK_PMUSTS[12]) when SPD mode is entered.
POR	POR Reset	√	√	-	After software writes 1 to clear PORF (SYS_RSTSTS[0]).
EINT	External Interrupt	√	-	-	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO	GPIO Interrupt	√	-	-	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO(PA~PD) Wake-up pin	rising or falling edge event, 61-pin	-	√	-	GPxWK(CLK_PMUSTS[11:8]) is cleared when SPD mode is entered.
GPIO(PC.0) Wake-up pin	rising or falling edge event , 1-pin	-	-	√	PINWK(CLK_PMUSTS[1]) is cleared when DPD mode is entered.
TIMER	Timer Interrupt	√	-	-	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
Wakeup timer	Wakeup by wake-up timer time-out	-	√	√	After software writes 1 to clear TMRWK (CLK_PMUSTS[1]) when SPD or DPD mode is entered.
WDT	WDT Interrupt	√	-	-	After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).
RTC	Alarm Interrupt	√	-	-	After software writes 1 to clear ALMIF (RTC_INTSTS[0]).
	Time Tick Interrupt	√	-	-	After software writes 1 to clear TICKIF (RTC_INTSTS[1]).
	Wakeup by RTC alarm	-	√	√	RTCWK (CLK_PMUSTS[5]) is cleared when DPD or SPD mode is entered.
	Wakeup by RTC tick time	-	√	√	RTCWK (CLK_PMUSTS[5]) is cleared when DPD or SPD mode is entered.
	Wakeup by tamper event	-	√	√	RTCWK (CLK_PMUSTS[5]) is cleared when DPD or SPD mode is entered.
UART	nCTS wake-up	√	-	-	After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).
	RX Data wake-up	√	-	-	After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).
	Received FIFO Threshold Wake-up	√	-	-	After software writes 1 to clear RFRTWKF (UARTx_WKSTS[2]).
	RS-485 AAD Mode Wake-up	√	-	-	After software writes 1 to clear RS485WKF (UARTx_WKSTS[3]).
	Received FIFO Threshold Time-out Wake-up	√	-	-	After software writes 1 to clear TOUTWKF (UARTx_WKSTS[4]).
USCI UART	CTS Toggle	√	-	-	After software writes 1 to clear WKF (UUART_WKSTS[0]).
	Data Toggle	√	-	-	After software writes 1 to clear WKF (UUART_WKSTS[0]).

USCI I²C	Data toggle	√	-	-	After software writes 1 to clear WKF (UI2C_WKSTS[0]).
	Address match	√	-	-	After software writes 1 to clear WKAKDONE (UI2C_PROTSTS[16], then writes 1 to clear WKF (UI2C_WKSTS[0]).
USCI SPI	SS Toggle	√	-	-	After software writes 1 to clear WKF (USPI_WKSTS[0]).
I²C	Address match wake-up	√	-	-	After software writes 1 to clear WKAKDONE (I2C_WKSTS[1]). Then software writes 1 to clear WKIF(I2C_WKSTS[0]).
USBD	1.Remote wake-up 2.Pulg in wake-up	√	-	-	After software writes 1 to clear BUSIF (USBD_INTSTS[0]).
USBH	1.Connection detected 2.Disconnect detected 3.Remote-wakeup	√	-	-	1.After write 1 to clear RHSC (HcInterruptStatus[7]). 2.After write 1 to clear RHSC (HcInterruptStatus[7]). 3.After write 1 to clear RHSC (HcInterruptStatus[7]). and port suspended.
OTG	ID pin state be change	√	-	-	After software writes 1 to set WKEN(OTG_CTL[5]).
ACMP	Comparator Power-Down Wake-Up Interrupt	√	-	-	After software writes 1 to clear WKIF0 (ACMP_STATUS[8]) and WKIF1 (ACMP_STATUS[9]).
	ACMPO status change	-	√	-	ACMPWK (CLK_PMUSTS[3]) is cleared when SPD mode is entered.
CAN	Incoming Data Toggle	√	-	-	After software writes 0 to clear WAKUP_STS (CAN_WU_STATUS[0])
SDH	Card detection	√	-	-	Clear CDIF0 (SDH_INTSTS[8]) after SDH wake-up.

Table 6.3-6 Condition of Entering Power-down Mode Again

6.3.4 System Power Distribution

In this chip, power distribution is divided into four segments:

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.2V or 1.26V power for digital operation and I/O pins.
- USB transceiver power from VBUS offers the power for operating the USB transceiver.
- RTC power from V_{BAT} provides the power for RTC and 80 bytes backup registers.

The outputs of internal voltage regulators, LDO and V_{DD}, require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). If system enters SPD mode SW_SPD switch needs to be turned off, and internal voltage regulator can be set to LDO mode or DC-DC converter mode. Figure 6.3-7 shows the power distribution.

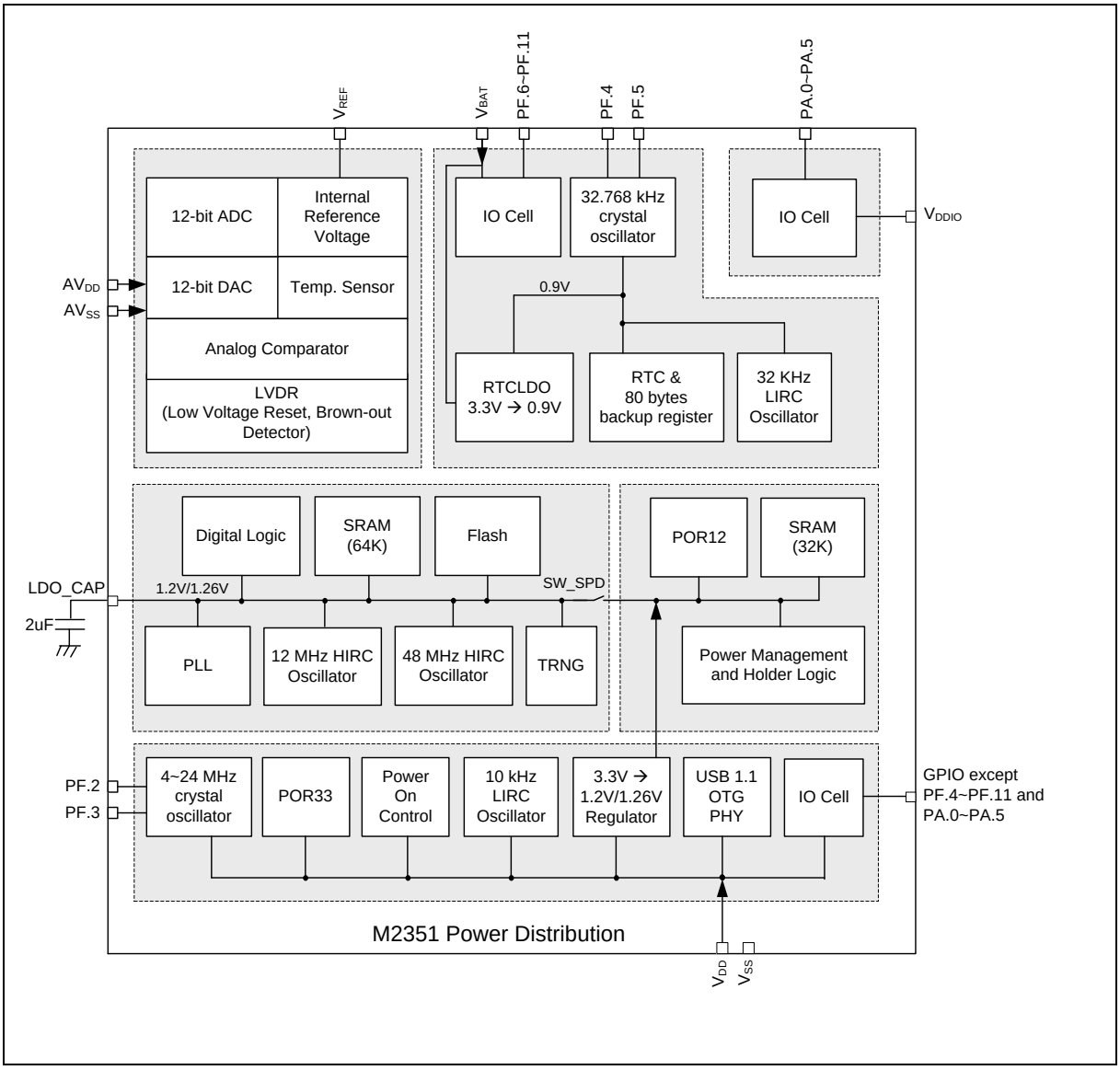


Figure 6.3-7 Power Distribution Diagram

6.3.5 Bus Matrix

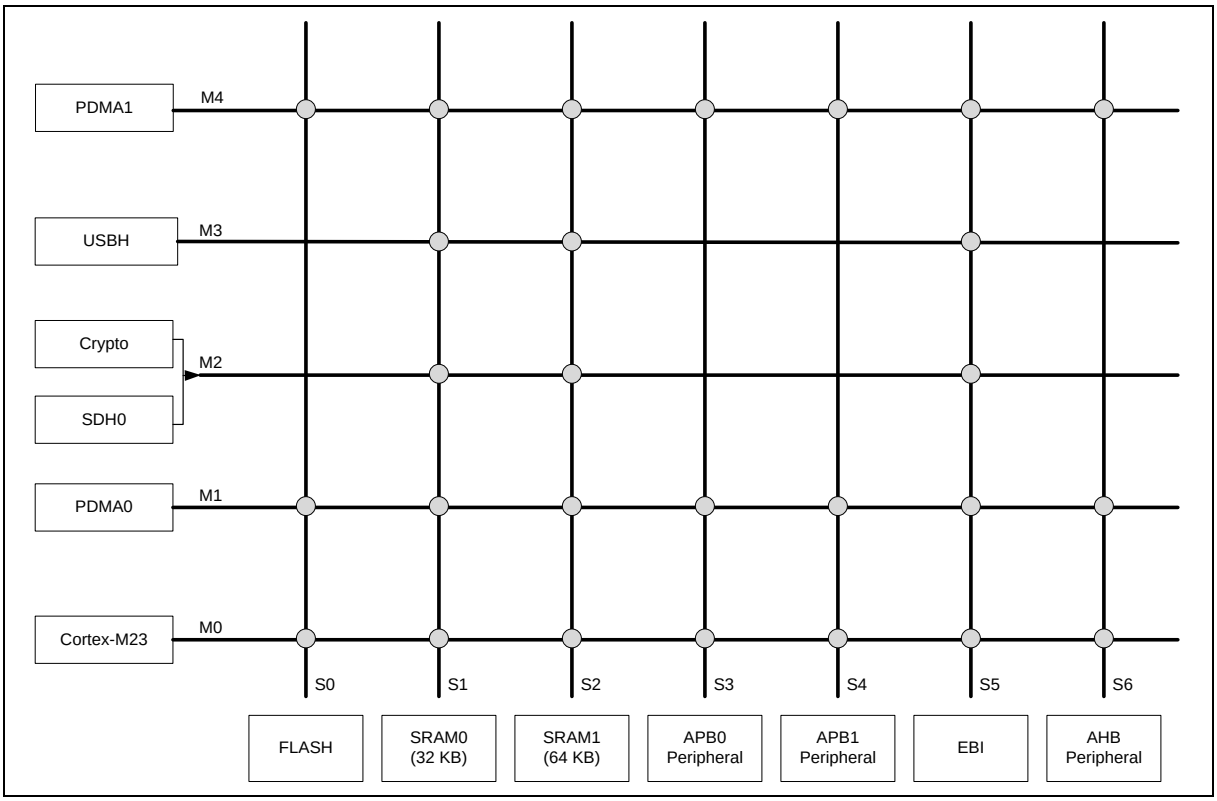


Figure 6.3-2 M2351 Bus Martix Architecture Diagram

Refer to Figure 6.3-2. This chip uses Advanced Microcontroller Bus Architecture (AMBA) protocol to implement system bus. The system has five masters and seven slaves, in which a different master can communicate with a different slave at the same time through Bus Matrix. The Cortex®-M23 core processor acts as the master in Bus Matrix, located on M0 to communicate with any slaves through Bus Matrix. PDMA0 and PDMA1 are Peripheral Direct Memory Access and act as the master in Bus Matrix, respectively located on M1 and M4, which can communicate with any slaves through Bus Matrix. SDH0 and Crypto share the same master bandwidth located on M2. USBH acts as the master role in Bus Matrix and is located on M3. The slave AHB Peripheral is the Advanced High-performance Bus (AHB) controller, and any master can communicate with any AHB peripheral through Bus Matrix.

6.3.6 System Memory Map

This chip provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.3-7. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. This chip implement Arm® Trust Zone Architecture as well as memory alias technique, secure code and non-secure code can run together on the chip well, while both have different memory view. Secure code view is shown in Table 6.2-1 and non-secure code view is shown in Table 6.2-2.

The NuMicro® M2351 series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0003_FFFF	FLASH_BA	FLASH Memory Space (256 KB)
0x0000_0000 – 0x0007_FFFF	FLASH_BA	FLASH Memory Space (512 KB)

0x2000_0000 – 0x2000_7FFF	SRAM0_BA	SRAM Memory Space (32 KB)
0x2000_8000 – 0x2001_7FFF	SRAM1_BA	SRAM Memory Space (64 KB)
0x6000_0000 – 0x6FFF_FFFF	EXTMEM_BA	External Memory Space (256 MB)
Secure Peripheral Controllers Space (0x4000_0000 – 0x400F_FFFF)		
0x4000_0000 – 0x4000_01FF	SYS_BA	System Control Registers (always secure)
0x4000_0200 – 0x4000_02FF	CLK_BA	Clock Control Registers (always secure)
0x4000_0300 – 0x4000_03FF	NMI_BA	NMI Control Registers (always secure)
0x4000_4000 – 0x4000_4FFF	GPIO_BA	GPIO Control Registers
0x4000_8000 – 0x4000_8FFF	PDMA0_BA	Peripheral DMA 0 Control Registers (always secure)
0x4000_9000 – 0x4000_9FFF	USBH_BA	USB Host Control Registers
0x4000_C000 – 0x4000_CFFF	FMC_BA	Flash Memory Control Registers (always secure)
0x4000_D000 – 0x4000_DFFF	SDH0_BA	SDHOST0 Control Registers
0x4001_0000 – 0x4001_0FFF	EBI_BA	External Bus Interface Control Registers
0x4001_8000 – 0x4000_8FFF	PDMA1_BA	Peripheral DMA 1Control Registers (secure or non-secure)
0x4003_1000 – 0x4003_1FFF	CRC_BA	CRC Generator Registers
0x4003_2000 – 0x4003_4FFF	CRPT_BA	Cryptographic Accelerator Registers
0x4002_F000 – 0x4002_FFFF	SCU_BA	Secure Configuration Unit Registers (always secure)
Secure APB Controllers Space (0x4004_0000 ~ 0x400F_FFFF)		
0x4004_0000 – 0x4004_0FFF	WDT_BA	Watchdog Timer Control Registers (always secure)
0x4004_1000 – 0x4004_1FFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4004_3000 – 0x4004_3FFF	EADC_BA	Enhanced Analog-Digital-Converter (EADC) Control Registers
0x4004_5000 – 0x4004_5FFF	ACMP01_BA	Analog Comparator 0/ 1 Control Registers
0x4004_7000 – 0x4004_7FFF	DAC_BA	DAC Control Registers
0x4004_8000 – 0x4004_8FFF	I2S0_BA	I^2S0 Interface Control Registers
0x4004_D000 – 0x4004_DFFF	OTG_BA	OTG Control Registers
0x4005_0000 – 0x4005_0FFF	TMR01_BA	Timer0/Timer1 Control Registers (always secure)
0x4005_1000 – 0x4005_1FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4005_8000 – 0x4005_8FFF	EPWM0_BA	EPWM0 Control Registers
0x4005_9000 – 0x4005_9FFF	EPWM1_BA	EPWM1 Control Registers
0x4005_A000 – 0x4005_AFFF	BPWM0_BA	BPWM0 Control Registers
0x4005_B000 – 0x4005_BFFF	BPWM1_BA	BPWM1 Control Registers
0x4006_0000 – 0x4006_0FFF	QSPI0_BA	Quad SPI0 Control Registers
0x4006_1000 – 0x4006_1FFF	SPI0_BA	SPI0 Control Registers
0x4006_2000 – 0x4006_2FFF	SPI1_BA	SPI1 Control Registers
0x4006_3000 – 0x4006_3FFF	SPI2_BA	SPI2 Control Registers

0x4006_4000 – 0x4006_4FFF	SPI3_BA	SPI3 Control Registers
0x4007_0000 – 0x4007_0FFF	UART0_BA	UART0 Control Registers
0x4007_1000 – 0x4007_1FFF	UART1_BA	UART1 Control Registers
0x4007_2000 – 0x4007_2FFF	UART2_BA	UART2 Control Registers
0x4007_3000 – 0x4007_3FFF	UART3_BA	UART3 Control Registers
0x4007_4000 – 0x4007_4FFF	UART4_BA	UART4 Control Registers
0x4007_5000 – 0x4007_5FFF	UART5_BA	UART5 Control Registers
0x4007_4000 – 0x4007_4FFF	Reserved	Reserved
0x4007_5000 – 0x4007_5FFF	Reserved	Reserved
0x4008_0000 – 0x4008_0FFF	I2C0_BA	I^2C0 Control Registers
0x4008_1000 – 0x4008_1FFF	I2C1_BA	I^2C1 Control Registers
0x4008_2000 – 0x4008_2FFF	I2C2_BA	I^2C2 Control Registers
0x4009_0000 – 0x4009_0FFF	SC0_BA	Smartcard Host 0 Control Registers
0x4009_1000 – 0x4009_1FFF	SC1_BA	Smartcard Host 1 Control Registers
0x4009_2000 – 0x4009_2FFF	SC2_BA	Smartcard Host 2 Control Registers
0x400A_0000 – 0x400A_0FFF	CAN0_BA	CAN0 Bus Control Registers
0x400B_0000 – 0x400B_0FFF	QEI0_BA	QEI0 Control Registers
0x400B_1000 – 0x400B_1FFF	QEI1_BA	QEI1 Control Registers
0x400B_4000 – 0x400B_4FFF	ECAP0_BA	ECAP0 Control Registers
0x400B_5000 – 0x400B_5FFF	ECAP1_BA	ECAP1 Control Registers
0x400B_9000 – 0x400B_9FFF	TRNG_BA	TRNG Control Registers
0x400C_0000 – 0x400C_0FFF	USBD_BA	USB Device Control Register
0x400D_0000 – 0x400D_0FFF	USCI0_BA	USCI0 Control Registers
0x400D_1000 – 0x400D_1FFF	USCI1_BA	USCI1 Control Registers

Table 6.3-7 Address Space Assignments for On-Chip Controllers

Address Space	Token	Controllers
Non-secure Peripheral Controllers Space (0x5000_0000 – 0x500F_FFFF)		
0x5000_4000 – 0x5000_4FFF	GPIO_BA	GPIO Control Registers
0x5000_9000 – 0x5000_9FFF	USBH_BA	USB Host Control Registers
0x5000_D000 – 0x5000_DFFF	SDH0_BA	SDHOST0 Control Registers
0x5001_0000 – 0x5001_0FFF	EBI_BA	External Bus Interface Control Registers
0x5001_8000 – 0x5000_8FFF	PDMA1_BA	Peripheral DMA 1Control Registers (secure or non-secure)
0x5003_1000 – 0x5003_1FFF	CRC_BA	CRC Generator Registers
0x5003_2000 – 0x5003_4FFF	CRPT_BA	Cryptographic Accelerator Registers
Non-secure APB Controllers Space (0x5004_0000 ~ 0x500F_FFFF)		
0x5004_1000 – 0x5004_1FFF	RTC_BA	Real Time Clock (RTC) Control Register
0x5004_3000 – 0x5004_3FFF	EADC_BA	Enhanced Analog-Digital-Converter (EADC) Control Registers
0x5004_5000 – 0x5004_5FFF	ACMP01_BA	Analog Comparator 0/ 1 Control Registers
0x5004_7000 – 0x5004_7FFF	DAC_BA	DAC Control Registers
0x5004_8000 – 0x5004_8FFF	I2S0_BA	I^2S0 Interface Control Registers
0x5004_D000 – 0x5004_DFFF	OTG_BA	OTG Control Registers
0x5005_1000 – 0x5005_1FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x5005_8000 – 0x5005_8FFF	EPWM0_BA	EPWM0 Control Registers
0x5005_9000 – 0x5005_9FFF	EPWM1_BA	EPWM1 Control Registers
0x5005_A000 – 0x5005_AFFF	BPWM0_BA	BPWM0 Control Registers
0x5005_B000 – 0x5005_BFFF	BPWM1_BA	BPWM1 Control Registers
0x5006_0000 – 0x5006_0FFF	QSPI0_BA	Quad SPI0 Control Registers
0x5006_1000 – 0x5006_1FFF	SPI0_BA	SPI0 Control Registers
0x5006_2000 – 0x5006_2FFF	SPI1_BA	SPI1 Control Registers
0x5006_3000 – 0x5006_3FFF	SPI2_BA	SPI2 Control Registers
0x5006_4000 – 0x5006_4FFF	SPI3_BA	SPI3 Control Registers
0x5007_0000 – 0x5007_0FFF	UART0_BA	UART0 Control Registers
0x5007_1000 – 0x5007_1FFF	UART1_BA	UART1 Control Registers
0x5007_2000 – 0x5007_2FFF	UART2_BA	UART2 Control Registers
0x5007_3000 – 0x5007_3FFF	UART3_BA	UART3 Control Registers
0x5007_4000 – 0x5007_4FFF	UART4_BA	UART4 Control Registers
0x5007_5000 – 0x5007_5FFF	UART5_BA	UART5 Control Registers
0x5007_4000 – 0x5007_4FFF	Reserved	Reserved
0x5007_5000 – 0x5007_5FFF	Reserved	Reserved
0x5008_0000 – 0x5008_0FFF	I2C0_BA	I^2C0 Control Registers

0x5008_1000 – 0x5008_1FFF	I2C1_BA	I²C1 Control Registers
0x5008_2000 – 0x5008_2FFF	I2C2_BA	I²C2 Control Registers
0x5009_0000 – 0x5009_0FFF	SC0_BA	Smartcard Host 0 Control Registers
0x5009_1000 – 0x5009_1FFF	SC1_BA	Smartcard Host 1 Control Registers
0x5009_2000 – 0x5009_2FFF	SC2_BA	Smartcard Host 2 Control Registers
0x500A_0000 – 0x500A_0FFF	CAN0_BA	CAN0 Bus Control Registers
0x500B_0000 – 0x500B_0FFF	QEI0_BA	QEI0 Control Registers
0x500B_1000 – 0x500B_1FFF	QEI1_BA	QEI1 Control Registers
0x500B_4000 – 0x500B_4FFF	ECAP0_BA	ECAP0 Control Registers
0x500B_5000 – 0x500B_5FFF	ECAP1_BA	ECAP1 Control Registers
0x500B_9000 – 0x500B_9FFF	TRNG_BA	TRNG Control Registers
0x500C_0000 – 0x500C_0FFF	USBD_BA	USB Device Control Register
0x500D_0000 – 0x500D_0FFF	USCI0_BA	USCI0 Control Registers
0x500D_1000 – 0x500D_1FFF	USCI1_BA	USCI1 Control Registers

Table 6.3-2 Non-secure Address Space Assignments for On-Chip Controllers

6.3.7 Implementation Defined Attribution Unit (IDAU)

6.3.7.1 Overview

The Arm®v8-M has the new feature called TrustZone®, which adds an additional security state to allow full isolation of two security levels. The processor security state is decided by the memory definition. For example, processor is in Secure state when the code is excuted in the Secure region. The memory map security state will be defined by the combination of:

- Internal Security Attribution Unit (SAU)
- Implementation Defined Attribution Unit (IDAU)

These attribution units define the memory space into four type regions:

- Secure Region: contains Secure program code or data
- Non-secure Callable Region (NSC): contains entry functions for Non-secure programs to access Secure functions
- Non-secure Region: contains Non-secure program code or data
- Exempt Region: exempt region will be exempted from security check

For each memory region defined by the SAU and IDAU has a region number generated by the SAU or by the IDAU. Region number is used for determine a group of memory share the same security attribute. Overlapping region numbers are not allow. For testing security attributes and region numbers, a new instruction “TT” (Test Target) is introduced. By using a TT instruction on the start and end addresses of the memory range, and identifying that both reside in the same region number, user can determine that the memory range is located entirely in same space. To be more specific, please refer to the Arm®v8-M Architecture Reference Manual. The M2351 IDAU memory map attributions and corresponding region numbers are shown in Figure 6.3-8. The address from 0xE000_0000 to 0xFFFF_FFFF is marked as exempt regions because the behavior of the address is fixed, so their security attributes don’t control by the SAU or IDAU.

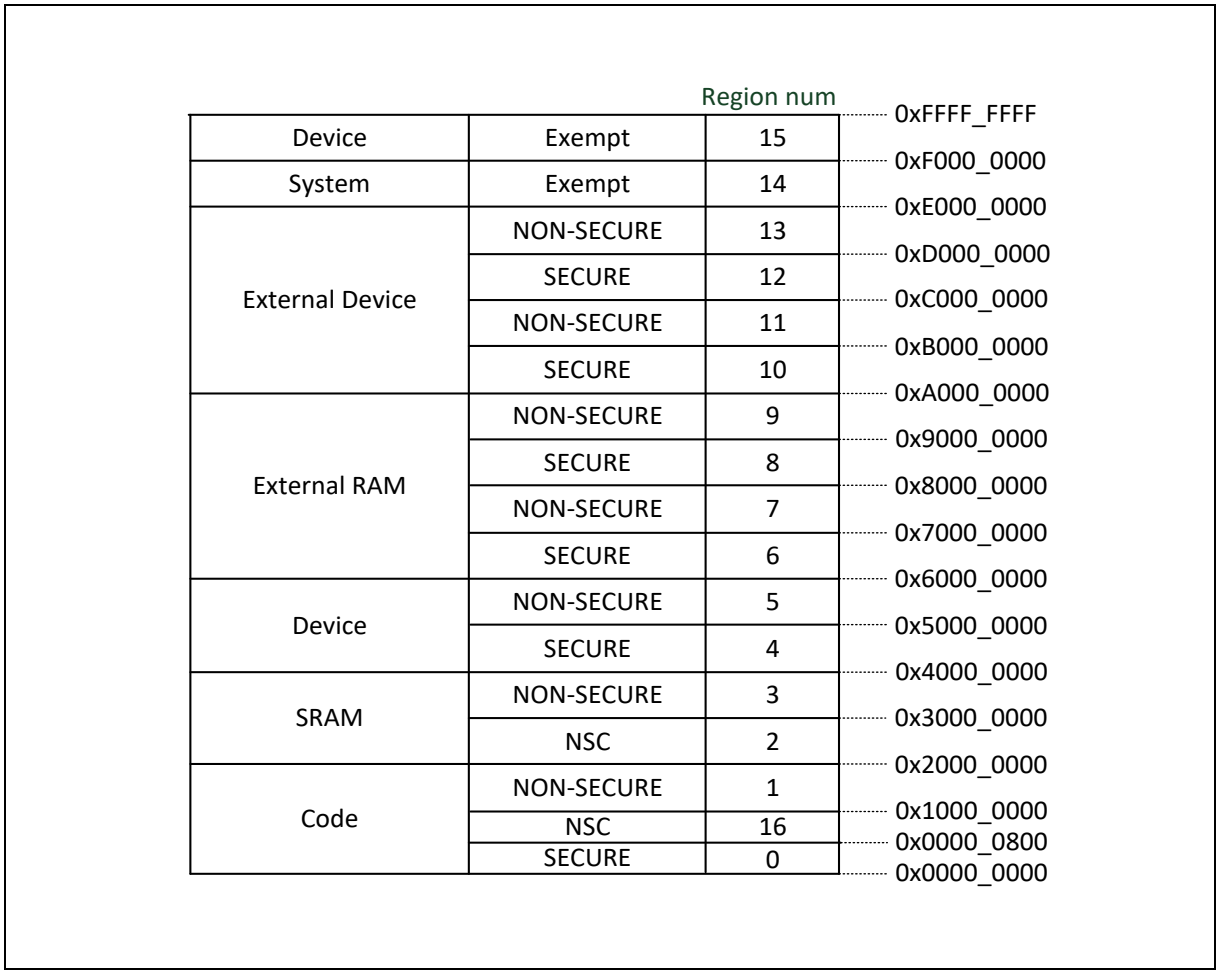


Figure 6.3-8 IDAU Memory Map

6.3.7.2 IDAU Block Diagram

The IDAU block diagram is shown in Figure 6.3-9. IDAU is security attribute unit connected outside of the processor. Both SAU and IDAU are responsible to response the security property of the address from processor, the only difference is that the memory security attribute of the SAU is configurable and the IDAU is fixed. After the processor compare the security property of the IDAU and SAU, it will take the highest security attribute applied. The hierarchy of security levels from high to low is: Secure > NSC > Non-secure.

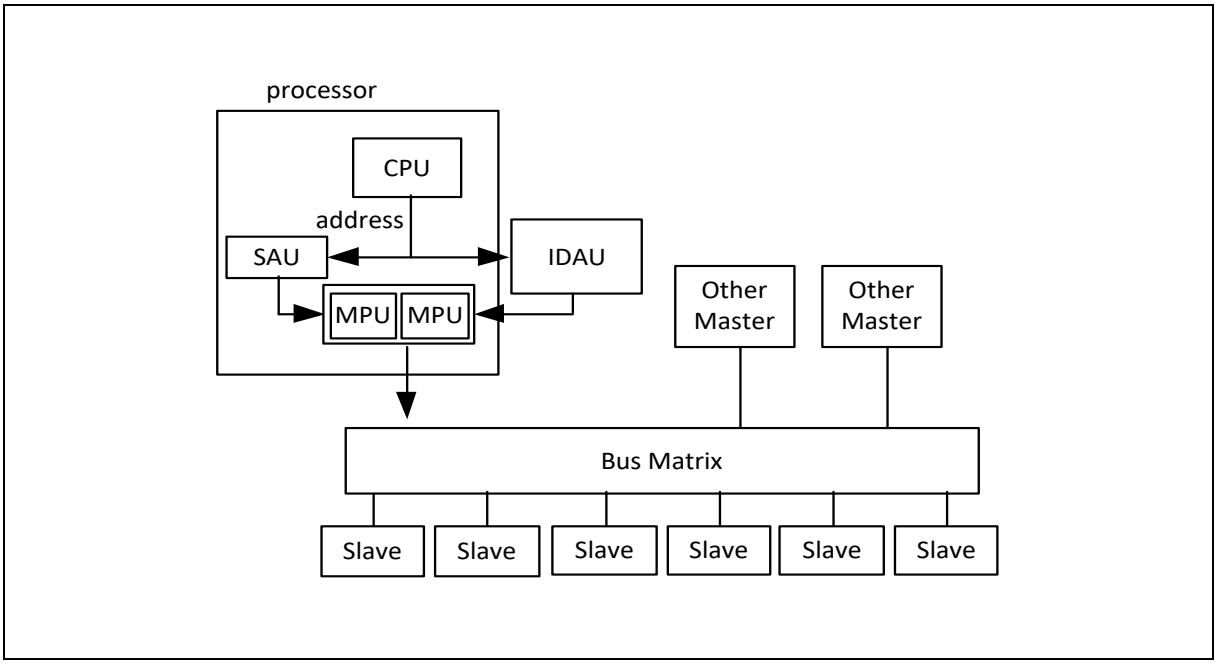


Figure 6.3-9 IDAU Block Diagram

6.3.8 SRAM Memory Orginization

This chip supports embedded SRAM with a total of 96 Kbytes size and the SRAM organization is separated into two banks: SRAM bank0 and SRAM bank1. The first bank has 32 Kbytes address space and the second bank has 64Kbyte address space. These two banks address space can be accessed simultaneously. The SRAM bank0 supports parity error check to make sure the chip is operating more stable.

- Supports total 96 Kbytes SRAM
- Supports byte / half word / word write
- Supports fixed 32 Kbytes SRAM bank0 for independent access
- Supports parity error check function for SRAM bank0
- Supports oversize response error
-

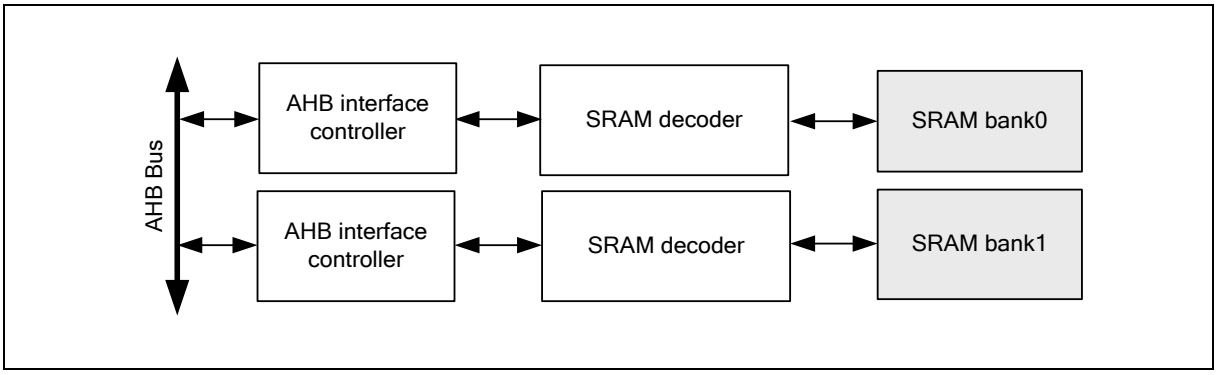


Figure 6.3-10 SRAM Block Diagram

Figure 6.3-11 shows the SRAM organization. There are two SRAM banks. The bank0 is addressed to 32 Kbytes and the bank1 is addressed to 64 Kbytes. The bank0 address space is from 0x2000_0000

to 0x2000_7FFF(Secure) or 0x3000_0000 to 0x3000_7FFF(Non-secure). The bank1 address space is from 0x2000_8000 to 0x2001_7FFF(Secure) or 0x3000_8000 to 0x3001_7FFF(Non-secure). The address between 0x2001_8000 to 0x2FFF_FFFF(Secure) and 0x3001_8000 to 0x3FFF_FFFF(Non-secure) is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

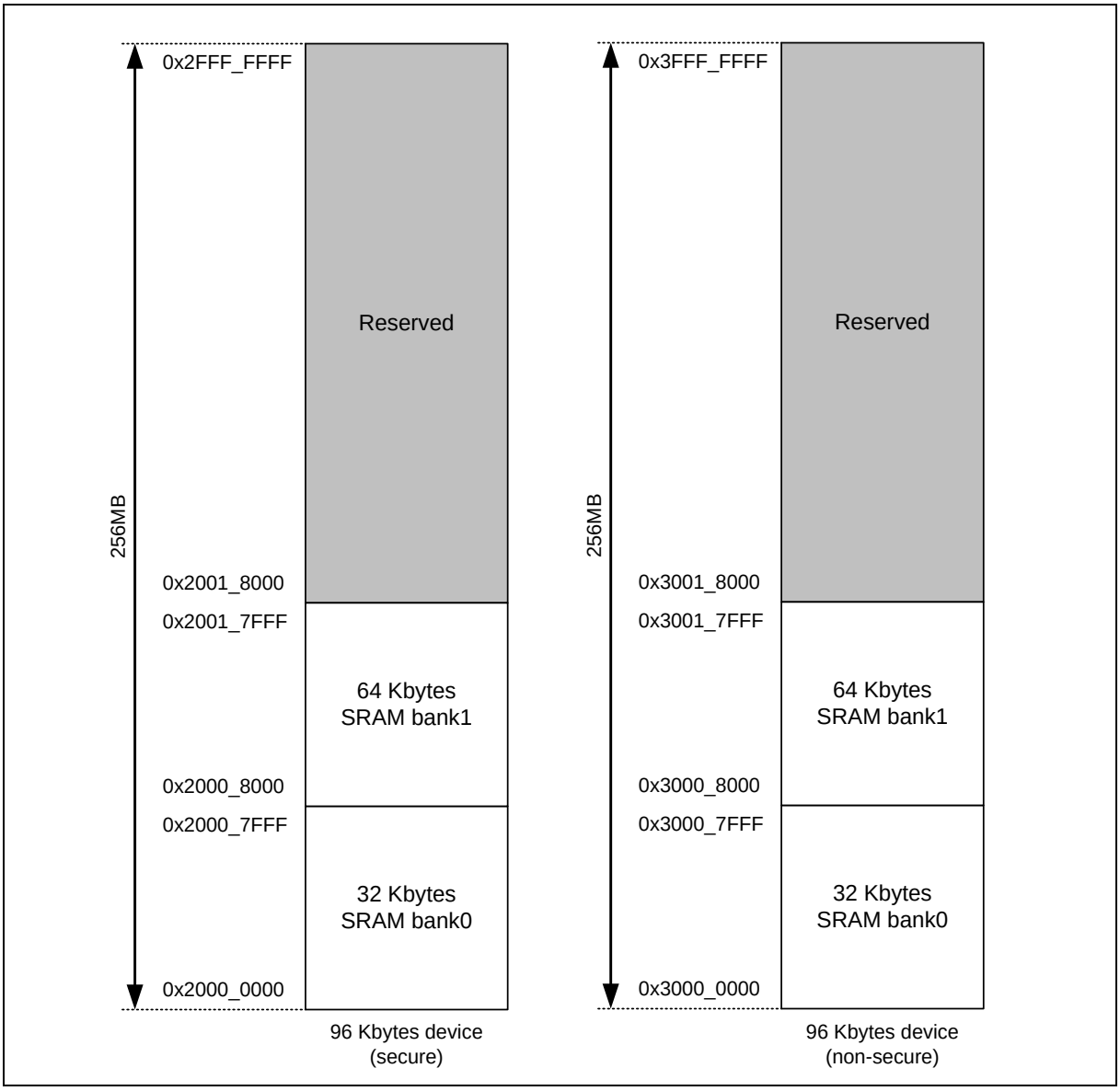


Figure 6.3-11 SRAM Memory Organization

SRAM bank0 has byte parity error check function. When CPU is accessing SRAM bank0, the parity error checking mechanism is dynamic operating. As parity error occurs, the PERRIF (SYS_SRAMSTS[0]) will be asserted to 1 and the SYS_SRAMEADR register will recode the address with the parity error. Chip will enter interrupt when SRAM parity error occurs if PERRIEN (SYS_SRAMICTL[0]) is set to 1. When SRAM parity error occurs, chip will stop detecting SRAM parity error until user writes 1 to clear the PERRIF(SYS_SRAMSTS[0]) bit.

SRAM Power Control

SRAM bank0 and bank1 have marco retention and power shut down function. Each SRAM marco can be configured to retention or power shut down mode independently by SRAMxPMn (SYS_SRAMPCTL[23:8], x=0-1 n=0-3). When chip entering power-down, each SRAM marco will enter retention or power shut down or keep operation mode depended on SRAMxPMn(SYS_SRAMPCTL[23:8], x=0-1 n=0-3).When chip power down wake up, SRAM marco will wake up from retention or power shut down mode. User must identify which SRAM marco that CPU first accessed for saving power down wake up time by STACK(SYS_SRAMPCTL[1:0]).

Figure 6.3-12 shows the SRAM marco number in bank0 and bank1. When chip power down wake up, the first wake up SRAM marco is depened on STACK (SYS_SRAMPCTL[1:0]), the rest SRAM marcos wake up in the order of marco number, from SRAM marco0 to SRAM marco7.

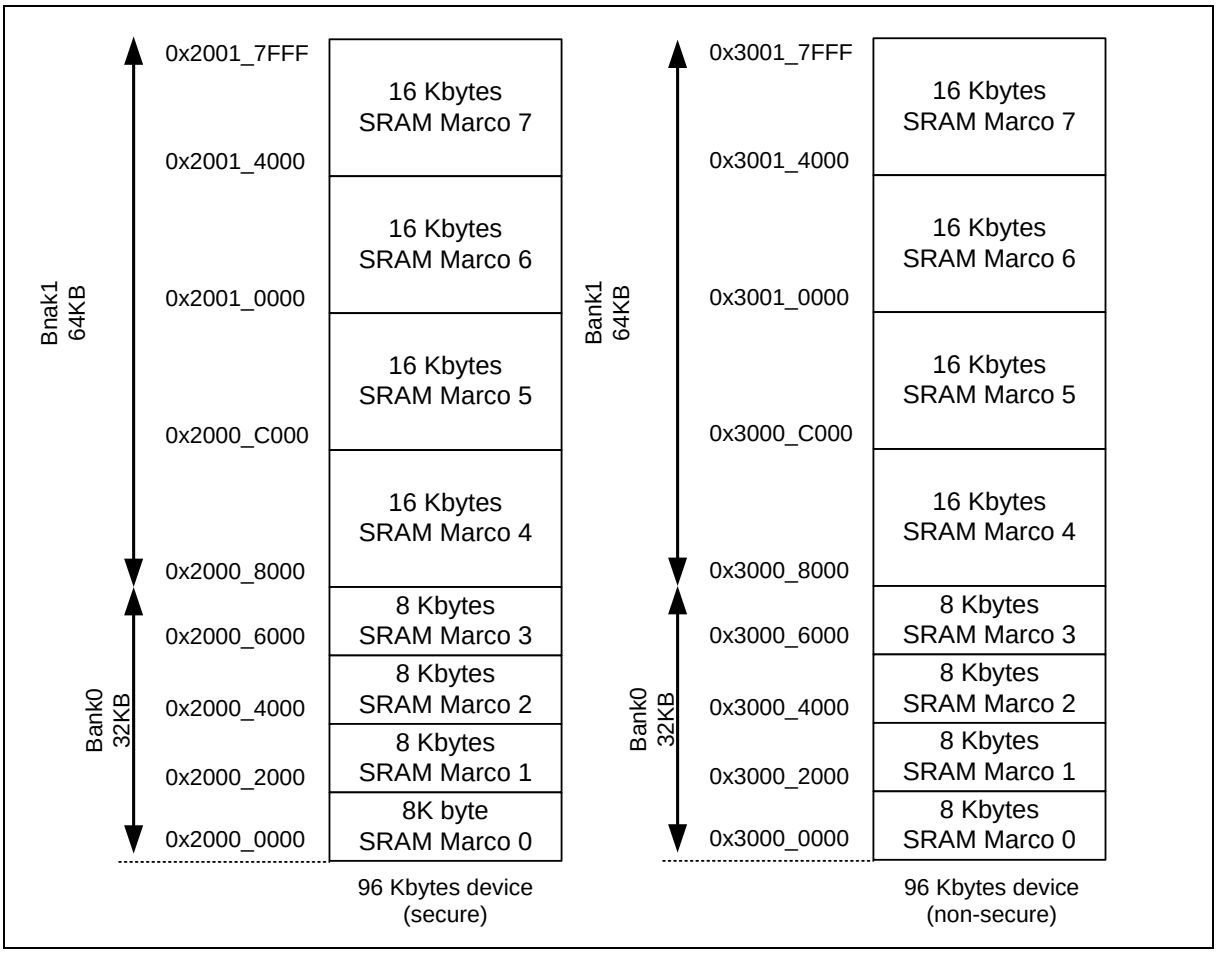


Figure 6.3-12 SRAM Marco Organization

6.3.9 Auto Trim

This chip supports auto-trim function: the HIRC trim (12 MHz RC oscillator, 48 MHz RC oscillator), according to the accurate external 32.768 kHz crystal oscillator or internal USB synchronous mode, to automatically get accurate HIRC output frequency, 0.25 % deviation within all temperature ranges.

For instance, the system needs an accurate 12 MHz clock. In such case, if neither using PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_TCTL12M[10] reference clock selection) to “1”, set FREQSEL (SYS_TCTL12M[1:0] trim frequency selection) to “01”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_TISTS12M[8] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation.

In another case, the system needs an accurate 48 MHz clock. In such case, if neither using PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_TCTL48M[10] reference clock selection) to “1”, set FREQSEL (SYS_TCTL48M[1:0] trim frequency selection) to “01”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_TISTS48M[8] HIRC48 frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation.

6.3.10 System Timer (SysTick)

The Cortex®-M23 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_VAL) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_LOAD) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_VAL value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_LOAD value rather than an arbitrary value when it is enabled.

If the SYST_LOAD is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “*Arm®Cortex®-M23 Technical Reference Manual*” and “*Arm®v8-M Architecture Reference Manual*”.

6.3.11 Nested Vectored Interrupt Controller (NVIC)

The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts. You can only fully access the NVIC from privileged mode, but you can cause interrupts to enter a pending state in user mode if you enable the Configuration and Control Register. Any other user mode access causes a bus fault. You can access all NVIC registers using byte, halfword, and word accesses unless otherwise stated. NVIC registers are located within the SCS (System Control Space). All NVIC registers and system debug registers are little-endian regardless of the endianness state of the processor.

The NVIC supports:

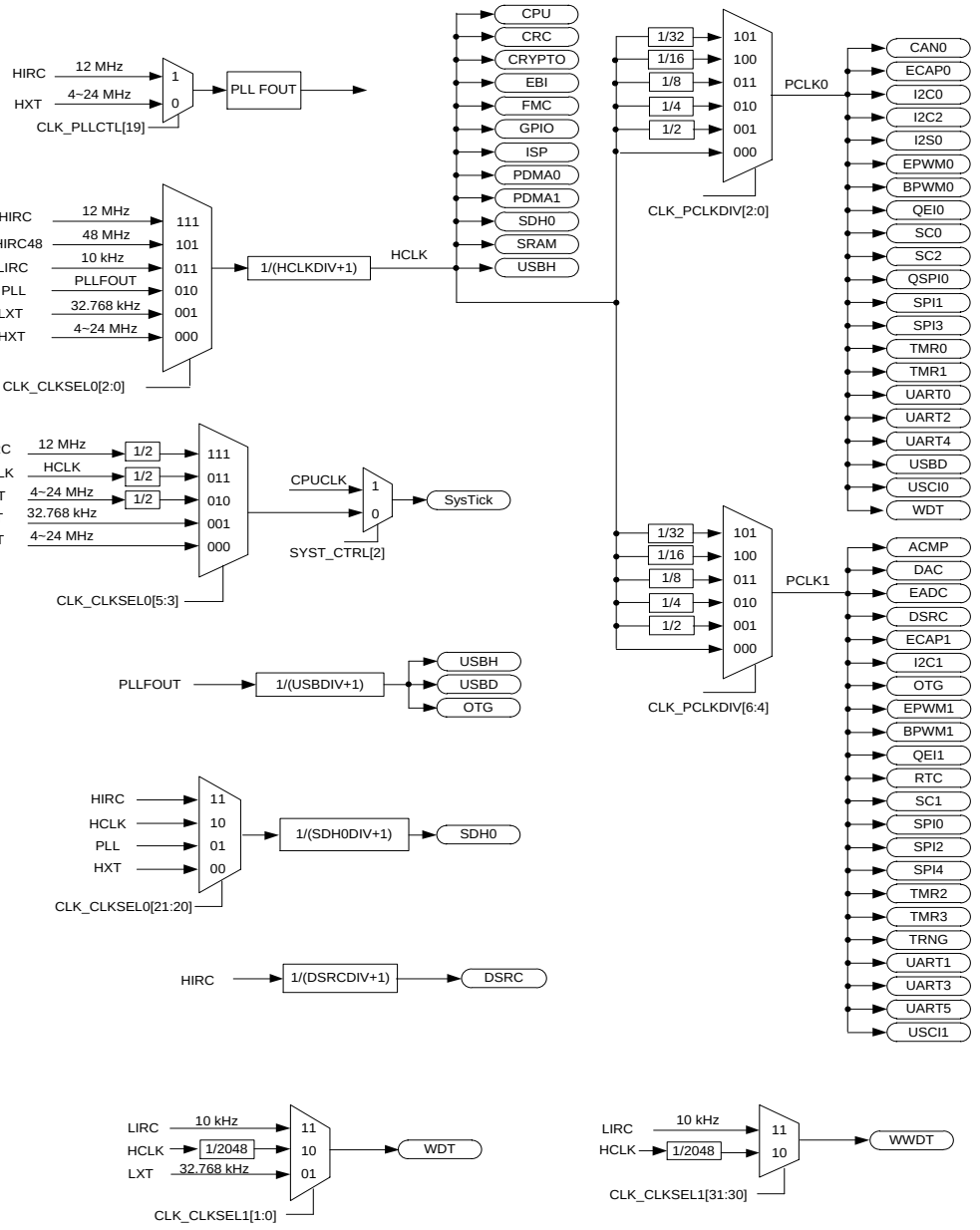
- An implementation-defined number of interrupts, in the range 1-240 interrupts.
- A programmable priority level of 0-3 for each interrupt; a higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.
- Level and pulse detection of interrupt signals.
- Dynamic reprioritization of interrupts.
- Grouping of priority values into group priority and subpriority fields.
- Interrupt tail-chaining.
- An external Non Maskable Interrupt (NMI)
- WIC with Ultra-low Power Sleep mode support

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

6.4 Clock Controller

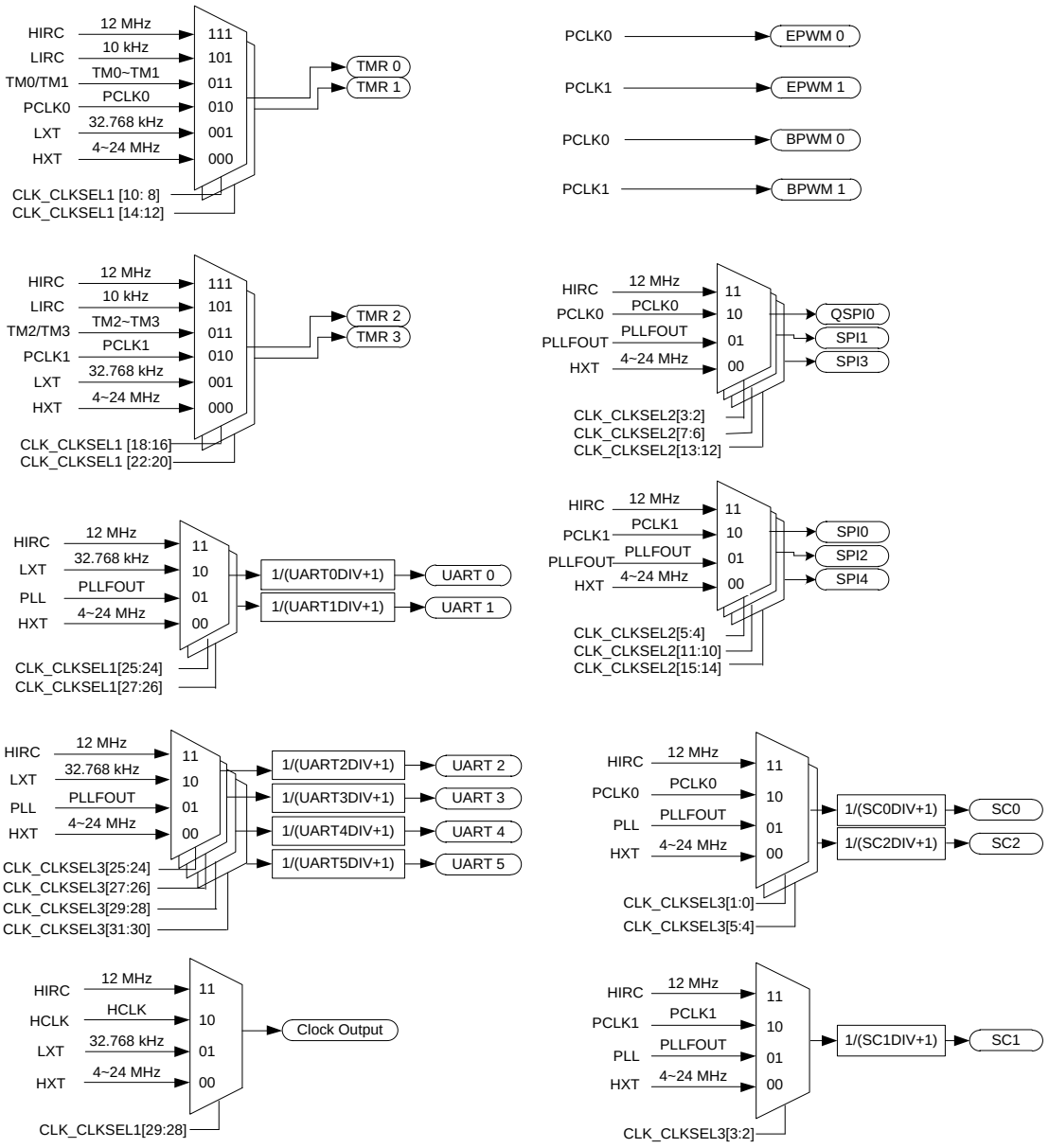
6.4.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN (CLK_PWRCTL[7]) and core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT), 48MHz internal high speed RC oscillator (HIRC48) and 12 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. Figure 6.4-1 to Figure 6.4-3 show the clock generator and the overview of the clock source control.



Note:
Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.4-1 Clock Generator Global View Diagram (1/3)



Note:
Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.4-2 Clock Generator Global View Diagram (2/3)

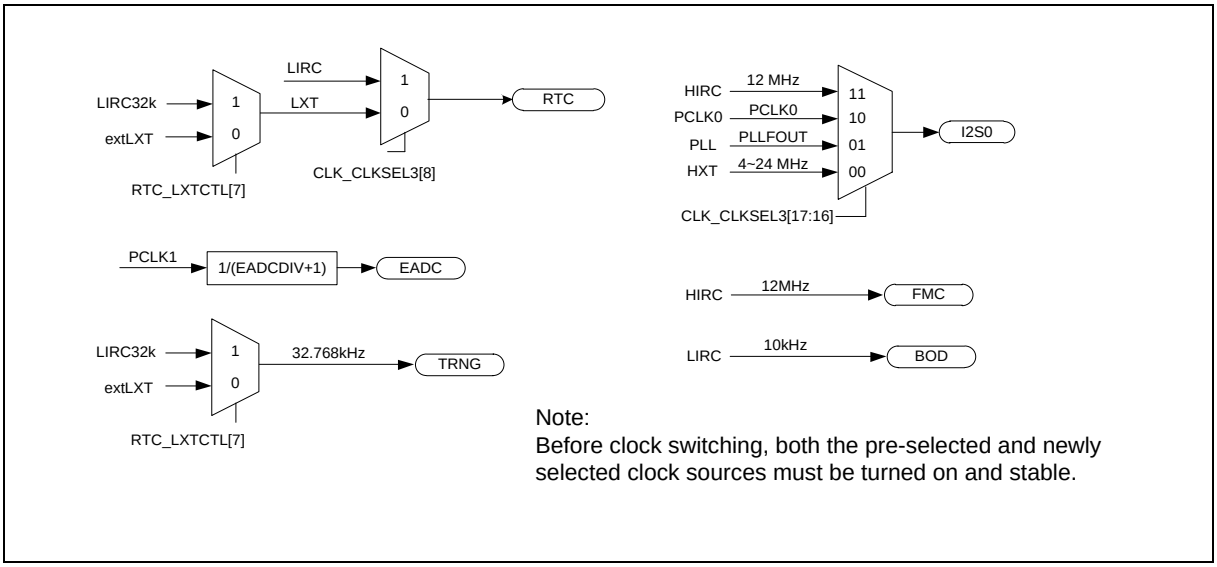
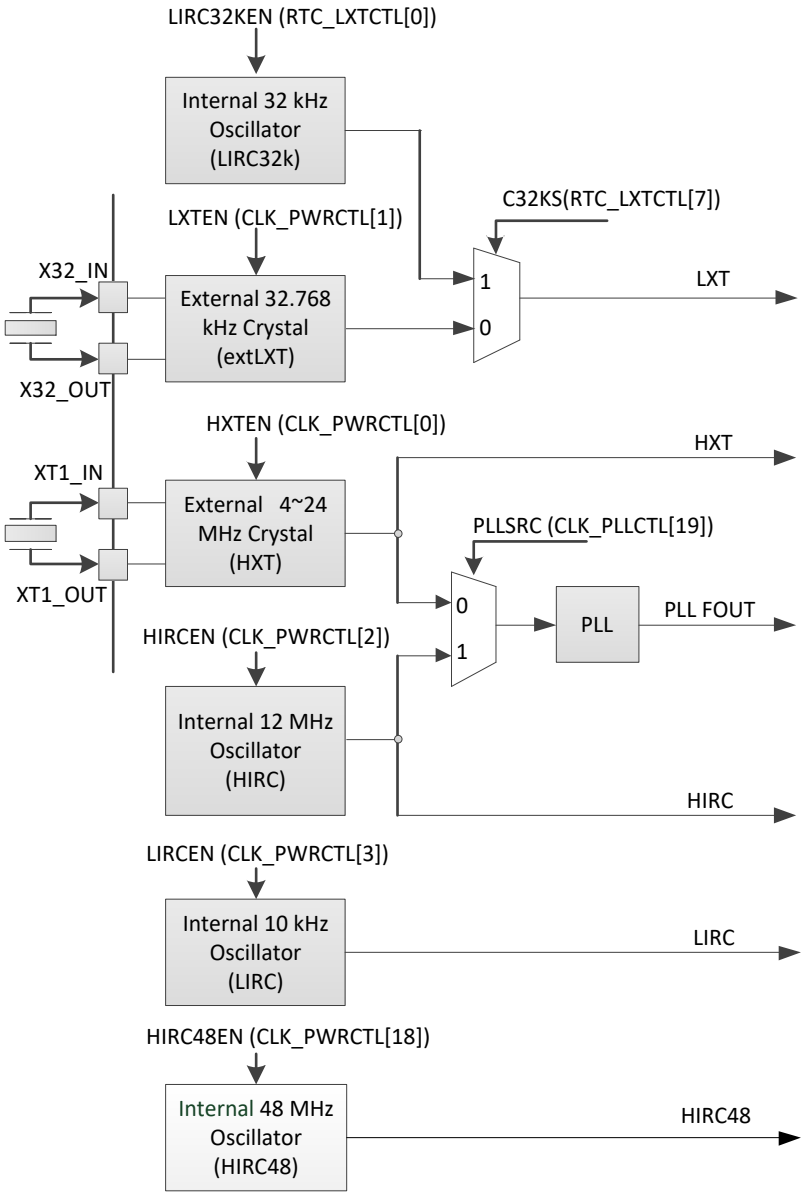


Figure 6.4-3 Clock Generator Global View Diagram (3/3)

6.4.2 Clock Generator

The clock generator consists of 6 clock sources, which are listed below:

- 32.768 kHz external low speed crystal oscillator (LXT)
- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLLFOUT), PLL source can be selected from external 4~24 MHz external high speed crystal (HXT) or 12 MHz internal high speed oscillator (HIRC)
- 12 MHz internal high speed RC oscillator (HIRC)
- 48 MHz internal high speed RC oscillator (HIRC48)
- 10 kHz internal low speed RC oscillator (LIRC)



Note:
Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.4-4 Clock Generator Block Diagram

Each of these clock sources has certain stable time to wait for clock operating at stable frequency. When clock source is enabled, a stable counter start counting and correlated clock stable index.

That is, HXTSTB (CLK_STATUS[0]), LXTSTB (CLK_STATUS[1]), PLLSTB (CLK_STATUS[2]), LIRCSTB (CLK_STATUS[3]), HIRCSTB (CLK_STATUS[4]), HIRC48STB (CLK_STATUS[6]), EXTLXTSTB (CLK_STATUS[8]) and LIRC32STB(CLK_STATUS[9]) these bits are set to 1 after the stable counter value reaches a defined value.

System and peripheral can use the clock as its operating clock only when correlate clock stable index

is set to 1. The clock stable index will be auto cleared when the clock source (HXTEN (CLK_PWRCTL[0]), LXTEN (CLK_PWRCTL[1]), LIRC32KEN (RTC_LXTCTL[0]), HIRCEN (CLK_PWRCTL[2]), LIRCEN (CLK_PWRCTL[3]), HIRC48EN (CLK_PWRCTL[18]) and PD (CLK_PLLCTL[16])) are disabled.

Besides, the clock stable index of HXT, HIRC, HIRC48 and PLL will be auto cleared when chip enters power-down and clock stable counter will re-count after chip wake-up if correlate clock is enabled.

6.4.3 System Clock and SysTick Clock

The system clock has 6 clock sources which are generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0[2:0]). The block diagram is shown in Figure 6.4-5.

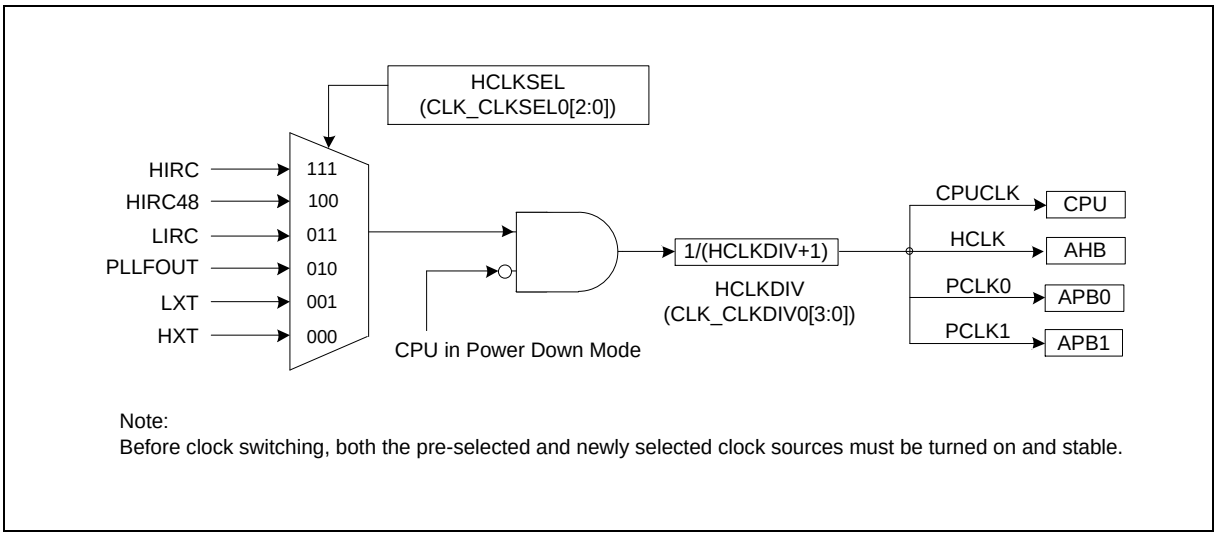


Figure 6.4-5 System Clock Block Diagram

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the HIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will auto switch to HIRC if HXT clock stop being detected on the following condition: system clock source comes from HXT or system clock source comes from PLL with HXT as the input of PLL. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIE (CLK_CLKDCTL[5]) is set to 1. HXT clock source stable flag, HXTSTB (CLK_STATUS[0]), will be cleared if HXT stops when using HXT fail detector function. User can try to recover HXT by disable HXT and enable HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recover to oscillate after re-enable action and user can switch system clock to HXT again.

The HXT clock stop detect and system clock switch to HIRC procedure is shown in Figure 6.4-6.

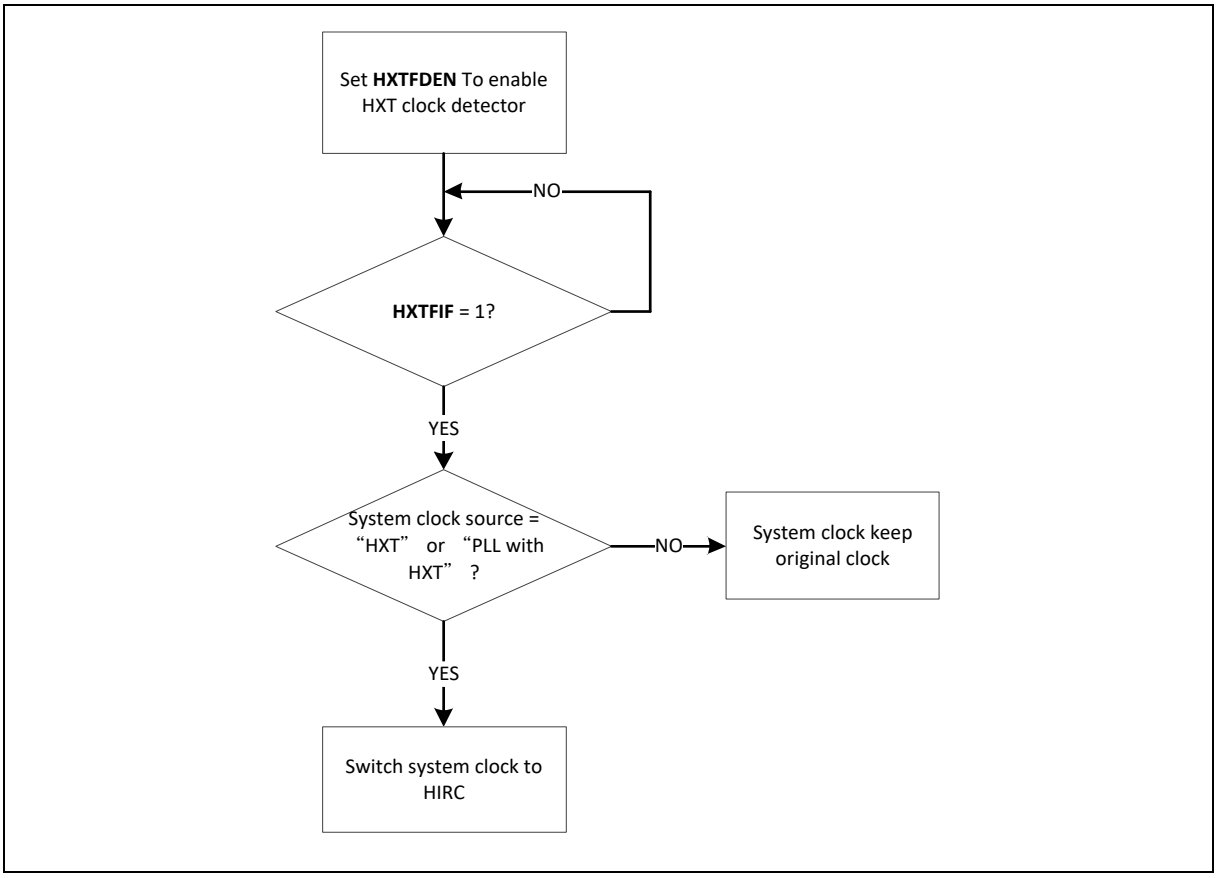


Figure 6.4-6 HXT Stop Protect Procedure

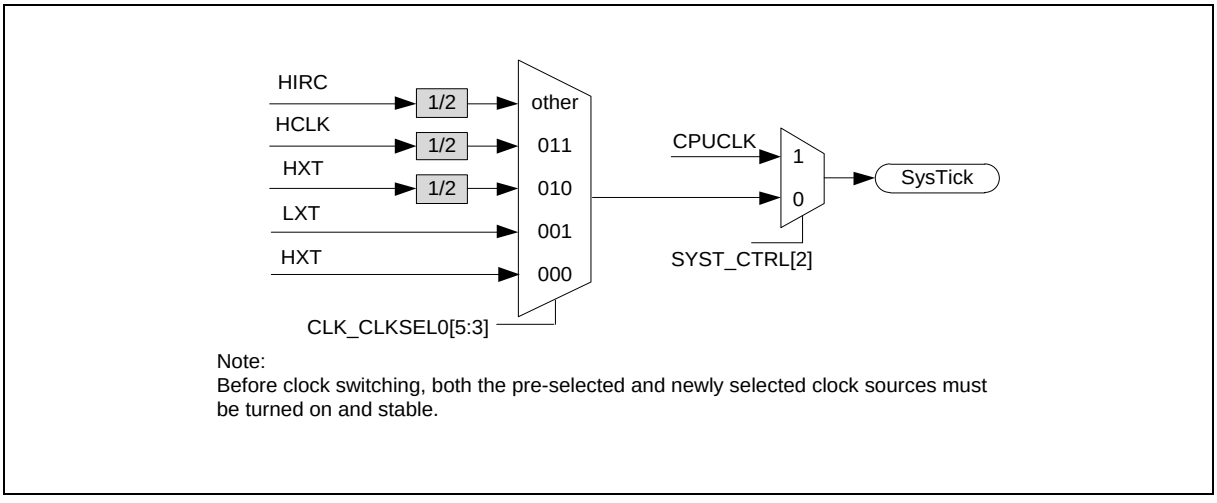


Figure 6.4-7 SysTick Clock Control Block Diagram

The clock source of SysTick in processor can use CPU clock or external clock (SYST_CTRL[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.4-7.

6.4.4 **Peripherals Clock**

Each peripheral clock has its own clock source selection. Refer to the CLK_CLKSEL1, CLK_CLKSEL2 and CLK_CLKSEL3 register.

6.4.5 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

For theses clocks, which still keep active, are listed below:

- Clock Generator
  - 10 kHz internal low speed RC oscillator (LIRC) clock
  - 32.768 kHz external low speed crystal oscillator (LXT) clock
- Peripherals Clock (When the modules adopt LXT or LIRC as clock source)

6.4.6 Clock Output

This device is equipped with a power-of-2 frequency divider which is composed by 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore, there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]). When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state.

If DIV1EN(CLK_CLKOCTL[5]) set to 1, the clock output clock (CLKO_CLK) will bypass power-of-2 frequency divider. The output divider clock will be output to CLKO pin directly.

When entering Power-down mode, clock output does not out put clock even if the CKO clock source is LXT.

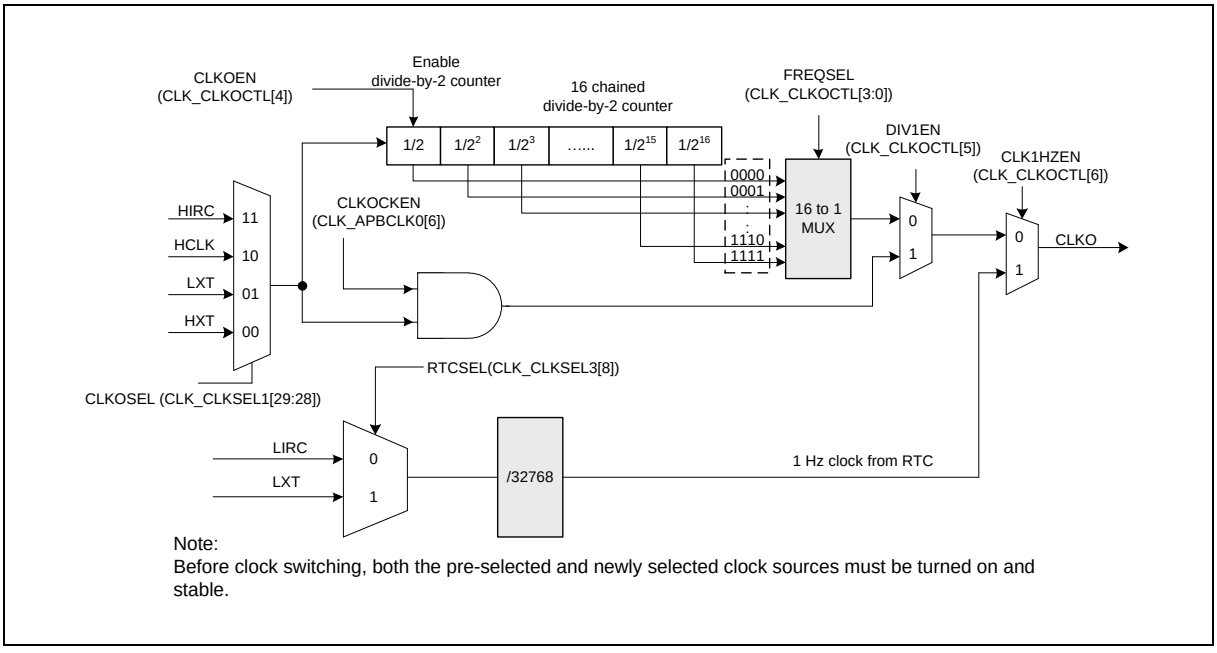


Figure 6.4-8 Clock Output Block Diagram

6.5 Security Configuration Unit (SCU)

6.5.1 Overview

Security configuration unit is designed for Arm® TrustZone®, and used to configure the security attribution of SRAM, GPIO and all other peripherals. SCU also collects AHB slaves' security violation response and generates SCU interrupt. When non-secure master tries to access SCU, SCU will response AHB bus error and generate SCU interrupt. The AHB bus error will cause system hardfault, if the master is the core processor. SCU is also equipped with a timer to monitor the duration of the core processor in non-secure state.

Note: SCU accepts secure access only.

Note: For details on Arm® TrustZone®, refer to the section "Arm® TrustZone®"

6.5.2 Features

- Configure SRAM's security attribution block by block
- Configure GPIOs' security attribution port by port
- Configure peripherals' security attribution
- Generate secure violation interrupt
- Equipped with a 24-bit timer as a non-secure state monitor

6.6 True Random Number Generator (TRNG)

6.6.1 Overview

The True Random Number Generator (TRNG) is used to generate the randomness by extracting from physical phenomena.

6.6.2 Features

- Generates 800 random bits per second

6.7 Flash Memeory Controller (FMC)

6.7.1 Overview

The FMC is equipped with dual-bank on-chip embedded Flash (BANK0 and BANK1) for application. Both BANK0 and BANK1 have 64/128/256 Kbytes space. Thus, the total size of Application ROM (APROM) is 128/256/512 Kbytes. A User Configuration block provides for system initiation in BANK0. A 4 Kbytes loader ROM (LDROM) is used for In-System-Programming (ISP) function in BANK0. A 2 Kbytes one-time-program ROM (OTP) is used for recording one-time-program data in BANK1. A 32K Secure Bootloader is used to check boot code integrity and authenticity, and consists of native ISP functions. A 4KB cache with zero wait cycle is used to improve Flash access performance. This chip also supports In-Application-Programming (IAP) function. User switches the code executing without chip reset after the embedded Flash is updated.

6.7.2 Features

- Supports dual-bank Flash macro for safe firmware upgrade
- Supports 128/256/512 Kbytes application ROM (APROM)
- Supports 4 Kbytes loader ROM (LDROM)
- Supports 4 XOM (Execution Only Memory) regions to conceal user program in APROM.
- Supports 16 bytes User Configuration block to control system initiation
- Supports 3 Kbytes one-time-program ROM (OTP)
- Supports 2 Kbytes page erase for all embedded Flash
- Supports block erase and bank erase for APROM, except XOM regions.
- Supports two level locks for protecting secure region and non-sec region.
- Supports Secure Bootloader with native In-System-Programming (ISP) functions
- Supports Secure Boot function for check boot code integrity and authenticity
- Supports Security Key protection function for APROM, LDROM, User Configuration block and KPROM protection
- Supports 32-bit/64-bit and multi-word Flash programming function
- Supports fast Flash programming verification function
- Supports CRC32 checksum calculation function
- Supports Flash all one verification function
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded Flash memory
- Supports cache memory to improve Flash access performance and reduce power consumption
- Supports auto-tuning Flash access cycle function to optimize the Flash access performance

6.8 General Purpose I/O (GPIO)

6.8.1 Overview

This chip has up to 107 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 107 pins are arranged in 8 ports named as PA, PB, PC, PD, PE, PF, PG and PH. PA, PB and PE has 16 pins on port. PC has 14 pins on port. PD has 15 pins on port. PF has 12 pins on port. PG has 10 pins on port. PH has 8 pins on port. Each of the 107 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOINI (CONFIG0[10]).

6.8.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Drive and High Slew Rate I/O mode
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - CIOINI = 0, all GPIO pins in Quasi-bidirectional mode after chip reset
  - CIOINI = 1, all GPIO pins in input mode after chip reset
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Enabling the pin interrupt function will also enable the wake-up function
- Improve access efficiency by using single cycle IO bus.

6.9 PDMA Controller (PDMA)

6.9.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. There are two PDMA controller PDMA0 and PDMA1. PDMA0 is secure PDMA, PDMA1 can be configured as secure or non-secure PDMA. Each PDMA controller has a total of 8 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

6.9.2 Features

- Supports 2 PDMA controller PDMA0 and PDMA1, PDMA0 is secure PDMA, PDMA1 can be configured as secure or non-secure PDMA.
- Supports 8 independently configurable channels
- Supports selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and USB, UART, USCI, SPI, EPWM, I^2C, I^2S, Timer, ADC, and DAC request
- Supports Scatter-Gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function on channel 0 and channel1
- Supports stride function from channel 0 to channel 5

6.10 Timer Controller (TMR)

6.10.1 Overview

The timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

The timer controller also provides four PWM generators. Each PWM generator supports two PWM output channels in independent mode and complementary mode. The output state of PWM output pin can be control by pin mask, polarity and break control, and dead-time generator.

6.10.2 Features

6.10.2.1 Timer Function Features

- Four sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger PWM, EADC, DAC and PDMA function
- Supports internal capture triggered while internal ACMP output signal transition
- Supports Inter-Timer trigger mode
- Supports event counting source from internal USB SOF signal

6.10.2.2 PWM Function Features

- Supports maximum clock frequency up to maximum PCLK
- Supports independent mode for PWM generator with two output channels
- Supports complementary mode for PWM generator with paired PWM output channel
  - 12-bit dead-time insertion with 12-bit prescale
- Supports 12-bit prescale from 1 to 4096
- Supports 16-bit PWM counter
  - Up, down and up-down count operation type
  - One-shot or auto-reload counter operation mode
- Supports mask function and tri-state enable for each PWM output pin
- Supports brake function
  - Brake source from pin, analog comparator and system safety events (clock failed,

Brown-out detection, SRAM parity error and CPU lockup)

- Brake pin noise filter control for brake source
- Edge detect brake source to control brake state until brake status cleared
- Level detect brake source to auto recover function after brake condition removed

- Supports interrupt on the following events:
  - PWM zero point, period point, up-count compared or down-count compared point events
  - Brake condition happened
- Supports trigger EADC on the following events:
  - PWM zero point, period, zero or period point, up-count compared or down-count compared point events

6.11 Watchdog Timer (WDT)

6.11.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

6.11.2 Features

- 18-bit free running up counter for WDT time-out interval
- Selectable time-out interval (24 ~ 218) and the time-out interval is 1.6 ms ~ 26.214 s if WDT_CLK = 10 kHz.
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026, 130, 18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as 10 kHz or LXT.

6.12 Window Watchdog Timer (WWDT)

6.12.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

6.12.2 Features

- 6-bit down counter value (CNTDAT, WWDT_CNT[5:0]) and 6-bit compare value (CMPDAT, WWDT_CTL[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL, WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

6.13 Real Time Clock (RTC)

6.13.1 Overview

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick and alarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

6.13.2 Features

- Supports external power pin V BAT.
- Supports real time counter in RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year, month, day) for RTC time and calendar check.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in RTC_TALM and RTC_CALM.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC_TAMSK and RTC_CAMSK.
- Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register.
- Optional support 1/128 second HZCNT in RTC_TIME and RTC_TALM.
- Supports Leap Year indication in RTC_LEAPYEAR register.
- Supports Day of the Week counter in RTC_WEEKDAY register.
- Frequency of RTC clock source compensate by RTC_FREQADJ register.
- All time and calendar message expressed in BCD format.
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
- Supports RTC Time Tick and Alarm Match interrupt.
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated.
- Supports Daylight Saving Time software control in RTC_DSTCTL.
- Supports up 3 pairs dynamic loop tamper pin or 6 individual tamper pin.
- Built-in LXT frequency monitor .
- Supports 80 bytes spare registers and tamper pins detection to clear the content of these spare registers.
- Supports Flash mass erase operate will also clear the 80 bytes spare registers content.

6.14 EPWM Generator and Capture Timer (EPWM)

6.14.1 Overview

The chip provides two EPWM generators — EPWM0 and EPWM1. Each EPWM supports 6 channels of EPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit EPWM counter with 16-bit comparator. The EPWM counter supports up, down and up-down counter types. EPWM uses comparator compared with counter to generate events. These events use to generate EPWM pulse, interrupt and trigger signal for EADC/DAC to start conversion.

The EPWM generator supports two standard EPWM output modes: Independent mode and Complementary mode, which have difference architecture. There are two output functions based on standard output modes: Group function and Synchronous function. Group function can be enabled under Independent mode or complementary mode. Synchronous function only enabled under complementary mode. Complementary mode has two comparators to generate various EPWM pulse with 12-bit dead-time generator and another free trigger comparator to generate trigger signal for EADC. For EPWM output control unit, it supports polarity output, independent pin mask and brake functions.

The EPWM generator also supports input capture function. It supports latch EPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened. Capture function also support PDMA to transfer captured data to memory.

6.14.2 Features

6.14.2.1 EPWM Function Features

- Supports maximum clock frequency up to maximum PLL frequency
- Supports up to two EPWM modules, each module provides 6 output channels
- Supports independent mode for EPWM output/Capture input channel
- Supports complementary mode for 3 complementary paired EPWM output channel
  - Dead-time insertion with 12-bit resolution
  - Synchronous function for phase control
  - Two compared values during one period
- Supports 12-bit prescaler from 1 to 4096
- Supports 16-bit resolution EPWM counter
  - Up, down and up/down counter operation type
- Supports one-shot or auto-reload counter operation mode
- Supports group function
- Supports synchronous function
- Supports mask function and tri-state enable for each EPWM pin
- Supports brake function
  - Brake source from pin, analog comparator and system safety events (clock failed, SRAM parity error, Brown-out detection and CPU lockup).
  - Noise filter for brake source from pin
  - Leading edge blanking (LEB) function for brake source from analog comparator
  - Edge detect brake source to control brake state until brake interrupt cleared

- Level detect brake source to auto recover function after brake condition removed

- Supports interrupt on the following events:
  - EPWM counter matches 0, period value or compared value
  - Brake condition happened
- Supports trigger EADC/DAC on the following events:
  - EPWM counter matches 0, period value or compared value
  - EPWM counter match free trigger comparator compared value (only for EADC)

6.14.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option
- Supports PDMA transfer function for EPWM all channels

6.15 Basic PWM Generator and Capture Timer (BPWM)

6.15.1 Overview

The chip provides two BPWM generators — BPWM0 and BPWM1. Each BPWM supports 6 channels of BPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit BPWM counter with 16-bit comparator. The BPWM counter supports up, down and up-down counter types, all 6 channels share one counter. BPWM uses the comparator compared with counter to generate events. These events are used to generate BPWM pulse, interrupt and trigger signal for EADC to start conversion. For BPWM output control unit, it supports polarity output, independent pin mask and tri-state output enable.

The BPWM generator also supports input capture function to latch BPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

6.15.2 Features

6.15.2.1 BPWM Function Features

- Supports maximum clock frequency up to maximum PLL frequency.
- Supports up to two BPWM modules; each module provides 6 output channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit prescalar from 1 to 4096
- Supports 16-bit resolution BPWM counter; each module provides 1 BPWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Supports interrupt in the following events:
  - BPWM counter matches 0, period value or compared value
- Supports trigger EADC in the following events:
  - BPWM counter matches 0, period value or compared value

6.15.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

6.16 Quadrature Encoder Interface (QEI)

6.16.1 Overview

There are two Quadrature Encoder Interfaces (QEI) QEI controllers in this device. The QEI decodes speed of rotation and motion sensor information and can be used in any application that uses a quadrature encoder for feedback.

6.16.2 Features

6.16.2.1 Quadrature Encoder Interface (QEI) Features

- Up to two QEI controllers, QEI0 and QEI1.
- Two QEI phase inputs, QEA and QEB; One Index input.
- A 32-bit up/down Quadrature Encoder Pulse Counter (QEI_CNT)
- A 32-bit software-latch Quadrature Encoder Pulse Counter Hold Register (QEI_CNTHOLD)
- A 32-bit Quadrature Encoder Pulse Counter Index Latch Register (QEI_CNTLATCH)
- A 32-bit Quadrature Encoder Pulse Counter Compare Register (QEI_CNTCMP) with a Pre-set Maximum Count Register (QEI_CNTMAX)
- One QEI control register (QEI_CTL) and one QEI Status Register (QEI_STATUS)
- Four Quadrature encoder pulse counter operation modes
  - Support x4 free-counting mode
  - Support x2 free-counting mode
  - Support x4 compare-counting mode
  - Support x2 compare-counting mode
- Encoder Pulse Width measurement mode
- Input frequency of QEA/QEB/IDX without noise filter must lower than PCLK/4
- Input frequency of QEA/QEB/IDX with noise filter must lower than Noise Filter Clk/8

6.17 Enhanced Input Capture Timer (ECAP)

6.17.1 Overview

This device provides up to two units of Input Capture Timer/Counter whose capture function can detect the digital edge-changed signal at channel inputs. Each unit has three input capture channels. The timer/counter is equipped with up counting, reload and compare-match capabilities.

6.17.2 Features

- Up to two Input Capture Timer/Counter units, CAP0 and CAP1.
- Each unit has 3 input channels.
- Each unit has its own interrupt vector.
- Each input channel has its own capture counter hold register.
- 24-bit Input Capture up-counting timer/counter.
- With noise filter in front end of input ports.
- Edge detector with three options:
  - Rising edge detection
  - Falling edge detection
  - Both edge detection
- Captured events reset and/or reload capture counter.
- Supports compare-match function.

6.18 UART Interface Controller (UART)

6.18.1 Overview

The chip provides six channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs Normal Speed UART and supports flow control function. The UART controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports ten types of interrupts. The UART controller also supports IrDA SIR, LIN and RS-485 function modes and auto-baud rate measuring function.

6.18.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT [15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
  - Support 9600 bps for UART_CLK is selected LXT.
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Supports for 3/16 bit duration for normal mode
- Supports LIN function mode (Only UART0 /UART1 with LIN function)
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detection function for receiver
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports PDMA transfer function

UART Feature	UART0/ UART1	UART2/UART3/ UART4/ UART5	SC_UART	USCI-UART
FIFO	16 Bytes	16 Bytes	4 Bytes	TX: 1byte RX: 2byte
Auto Flow Control (CTS/RTS)	√	√	-	√
IrDA	√	√	-	-
LIN	√	-	-	-
RS-485 Function Mode	√	√	-	√
nCTS Wake-up	√	√	-	√
Imcoming Data Wake-up	√	√	-	√
Received Data FIFO reached threshold Wake-up	√	√	-	-
RS-485 Address Match (AAD mode) Wake-up	√	√	-	-
Auto-Baud Rate Measurement	√	√	-	√
STOP Bit Length	1, 1.5, 2 bit	1, 1.5, 2 bit	1, 2 bit	1, 2 bit
Word Length	5, 6, 7, 8 bits	5, 6, 7, 8 bits	5, 6, 7, 8 bits	6~13 bits
Even / Odd Parity	√	√	√	√
Stick Bit	√	√	-	-
Note: √= Supported				

Table 6.18-1 NuMicro® M2351 Series UART Features

6.19 Smart Card Host Interface (SC)

6.19.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal.

6.19.2 Features

- ISO 7816-3 T = 0, T = 1 compliant
- EMV2000 compliant
- Three ISO 7816-3 ports
- Separates receive/transmit 4 byte entry FIFO for data payloads
- Programmable transmission clock frequency
- Programmable receiver buffer trigger level
- Programmable guard time selection (11 ETU ~ 267 ETU)
- One 24-bit timer and two 8-bit timers for Answer to Request (ATR) and waiting times processing
- Supports auto direct / inverse convention function
- Supports transmitter and receiver error retry and error number limiting function
- Supports hardware activation sequence process, and the time between PWR on and CLK start is configurable
- Supports hardware warm reset sequence process
- Supports hardware deactivation sequence process
- Supports hardware auto deactivation sequence when detected the card removal
- Supports UART mode
  - Full duplex, asynchronous communications
  - Separates receiving / transmitting 4 bytes entry FIFO for data payloads
  - Supports programmable baud rate generator
  - Supports programmable receiver buffer trigger level
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting EGT (SCn_EGT[7:0])
  - Programmable even, odd or no parity bit generation and detection
  - Programmable stop bit, 1- or 2- stop bit generation

6.20 I²S Controller (I²S)

6.20.1 Overview

The I²S controller consists of I²S protocol to interface with external audio CODEC. Two 16-level depth FIFO for reading path and writing path respectively are capable of handling 8/16/24/32 bits audio data sizes. A PDMA controller handles the data movement between FIFO and memory.

6.20.2 Features

- Supports Master mode and Slave mode
- Capable of handling 8, 16, 24 and 32 bits data sizes in each audio channel
- Supports monaural and stereo audio data
- Supports I²S protocols: Philips standard, MSB-justified, and LSB-justified data format
- Supports PCM protocols: PCM standard, MSB-justified, and LSB-justified data format
- PCM protocol supports TDM multi-channel transmission in one audio sample, and the number of data channel can be set as 2, 4, 6, or 8
- Provides two 16-level FIFO data buffers, one for transmitting and the other for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary
- Supports two PDMA requests, one for transmitting and the other for receiving

6.21 Serial Peripheral Interface (SPI)

6.21.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The M2351 series contains up to four sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device and supports the PDMA function to access the data buffer. Each SPI controller also supports I^2S mode to connect external audio CODEC.

6.21.2 Features

- SPI Mode
  - Up to four sets of SPI controllers
  - Supports Master or Slave mode operation
  - Configurable bit length of a transaction word from 8 to 32-bit
  - Provides separate 4-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports Byte or Word Suspend mode
  - Supports PDMA transfer
  - Supports one data channel half-duplex transfer
  - Supports receive-only mode
- I^2S Mode
  - Supports Master or Slave
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Each provides two 4-level FIFO data buffers, one for transmitting and the other for receiving
  - Supports monaural and stereo audio data
  - Supports PCM mode A, PCM mode B, I^2S and MSB justified data format
  - Supports two PDMA requests, one for transmitting and the other for receiving

6.22 Quad Serial Peripheral Interface (QSPI)

6.22.1 Overview

The Quad Serial Peripheral Interface (QSPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The M2351 series contains one QSPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device.

The QSPI controller supports 2-bit Transfer mode to perform full-duplex 2-bit data transfer and also supports Dual and Quad I/O Transfer mode and the controller supports the PDMA function to access the data buffer.

6.22.2 Features

- Supports Master or Slave mode operation
- Supports 2-bit Transfer mode
- Supports Dual and Quad I/O Transfer mode
- Configurable bit length of a transaction word from 8 to 32-bit
- Provides separate 8-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports Byte Reorder function
- Supports Byte or Word Suspend mode
- Supports PDMA transfer
- Supports 3-Wire, no slave selection signal, bi-direction interface
- Supports one data channel half-duplex transfer
- Supports receive-only mode

6.23 I²C Serial Interface Controller (I²C)

6.23.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are three sets of I²C controllers which support Power-down wake-up function.

6.23.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to three I²C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports High speed mode 3.4Mbps
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing and 10-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports PDMA with one buffer capability
- Supports setup/hold time programmable
- Supports Bus Management (SM/PM compatible) function

6.24 USCI - Universal Serial Control Interface Controller (USCI)

6.24.1 Overview

The Universal Serial Control Interface (USCI) is a flexible interface module covering several serial communication protocols. The user can configure this controller as UART, SPI, or I^2C functional protocol.

6.24.2 Features

The controller can be individually configured to match the application needs. The following protocols are supported:

- UART
- SPI
- I^2C

6.25 USCI – UART Mode

6.25.1 Overview

The asynchronous serial channel UART covers the reception and the transmission of asynchronous data frames. It performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the controller. The receiver and transmitter being independent, frames can start at different points in time for transmission and reception.

The UART controller also provides auto flow control. There are two conditions to wake-up the system.

6.25.2 Features

- Supports one transmit buffer and two receive buffer for data payload
- Supports hardware auto flow control function
- Supports programmable baud-rate generator
- Support 9-bit Data Transfer (Support 9-bit RS-485)
- Baud rate detection possible by built-in capture event of baud rate generator
- Supports PDMA capability
- Supports Wake-up function (Data and nCTS Wakeup Only)

6.26 USCI - SPI Mode

6.26.1 Overview

The SPI protocol of USCI controller applies to synchronous serial data communication and allows full duplex transfer. It supports both master and Slave operation mode with the 4-wire bi-direction interface. SPI mode of USCI controller performs a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI mode is selected by FUNMODE (USCI_CTL[2:0]) = 0x1

This SPI protocol can operate as master or Slave mode by setting the SLAVE (USCI_PROTCTL[0]) to communicate with the off-chip SPI Slave or master device. The application block diagrams in master and Slave mode are shown below.

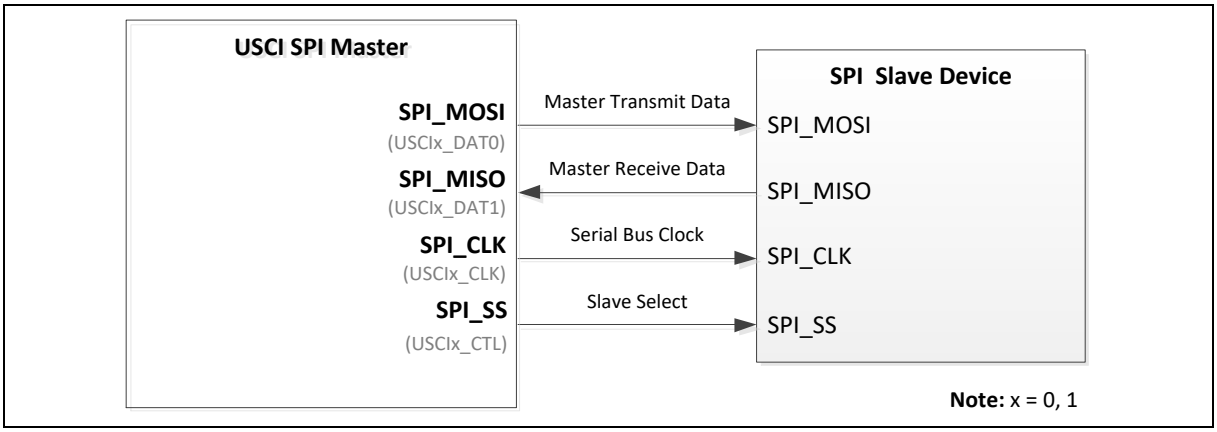


Figure 6.26-1 SPI Master Mode Application Block Diagram

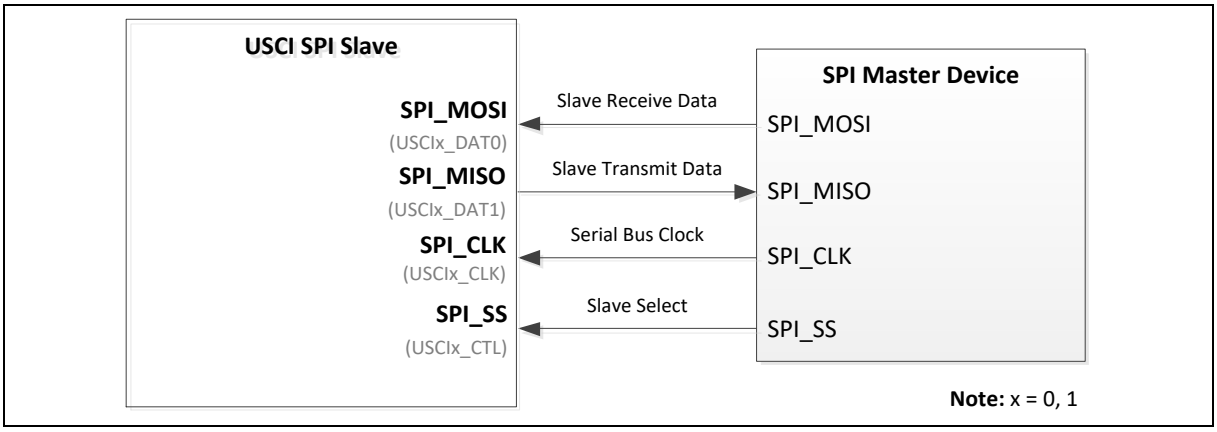


Figure 6.26-2 SPI Slave Mode Application Block Diagram

6.26.2 Features

- Supports Master or Slave mode operation (the maximum frequency -- Master = f_{PCLK} / 2, Slave < f_{PCLK} / 5)
- Configurable bit length of a transfer word from 4 to 16-bit
- Supports one transmit buffer and two receive buffers for data payload
- Supports MSB first or LSB first transfer sequence

- Supports Word Suspend function
- Supports PDMA transfer
- Supports 3-wire, no slave select signal, bi-direction interface
- Supports wake-up function by slave select signal in Slave mode
- Supports one data channel half-duplex transfer

6.27 USCI - I²C Mode

6.27.1 Overview

On I²C bus, data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 6.27-1 for more detailed I²C BUS Timing.

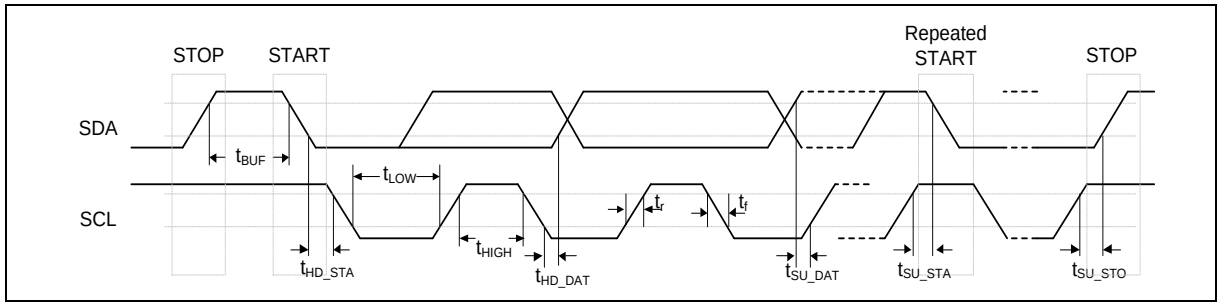


Figure 6.27-1 I²C Bus Timing

The device's on-chip I²C provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. The I²C mode is selected by FUNMODE (USCI_CTL [2:0]) = 100B. When enable this port, the USCI interfaces to the I²C bus via two pins: SDA and SCL. When I/O pins are used as I²C ports, user must set the pins function to I²C in advance.

Note: Pull-up resistor is needed for I²C operation because the SDA and SCL are set to open-drain pins when USCI is selected to I²C operation mode .

6.27.2 Features

- Full master and slave device capability
- Supports of 7-bit addressing, as well as 10-bit addressing
- Communication in standard mode (100 kBit/s) or in fast mode (up to 400 kBit/s)
- Supports multi-master bus
- Supports one transmit buffer and two receive buffer for data payload
- Supports 10-bit bus time-out capability
- Supports bus monitor mode.
- Supports Power down wake-up by data toggle or address match
- Supports setup/hold time programmable
- Supports multiple address recognition (two slave address with mask option)

6.28 Controller Area Network (CAN)

6.28.1 Overview

The C_CAN consists of the CAN Core, Message RAM, Message Handler, Control Registers and Module Interface. The CAN Core performs communication according to the CAN protocol version 2.0 part A and B. The bit rate can be programmed to values up to 1MBit/s. For the connection to the physical layer, additional transceiver hardware is required.

For communication on a CAN network, individual Message Objects are configured. The Message Objects and Identifier Masks for acceptance filtering of received messages are stored in the Message RAM. All functions concerning the handling of messages are implemented in the Message Handler. These functions include acceptance filtering, the transfer of messages between the CAN Core and the Message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

The register set of the C_CAN can be accessed directly by the software through the module interface. These registers are used to control/configure the CAN Core and the Message Handler and to access the Message RAM.

6.28.2 Features

- Supports CAN protocol version 2.0 part A and B
- Bit rates up to 1 MBit/s
- 32 Message Objects
- Each Message Object has its own identifier mask
- Programmable FIFO mode (concatenation of Message Objects)
- Maskable interrupt
- Disabled Automatic Re-transmission mode for Time Triggered CAN applications
- Programmable loop-back mode for self-test operation
- 16-bit module interfaces to the AMBA APB bus
- Supports wake-up function

6.29 Secure Digital Host Controller (SDH)

6.29.1 Overview

The Secure Digital Host Controller (SD Host) has DMAC unit and SD unit. The DMAC unit provides a DMA (Direct Memory Access) function for SD to exchange data between system memory and shared buffer (128 bytes), and the SD unit controls the interface of SD/SDHC. The SDHOST controller can support SD/SDHC and cooperated with DMAC to provide a fast data transfer between system memory and cards.

6.29.2 Features

- AMBA AHB master/slave interface compatible, for data transfer and register read/write.
- Supports single DMA channel.
- Supports hardware Scatter-Gather function.
- Using single 128 Bytes shared buffer for data exchange between system memory and cards.
- Synchronous design for DMA with single clock domain, AHB bus clock (HCLK).
- Interface with DMAC for register read/write and data transfer.
- Supports SD/SDHC card.
- Completely asynchronous design for Secure Digital with two clock domains, HCLK and Engine clock, note that frequency of HCLK should be higher than the frequency of peripheral clock.

6.30 External Bus Interface (EBI)

6.30.1 Overview

This chip is equipped with an external bus interface (EBI) for external device use. To save the connections between an external device and a chip, EBI is operating at address bus and data bus multiplex mode. The EBI supports three chip selects that can connect three external devices with different timing setting requirements.

6.30.2 Features

- Supports up to three memory banks
- Supports dedicated external chip select pin with polarity control for each bank
- Supports accessible space up to 1 Mbytes for each bank, actually external addressable space is dependent on package pin out
- Supports 8-/16-bit data width
- Supports byte write in 16-bit data width mode
- Supports Address/Data multiplexed Mode
- Supports Timing parameters individual adjustment for each memory block
- Supports LCD interface i80 mode
- Supports PDMA mode
- Supports variable external bus base clock (MCLK) which based on HCLK
- Supports configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R)
- Supports address bus and data bus separate mode

6.31 USB 1.1 Device Controller (USBD)

6.31.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and supports control/bulk/interrupt/isochronous transfer types.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 1 Kbytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SIE. User needs to set the effective starting address of SRAM for each endpoint buffer through buffer segmentation register (USBD_BUFSEGx).

There are 12 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of “Endpoint Control” is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are four different interrupt events in this controller. They are the no-event-wake-up, device plug-in or plug-out event, USB events, like IN ACK, OUT ACK etc, and BUS events, like suspend and resume, etc. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USBD_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register (USBD_EPSTS0 and USBD_EPSTS1) to acknowledge what kind of event occurring in this endpoint.

A software-disconnect function is also supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables SE0 bit (USBD_SE0), the USB controller will force the output of USB_D+ and USB_D- to level low and its function is disabled. After disable the SE0 bit, host will enumerate the USB device again.

For more information on the Universal Serial Bus, please refer to *Universal Serial Bus Specification Revision 1.1.*

6.31.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 4 different interrupt events (NEVWK, VBDET, USB and BUS)
- Supports Control/Bulk/Interrupt/Isochronous transfer type
- Supports suspend function when no bus activity existing for 3 ms
- Supports 12 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 1 Kbytes buffer size
- Provides remote wake-up capability

6.32 USB 1.1 Host Controller (USBH)

6.32.1 Overview

This chip is equipped with a USB 1.1 Host Controller (USBH) that supports Open Host Controller Interface (OpenHCI, OHCI) Specification, a register-level description of a host controller, to manage the devices and data transfer of Universal Serial Bus (USB).

The USBH supports an integrated Root Hub with a USB port, a DMA for real-time data transfer between system memory and USB bus, port power control and port over current detection.

The USBH is responsible for detecting the connect and disconnect of USB devices, managing data transfer, collecting status and activity of USB bus, providing power control and detecting over current of attached USB devices.

6.32.2 Features

- Compliant with Universal Serial Bus (USB) Specification Revision 1.1.
- Supports Open Host Controller Interface (OpenHCI) Specification Revision 1.0.
- Supports both full-speed (12Mbps) and low-speed (1.5Mbps) USB devices.
- Supports Control, Bulk, Interrupt and Isochronous transfers.
- Supports an integrated Root Hub.
- Supports a USB host port shared with USB device (OTG function).
- Supports port power control and port over current detection.
- Supports DMA for real-time data transfer.

6.33 USB On-The-Go (OTG)

6.33.1 Overview

The OTG controller interfaces to USB PHY and USB controllers which consist of a USB 1.1 host controller and a USB 2.0 FS device controller. The OTG controller supports HNP and SRP protocols defined in the “On-The-Go and Embedded Host Supplement to the USB 2.0 Revision 2.0 Specification”.

USB frame, including USB host, USB device, and OTG controller, can be configured as Host-only, Device-only, ID-dependent or OTG Device mode defined in USBROLE (SYS_USBPHY[1:0]). In Host-only mode, USB frame acts as USB host. USB frame can support both full-speed and low-speed transfer. In Device-only mode, USB frame acts as USB device. USB frame only supports full-speed transfer. In ID-dependent mode, USB frame can be USB Host or USB device depending on USB_ID pin state. In OTG device mode, the role of USB frame depends on the definition of OTG specification. USB frame only supports full-speed transfer when OTG device acts as a peripheral.

6.33.2 Features

- Built in USB PHY
- Configurable to operate as:
  - Host-only
  - Device-only
  - ID-dependent: The role of USB frame is only dependent on USB_ID pin value--as USB Host (USB_ID pin is low) or USB Device (USB_ID pin is high). Not support HNP or SRP protocol.
  - OTG device: dependent on USB_ID pin status to be A-device (USB_ID pin is low) or B-device (USB_ID pin is high). Support HNP and SRP protocols.

6.34 CRC Controller (CRC)

6.34.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32 settings.

6.34.2 Features

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to write data to perform CRC operation

6.35 Cryptographic Accelerator (CRYPTO)

6.35.1 Overview

The Crypto (Cryptographic Accelerator) includes a secure pseudo random number generator (PRNG) core and supports AES, DES/TDES, SHA and ECC algorithms.

The PRNG core supports 64 bits, 128 bits, 192 bits, and 256 bits random number generation.

The AES accelerator is an implementation fully compliant with the AES (Advance Encryption Standard) encryption and decryption algorithm. The AES accelerator supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2, and CBC-CS3 mode.

The DES/TDES accelerator is an implementation fully compliant with the DES and Triple DES encryption/decryption algorithm. The DES/TDES accelerator supports ECB, CBC, CFB, OFB, and CTR mode.

The SHA accelerator is an implementation fully compliant with the SHA-160, SHA-224, SHA-256, and SHA-384.

The ECC accelerator is an implementation fully compliant with elliptic curve cryptography by using polynomial basis in binary field and prime filed.

6.35.2 Features

- PRNG
  - Supports 64 bits, 128 bits, 192 bits, and 256 bits random number generation
- AES
  - Supports FIPS NIST 197
  - Supports SP800-38A and addendum
  - Supports 128, 192, and 256 bits key
  - Supports both encryption and decryption
  - Supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2, and CBC-CS3 mode
  - Supports key expander
- DES
  - Supports FIPS 46-3
  - Supports both encryption and decryption
  - Supports ECB, CBC, CFB, OFB, and CTR mode
- TDES
  - Supports FIPS NIST 800-67
  - Implemented according to the X9.52 standard
  - Supports two keys or three keys mode
  - Supports both encryption and decryption
  - Supports ECB, CBC, CFB, OFB, and CTR mode
- SHA
  - Supports FIPS NIST 180, 180-2
  - Supports SHA-160, SHA-224, SHA-256, and SHA-384
- ECC

- Supports both prime field GF(p) and binary filed GF(2^m)
- Supports NIST P-192, P-224, P-256, P-384, and P-521
- Supports NIST B-163, B-233, B-283, B-409, and B-571
- Supports NIST K-163, K-233, K-283, K-409, and K-571
- Supports point multiplication, addition and doubling operations in GF(p) and GF(2^m)
- Supports modulus division, multiplication, addition and subtraction operations in GF(p)

6.36 Enhanced 12-bit Analog-to-Digital Converter (EADC)

6.36.1 Overview

The chip contains one 12-bit successive approximation analog-to-digital converter (SAR ADC converter) with 16 external input channels and 3 internal channels. The ADC converter can be started by software trigger, EPWM0/1 triggers, BPWM0/1 triggers, timer0~3 overflow pulse triggers, ADINT0, ADINT1 interrupt EOC (End of conversion) pulse trigger and external pin (EADC0_ST) input signal.

6.36.2 Features

- Analog input voltage range: 0~ VREF (Max to 3.6V)
- Reference voltage from VREF pin
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 16 single-end analog external input channels or 8 pair differential analog input channels
- Up to 3 internal channels: band-gap voltage (V_{BG}), temperature sensor (V_{TEMP}), and Battery power (V_{BAT})
- Four ADC interrupts (ADINT0~3) with individual interrupt vector addresses
- Maximum ADC clock frequency is 64 MHz
- Up to 3.76 MSPS conversion rate
- Configurable ADC internal sampling time.
- 12-bit, 10-bit, 8-bit, 6-bit configurable resolution.
- Supports calibration and load calibration words capability.
- Supports internal reference voltage V_{REF}: 1.6V, 2.0V, 2.5V, and 3.0V.
- Supports three power saving modes:
  - Deep Power-down mode
  - Power-down mode
  - Standby mode
- Up to 19 sample modules
  - Each of sample modules which is configurable for ADC converter channel EADC_CH0~15 and trigger source
  - Sample module 16~18 is fixed for ADC channel 16, 17, 18 input sources as band-gap voltage, temperature sensor, and battery power (V_{BAT})
  - Double buffer for sample control logic module 0~3
  - Configurable sampling time for each sample module
  - Conversion results are held in 19 data registers with valid and overrun indicators
- An ADC conversion can be started by:
  - Write 1 to SWTRGn (EADC_SWTRG[n], n = 0~18)
  - External pin EADC0_ST
  - Timer0~3 overflow pulse triggers
  - ADINT0 and ADINT1 interrupt EOC (End of conversion) pulse triggers
  - EPWM/BPWM triggers

- Supports PDMA transfer
- Conversion Result Monitor by Compare Mode

6.37 Digital to Analog Converter (DAC)

6.37.1 Overview

The DAC module is a 12-bit, voltage output digital-to-analog converter. It can be configured to 12- or 8-bit output mode and can be used in conjunction with the PDMA controller. The DAC integrates a voltage output buffer that can be used to reduce output impendence and drive external loads directly without having to add an external operational amplifier.

6.37.2 Features

- Analog output voltage range: 0~$AV_{DD.}$
- Supports 12- or 8-bit output mode.
- Rail to rail settle time 8us.
- Supports up to two 12-bit 1 MSPS voltage type DAC.
- Reference voltage from internal reference voltage (INT_VREF), V_{REF} pin.
- DAC maximum conversion updating rate 1 MSPS.
- Supports voltage output buffer mode and bypass voltage output buffer mode.
- Supports software and hardware trigger, including Timer0~3, EPWM0, EPWM1, and external trigger pin to start DAC conversion.
- Supports PDMA mode.
- Supports group mode of synchronized update capability for two DACs.

6.38 Analog Comparator Controller (ACMP)

6.38.1 Overview

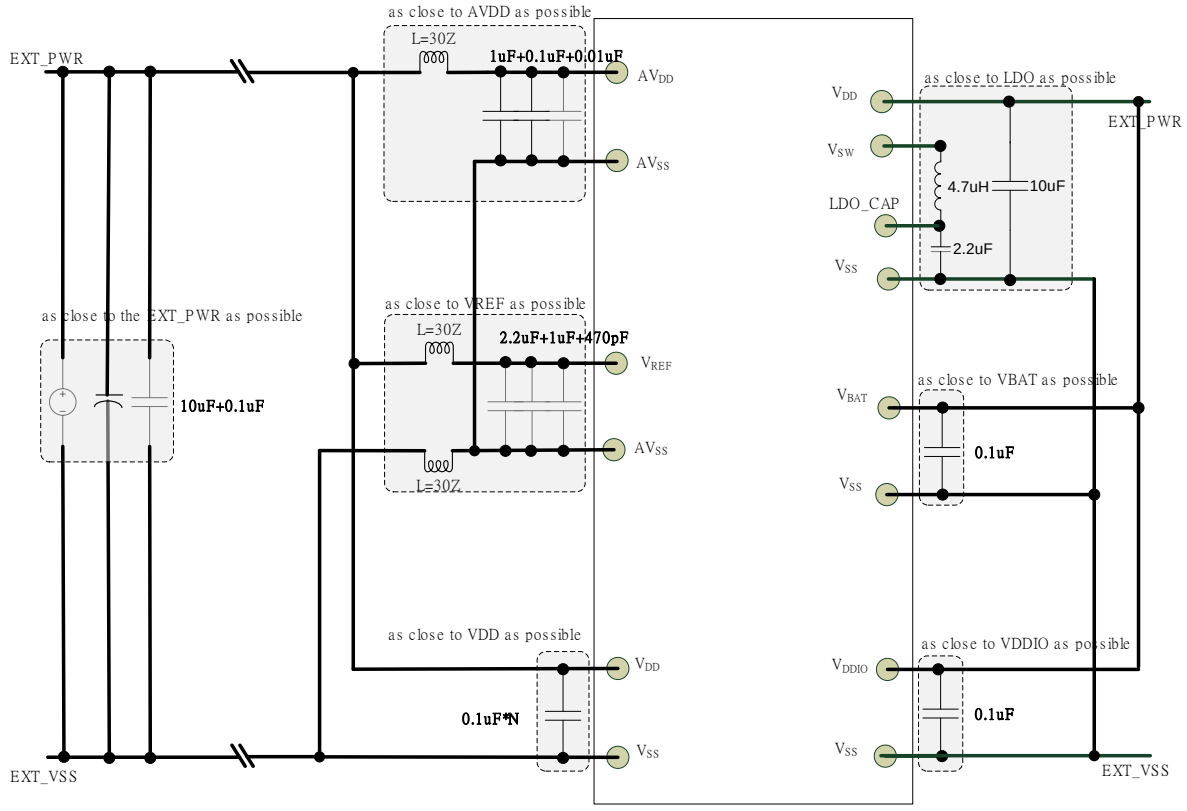
The chip provides two comparators. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. Each comparator can be configured to generate an interrupt when the comparator output value changes.

6.38.2 Features

- Analog input voltage range: 0 ~ AV_{DD} (voltage of AV_{DD} pin)
- Up to two rail-to-rail analog comparators
- Supports hysteresis function
  - Supports programmable hysteresis window: 0mV, 10mV, 20mV and 30mV
- Supports wake-up function
- Supports programmable propagaion speed and low power consumption
- Selectable input sources of positive input and negative input
- ACMP0 supports:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP0_P0, ACMP0_P1, ACMP0_P2, or ACMP0_P3
  - 4 negative sources:
    - ACMP0_N
    - Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (V_{BG})
    - DAC0 output (DAC0_OUT)
- ACMP1 supports
  - 4 multiplexed I/O pins at positive sources:
    - ACMP1_P0, ACMP1_P1, ACMP1_P2, or ACMP1_P3
  - 4 negative sources:
    - ACMP1_N
    - Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (V_{BG})
    - DAC0 output (DAC0_OUT)
- Shares one ACMP interrupt vector for all comparators
- Interrupts generated when compare results change (Interrupt event condition is programmable)
- Supports triggers for break events and cycle-by-cycle control for PWM
- Supports window compare mode and window latch mode

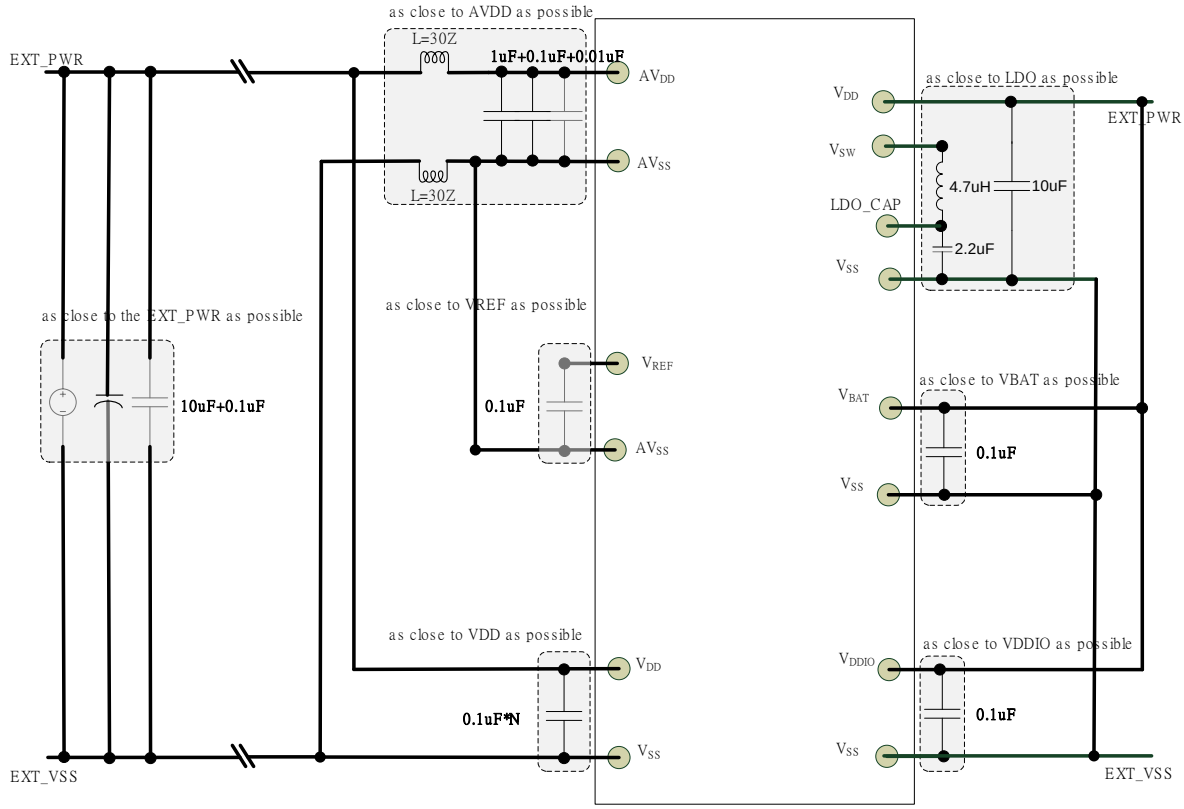
7 APPLICATION CIRCUIT

7.1 Power Supply Scheme with External V_{REF}



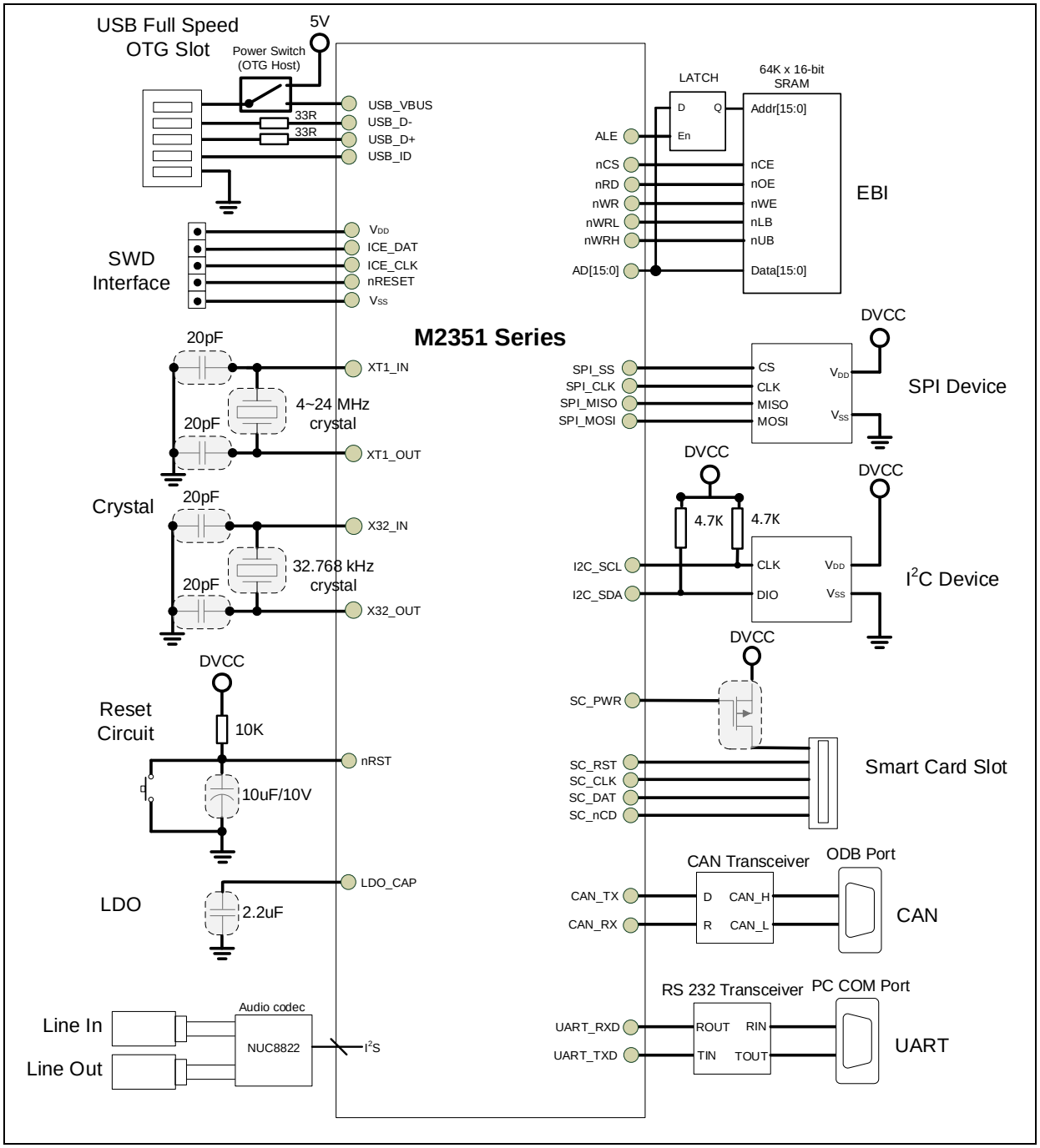
Note:V_{DD} which is near LDO need to be connected to 10 uF.(ex. QFN33 pin 27; LQFP64 pin 51; LQFP128 pin 114)

7.2 Power Supply Scheme with Internal V_{REF}



Note:V_{DD} which is near LDO need to be connected to 10 uF.(ex. QFN33 pin 27; LQFP64 pin 51; LQFP128 pin 114)

7.3 Peripheral Application Scheme



*__Note:__ USB_ID could be floating using USB or USB HS without OTG.

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Stesses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.1.1 Voltage Characteristics

Symbol	Parameter	Min	Max	Unit
V_{DD}-V_{SS}	DC Power Supply	-0.3	4.0	V
V_{DDIO}-V_{SS}	V_{DDIO} Power Supply	-0.3	4.0	V
V_{Bat}	RTC domain Power Supply	-0.3	4.0	V
$\|V_{DDX} – V_{DD}\|$	Variations between different power pins	-	50	mV
$\|V_{DD} –AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
$\|V_{SSX}$ - $V_{SS}\|$	Variations between different ground pins	-	50	mV
$\|V_{SS}$ - $AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input Voltage on 5V-tolerance GPIO	V_{SS}-0.3	5.5	V
	Input Voltage on RTC domain (PF.6 ~ PF.11)	V_{SS}-0.3	4.0	V
	Input Voltage on any other pin[*2]	V_{SS}-0.3	4.0	V

Note:

1. All main power (V_{DD}, AV_{DD}) and ground (V_{SS}, AV_{SS}) pins must always be connected to the external power supply, in the permitted range.
2. Non 5V-tolerance PIN: PA.8 ~ 15; PB.0 ~ 15; PD.10, 11, 12; PF.2, 3, 4, 5; All USB High Speed pin and nRESET pin.

Table 8.1-1 Voltage Characteristics

8.1.2 Current Characteristics

Symbol	Parameter	Max	Unit
I_{DD}	Maximum Current into V_{DD}	200	mA
I_{DDIO}	Maximum Current into V_{DDIO}	100	
I_{BAT}	Maximum Current into V_{BAT}	100	
I_{SS}	Maximum Current out of V_{SS}	100	
I_{IO}	Maximum Current sunk by a I/O Pin	20	
	Maximum Current Sourced by a I/O Pin	20	
	Maximum Current Sunk by Total I/O Pins	100	
	Maximum Current Sourced by Total I/O Pins	100	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by VIN>AVDD and a negative injection is caused by VIN<VSS. IINJ(PIN) must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 8.1-2 Current Characteristics

8.1.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA})$

- T_A = ambient temperature (℃)
- θ_{JA} = thermal resistance junction-ambient (℃/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Parameter	Min	Max	Unit
T_A	Operating Temperature	-40	105	°C
T_J	Junction temperature	-40	125	
T_{ST}	Storage Temperature	-65	150	

Table 8.1-3 Thermal Characteristics

8.1.4 EMC Characteristics

8.1.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

8.1.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latchup

performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

8.1.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system..

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International ElectrotechnicalCommission (IEC).

Symbol	Ratings	Conditions	Max	Unit
V_{EFTB} [*3] [*4]	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP128, T_A = +25 °C, f_{HCLK} = 64 MHz,	4.4	kV
$V_{ESD(HBM)}$ [*5]	Electrostatic discharge voltage (human body model)	T_A = +25 °C	2	
$V_{ESD(CDM)}$ [*6]	Electrostatic discharge voltage (charge device model)	T_A = +25 °C	0.5	
LU [*7]	Static latch-up class	T_A = +25 °C	400	mA

Note:

1. Guaranteed by characterization results, not tested in production.
2. On V_{BAT} pin, VESD(HBM) is limited to 1000V.
3. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test.
4. The performace cretia class is 4A.
5. Determined according to JEDEC EIA/JESD78 standard.
6. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
7. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.

Table 8.1-4 EMC Characteristics

8.2 General Operating Conditions

(V_{DD}-V_{SS} = 1.7 ~ 3.6V, T_A = 25°C, HCLK = 64 MHz unless otherwise specified.)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HCLK}	Internal AHB clock frequency		-	-	64	MHz
V_{DD}	Operation Voltage		1.7	-	3.6	V
AV_{DD}[*1]	Analog Operation Voltage		V_{DD}			
V_{DDIO}	Power supply for PA.0 ~ 5		1.7	-	3.6	
V_{BAT}	RTC Operation voltage for PF.6 ~ PF.11		1.7	-	3.6	
V_{LDO}	LDO Output Voltage		1.08	1.2	1.32	
V_{BG}	Band-gap Voltage		1.18	-	1.21	
C_{LDO}[*2]	LDO Output capacitance on each pin		-	2.2	-	uF

Note:

1. It is recommended to power VDD and AVDD from the same source. A maximum difference of 0.3 V between VDD and AVDD can be tolerated during power-on and power-off operation .
2. To ensure stability, an external 1 µF output capacitor, CLDO must be connected between the LDO_CAP pin and the closest GND pin of the device. Solid tantalum and multilayer ceramic capacitors are suitable as output capacitor. Additional 100 nF bypass capacitor between LDO_CAP pin and the closest GND pin of the device helps decrease output noise and improves the load transient response.

8.3 DC Electrical Characteristics

8.3.1 Typical Current Consumption

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- ALL GPIO pins are in push pull mode, output high.
- LDO = 1.26V
- The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.
- $V_{DD} = V_{BAT} = AV_{DD} = V_{DDIO}$
- When the peripherals are enabled HCLK is the system clock, $f_{PCLK0, 1} = f_{HCLK}/2$.
- Program run while(1){} from Flash.

8.3.1.1 LDO Normal Mode

Symbol	Conditions	f_{HCLK}	HXT/LXT	HIRC / HIRC48 / LIRC	PLL	T_A		unit
						25 °C	105 °C[*1]	
I_{DD}	Normal Run, executed from Flash, V_{DD} = 3.3V, V_{sw} without Inductance, all peripherals disable	64 MHz[*2]	12MHz	-	V	6.2	7.1	mA
		48 MHz[*3]	12MHz	-	V	5.2	6.0	
		12MHz[*4]	12MHz	-	-	1.7	2.4	
		6 MHz[*5]	12MHz	-	-	1.4	2.2	
		4 MHz[*6]	12MHz	-	-	1.2	1.9	
		2 MHz[*7]	12MHz	-	-	1.1	1.8	
		64 MHz[*2]		12MHz	V	6.9	7.6	
		48 MHz[*3]	-	12MHz	V	4.2	4.9	
		48 MHz[*3]	-	48MHz		3.8	4.5	
		12MHz[*4]	-	12MHz	-	1.3	1.9	
		6 MHz[*5]	-	12MHz	-	0.8	1.4	
		4 MHz[*6]	-	12MHz	-	0.7	1.4	
		2 MHz[*7]	-	12MHz	-	0.5	1.2	
		32.768 KHz	32.768 kHz	-	-	0.1	0.8	
		10KHz	-	10KHz	-	0.1	0.8	
	Normal run, executed from Flash, V_{DD} = 3.3V, V_{sw} without Inductance, all peripherals enabled	64 MHz[*2]	12MHz	-	V	14.1	15.1	
		48 MHz[*3]	12MHz	-	V	11.0	11.8	
		12MHz[*4]	12MHz	-	-	3.7	4.4	
		6 MHz[*5]	12MHz	-	-	2.8	3.5	
		4 MHz[*6]	12MHz	-	-	2.3	3.1	
		2 MHz[*7]	12MHz	-	-	2.0	2.8	
		64 MHz[*2]	-	12MHz	V	13.7	14.4	
		48 MHz[*3]	-	12MHz	V	9.6	10.2	

		48 MHz[*3]	-	48MHz		9.1	9.8	
		12MHz[*4]	-	12MHz	-	3.1	3.8	
		6 MHz[*5]	-	12MHz	-	1.9	2.5	
		4 MHz[*6]	-	12MHz	-	1.6	2.2	
		2 MHz[*7]	-	12MHz	-	1.3	1.9	
		32.768 KHz	32.768 kHz	-	-	0.8	1.5	
		10KHz	-	10KHz	-	0.9	1.6	

Note:

1. Guaranteed by characterization results, not tested in production.
2. In this case HCLK = system clock, system clock = 64MHz, LDO = 1.26V
3. In this case HCLK = system clock, system clock = 48MHz, LDO = 1.2V
4. In this case HCLK = system clock, system clock = 12MHz, LDO = 1.2V
5. In this case HCLK = system clock/2, system clock = 12MHz, LDO = 1.2V
6. In this case HCLK = system clock/3, system clock = 12MHz, LDO = 1.2V
7. In this case HCLK = system clock/6, system clock = 12MHz, LDO = 1.2V
8. When analog peripheral blocks such as ADC and ACMP are ON, an additional power consumption should be considered.

Table 8.3-1 Current Consumption in LDO Normal Run Mode

8.3.1.2 DC-DC Normal Mode

Symbol	Conditions	f_{HCLK}	HXT/LXT	HIRC / HIRC48 / LIRC	PLL	T_A		unit
						25 °C	105 °C	
I_{DD}	Normal Run, executed from Flash, V_{DD} = 3.3V, V_{sw} with Inductance, all peripherals disable	64 MHz[*2]	12MHz	-	V	3.1	3.6	mA
		48 MHz[*3]	12MHz	-	V	2.7	3.1	
		12MHz[*4]	12MHz	-	-	1.1	1.5	
		6 MHz[*5]	12MHz	-	-	1.0	1.3	
		4 MHz[*6]	12MHz	-	-	0.9	1.2	
		2 MHz[*7]	12MHz	-	-	0.8	1.2	
		64 MHz[*2]	-	12MHz	V	2.9	3.3	
		48 MHz[*3]	-	12MHz	V	1.9	2.2	
		48 MHz[*3]	-	48MHz		1.7	2.0	
		12MHz[*4]	-	12MHz	-	0.7	1.0	
		6 MHz[*5]	-	12MHz	-	0.5	0.7	
		4 MHz[*6]	-	12MHz	-	0.4	0.7	
		2 MHz[*7]	-	12MHz	-	0.3	0.6	
		32.768 KHz	32.768 kHz	-	-	0.1	0.4	
		10KHz	-	10KHz	-	0.1	0.4	
	Normal run, executed from Flash, V_{DD} = 3.3V, V_{sw} with Inductance, all peripherals enabled	64 MHz[*2]	12MHz	-	V	6.7	7.2	
		48 MHz[*3]	12MHz	-	V	5.3	5.7	
		12MHz[*4]	12MHz	-	-	2.0	2.4	
		6 MHz[*5]	12MHz	-	-	1.6	2.0	
		4 MHz[*6]	12MHz	-	-	1.5	1.8	

		2 MHz[*7]	12MHz	-	-	1.3	1.7	
		64 MHz[*2]		12MHz	V	6.5	6.8	
		48 MHz[*3]	-	12MHz	V	4.2	4.5	
		48 MHz[*3]	-	48MHz		4.0	4.3	
		12MHz[*4]	-	12MHz	-	1.4	1.7	
		6 MHz[*5]	-	12MHz	-	0.9	1.2	
		4 MHz[*6]	-	12MHz	-	0.8	1.1	
		2 MHz[*7]	-	12MHz	-	0.7	1.0	
		32.768 KHz	32.768 kHz	-	-	0.5	0.8	
		10KHz	-	10KHz	-	0.5	0.8	

Note:

1. Guaranteed by characterization results, not tested in production.
2. In this case HCLK = system clock, system clock = 64MHz, LDO = 1.26V
3. In this case HCLK = system clock, system clock = 48MHz, LDO = 1.2V
4. In this case HCLK = system clock, system clock = 12MHz, LDO = 1.2V
5. In this case HCLK = system clock/2, system clock = 12MHz, LDO = 1.2V
6. In this case HCLK = system clock/3, system clock = 12MHz, LDO = 1.2V
7. In this case HCLK = system clock/6, system clock = 12MHz, LDO = 1.2V
8. When analog peripheral blocks such as ADC and ACMP are ON, an additional power consumption should be considered.

Table 8.3-2 Current Consumption in DC-DC Normal Run Mode

8.3.1.3 LDO Idle Mode

Symbol	Conditions	f_{HCLK}	HXT/LXT	HIRC/LIRC	PLL	T_A		Unit
						25 °C	105 °C[*1]	
I_{DD}	Idle mode, executed from Flash, V_{DD} = 3.3V, Vsw without Inductance, all peripherals disabled	64 MHz[*2]	12MHz	-	V	2.9	3.7	mA
		48 MHz[*3]	12MHz	-	V	2.4	3.1	
		12MHz[*4]	12MHz	-	-	1.1	1.8	
		6 MHz[*5]	12MHz	-	-	1.0	1.7	
		4 MHz[*6]	12MHz	-	-	1.0	1.7	
		2 MHz[*7]	12MHz	-	-	1.0	1.7	
		64 MHz[*2]		12MHz	V	2.3	3.1	
		48 MHz[*3]	-	12MHz	V	1.8	2.5	
		48 MHz[*3]	-	48MHz		1.4	2.1	
		12MHz[*4]	-	12MHz	-	0.6	1.2	
		6 MHz[*5]	-	12MHz	-	0.5	1.1	
		4 MHz[*6]	-	12MHz	-	0.5	1.1	
		2 MHz[*7]	-	12MHz	-	0.4	1.0	
		32.768 KHz	32.768 kHz	-	-	0.1	0.8	
		10KHz	-	10KHz	-	0.1	0.8	
	Idle mode, executed from Flash, V_{DD} = 3.3V, Vsw without Inductance, all peripherals	64 MHz[*2]	12MHz	-	V	10.9	11.9	
		48 MHz[*3]	12MHz	-	V	8.2	9.0	

	enabled	12MHz[*4]	12MHz	-	-	3.0	3.7	
		6 MHz[*5]	12MHz	-	-	2.3	3.0	
		4 MHz[*6]	12MHz	-	-	2.0	2.8	
		2 MHz[*7]	12MHz	-	-	1.8	2.5	
		64 MHz[*2]		12MHz	V	10.0	10.7	
		48 MHz[*3]	-	12MHz	V	7.4	8.0	
		48 MHz[*3]	-	48MHz		6.9	7.5	
		12MHz[*4]	-	12MHz	-	2.2	2.8	
		6 MHz[*5]	-	12MHz	-	1.5	2.1	
		4 MHz[*6]	-	12MHz	-	1.2	1.9	
		2 MHz[*7]	-	12MHz	-	1.0	1.6	
		32.768 KHz	32.768 kHz	-	-	0.7	1.3	
		10KHz	-	10KHz	-	0.8	1.4	

Note:

1. Guaranteed by characterization results, not tested in production.
2. In this case HCLK = system clock, system clock = 64MHz, LDO = 1.26V
3. In this case HCLK = system clock, system clock = 48MHz, LDO = 1.2V
4. In this case HCLK = system clock, system clock = 12MHz, LDO = 1.2V
5. In this case HCLK = system clock/2, system clock = 12MHz, LDO = 1.2V
6. In this case HCLK = system clock/3, system clock = 12MHz, LDO = 1.2V
7. In this case HCLK = system clock/6, system clock = 12MHz, LDO = 1.2V
8. When analog peripheral blocks such as ADC and ACMP are ON, an additional power consumption should be considered.

Table 8.3-3 Current consumption in LDO Idle mode

8.3.1.4 DC-DC Idle Mode

Symbol	Conditions	f_{HCLK}	HXT/LXT	HIRC/LIRC	PLL	T_A		unit
						25 °C	105 °C[*1]	
I_{DD}	Idle mode, executed from Flash, V_{DD} = 3.3V, V_{sw} with Inductance, all peripherals disabled	64 MHz[*2]	12MHz	-	V	1.6	2.1	mA
		48 MHz[*3]	12MHz	-	V	1.4	1.8	
		12MHz[*4]	12MHz	-	-	0.9	1.2	
		6 MHz[*5]	12MHz	-	-	0.8	1.2	
		4 MHz[*6]	12MHz	-	-	0.8	1.2	
		2 MHz[*7]	12MHz	-	-	0.8	1.1	
		64 MHz[*2]		12MHz	V	1.1	1.5	
		48 MHz[*3]	-	12MHz	V	0.9	1.2	
		48 MHz[*3]	-	48MHz		0.7	1.0	
		12MHz[*4]	-	12MHz	-	0.4	0.7	
		6 MHz[*5]	-	12MHz	-	0.3	0.6	
		4 MHz[*6]	-	12MHz	-	0.3	0.6	
		2 MHz[*7]	-	12MHz	-	0.3	0.6	
		32.768 KHz	32.768 kHz	-	-	0.1	0.6	

		10KHz	-	10KHz	-	0.1	0.4	
	Idle mode, executed from Flash, V_{DD} = 3.3V, V_{sw} with Inductance, all peripherals enabled	64 MHz[*2]	12MHz	-	V	5.3	5.8	
		48 MHz[*3]	12MHz	-	V	4.0	4.4	
		12MHz[*4]	12MHz	-	-	1.7	2.1	
		6 MHz[*5]	12MHz	-	-	1.4	1.8	
		4 MHz[*6]	12MHz	-	-	1.3	1.7	
		2 MHz[*7]	12MHz	-	-	1.2	1.6	
		64 MHz[*2]		12MHz	V	4.6	4.9	
		48 MHz[*3]	-	12MHz	V	3.3	3.5	
		48 MHz[*3]	-	48MHz		3.1	3.4	
		12MHz[*4]	-	12MHz	-	1.0	1.3	
		6 MHz[*5]	-	12MHz	-	0.7	1.0	
		4 MHz[*6]	-	12MHz	-	0.6	0.9	
		2 MHz[*7]	-	12MHz	-	0.5	0.8	
		32.768 KHz	32.768 kHz	-	-	0.4	0.7	
		10KHz	-	10KHz	-	0.4	0.7	

Note:

1. Guaranteed by characterization results, not tested in production.
2. In this case HCLK = system clock, system clock = 64MHz, LDO = 1.26V
3. In this case HCLK = system clock, system clock = 48MHz, LDO = 1.2V
4. In this case HCLK = system clock, system clock = 12MHz, LDO = 1.2V
5. In this case HCLK = system clock/2, system clock = 12MHz, LDO = 1.2V
6. In this case HCLK = system clock/3, system clock = 12MHz, LDO = 1.2V
7. In this case HCLK = system clock/6, system clock = 12MHz, LDO = 1.2V
8. When analog peripheral blocks such as ADC and ACMP are ON, an additional power consumption should be considered.

Table 8.3-4 Current Consumption in DC-DC Idle Mode

8.3.1.5 LDO Power-down Mode

Symbol	Conditions	LXT	LIRC	PLL	T_A	LDO	Unit
I_{DD_FWPD}	Power-down mode, VDD = 3.3V, all peripherals disabled, SRAM retention	-	-	-	-40 °C	96.5	uA
					25 °C	128.3	
					55 °C	225.0	
					85 °C	462.1	
					105 °C	698.0	
	Power-down mode, VDD = 3.3V, all peripherals disabled, no SRAM retention				-40 °C	91.0	
					25 °C	107.7	
					55 °C	131.6	

					85 °C	189.2
					105 °C	271.8
	Power-down mode, VDD = 3.3V, RTC/WDT/Timer/UART enabled, SRAM retention	V	-	-	-40 °C	96.9
					25 °C	129.0
					55 °C	225.9
					85 °C	468.8
					105 °C	715.0
	Power-down mode, VDD = 3.3V, RTC/WDT/Timer/UART enabled, no SRAM retention				-40 °C	91.8
					25 °C	109.1
					55 °C	132.8
					85 °C	190.5
					105 °C	273.4
	Power-down mode, VDD = 3.3V, RTC/WDT/Timer use LIRC, SRAM retention	-	V	-	-40 °C	95.9
					25 °C	128.1
					55 °C	224.6
					85 °C	455.8
					105 °C	737.5
	Power-down mode, VDD = 3.3V, RTC/WDT/Timer use LIRC, no SRAM retention				-40 °C	91.4
					25 °C	107.9
					55 °C	131.7
					85 °C	189.6
					105 °C	272.0
	Power-down mode, VDD = 3.3V, WDT/Timer use LIRC, RTC/UART use LXT, SRAM retention	V	V	-	-40 °C	96.6
					25 °C	129.2
					55 °C	225.7
					85 °C	446.8
					105 °C	737.5
	Power-down mode, VDD = 3.3V, WDT/Timer use LIRC, RTC/UART use LXT, no SRAM retention				-40 °C	92.4
					25 °C	109.2
					55 °C	133.0
					85 °C	191.3
					105 °C	273.5
I_{DD_PD}	Power-down mode, VDD = 3.3V, all peripherals disabled, SRAM retention	-	-	-	-40 °C	18.2
					25 °C	40.3
					55 °C	115.9
					85 °C	282.9

					105 °C	737.5	
	Power-down mode, VDD = 3.3V, all peripherals disabled, no SRAM retention				-40 °C	12.5	
					25 °C	20.2	
					55 °C	35.7	
					85 °C	79.0	
					105 °C	140.1	
	Power-down mode, VDD = 3.3V, RTC/WDT/Timer/UART enabled, SRAM retention	V	-	-	-40 °C	19.2	
					25 °C	41.5	
					55 °C	117.1	
					85 °C	289.9	
					105 °C	498.8	
	Power-down mode, VDD = 3.3V, RTC/WDT/Timer/UART enabled, no SRAM retention				-40 °C	13.5	
					25 °C	21.6	
					55 °C	37.1	
					85 °C	80.3	
					105 °C	141.8	
	Power-down mode, VDD = 3.3V, RTC/WDT/Timer use LIRC, SRAM retention	-	V	-	-40 °C	18.6	
					25 °C	40.7	
					55 °C	116.3	
					85 °C	292.9	
					105 °C	500.0	
	Power-down mode, VDD = 3.3V, RTC/WDT/Timer use LIRC, no SRAM retention				-40 °C	12.9	
					25 °C	20.4	
					55 °C	36.0	
					85 °C	78.7	
					105 °C	140.5	
	Power-down mode, VDD = 3.3V, WDT/Timer use LIRC, RTC/UART use LXT, SRAM retention	V	V	-	-40 °C	19.3	
					25 °C	41.7	
					55 °C	117.6	
					85 °C	288.6	
					105 °C	503.2	
	Power-down mode, VDD = 3.3V, WDT/Timer use LIRC, RTC/UART use LXT, no SRAM retention				-40 °C	13.9	
					25 °C	21.7	
					55 °C	37.4	
					85 °C	80.0	
					105 °C	142.2	

I_{DD_LLPD}	Power-down mode, VDD = 3.3V, all peripherals disabled, SRAM retention	-	-	-	-40 °C	6.2	uA
					25 °C	15.8	
					55 °C	55.5	
					85 °C	154.5	
					105 °C	299.3	
	Power-down mode, VDD = 3.3V, all peripherals disabled, no SRAM retention				-40 °C	4.6	
					25 °C	8.2	
					55 °C	17.0	
					85 °C	44.4	
					105 °C	88.0	
	Power-down mode, VDD = 3.3V, RTC/WDT/Timer/UART enabled, SRAM retention	V	-	-	-40 °C	7.0	
					25 °C	16.9	
					55 °C	56.8	
					85 °C	156.2	
					105 °C	301.1	
	Power-down mode, VDD = 3.3V, RTC/WDT/Timer/UART enabled, no SRAM retention				-40 °C	5.4	
					25 °C	9.6	
					55 °C	18.3	
					85 °C	45.8	
					105 °C	89.7	
	Power-down mode, VDD = 3.3V, RTC/WDT/Timer use LIRC, SRAM retention	-	V	-	-40 °C	6.3	
					25 °C	16.1	
					55 °C	55.8	
					85 °C	157.3	
					105 °C	299.6	
	Power-down mode, VDD = 3.3V, RTC/WDT/Timer use LIRC, no SRAM retention				-40 °C	4.7	
					25 °C	8.4	
					55 °C	17.2	
					85 °C	44.4	
					105 °C	88.5	
	Power-down mode, VDD = 3.3V, WDT/Timer use LIRC, RTC/UART use LXT, SRAM retention	V	V	-	-40 °C	7.2	
					25 °C	17.2	
					55 °C	57.0	
					85 °C	161.2	
					105 °C	301.0	
	Power-down mode, VDD = 3.3V, WDT/Timer use				-40 °C	5.7	

	LIRC, RTC/UART use LXT, no SRAM retention				25 °C	9.6	
					55 °C	18.6	
					85 °C	45.8	
					105 °C	90.1	
I_{DD_ULLPD}	Power-down mode, VDD = 3.3V, all peripherals disabled, SRAM retention	-	-	-	-40 °C	4.4	uA
					25 °C	11.7	
					55 °C	43.6	
					85 °C	132.6	
					105 °C	251.4	
	Power-down mode, VDD = 3.3V, all peripherals disabled, no SRAM retention				-40 °C	3.3	
					25 °C	6.2	
					55 °C	13.6	
					85 °C	37.1	
					105 °C	76.4	
	Power-down mode, VDD = 3.3V, RTC/WDT/Timer/UART enabled, SRAM retention	V	-	-	-40 °C	5.4	
					25 °C	12.8	
					55 °C	44.9	
					85 °C	134.6	
					105 °C	252.7	
	Power-down mode, VDD = 3.3V, RTC/WDT/Timer/UART enabled, no SRAM retention				-40 °C	4.3	
					25 °C	7.6	
					55 °C	14.8	
					85 °C	38.4	
					105 °C	78.0	
	Power-down mode, VDD = 3.3V, RTC/WDT/Timer use LIRC, SRAM retention	-	V	-	-40 °C	4.6	
					25 °C	11.9	
					55 °C	43.9	
					85 °C	133.3	
					105 °C	251.2	
	Power-down mode, VDD = 3.3V, RTC/WDT/Timer use LIRC, no SRAM retention				-40 °C	3.5	
					25 °C	6.5	
					55 °C	13.9	
					85 °C	37.4	
					105 °C	76.7	
	Power-down mode, VDD = 3.3V, WDT/Timer use LIRC, RTC/UART use LXT, SRAM retention	V	V	-	-40 °C	5.5	
					25 °C	13.0	

					55 °C	45.2
					85 °C	134.0
					105 °C	252.6
	Power-down mode, VDD = 3.3V, WDT/Timer use LIRC, RTC/UART use LXT, no SRAM retention				-40 °C	4.4
					25 °C	7.7
					55 °C	15.3
					85 °C	38.8
					105 °C	78.3
I_{DD_SPD}	Standby Power-down mode(SPD), VDD = 3.3V, all peripherals disabled	-	-	-	-40 °C	2.1
					25 °C	2.8
					55 °C	3.9
					85 °C	8.1
					105 °C	15.5
	Standby Power-down mode (SPD), VDD = 3.3V, RTC enabled	V	-	-	-40 °C	3.0
					25 °C	3.9
					55 °C	5.0
					85 °C	9.5
					105 °C	17.2
	Standby Power-down mode (SPD), VDD = 3.3V, RTC enabled	-	V	-	-40 °C	2.1
					25 °C	2.8
					55 °C	3.9
					85 °C	8.3
					105 °C	15.6
I_{DD_DPD}	Deep Power-down mode (DPD), VDD = 3.3V, all peripherals disabled	-	-	-	-40 °C	1.0
					25 °C	1.5
					55 °C	1.9
					85 °C	4.2
					105 °C	8.2
	Deep Power-down mode(DPD), RTC enable[*1]	V	-	-	-40 °C	1.9
					25 °C	2.4
					55 °C	3.3
					85 °C	5.6
					105 °C	9.8
	Deep Power-down mode(DPD), RTC enable[*1]	-	V	-	-40 °C	0.9
					25 °C	1.6
					55 °C	2.0

					85 °C	4.2	
					105 °C	8.3	

Note:

1. VDD = AVDD = VBAT = VDDIO = 3.3V
2. Guaranteed by characterization results, not tested in production.
3. When analog peripheral blocks such as ADC and ACMP are ON, an additional power consumption should be considered.

Table 8.3-5 Chip Current Consumption in Power-down Mode

8.3.1.6 Current Consumption for RTC Domain

Symbol	Conditions	LXT	T_A	LDO	DCDC	Unit
I_{BAT}	RTC enabled, operating current, V_{BAT} = 3.6V	V	-40 °C	2.3	2.0	uA
			25 °C	2.5	2.4	
			55 °C	3.1	3.0	
			85 °C	4.9	4.7	
			105 °C	7.8	7.1	
	RTC enabled, operating current, V_{BAT} = 3.3V	V	-40 °C	2.0	1.9	
			25 °C	2.3	2.5	
			55 °C	2.8	2.9	
			85 °C	4.7	4.8	
			105 °C	7.5	7.5	
	RTC enabled, operating current, V_{BAT} = 1.7V	V	-40 °C	1.9	1.9	
			25 °C	2.3	2.2	
			55 °C	2.8	2.8	
			85 °C	4.5	4.1	
			105 °C	7.3	7.3	
	RTC disabled, operating current, V_{BAT} = 3.6V	V	-40 °C	1.0	1.2	
			25 °C	1.4	1.3	
			55 °C	1.8	1.6	
			85 °C	3.6	3.5	
			105 °C	6.2	5.7	
	RTC disabled, operating current, V_{BAT} = 3.3V	V	-40 °C	0.9	1.1	
			25 °C	1.3	1.2	
			55 °C	1.7	1.6	
			85 °C	3.4	3.2	
			105 °C	6.0	5.9	

	RTC disabled, operating current, V_{BAT} = 1.7V	V	-40 °C	0.9	0.9	
			25 °C	1.1	1.2	
			55 °C	1.5	1.6	
			85 °C	3.0	2.9	
			105 °C	5.7	5.7	
Note: Guaranteed by characterization results, not tested in production.						

Table 8.3-6 Current Consumption for V_{BAT}

8.3.2 On-chip Peripheral Current Consumption

- All GPIO pins are in push pull mode, output high.
- LDO = 1.26V
- The typical values for T_A= 25 ˚C and V_{DD} = 3.3 V unless otherwise specified.
- When the peripherals are enabled HCLK is the system clock, f_{HCLK} = 64 MHz, $f_{PCLK0, 1}$ = f_{HCLK}/2.

Peripheral	I_{DD}	Unit
PDMA0	24.8	uA
PDMA1	24	
ISP	0.1	
EBI	6.1	
SDH0	36.5	
CRC	2.5	
CRPT	6	
FMC	30	
USBH	50	
SRAM0IDLE	6.2	
SRAM1IDLE	4.8	
WDT	1.3	
RTC	3.8	
TMR0	5.1	
TMR1	4.9	
TMR2	4.6	
TMR3	4.9	
CLKO	0.2	
ACMP01	4	
I2C0	1.1	
I2C1	1	

I2C2	0.8	
QSPI0	10.5	
SPI0	13.9	
SPI1	11.5	
SPI2	16.5	
UART0	6	
UART1	8.4	
UART2	4.9	
UART3	7.3	
UART4	4.9	
UART5	7.7	
CAN0	8.2	
OTG	15.2	
USBDC	38.7	
EADC	12.7	
I2S0	2.9	
SC0	2.8	
SC1	5.3	
SC2	2.6	
SPI3	12.8	
USCI0	5.9	
USCI1	7.2	
DAC	1.4	
EPWM0	8.3	
EPWM1	10.4	
BPWM0	3.1	
BPWM1	5.2	
QEI0	2.1	
QEI1	3.4	
TRNG	28.8	
ECAP0	1.8	
ECAP1	3.4	

Note: Guaranteed by characterization results, not tested in production.

8.3.3 Wakeup Time

- The wakeup times given in Table 8.3-7 is measured on a wakeup phase with a 12 MHz HIRC oscillator. The clock source used to wake up the device depends from the current operating mode:
  - Fast-wakeup, power down, low leakage Power-down mode: the clock source is the RC oscillator
  - Standby and Deep Power-down mode: the clock source is the clock that was set before entering Sleep mode.
- The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.
- The clock source is the RC oscillator from HIRC.

Symbol	Parameter	Typ[*1]	Unit
t_{WU_IDLE}	Wakeup from IDLE mode	1.63[*2]	µs
t_{WU_FWPD}	Wakeup from Fast-wakeup Power-down mode	9.0[*2]	
t_{WU_NPD}	Wakeup from normal Power-down mode	11.5[*2]	
t_{WU_LLPD}	Wakeup from low leakage Power-down mode	60[*2]	
t_{WU_ULLPD}	Wakeup from ultra low leakage power down	61[*2]	
t_{WU_SPD}	Wakeup from Standby Power-down mode (SPD)	525[*2]	
t_{WU_DPD}	Deep Power-down mode (DPD)	183[*3]	

Note:

1. Guaranteed by characterization results, not tested in production.
2. The wake up source is GPIO(PA.0) wake up.
3. The wake up source is GPIO(PC.0) wake up.
4. Based on test during characterization, not tested in production.
5. The wakeup times are measured from the wakeup event to the point in which the application code reads the first

Table 8.3-7 Low-power Mode Wakeup Timings

8.3.4 I/O DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL1}	Input Low Voltage (TTL input)	0.8	-	-	V	$V_{DD} = V_{DDIO} = 3.6$ V
		0.56	-	-	V	$V_{DD} = V_{DDIO} = 1.7$ V
V_{IH1}	Input High Voltage (TTL input)	-	-	2	V	$V_{DD} = V_{DDIO} = 3.6$V
		-	-	1.04	V	$V_{DD} = V_{DDIO} = 1.7$V
V_{IL2}	Input Low Voltage (Schmitt input)	$0.3*V_{DD}$	-	-	V	$V_{DD} = V_{DDIO} = 3.6$V
		$0.3*V_{DD}$	-	-		$V_{DD} = V_{DDIO} = 1.7$V
V_{IH2}	Input High Voltage (Schmitt input)	-	-	$0.7*V_{DD}$	V	$V_{DD} = V_{DDIO} = 3.6$V
				$0.7*V_{DD}$		$V_{DD} = V_{DDIO} = 1.7$V
V_{HY}	Hysteresis voltage of (Schmitt input)	-	$0.2V_{DD}$	-	V	
I_{LK}	Input Leakage Current	-1	-	1	μA	$V_{DD} = V_{DDIO} = 3.6$V, $0 < V_{IN} < V_{DD}$, Open-drain or input only mode
I_{IL}	Logic 0 Input Current (Quasi-bidirectional mode)	-	67.9	-	uA	$V_{DD} = V_{DDIO} = 3.6$V, $V_{IN} = 0$V
R_{PU}	Input Pull Up Resistor	-	53	-	KΩ	$V_{DD} = V_{DDIO} = 3.3$V
		-	53	-	KΩ	$V_{DD} = V_{DDIO} = 1.8$V
R_{PD}	Input Pull down Resistor	-	53	-	KΩ	$V_{DD} = V_{DDIO} = 3.3$V
		-	53	-	KΩ	$V_{DD} = V_{DDIO} = 1.8$V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.
3. To sustain a voltage higher than VDD +0.3 V, the internal pull-up resistors must be disabled. Leakage could be higher than the maximum value, if positive current is injected on adjacent pins

Table 8.3-8 PIN input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR1}	Source Current (Quasi-bidirectional Mode, Set GPIO to output HIGH, Apply GPIO pin $V_{IN}=(V_{DD}-0.4)$V for V_{DD} and measure the source current)	-7.939	-	-6.934	uA	$V_{DD} = V_{DDIO} = 3.3$V
I_{SR2}		-7.939	-	-6.934	uA	$V_{DD} = V_{DDIO} = 1.8$V
I_{SR3}	Source Current (Push-pull Mode, Set GPIO to output HIGH, Apply GPIO pin $VIN=(V_{DD}-0.4)$V for V_{DD} and measure the source current)	-20.629	-	-3.43	mA	$V_{DD} = V_{DDIO} = 3.3$V
I_{SR4}		-14.326	-	-4.392	mA	$V_{DD} = V_{DDIO} = 1.8$V
I_{SK1}	Sink Current	3.576	-	19.98	mA	$V_{DD} = V_{DDIO} = 3.3$V

I_{SK2}	(Quasi-bidirectional, Push-pull Mode, Set GPIO to output LOW, Apply GPIO pin VIN=(V_{SS}+0.4)V for V_{SS} and measure the source current)	4.102	-	12.351	mA	V_{DD} = V_{DDIO} = 1.8V
I_{TL}	Logic 1 to 0 Transition Current (Quasi-bidirectional Mode)	-	-70	-	uA	V_{DD} = V_{DDIO} = 3.3V V_{IN}=2.0V
C_{IO}	I/O pin capacitance	-	4.2	-	pF	

Notes:

1. Guaranteed by characterization result, not tested in production.
2. The ISR and ISK must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣIDD and ΣISS.

Table 8.3-9 PIN Output Characteristics

Symbol	Parameter	Min	Typ	Max	unit	Test Conditions
V_{ILR}	Negative going threshold (Schmitt input), nRESET	-	-	0.3*V_{DD}	V	V_{DD} = 3.3V
V_{IHR}	Positive going threshold (Schmitt Input), nRESET	0.7*V_{DD}	-	-	V	V_{DD} = 3.3V
R_{RST}	Internal nRESET pin pull up resistor	50	-	56.8	KΩ	
t_{FR1}	nRESET input filtered time	-	32	-	uS	
t_{FR2}	nRESET input filtered time under SPD and DPD mode	-	300	-	nS	V_{DD} = 3.3V,

Notes:

1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 8.3-10 nRESET Pin Characteristics

8.3.5 Winbond Secure Flash W77F32W Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Standby Current	Icc1	/CS = VCC, VIN = GND or VCC		25	100(1)	µA
Power-down Current	Icc2	/CS = VCC, VIN = GND or VCC		0.5	35	µA
Data Read Current Quad mode 10MHz	Icc3			12	16	mA
Data Read Current Quad mode 50MHz	Icc3			22	28	mA
Current Byte Program	Icc5	/CS = VCC		18	35	mA
Current Sector Erase	Icc6	/CS = VCC		20	32	mA

1.Internal Operation may continue for some time after /CS de-assertion

Table 8.3-11 M2351SF Internal Secure Flash Electical Characteristics

8.4 AC Electrical Characteristics

8.4.1 External 4~24 MHz High Speed Crystal (HXT) Characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

- T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{DD}	Operating Voltage	1.7	3.0	3.6	V	
R_f	Feedback resister	-	1000	-	kΩ	
f_{HXT}	Oscillator frequency	4	-	24	MHz	V_{DD} = 1.8 ~ 3.3V
T_{HXT}	Temperature Range	-40	-	105	°C	
I_{HXT_INV}	Current Consumption (INV-type Crystal)	-	620	-	mA	4MHz
		-	1088	-		12MHz
		-	1943	-		16MHz
		-	2085	-		24MHz
I_{HXT_GM}	Current Consumption (GM-type Crystal)	-	230	-	µA	4MHz
		-	364	-		12MHz
		-	400	-		16MHz
		-	620	-		24MHz
T_{S_GM}	Stable time (GM-type)	-	2026	-	µs	4MHz
		-	602	-		12MHz
		-	440	-		16MHz
		-	401	-		24MHz
T_{S_INV}	Stable time (INV-type)	-	2322	-	µs	4MHz
		-	619	-		12MHz
		-	443	-		16MHz
		-	419	-		24MHz
	Clock Duty	45	50	55	%	

Notes:
1. Guaranteed by characterization, not tested in production.

Table 8.4-1 External 4~24 MHz High Speed Crystal (HXT) Oscillator

8.4.1.1 *Typical Crystal Application Circuits*

Crystal	C1	C2
4~24 MHz	5~20pF	5~20pF

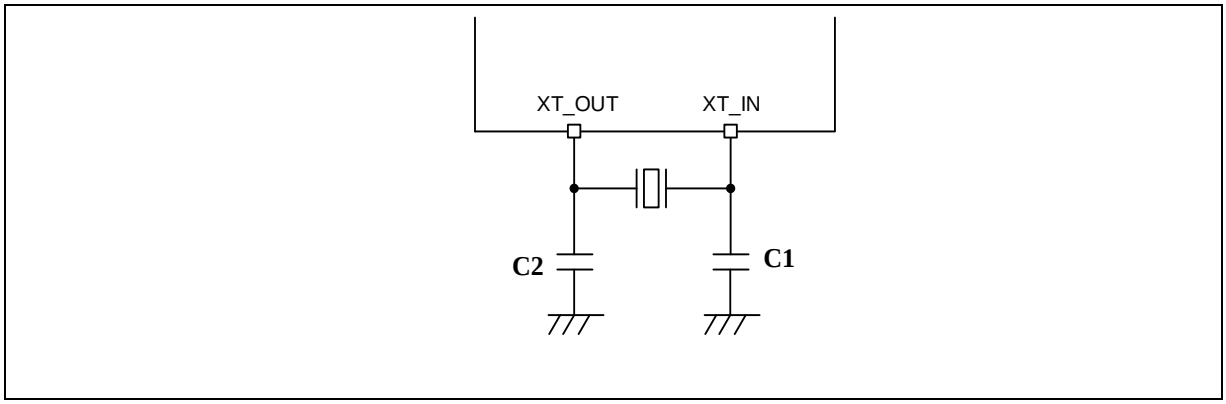
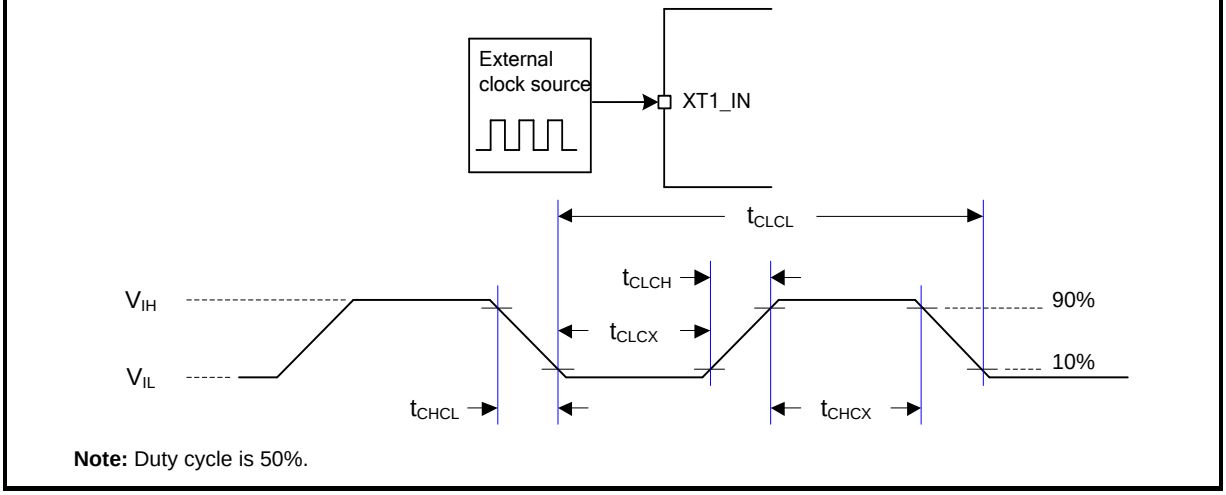


Figure 8.4-1 Typical Crystal Application Circuit

8.4.2 External 4~24 MHz High Speed Crystal (OSC) Input Clock

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
t_{CHCX}	Clock High Time	18	-	-	nS	
t_{CLCX}	Clock Low Time	18	-	-	nS	
t_{CLCH}	Clock Rise Time	-	-	10	nS	
t_{CHCL}	Clock Fall Time	-	-	10	nS	
V_{IH}	Input High Voltage	0.7*V_{DD}	-	-	V	
V_{IL}	Input Low Voltage	-	-	0.3*V_{DD}	V	



Note: Duty cycle is 50%.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
Note: Guaranteed by design, not tested in production.						

8.4.3 External 32.768 kHz Low Speed Crystal (LXT) Characteristics

The low-speed external (LXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the X32_OUT and X32_IN pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{BAT}	Operation Voltage	1.7	-	3.6	V	
f_{LXT}	Oscillator frequency	-	32.768	-	kHz	V_{BAT} = 1.7 ~ 3.6 V
T_{LXT}	Temperature	-40	-	105	°C	
I_{LXT}	Operating current	-	0.45	-	µA	V_{BAT} = 3.3V
	Duty cycle	45	-	55	%	
T_S	Stable Time	-	372	-	ms	
Notes: 1. Guaranteed by characterization, not tested in production.						

Table 8.4-2 External 32.768 kHz Crystal

8.4.3.1 Typical Crystal Application Circuits

Crystal	C1	C2
32.768 kHz	5~20pF	5~20pF

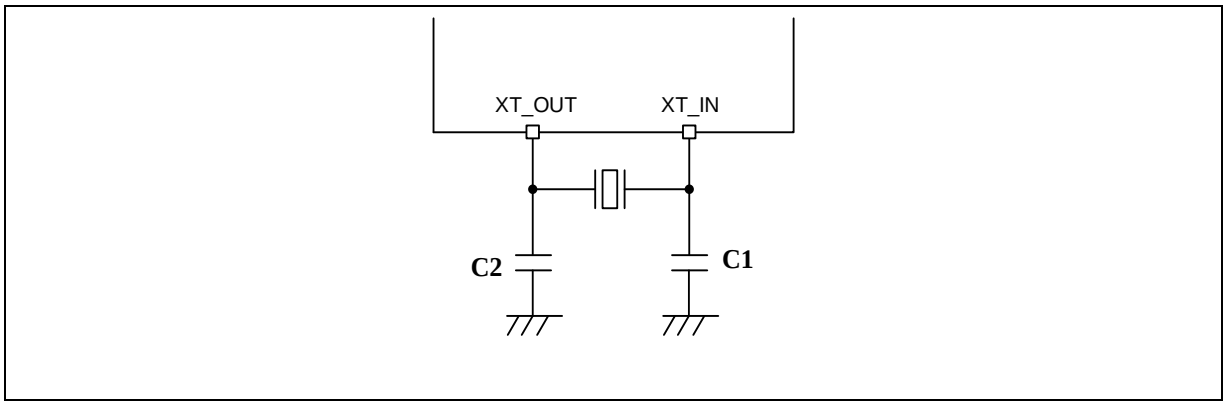
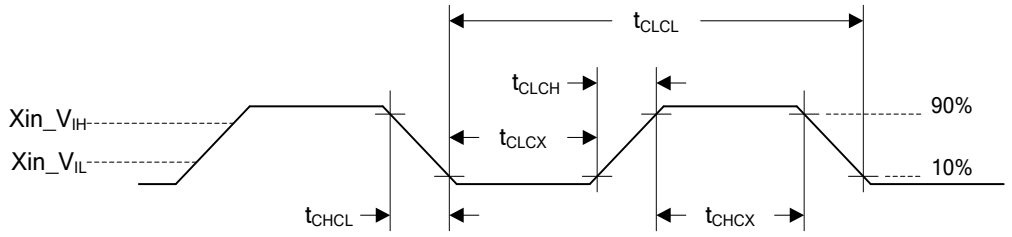


Figure 8.4-2 Typical Crystal Application Circuit

8.4.4 External 32.768 kHz Low Speed Crystal (OSC) Input Clock

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Clock High Time	t_{CHCX}	450	-	-	ns	
Clock Low Time	t_{CLCX}	450	-	-	ns	

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Clock Rise Time	t_{CLCH}	-	-	50	ns	
Clock Fall Time	t_{CHCL}	-	-	50	ns	
LXT Input Pin Input High Voltage	Xin_VIH	0.7*VDD	-	-	V	
LXT Input Pin Input Low Voltage	Xin_VIL	-	-	0.3*VDD	V	



Note: *Duty cycle is 50%.*

8.4.5 12 MHz Internal High Speed RC Oscillator (HIRC)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{HRC}	Supply voltage	1.7	-	3.6	V	
f_{HRC}	Center Frequency	-	12	-	MHz	
	Internal Oscillator Frequency[*1]	-0.6	-	0.6	%	T_A = 25 °C, V_{DD} = 3.3V
		-3.6	-	2.7	%	T_A = -40°C ~ +105 °C, V_{DD} = 1.7 ~ 3.6V
I_{HRC}	Operating current	-	70	-	μA	
T_S	Stable time	-	3	-	us	

Note: Guaranteed by characterization, not tested in production.

8.4.6 48 MHz Internal High Speed RC Oscillator (HIRC48)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{HRC}	Supply voltage	1.7	-	3.6	V	
f_{HRC}	Center Frequency	-	48	-	MHz	
	Frequency drift over temperarure and volatge [*1]	-0.285	-	0.8715	%	T_A = 25 °C, V_{DD} = 3.3V
		-3.555	-	2.41	%	T_A = -40°C ~ +105 °C, V_{DD} = 1.7 ~ 3.6V
I_{HRC}	Operating current	-	100	-	μA	

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
T_S	Stable time	-	5	-	us	
Note: Guaranteed by characterization, not tested in production.						

8.4.7 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{LRC}	Supply voltage	1.7	-	3.6	V	
F_{LRC}	Center Frequency		10		kHz	
	Frequency drift over temperarure and volatge [*1]	-40.476	-	49.772	%	V_{DD}=1.7V~3.6V, T_A=-40~105°C
I_{LRC}	Operating current	-	0.29	-	μA	V_{DD} = 3.3V
T_S	Stable time	-	200	-	μs	
Note: Guaranteed by characterization, not tested in production.						

8.4.8 PLL Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock		4	-	24	MHz
f_{PLL_OUT}	PLL multiplier output clock		50	-	200	MHz
Jitter	Cycle-to-cycle Jitter[*2]	Peak to peak at 144M	-	250	-	ps
I_{DD}	Power consumption	V_{DD}=3.3Vat 200MHz	-	1	-	mA

Note:

1. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production.

8.4.9 I/O AC Characteristics

Px_SLEWCTL	Symbol	Parameter	Conditions		Typ	Unit
00	$t_{f(IO)out}$	Output high to low level fall time (90~10%)	V_{DD} = 3.6 V	C_L = 51 pF	4.1	ns
				C_L = 30 pF	2.9	
			V_{DD} = 1.7 V	C_L = 51 pF	9.7	
				C_L = 30 pF	7.3	
	$t_{r(IO)out}$	Output low to high level rise time (10~90%)	V_{DD} = 3.6 V	C_L = 51 pF	4.4	
				C_L = 30 pF	3.3	
			V_{DD} = 1.7 V	C_L = 51 pF	10.0	
				C_L = 30 pF	7.3	
01	$t_{f(IO)out}$	Output high to low level fall time (90~10%)	V_{DD} = 3.6 V	C_L = 51 pF	3.4	
				C_L = 30 pF	2.2	
			V_{DD} = 1.7 V	C_L = 51 pF	7.4	
				C_L = 30 pF	4.9	
	$t_{r(IO)out}$	Output low to high level rise time (10~90%)	V_{DD} = 3.6 V	C_L = 51 pF	3.1	
				C_L = 30 pF	2.0	
			V_{DD} = 1.7 V	C_L = 51 pF	7.2	
				C_L = 30 pF	4.7	
10	$t_{f(IO)out}$	Output high to low level fall time (90~10%)	V_{DD} = 3.6 V	C_L = 51 pF	3.4	
				C_L = 30 pF	2.2	
			V_{DD} = 1.7 V	C_L = 51 pF	7.4	
				C_L = 30 pF	4.9	
	$t_{r(IO)out}$	Output low to high level rise time (10~90%)	V_{DD} = 3.6 V	C_L = 51 pF	3.1	
				C_L = 30 pF	2.0	
			V_{DD} = 1.7 V	C_L = 51 pF	7.2	
				C_L = 30 pF	4.7	

Notes:

1. Guaranteed by characterization result, not tested in production.
2. CL is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.
4. The I/O dynamic current consumption is defined by $I_{DIO} = V_{DD} \times f_{IO} \times (C_{IO} + C_L)$

Table 8.4-3 I/O AC Characteristics

8.5 Analog Electrical Characteristics

8.5.1 LDO

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	DC Power Supply	1.7	-	3.6	V	
V_{LDO}	Output Voltage	1.134	1.26	1.386	V	Turbo mode
		1.08	1.20	1.32	V	Normal run mode
		0.864	0.96	1.056	V	Low leakage power-down mode
		0.774	0.86	0.946	V	Ultra low leakage Power-down mode
T_A	Temperature	-40	-	105	℃	

Note:

1. It is recommended a 0.1μF bypass capacitor is connected between VDD and the closest VSS pin of the device.
2. For ensuring power stability, a 2.2μF Capacitor must be connected between LDO_CAP pin and the closest VSS pin of the device.
3. For ensuring power stability, a 2.2μF Capacitor must be connected between LDO_CAP pin and the closest VSS pin of the device.

8.5.2 DC-DC

Typical values are at V_{DD} = 3.3V, TA = 25°C, Vsw is connected to 4.7uH inductance and LDO_CAP is connected to 2.2uF capacitance unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{IN}	Input Voltage Range	1.7	-	3.6	V	
V_{OUT}	Output Voltage Range	1.2	1.26	1.4	V	
		1.15	1.20	1.33	V	
I_{OUT_MAX}	Maximum DC Output Current	-	-	30	mA	V_{IN}>1.7V
I_{Q_DCDC}	Quiescent Current	-	-	15	uA	No load, normal mode, only buck regulator
V_{LINE}	Line Regulation	-5	-	5	%	I_{OUT}=30mA, V_{IN}=1.7V to 3.6V
V_{LOAD}	Load Regulation	-5	-	5	%	I_{OUT}=0.2mA to 30mA
P_{EFF}	Power Efficiency	-	80	-	%	I_{OUT}= 2~30mA L_{OUT} = 4.7uH, DCR ≤ 180mΩ

Note:

1. It is recommended a 2.2μF and 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a 2.2μF Capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.

8.5.3 Low-Voltage Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Supply Voltage	0	-	3.6	V	
T_A	Temperature	-40	-	105	℃	-
I_{LVR}	Operating Current	-	0.5	-	uA	AV_{DD} = 3.6V
V_{LVR} *	Threshold Voltage	-	1.5	-	V	
I_{BOD}	Operating Current	-	65	-	μA	AV_{DD} = 3.6V
V_{BOD_F}	Brown-out Voltage (Falling edge)	-	3	-	V	BODVL (SYS_BODCTL[18:16]) = 111
		-	2.8	-	V	BODVL (SYS_BODCTL[18:16]) = 110
		-	2.6	-	V	BODVL (SYS_BODCTL[18:16]) = 101
		-	2.4	-	V	BODVL (SYS_BODCTL[18:16]) = 100
		-	2.2	-	V	BODVL (SYS_BODCTL[18:16]) = 011
		-	2.0	-	V	BODVL (SYS_BODCTL[18:16]) = 010
		-	1.8	-	V	BODVL (SYS_BODCTL[18:16]) = 001
		-	1.6	-	V	BODVL (SYS_BODCTL[18:16]) = 000
V_{BOD_R}	Brown-out Voltage (Rising edge)	-	3	-	V	BODVL (SYS_BODCTL[18:16]) = 111
		-	2.8	-	V	BODVL (SYS_BODCTL[18:16]) = 110
		-	2.6	-	V	BODVL (SYS_BODCTL[18:16]) = 101
		-	2.4	-	V	BODVL (SYS_BODCTL[18:16]) = 100
		-	2.2	-	V	BODVL (SYS_BODCTL[18:16]) = 011
		-	2.0	-	V	BODVL (SYS_BODCTL[18:16]) = 010
		-	1.8	-	V	BODVL (SYS_BODCTL[18:16]) = 001
		-	1.6	-	V	BODVL (SYS_BODCTL[18:16]) = 000
T_{BOD_RE}	Respond Time	-	1	-	ms	
V_{POR}	Reset Voltage	-	1.45	-	V	
RRV_{DD}	V_{DD} Raising Rate to Ensure Power-on Reset	10	-	-	us/V	

FRV_{DD}	V_{DD} Falling Rate to Ensure Power-on Reset	500	-	-	us/V	
t_{POR}	Minimum Time for V_{DD} Stays at VPOR to Ensure Power-on Reset	500	-	-	us	

Note :

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

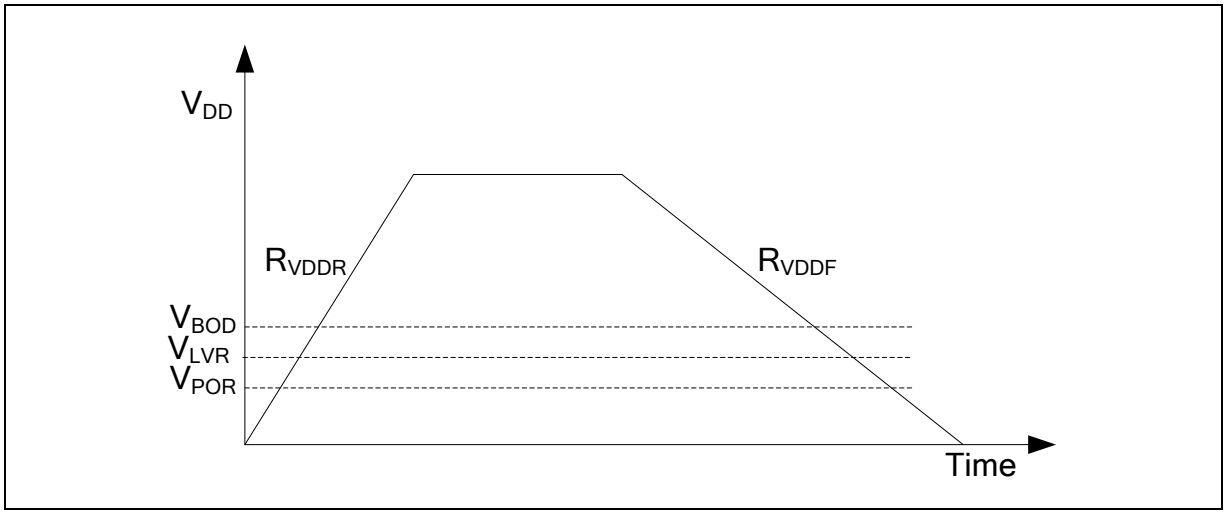


Figure 8.5-1 Power-up Ramp Condition

8.5.4 Internal Voltage Reference

- The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 ˚C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{REF_INT}	Internal reference voltage	-	1.6	-	V	AV_{DD} > 2.0v
		-	2.0	-		AV_{DD} > 2.2v
		-	2.5	-		AV_{DD} > 2.7v
		-	3.0	-		AV_{DD} > 3.2v
T_s	stable time	-	-	2	ms	C_L =4.7 uF, V_{REF} initial=0
		-	-	48	us	C_L =0.1 uF, V_{REF} initial=0
Note: Guaranteed by characterization, not tested in production.						

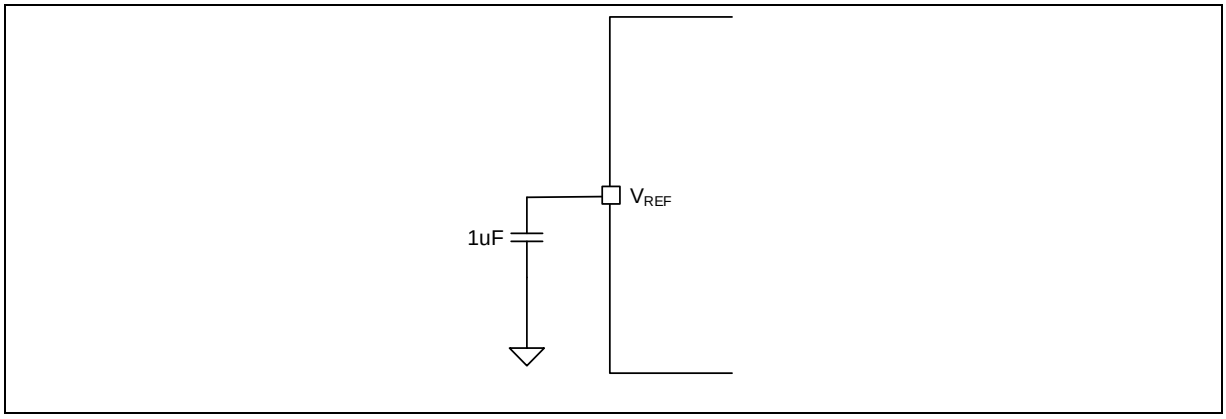


Figure 8.5-2 Typical Connection with Internal Voltage Reference

8.5.5 12-bit ADC

8.5.5.1 Fast Speed Channel

Symbol	Parameter	Min.[*1]	Typ.	Max.[*1]	Unit	Test Conditions
AV_{DD}	Operating voltage	3.3	-	3.6	V	$AV_{DD} = V_{DD}$
V_{REF}	Reference voltage	-	AV_{DD}	-	V	
T_A	Temperature	-40	-	105	℃	
I_{ADC}	Operating current (AV_{DD} current) (Enable ADC and disable all other analog modules)	470	-	520	uA	$AV_{DD} = V_{DD} = V_{REF}$ = 3.3V ADC Clock Rate = 64 MHz High speed channel
	Resolution	-	-	12	Bit	
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
F_{ADC}	ADC Clock frequency	0.14	-	64	MHz	High speed channel
T_{SMP}	Sampling Time	3	-	258	$1/F_{ADC}$	
T_{CONV}	Conversion time	17	-	272	$1/F_{ADC}$	$T_{CONV} = T_{SMP} + 14$
F_{SPS}	Sampling Rate (F_{ADC}/T_{CONV})	-	-	3.76	MSPS	High speed channel
T_{PU}	Power-up time	20	-	-	μs	
INL	Integral Non-Linearity Error	-6.6	-	2.7	LSB	$V_{REF} = AV_{DD}$
DNL	Differential Non-Linearity Error	-1	-	6.6	LSB	$V_{REF} = AV_{DD}$
E_G	Gain error	-0.6	-	2.0	LSB	$V_{REF} = AV_{DD}$
E_{OFFSET}	Offset error	-0.37	-	3.0	LSB	$V_{REF} = AV_{DD}$
E_A	Absolute Error	-5.94	-	6.5	LSB	$V_{REF} = AV_{DD}$
C_{IN}	Internal Capacitance[*1]	-	5	-	pF	
-	Monotonic	Guaranteed			-	

Note:

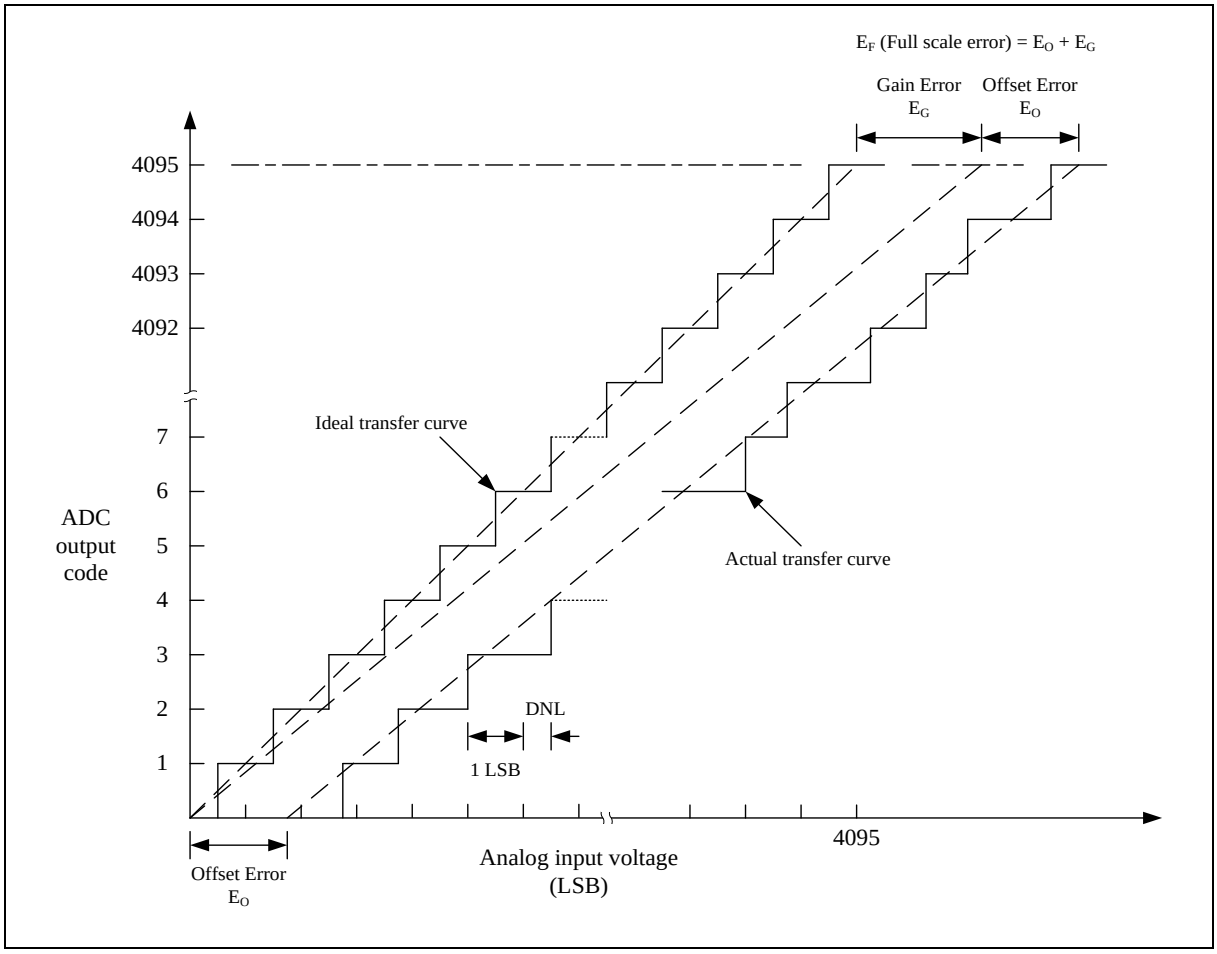
1. Guaranteed by characterization, not tested in production.
2. R_{EX} max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resoluton) and k is the number of sampling clocks (T_{SMP}). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy. $R_{EX} = \frac{k}{f_{ADC} \times C_{IN} \times \ln(2^{N+2})} - R_{IN}$

8.5.5.2 Low Speed Channel

Symbol	Parameter	Min. [*1]	Typ.	Max. [*1]	Unit	Test Conditions
AV_{DD}	Operating voltage	1.7	-	3.6	V	$AV_{DD} = V_{DD}$
V_{REF}	Reference voltage	-	AV_{DD}	-	V	
T_A	Temperature	-40	-	105	℃	

Symbol	Parameter	Min. [*1]	Typ.	Max. [*1]	Unit	Test Conditions
I_{ADC1}	Operating current (AV_{DD} current) (Enable ADC and disable all other analog modules)	223	-	237	uA	AV_{DD} = V_{DD} = V_{REF} = 3.3V ADC Clock Rate = 34 MHz low speed channel
		140	-	147		AV_{DD} = V_{DD} = V_{REF} = 1.7V ADC Clock Rate = 34 MHz low speed channel
I_{ADC2}		112	-	119	uA	AV_{DD} = V_{DD} = V_{REF} = 3.3V ADC Clock Rate = 14 MHz low speed channel
		72	-	75		AV_{DD} = V_{DD} = V_{REF} = 1.7V ADC Clock Rate = 14 MHz low speed channel
	Resolution	-	-	12	Bit	
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
F_{ADC}	ADC Clock frequency	0.14	-	64	MHz	Low speed channel
T_{SMP}	Sampling Time	3	-	258	$1/F_{ADC}$	
T_{CONV}	Conversion time	17	-	272	$1/F_{ADC}$	T_{CONV} = T_{SMP} + 14
F_{SPS}	Sampling Rate (F_{ADC}/T_{CONV})	-	-	2	MSPS	Low speed channel
T_{PU}	Power-up time	20	-	-	µs	
INL	Integral Non-Linearity Error	-3.4	-	4.1	LSB	V_{REF} = AV_{DD}
DNL	Differential Non-Linearity Error	-1	-	2.1	LSB	V_{REF} = AV_{DD}
E_G	Gain error	-3.1	-	3.6	LSB	V_{REF} = AV_{DD}
E_{OFFSET}	Offset error	-1.3	-	2.8	LSB	V_{REF} = AV_{DD}
E_A	Absolute Error	2.8	-	7.3	LSB	V_{REF} = AV_{DD}
C_{IN}	Internal Capacitance[*1]	-	5	-	pF	
-	Monotonic	Guaranteed			-	

Note: Guaranteed by characterization, not tested in production.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

Note: GND < EADC_CHx < V_{REF}

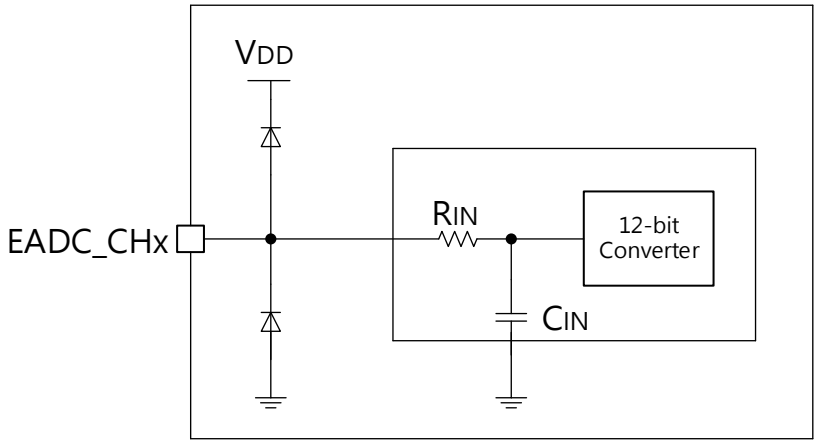


Figure 8.5-3 Typical Connection Using the ADC

8.5.6 Temperature Sensor

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Operating Voltage	1.7	-	3.6	V
T_A	Temperature Range	40	-	105	°C
I_{TEMP}	Current Consumption [*3]	-	16	-	µA
T_c	Temperature Coefficient [*3]	-1.77	-1.82	-1.86	mV/°C
V_{os}	Offset Voltage when T_A = 0°C [*3]	710	720	730	mV
t_S	Stable time[*2]	-	1	-	µs
T_{S_temp}	ADC sampling time when reading the temperature (5pF cap load) [*1]	-	3	-	µs

Note:

1. V_{TEMP} (mV) = Temperature Coefficient (mV/°C) x Temperature (°C) + Offset (mV)
2. Guaranteed by design, not tested in production
3. Guaranteed by characteristic, not tested in production

8.5.7 Digital to Analog Converter (DAC)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
AV_{DD}	Analog supply voltage	1.8	-	3.6	V	
N_R	Resolution		12		bit	
V_{REF}	Reference supply voltage	1.5		AV_{DD}	V	$V_{REF} \le AV_{DD}$
DNL	Differential non-linearity error[*4]	-	-	±2	LSB	12-bit mode
		-	-	±0.5	LSB	10-bit mode
INL	Integral non-linearity error[*4]	-	-	±4	LSB	12-bit mode
		-	-	±1	LSB	10-bit mode
OE	Offset Error[*4]	-	-	±6	LSB	12-bit mode DACOUT buffer ON
		-	-	±4	LSB	12-bit mode DACOUT buffer OFF
		-	-	±2	LSB	10-bit mode
GE	Gain Error[*4]	-12	-	4	LSB	12-bit mode DACOUT buffer ON
		-	-	±4	LSB	12-bit mode DACOUT buffer OFF
		-	-	±2	LSB	10-bit mode
AE	Absolute Error[*4]	-	-	±10	LSB	12-bit mode DACOUT buffer ON

		-	-	±4	LSB	12-bit mode DACOUT buffer OFF
		-	-	±2	LSB	10-bit mode
T_A	Temperature	-40	-	105	℃	
	Monotonic	10-bit guaranteed				
V_O	Output Voltage	0.2	-	AV_{DD} - 0.2	V	DACOUT buffer ON
R_{LOAD}	Resistive load[*2]	7.5	-	-	kΩ	DACOUT buffer ON
Ro	Output impedance[*4]	-	10	12	kΩ	DACOUT buffer OFF
C_{LOAD}	Capacitive load[*3]	-	-	50	pF	-
I_{AVDD}	Current consumption on AV_{DD} supply[*4]	175	-	195	µA	AV_{DD} = 3.6V, no load, lowest code (0x000)
		390	-	426		AV_{DD} = 3.6V, no load, middle code (0x800)
I_{REF}	Current consumption on AV_{DD} supply[*4]	-	170	240	µA	V_{REF} =3.6V, no load, middle code (0x800)
T_S	Settling Time	-	5	6	µs	Full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value +/-1 LSB, C_{LOAD}=50p, R_{LOAD} =7.5k
F_s	Update Rate	-	1	-	MSPS	Max frequency for a correct DAC_OUT change from core i to i+1LSB, C_{LOAD} = 50pF and R_{LOAD} >= 5Kohm
T_{WAKEUP}	Wake-up Time	-	9	15	µs	Wakeup time from OFF state. Input code between lowest and highest possible codes.
PSRR	Power Supply Rejection Ratio[*1]	-	-60	-40	dB	No R_{LOAD}, C_{LOAD} = 50pF

Note:

1. Guaranteed by design, not tested in production
2. Resistive load between DACOUT and AV_{SS}.
3. Capacitive load at DACOUT pin.
4. Guaranteed based on test during characterization.

8.5.8 Analog Comparator Controller (ACMP)

- The maximum values are obtained for V_{DD} = 3.6V and maximum ambient temperature (T_A), and the typical values for T_A= 25 ˚C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Comments
AV_{DD}	Analog supply voltage	1.8	-	3.6	V	
T_A	Temperature	-40	-	105	℃	
I_{DD}	Operating current	-	1.5	-	μA	MODESEL[1:0] = 00
		-	2.9	-		MODESEL[1:0] = 01
		-	11.4	-		MODESEL[1:0] = 10
		-	39.3	-		MODESEL[1:0] = 11
V_{CM}	Input common mode voltage range [*2]	0.1	-	AV_{DD} - 0.1		
V_{DI}	Differential input voltage sensitivity [*2]	10	20	-	mV	Hysteresis disable
V_{offset}	Input offset voltage	-	-	12	mV	Hysteresis disable,
V_{hys}	Hysteresis window	-	0	-	mV	HYSSEL[1:0] = 00
		-	15	-		HYSSEL[1:0] = 01
		-	28	-		HYSSEL[1:0] = 10
		-	39	-		HYSSEL[1:0] = 11
A_v	DC voltage Gain[*1]	-	70	-	dB	
T_d	Propagation delay[*2]	-	-	0.14	us	Hysteresis disable MODESEL[1:0] = 00
		-	-	0.2		Hysteresis disable MODESEL[1:0] = 01
		-	-	0.7		Hysteresis disable MODESEL[1:0] = 10
		-	-	1.5		Hysteresis disable MODESEL[1:0] = 11
T_{Setup}	Setup time[*2]	-	-	82	ns	Hysteresis disable MODESEL[1:0] = 00
		-	-	124		Hysteresis disable MODESEL[1:0] = 01
		-	-	274		Hysteresis disable MODESEL[1:0] = 10
		-	-	419		Hysteresis disable MODESEL[1:0] = 11

Note:

1. Guaranteed by design, not tested in production.
2. Guaranteed by characteristic, not tested in production.

8.6 Flash DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply Voltage	1.08		1.32	V	T_A = 25℃
N_{ENDUR}	Endurance	10000	-	-	cycles[2]	
T_{RET}	Data Retention	-	23.3	-	year	10 kcycles, Tj = 75℃
		-	10.0	-		10 kcycles, Tj = 85℃
		-	2.2	-		10 kcycles, Tj = 105℃
		-	0.5	-		10 kcycles, Tj = 125℃
T_{ERASE}	Page Erase Time	92	-	160	mS	T_A = 25℃
T_{MER}	Mass Erase Time	201	-	320		
T_{PROG}	Program Time	42	-	50	uS	
I_{DD1}	Read Current	-	-	4.12	mA	
I_{DD2}	Program Current	-	-	5	mA	
I_{DD3}	Erase Current	-	-	5	uA	

Note:

1. V_{FLA} is source from chip LDO output voltage.
2. Number of program/erase cycles.
3. This table is guaranteed by design, not test in production.

8.7 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.2	-	uS
t_{HIGH}	SCL high period	4	-	0.6	-	uS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	1.2	-	uS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	uS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	uS
t_{BUF}	Bus free time	4.7 [3]	-	1.2 [3]	-	uS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0 [4]	3.45 [5]	20+0.1Cb [4]	0.8[5]	uS
t_r	SCL/SDA rise time	-	1000	-	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

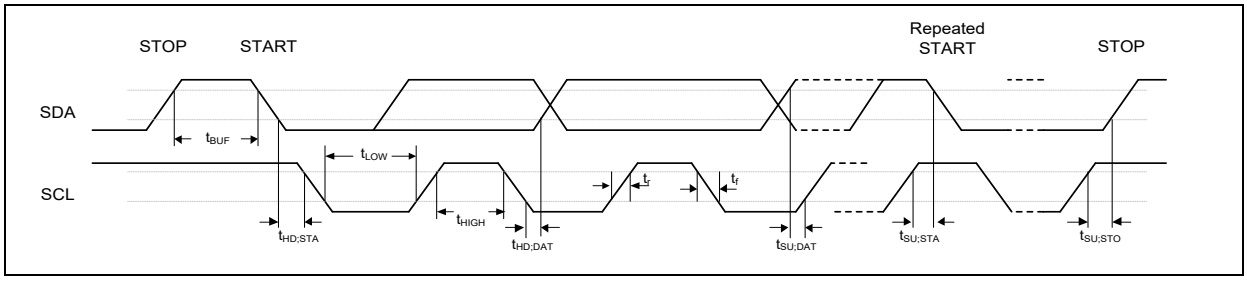


Figure 8.7-1 I²C Timing Diagram

8.8 SPI Dynamic Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
SPI Master Mode (V_{DD} = 3.0~3.6 V, 30 PF loading Capacitor)					
t_{CLKL}	Clock output High time [*1]	-	-	T_{SPICLK} / 2	ns
t_{CLKH}	Clock output Low time [*1]	-	-	T_{SPICLK} / 2	ns
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2	-	-	ns
t_V	Data output valid time	-	0	1	ns

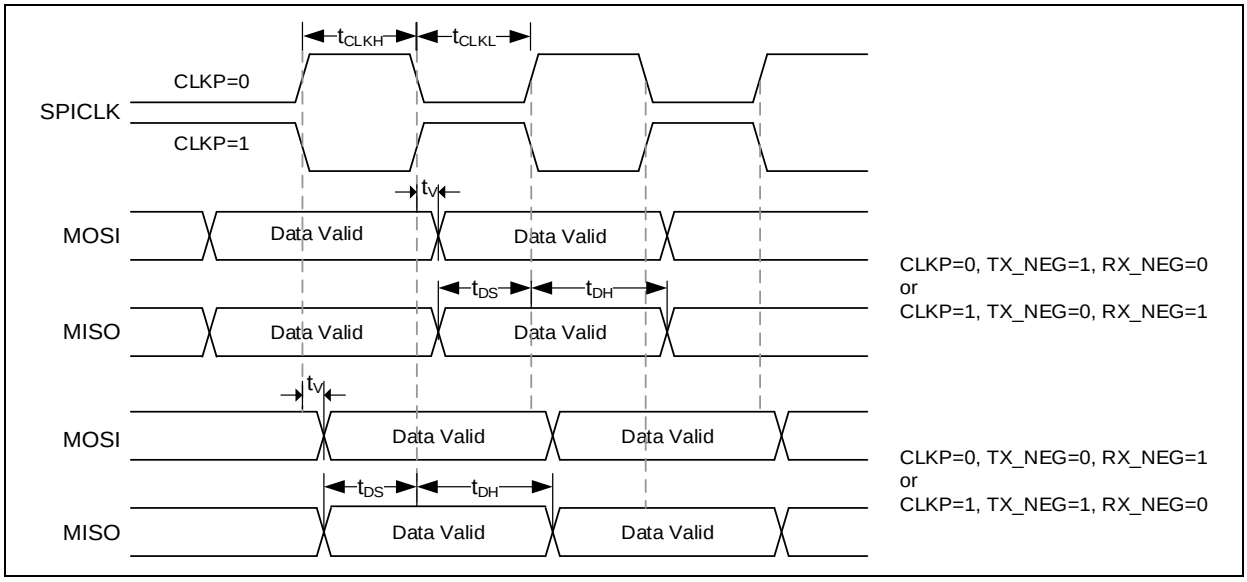


Figure 8.8-1 SPI Master Mode Timing Diagram

Symbol	Parameter	Min	Typ	Max	Unit
SPI Slave Mode (V_{DD} = 3.0~3.6V, 30 PF Loading Capacitor)					
t_{CLKL}	Clock output High time [*1]	-	-	T_{SPICLK} / 2	Peripheral clock
t_{CLKH}	Clock output Low time [*1]	-		T_{SPICLK} / 2	Peripheral clock
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	Peripheral clock
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	Peripheral clock
t_{DS}	Data input setup time	0	-	-	ns
t_{DH}	Data input hold time	2	-	-	ns
t_V	Data output valid time	-	-	8	ns

t_{CLKH}	Clock output High time [*1]	-	-	T_{SPICLK} / 2	ns

Note: The minimum clock period for SPICLK is 41.67 ns (24 MHz).

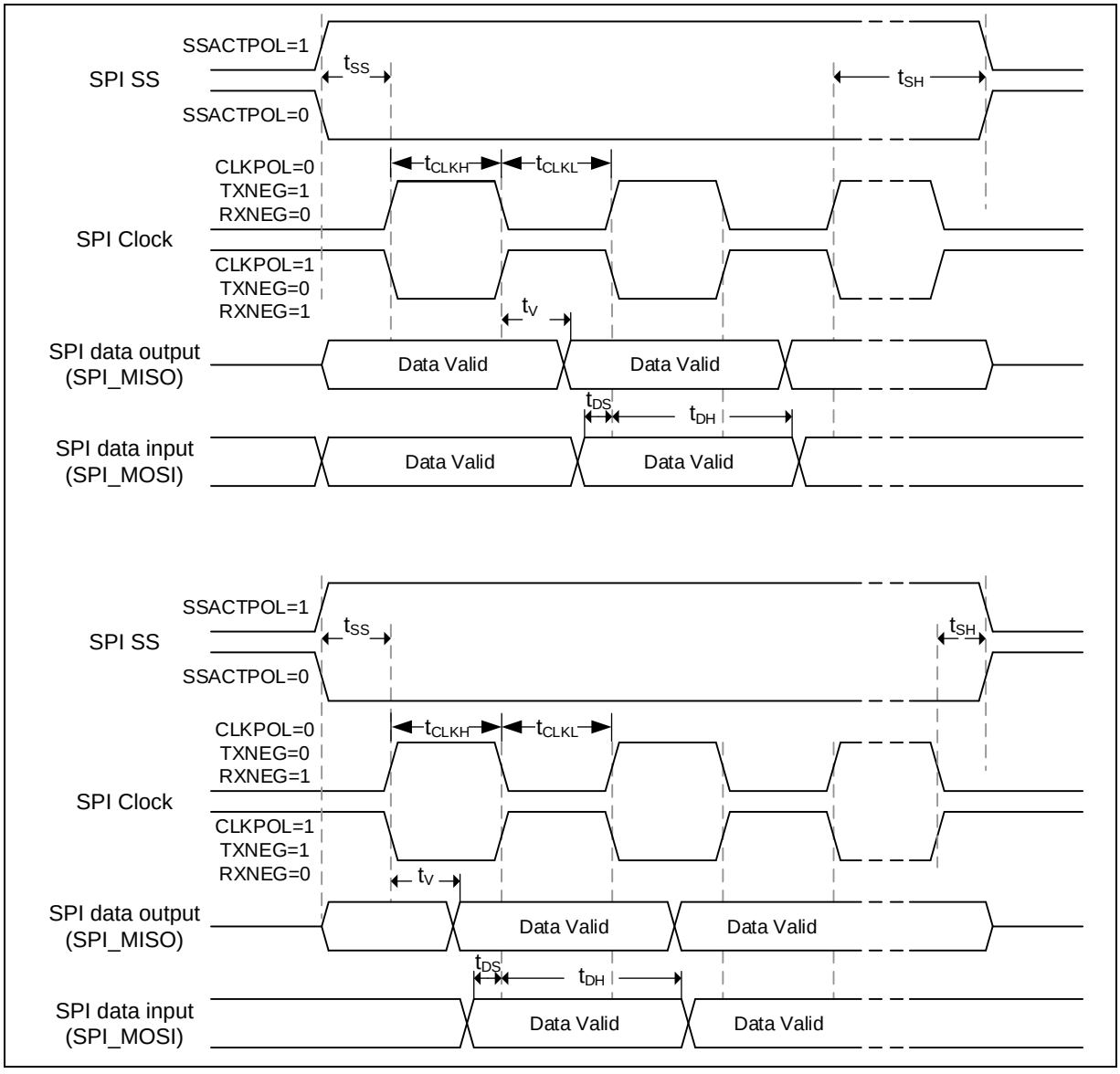


Figure 8.8-2 SPI Slave Mode Timing Diagram

8.9 I²S Dynamic Characteristics

Symbol	Parameter	Min	Max	Unit	Test Conditions
$t_{w(CKH)}$	I²S clock high time	39	-	ns	Master f_{PCLK} = MHz, data: 24 bits, audio frequency = 256 kHz
$t_{w(CKL)}$	I²S clock low time	39	-		
$t_{v(WS)}$	WS valid time	2	12		Master mode
$t_{h(WS)}$	WS hold time	1	-		Master mode
$t_{su(WS)}$	WS setup time	24	-		Slave mode
$t_{h(WS)}$	WS hold time	0	-		Slave mode
$DuCy_{(SCK)}$	I²S slave input clock duty cycle	35	65	%	Slave mode
$t_{su(SD\_MR)}$	Data input setup time	22	-	ns	Master receiver
$t_{su(SD\_SR)}$		10	-		Slave receiver
$t_{h(SD\_MR)}$	Data input hold time	7	-		Master receiver
$t_{h(SD\_SR)}$		8	-		Slave receiver
$t_{v(SD\_ST)}$	Data output valid time	-	21		Slave transmitter (after enable edge)
$t_{h(SD\_ST)}$	Data output hold time	4	-		Slave transmitter (after enable edge)
$t_{v(SD\_MT)}$	Data output valid time	-	7		Master transmitter (after enable edge)
$t_{h(SD\_MT)}$	Data output hold time	0	-		Master transmitter (after enable edge)

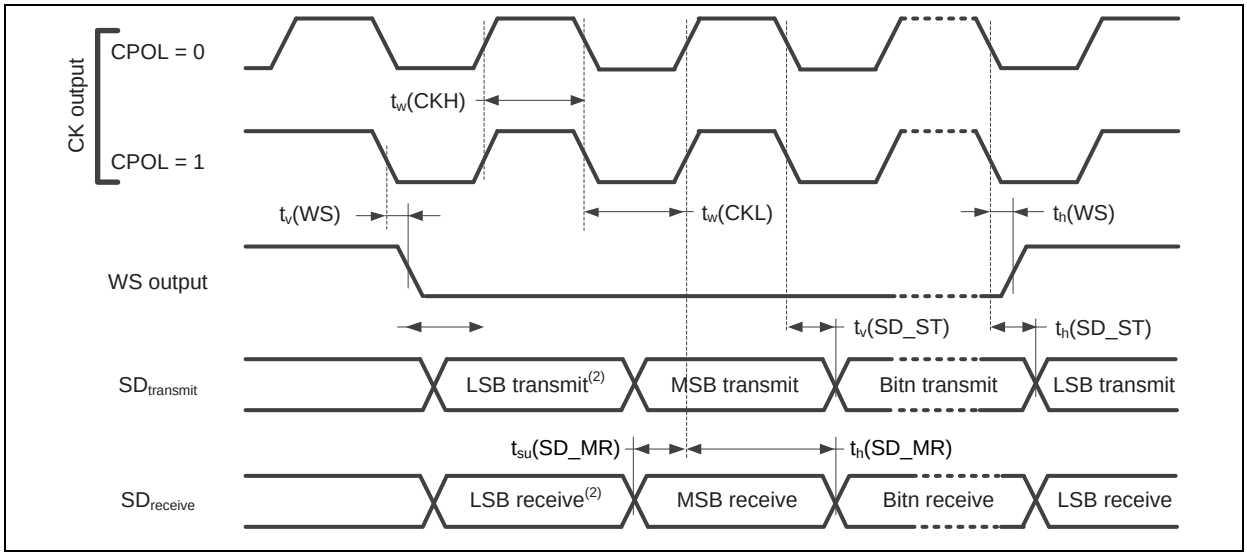


Figure 8.9-1 I²S Master Mode Timing Diagram

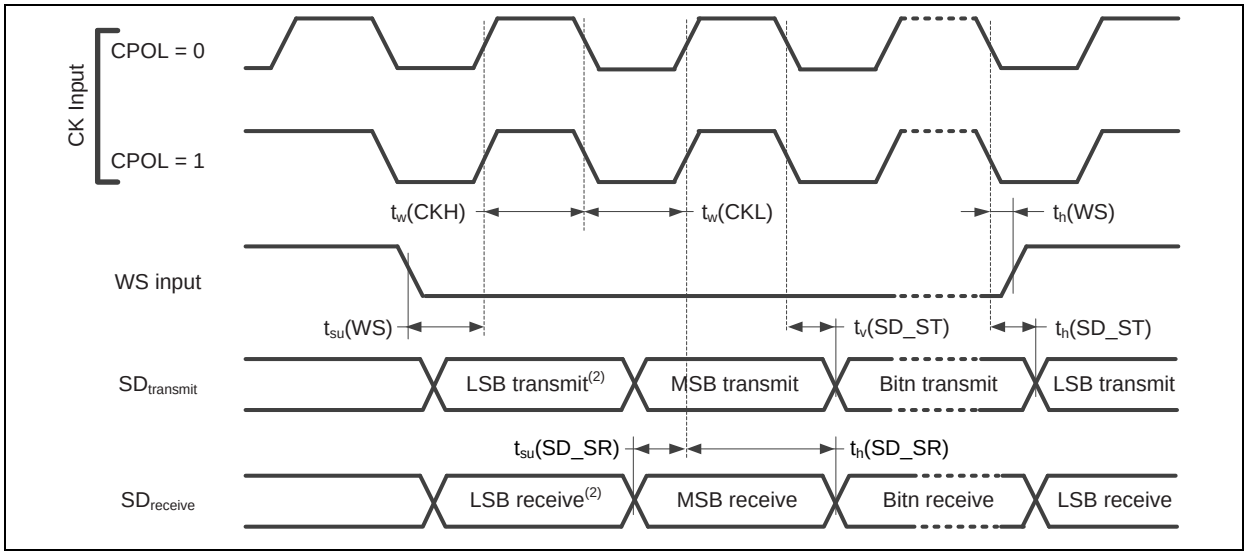


Figure 8.9-2 I²S Slave Mode Timing Diagram

8.10 USCI - I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.2	-	uS
t_{HIGH}	SCL high period	4	-	0.6	-	uS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	1.2	-	uS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	uS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	uS
t_{BUF}	Bus free time	4.7 [3]	-	1.2 [3]	-	uS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0 [4]	3.45 [5]	20+0.1Cb [4]	0.8[5]	uS
t_r	SCL/SDA rise time	-	1000	-	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

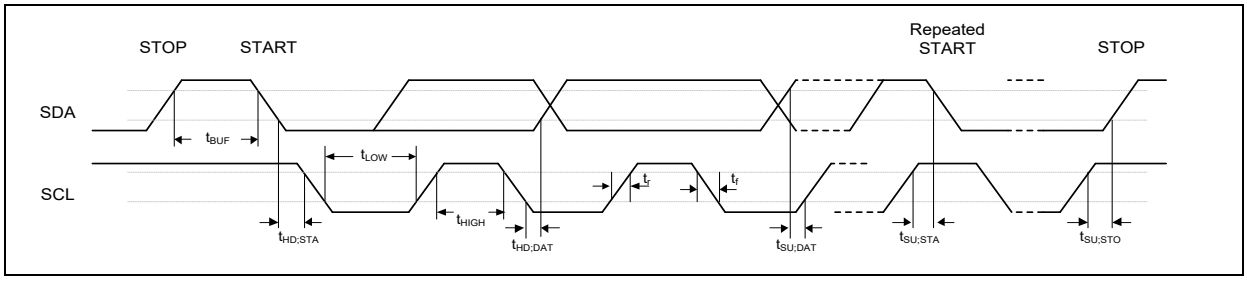


Figure 8.10-1 I²C Timing Diagram

8.11 USCI - SPI Dynamic Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{CLKH}	Clock output High time [*1]	-	-	T_{SPICLK} / 2	ns
t_{CLKL}	Clock output Low time [*1]	-	-	T_{SPICLK} / 2	ns
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2	-	-	ns
t_V	Data output valid time	-	0	1	ns
Note: The minimum clock period for SPICLK is 41.67 ns (24 MHz).					

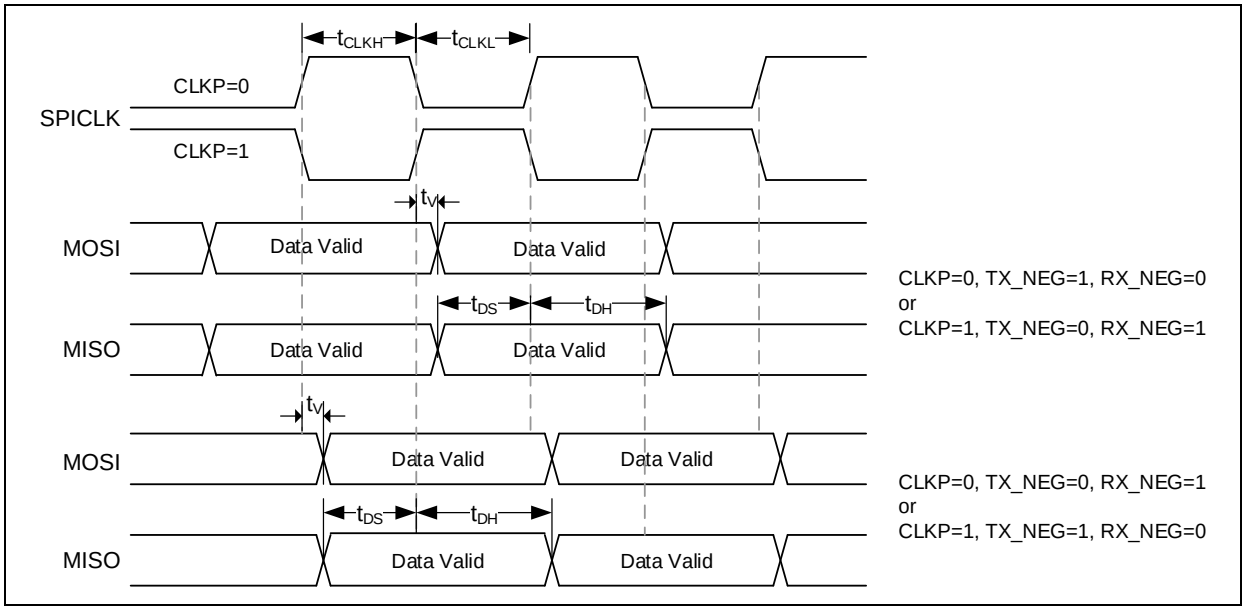


Figure 8.11-1 SPI Master Mode Timing Diagram

Symbol	Parameter	Min	Typ	Max	Unit
t_{CLKH}	Clock output High time [*1]	-	-	T_{SPICLK} / 2	ns
t_{CLKL}	Clock output Low time [*1]	-		T_{SPICLK} / 2	ns
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	ns
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	ns
t_{DS}	Data input setup time	0	-	-	ns
t_{DH}	Data input hold time	2	-	-	ns
t_V	Data output valid time	-		8	ns
t_{CLKH}	Clock output High time [*1]	-	-	T_{SPICLK} / 2	ns

Note: The minimum clock period for SPICLK is 41.67 ns (24 MHz).

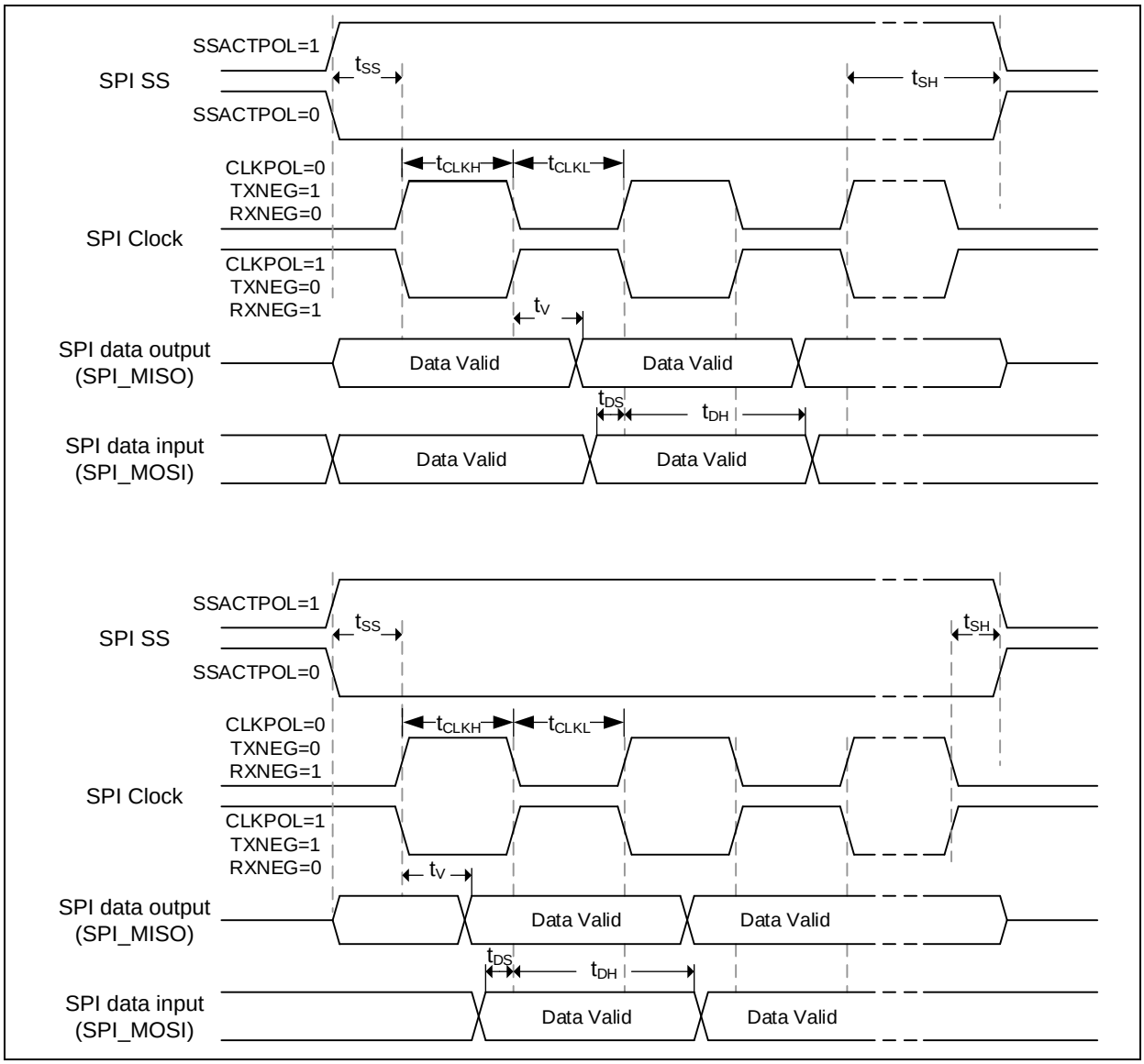


Figure 8.11-2 SPI Slave Mode Timing Diagram

8.12 USB Characteristics

8.12.1 USB Full-Speed PHY Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Power	3	3.3	3.6	V	-
V_{IH}	Input High (driven)	2.0	-	-	V	
V_{IL}	Input Low	-	-	0.8	V	-
V_{DI}	Differential Input Sensitivity	0.2	-	-	V	|PADP-PADM|
V_{CM}	Differential Common-mode Range	0.8	-	2.5	V	Includes V_{DI} range
V_{SE}	Single-ended Receiver Threshold	0.8	-	2.0	V	-
	Receiver Hysteresis	-	200	-	mV	-
V_{OL}	Output Low (driven)	0	-	0.3	V	-
V_{OH}	Output High (driven)	2.8	-	3.6	V	-
V_{CRS}	Output Signal Cross Voltage	1.3	-	2.0	V	-
R_{PU}	Pull-up Resistor	1.425	-	1.575	kΩ	-
R_{PD}	Pull-down Resistor	14.25	-	15.75	kΩ	
V_{TRM}	Termination Voltage for Uptream port pull up (RPU)	3.0	-	3.6	V	
Z_{DRV}	Driver Output Resistance	-	10	-	Ω	Steady state drive*
C_{IN}	Transceiver Capacitance	-	-	20	pF	Pin to GND
T_{FR}	Rise Time	4	-	20	ns	C_L=50p
T_{FF}	Fall Time	4	-	20	ns	C_L=50p
T_{FRFF}	Rise and Fall Time Matching	90	-	111.11	%	$T_{FRFF}=T_{FR}/T_{FF}$

Note:

1. Guaranteed by design, not tested in production.
2. To ensure stability, an external 1 μF output capacitor, 1uF external capacitor must be connected between the USB_VDD33_CAP pin and the closest GND pin of the device.
3. USB_D+ and USB_D- must be connected with series resistors to fit USB Full-speed spec request (28 ~ 44Ω).

8.13 SDIO Characteristics

8.13.1 Default Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_SD\_CLK}$	SD_CLK Period (Data Transfer Mode)	40	-	-	ns	-
$T_{P\_SD\_CLK\_ID}$	SD_CLK Period (Identification Mode)	2,500	-	-	ns	
$T_{H\_SD\_CLK}$	SD_CLK High Time	-	20	-	ns	-
$T_{L\_SD\_CLK}$	SD_CLK Low Time	-	20	-	ns	-
$T_{SU\_SD\_IN}$	SD_DATA Setup Time to SD_CLK Rising	5	-	-	ns	-
$T_{HD\_SD\_IN}$	SD_DATA Hold Time from SD_CLK Rising	5	-	-	ns	-
$T_{DLY\_SD\_OUT}$	SD_CLK Falling to Valid SD_DATA Delay	-	-	14	ns	-

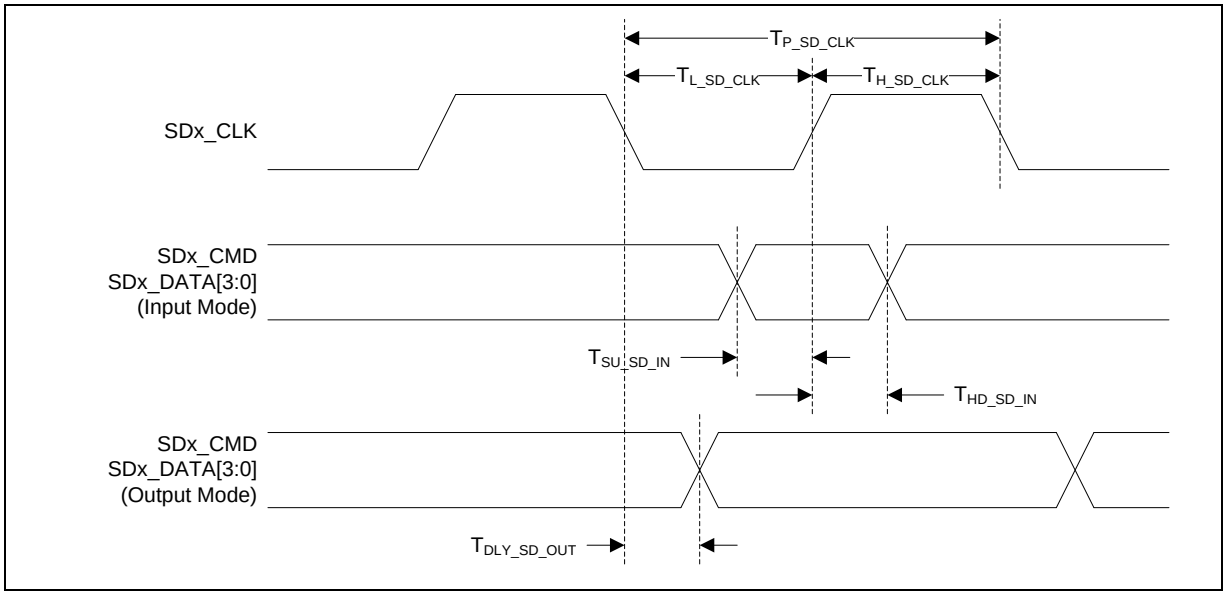


Figure 8.13-1 SDIO Default Mode

8.13.2 SDIO Dynamic Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_SD\_CLK}$	SD_CLK Period	20	-	-	ns	-
$T_{H\_SD\_CLK}$	SD_CLK High Time	7	-	-	ns	-
$T_{L\_SD\_CLK}$	SD_CLK Low Time	7	-	-	ns	-
$T_{SU\_SD\_IN}$	SD_DATA Setup Time to SD_CLK Rising	6	-	-	ns	-
$T_{HD\_SD\_IN}$	SD_DATA Hold Time from SD_CLK Rising	2	-	-	ns	-
$T_{DLY\_SD\_OUT}$	SD_CLK Falling to Valid SD_DATA Delay	-	-	14	ns	-
$T_{HD\_SD\_OUT}$	SD_DATA Hold Time from SD_CLK Rising	2.5	-	-	ns	-

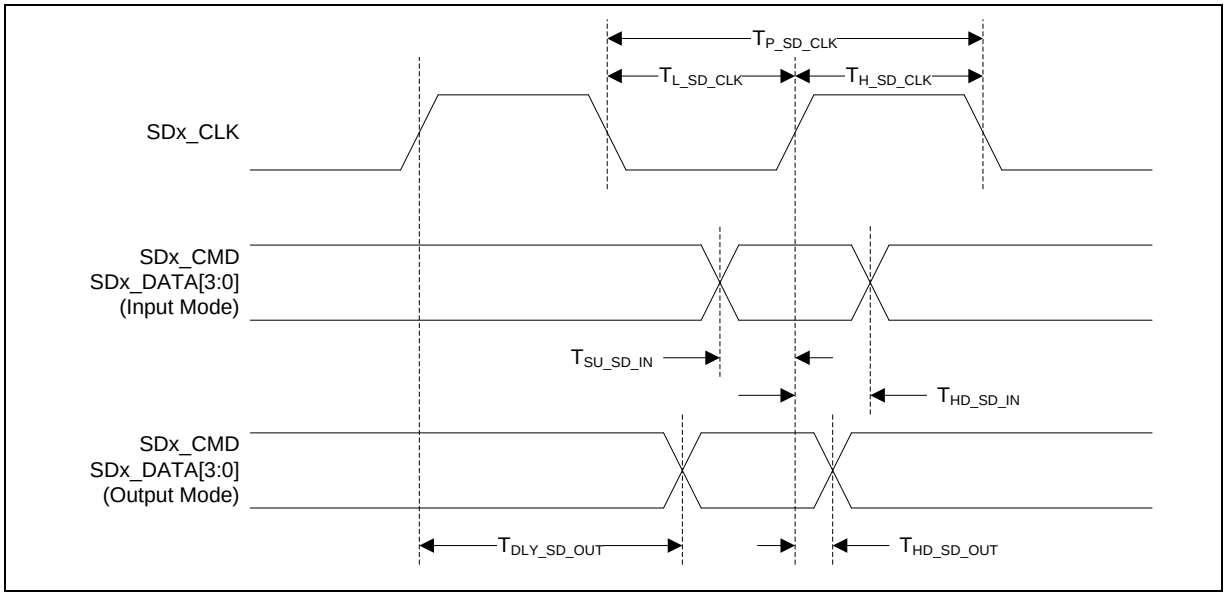
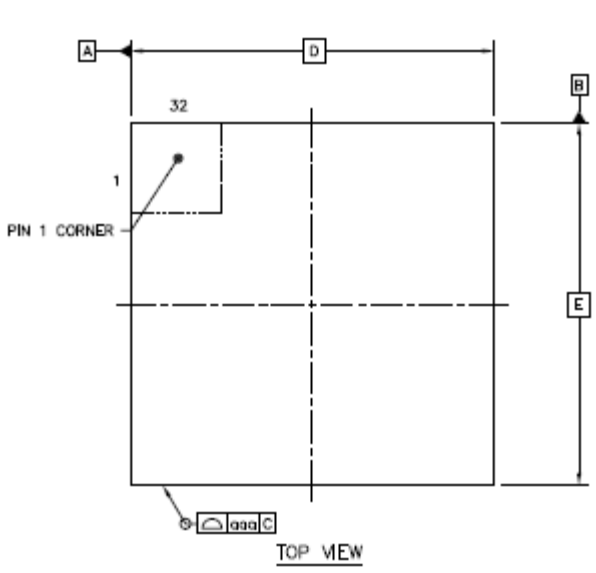


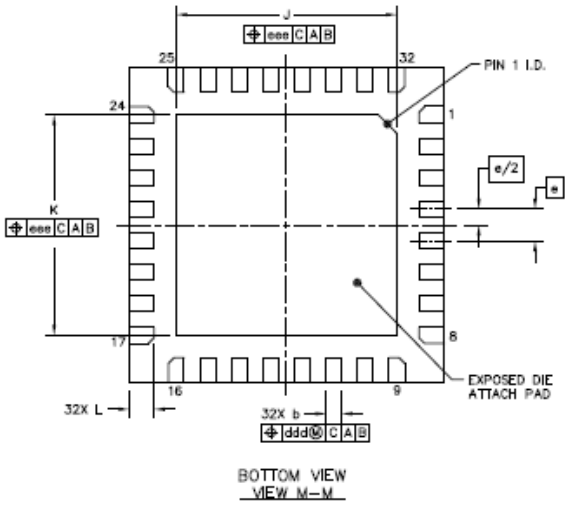
Figure 8.13-2 SDIO High-speed Mode

9 PACKAGE DIMENSIONS

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

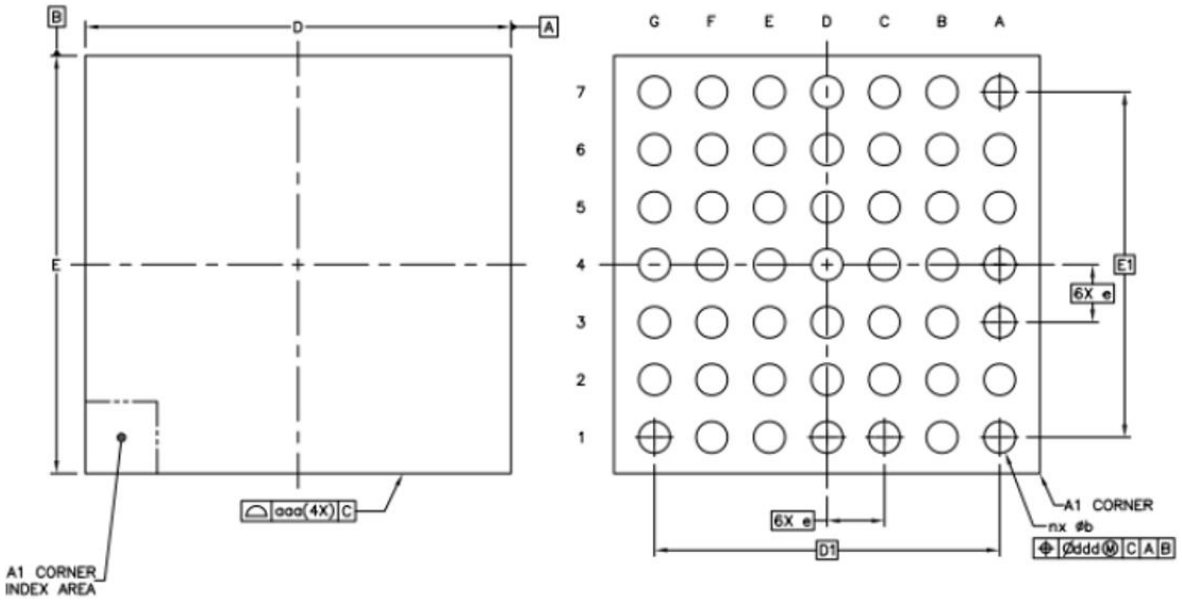
9.1 QFN 33 (5x5x0.8 mm Pitch 0.5 mm)



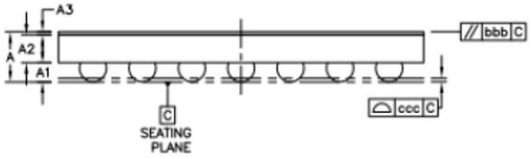


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

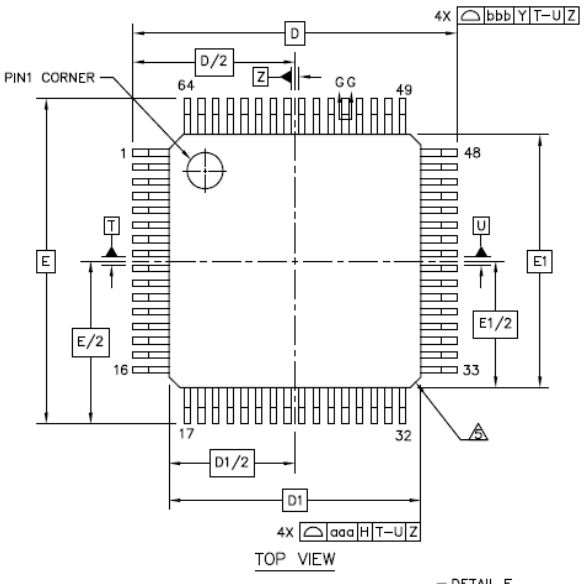
9.2 WLCSP 49 (2.960x2.905x0.405 mm Ball_Pitch 0.40mm, Ball_Diameter 0.20mm)



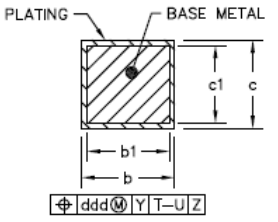
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.347	0.405	0.463
STAND OFF		A1	0.125	---	0.185
WAFER THICKNESS		A2	0.2	0.225	0.25
FILM THICKNESS		A3	0.022	0.025	0.028
BODY SIZE	X	D	2.96		
	Y	E	2.905		
BALL/BUMP PITCH	X	SD	---		BSC
	Y	SE	---		BSC
EDGE BALL CENTER TO CENTER	X	D1	2.4		BSC
	Y	E1	2.4		BSC
PITCH		e	0.4		BSC
BALL DIAMETER (SIZE)			0.2		
BALL/BUMP WIDTH		b	0.19	---	0.25
BALL/BUMP COUNT		n	49		
PACKAGE EDGE TOLERANCE		aaa	0.03		
WAFER FLATNESS		bbb	0.06		
COPLANARITY		ccc	0.03		
BALL/BUMP OFFSET (PACKAGE)		ddd	0.015		

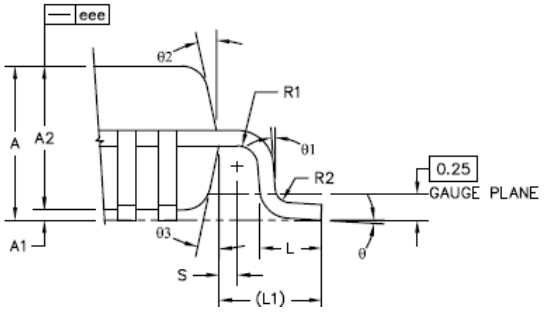


9.3 LQFP 64 (7x7x1.4 mm Footprint 2.0 mm)

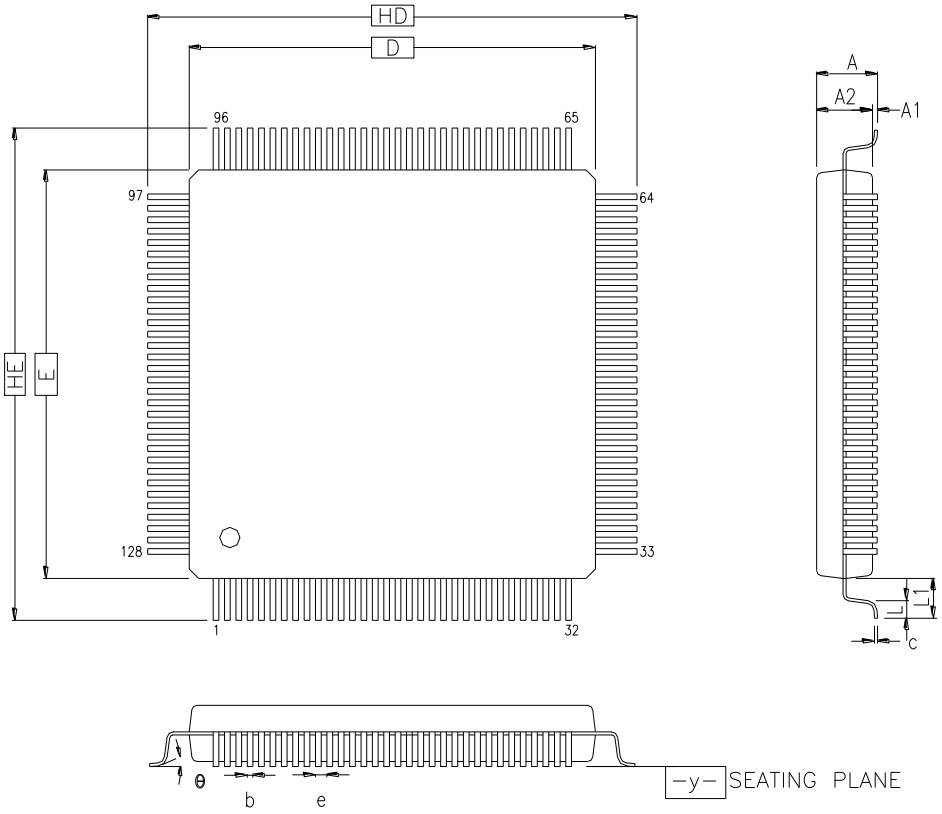


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		





9.4 LQFP 128 (14x14x1.4 mm Footprint 2.0 mm)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

10 ABBREVIATIONS

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EADC	Enhanced Analog-to-Digital Converter
EBI	External Bus Interface
EMAC	Ethernet MAC Controller
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	12 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface

SD	Secure Digital
SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TK	Touch Key
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

11 REVISION HISTORY

Date	Revision	Description
2018.08.24	1.00	• Initial version.
2019.02.15	1.01	• Added electrical characteristics information.
2019.10.09	1.02	• Added M2351SF related data
2024.02.02	1.03	• Updated data retention value in section 8.6 • Added V_{LDO} maximum and minimum value in section 8.5.1 • Updated HIRC12M maximum and minimum value in section 8.4.5 • Updated WLCSP49 Pin Diagram and Pin Description in the section 4 • Added WLCSP49 Package Dimensions in the section 9.2