# MOS INTEGRATED CIRCUITS

# M 2708
# M 2704

**PRELIMINARY DATA**

## M 2708-8K BIT (1024 X 8) UV ERASABLE PROM
## M 2704-4K BIT ( 512 X 8) UV ERASABLE PROM

- STANDARD POWER SUPPLES: +12V, +5V, -5V
- TTL COMPATIBLE: ALL INPUTS AND OUTPUTS DURING BOTH READ AND PROGRAM MODES
- THREE-STATE OUTPUT
- ORGANIZATION: M 2708-1024 X 8-BIT IN A 24-LEAD DUAL IN-LINE PACKAGE
  M 2704-512 X 8-BIT IN A 24-LEAD DUAL IN-LINE PACKAGE
- ACCESS TIME: 450 ns MAX.
- FAST PROGRAMMING: TYP. 100 sec. FOR ALL 8K BITS
- LOW POWER CONSUMPTION DURING PROGRAMMING

The M 2708 and the M 2704 are high-speed 1024 x 8/512 x 8-bit erasable and electrically reprogrammable static ROMs (EPROM) manufactured in N-channel silicon gate MOS technology. They are supplied in 24-lead dual in-line ceramic package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the devices. The devices are fully static and therefore require no clocks to operate.

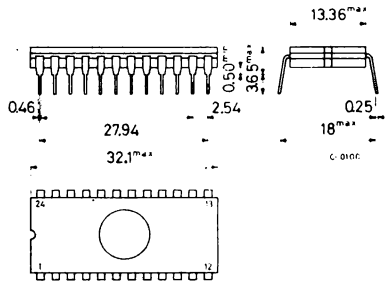
## ABSOLUTE MAXIMUM RATINGS

| | | | |
|---|---|---|---|
| $V_{DD}$ | $V_{DD}$ with respect to $V_{BB}$ | +20V to -0.3 | V |
| $V_{CC}$, $V_{SS}$ | $V_{CC}$ and $V_{SS}$ with respect to $V_{BB}$ | +15V to -0.3 | V |
| $V_{BB}$ | All input or output voltages with respect to $V_{BB}$ during read | +15V to -0.3 | V |
| $\overline{CS}$/WE | Input with respect to $V_{BB}$ during programming | +20V to -0.3 | V |
| | Program input with respect to $V_{BB}$ | +35V to -0.3 | V |
| $P_{tot}$ | Power dissipation | 1.5 | W |
| $T_{amb}$ | Ambient temperature under bias | -25 °C to + 85 | °C |
| $T_{stg}$ | Storage temperature | -65 °C to +125 | °C |

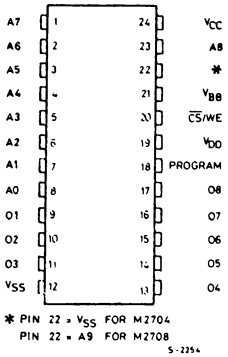
**ORDERING NUMBERS:** M 27 XX F1 for dual in-line ceramic package, frit seal

## MECHANICAL DATA

dimensions in mm



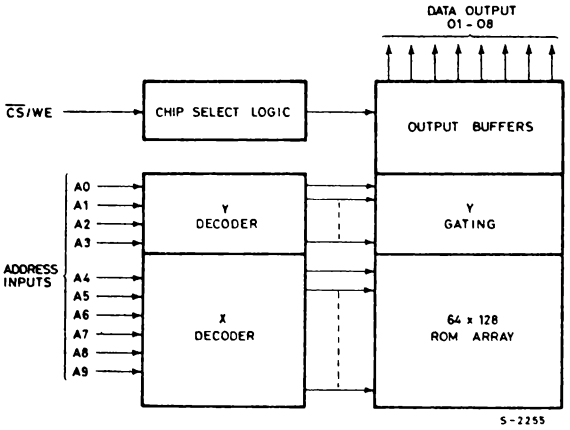
## PIN CONNECTIONS




## PIN NAMES

| | |
|---|---|
| A0-A9 | ADDRESS INPUTS |
| 01-08 | DATA OUTPUTS |
| $\overline{CS}$/WE | CHIP SELECT/WRITE ENABLE INPUT |

## BLOCK DIAGRAM




| MODE | PIN NUMBER | | | | | | |
|---|---|---|---|---|---|---|---|
| | 9,11,13,17 | 12 | 18 | 19 | 20 | 21 | 24 |
| READ | $D_{OUT}$ | $V_{SS}$ | $V_{SS}$ | $V_{DD}$ | $V_{IL}$ | $V_{BB}$ | $V_{CC}$ |
| PROGRAM | $D_{IN}$ | $V_{SS}$ | Pulsed $V_{IHP}$ | $V_{DD}$ | $V_{IHW}$ | $V_{BB}$ | $V_{CC}$ |

## READ OPERATION

**D.C. AND OPERATING CHARACTERISTICS** ($V_{CC}$ = +5V ± 5%, $V_{DD}$ = +12V ± 5%, $V_{BB}$ = -5V ± 5%, $V_{SS}$ = 0V, $T_{amb}$ = 0 to 70°C unless otherwise specified)

| Parameter | | Test conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ.* | Max. | |
| $I_{LI}$ | Address and chip select input sink current | $V_I$ = 5.25V or $V_I = V_{IL}$ | | 1 | 10 | µA |
| $I_{LO}$ | Output leakage current | $V_O$ = 5.25V, $\overline{CS}$/WE = 5V | | 1 | 10 | µA |
| $I_{DD}$ | $V_{DD}$ supply current | Worst case supply current: all inputs high $\overline{CS}$/WE = 5V $T_{amb}$ = 0°C | | 50 | 65 | mA |
| $I_{CC}$ | $V_{CC}$ supply current | | | 6 | 10 | mA |
| $I_{BB}$ | $V_{BB}$ supply current | | | 30 | 45 | mA |
| $V_{IL}$ | Input low voltage | | $V_{SS}$ | | 0.65 | V |
| $V_{IH}$ | Input high voltage | | 3 | | $V_{CC}$+1 | V |
| $V_{OL}$ | Output low voltage | $I_{OL}$ = 1.6 mA | | | 0.45 | V |
| $V_{OH1}$ | Output high voltage | $I_{OH}$ = -100 µA | 3.7 | | | V |
| $V_{OH2}$ | Output high voltage | $I_{OH}$ = -1 mA | 2.4 | | | V |
| $P_{tot}$ | Power dissipation | $T_{amb}$ = 70°C | | | 800 | mW |

* Typical values are for $T_{amb}$ = 25°C and nominal supply voltage.

**A.C. CHARACTERISTICS** ($V_{CC}$ = +5V ± 5%, $V_{DD}$ = +12V ± 5%, $V_{BB}$ = -5V ± 5%, $V_{SS}$ = 0V, $T_{amb}$ = 0 to 70 °C unless otherwise specified)

| Parameter | | M 2708-1 | | | M 2708 | | | M 2708-4 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| $t_{ACC}$ | Address to output delay | | 280 | 350 | | 280 | 450 | | 350 | 700 | ns |
| $t_{\overline{CO}}$ | Chip select to output delay | | 60 | 120 | | 60 | 120 | | 80 | 170 | ns |
| $t_{DF}$ | Chip de-select to output float | 0 | | 120 | 0 | | 120 | 0 | | 170 | ns |
| $t_{OH}$ | Address to output hold | 0 | | | 0 | | | 0 | | | ns |

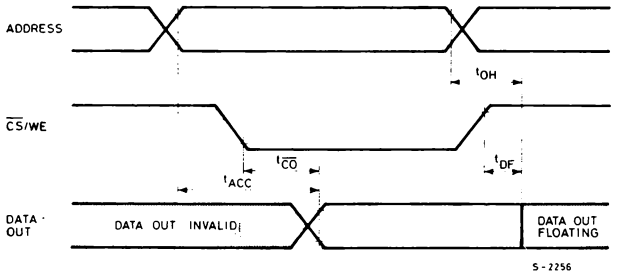
## CAPACITANCE ($T_{amb}$ = 25°C, f = 1 MHz)

| Parameter | | Test conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $C_I$ | Input capacitance | $V_I$ = 0V | | 4 | 6 | pF |
| $C_O$ | Output capacitance | $V_O$ = 0V | | 8 | 12 | pF |

## DYNAMIC TEST CONDITIONS:

Output load = 1 TTL gate and $C_L$ = 100 pF
Input Rise and Fall Times = ⩽ 20 ns
Timing Measurement Reference Levels = 0.8V and 2.8V for inputs; 0.8V and 2.4V for outputs.
Input Pulse levels = 0.65V to 3V.

## WAVEFORMS




## PROGRAMMING

Initially, and after each erasure, all bits of the M 2708/2704 are in the "1" state (output high). Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The circuit is set up for the programming operation by raising the $\overline{CS}$/WE input (pin 20) to +12V. The word address is selected in the same manner as in the read mode. Data to be programmed are presented, 8-bits in parallel, to the data output lines (01-08). The logic levels for address and data lines and the supply voltages are the same as for the read mode. After address and data set up, one program pulse for address is applied to the program input (pin 18). One pass through all addresses is defined as a program loop. The number of loops (N) required is a function of the program pulse width ($t_{pw}$) according to $Nxt_{pw} \geqslant 100$ ms.

The width of the program pulse is from 0.1 to 1 ms. The number of loops (N) is from a minimum of 100 ($t_{pw}$= 1 ms) to greater than 1000 ($t_{pw}$= 0.1 ms). There must be N successive loops through all 1024 address. It is not permitted to apply N program pulses to an address and then change to the next address to be programmed.

Caution should be observed regarding the end of a program sequence. The $\overline{CS}$/WE falling edge transition must occur before the first address transition when changing from a program to a read cycle. The program pin should also be pulled down to $V_{ILP}$ with an active instead of a passive device. This pin will source a small current ($I_{PL}$) when $\overline{CS}$/WE is at $V_{IHW}$ (12V) and the program is at $V_{ILP}$. Truth table formats for printed cards and paper tape must be compatible with Intel ones.

## ERASURE CHARACTERISTICS

The erasure characteristics of the M 2708 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 Å range. Data show that constant exposure to room level fluorescent lighting could erase the typical M 2708 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight.

The recommended erasure procedure for the M 2708 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity X exposure time) for erasure should be a minimum of 15 W-sec/cm$^2$. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12000 $\mu$W/cm$^2$ power rating. The M 2708 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

## PROGRAM CHARACTERISTICS

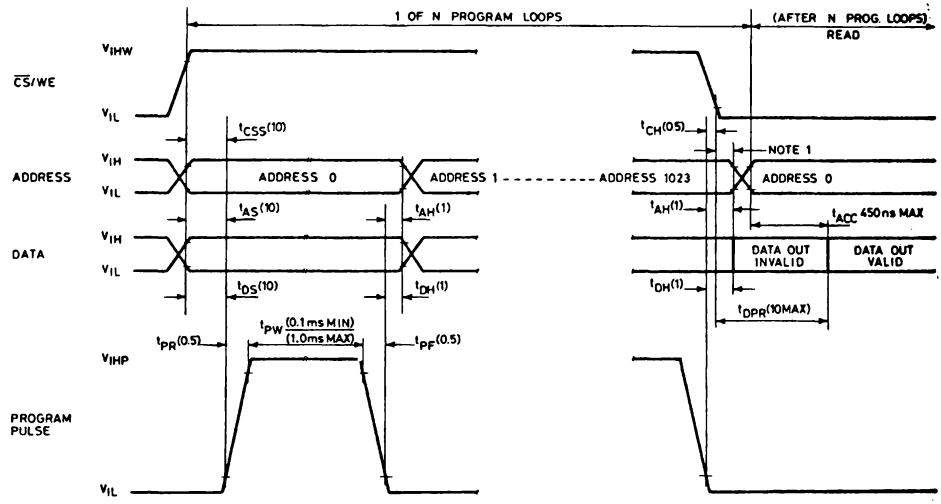
D.C. PROGRAMMING CHARACTERISTICS ($T_{amb}$= 25°C, $V_{CC}$= +5V ± 5%, $V_{DD}$= +12V ± 5%, $V_{BB}$= -5V ± 5%, $V_{SS}$= 0V unless otherwise specified)

| Parameter | | Test conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $I_{LI}$ | Address CS/W input sink current | $V_i$ = 5.25V | | | 10 | µA |
| $I_{IPL}$ | Program pulse source current | | | | 3 | mA |
| $I_{IPH}$ | Program pulse sink current | | | | 20 | mA |
| $I_{DD}$ | $V_{DD}$ supply current | Worst case supply current all inputs high $\overline{CS}$/WE= 5V; $T_{amb}$= 0° C | | 50 | 65 | mA |
| $I_{CC}$ | $V_{CC}$ supply current | | | 6 | 10 | mA |
| $I_{BB}$ | $V_{BB}$ supply current | | | 30 | 45 | mA |
| $V_{IL}$ | Input low level (except program) | | $V_{SS}$ | | 0.65 | V |
| $V_{IH}$ | Input high level for all address or data | | 3 | | $V_{CC}$+1 | V |
| $V_{IHW}$ | $\overline{CS}$/WE input high level | referenced to $V_{SS}$ | 11.4 | | 12.6 | V |
| $V_{IHP}$ | Program pulse high level | referenced to $V_{SS}$ | 25 | | 27 | V |
| $V_{ILP}$ | Program pulse low level | $V_{IHP}$-$V_{ILP}$= 25V min. | $V_{SS}$ | | 1 | V |

## A.C. PROGRAMMING CHARACTERISTICS

| Parameter | | Test conditions | Values | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $t_{AS}$ | Address setup time | | 10 | | | µs |
| $t_{CSS}$ | $\overline{CS}$/WE setup time | | 10 | | | µs |
| $t_{DS}$ | Data setup time | | 10 | | | µs |
| $t_{AH}$ | Address hold time | | 1 | | | µs |
| $t_{CH}$ | $\overline{CS}$/WE hold time | | 0.5 | | | µs |
| $t_{DH}$ | Data hold time | | 1 | | | µs |
| $t_{DF}$ | Chip deselect to output float delay | | 0 | | 120 | ns |
| $t_{DPR}$ | Program to read delay | | | | 10 | µs |
| $t_{PW}$ | Program pulse width | | 0.1 | | 1 | ms |
| $t_{PR}$ | Program pulse rise time | | 0.5 | | 2 | µs |
| $t_{PF}$ | Program pulse fall time | | 0.5 | | 2 | µs |

## PROGRAMMING WAVEFORMS




NOTE 1: THE $\overline{CS}/WE$ TRANSITION MUST OCCUR AFTER THE PROGRAM PULSE TRANSITION AND BEFORE THE ADDRESS TRANSITION
NOTE 2: NUMBERS IN ( ) INDICATE MINIMUM TIMING IN $\mu s$ UNLESS OTHERWISE SPECIFIED

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