



# M27128A

## NMOS 128 Kbit (16Kb x 8) UV EPROM

NOT FOR NEW DESIGN

- FAST ACCESS TIME: 200ns
- EXTENDED TEMPERATURE RANGE
- SINGLE 5 V SUPPLY VOLTAGE
- LOW STANDBY CURRENT: 40mA max
- TTL COMPATIBLE DURING READ and PROGRAM
- FAST PROGRAMMING ALGORITHM
- ELECTRONIC SIGNATURE
- PROGRAMMING VOLTAGE: 12V

### DESCRIPTION

The M27128A is a 131,072 bit UV erasable and electrically programmable memory EPROM. It is organized as 16,384 words by 8 bits.

The M27128A is housed in a 28 Pin Window Ceramic Frit-Seal Dual-in-Line package. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written to the device by following the programming procedure.

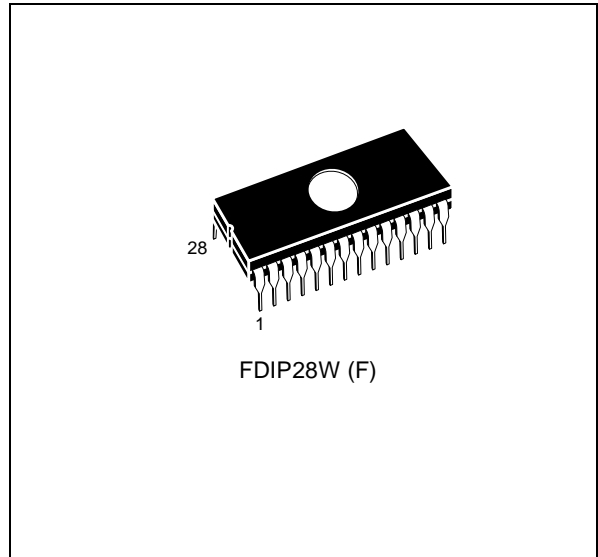
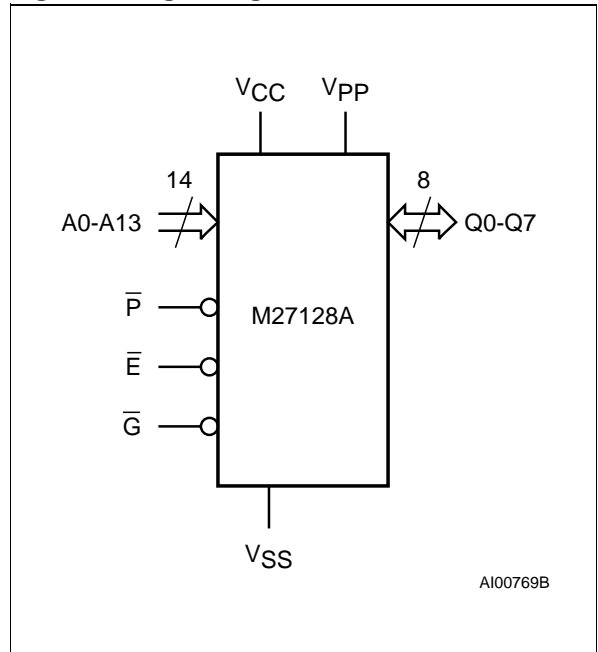


Figure 1. Logic Diagram

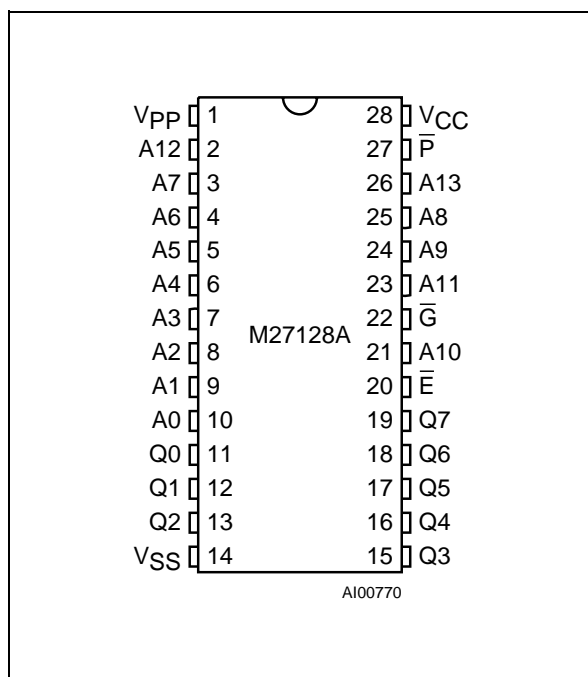


**Table 2. Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
T <sub>A</sub>	Ambient Operating Temperature	grade 1 grade 6	°C
T <sub>BIAS</sub>	Temperature Under Bias	grade 1 grade 6	°C
T <sub>STG</sub>	Storage Temperature		°C
V <sub>IO</sub>	Input or Output Voltages		V
V <sub>CC</sub>	Supply Voltage		V
V <sub>A9</sub>	A9 Voltage		V
V <sub>PP</sub>	Program Supply		V

**Note:** Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Figure 2. DIP Pin Connections**



**DEVICE OPERATION**

The seven modes of operation of the M27128A are listed in the Operating Modes table. A single 5V power supply is required in the read mode. All inputs are TTL levels except for V<sub>PP</sub> and 12V on A9 for Electronic Signature.

**Read Mode**

The M27128A has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ( $\bar{E}$ ) is the power control and should be used for device selection. Output Enable ( $\bar{G}$ ) is the output control and should be used to gate data to the output pins, independent of device selection.

Assuming that the addresses are stable, address access time (t<sub>AVQV</sub>) is equal to the delay from  $\bar{E}$  to output (t<sub>ELQV</sub>). Data is available at the outputs after the falling edge of  $\bar{G}$ , assuming that  $\bar{E}$  has been low and the addresses have been stable for at least t<sub>AVQV</sub>-t<sub>GLQV</sub>.

**Standby Mode**

The M27128A has a standby mode which reduces the maximum active power current from 85mA to 40mA. The M27128A is placed in the standby mode by applying a TTL high signal to the  $\bar{E}$  input. When in the standby mode, the outputs are in a high impedance state, independent of the  $\bar{G}$  input.

**Two Line Output Control**

Because EPROMs are usually used in larger memory arrays, this product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

- a. the lowest possible memory power dissipation,
- b. complete assurance that output bus contention will not occur.

**DEVICE OPERATION** (cont'd)

For the most efficient use of these two control lines,  $\bar{E}$  should be decoded and used as the primary device selecting function, while  $\bar{G}$  should be made a common connection to all devices in the array and connected to the  $\overline{READ}$  line from the system control bus.

This ensures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is required from a particular memory device.

**System Considerations**

The power switching characteristics of fast EPROMs require careful decoupling of the devices. The supply current,  $I_{CC}$ , has three segments that are of interest to the system designer: the standby current level, the active current level, and transient current peaks that are produced by the falling and rising edges of  $\bar{E}$ . The magnitude of this transient current peaks is dependent on the capacitive and inductive loading of the device at the output. The associated transient voltage peaks can be suppressed by complying with the two line output control and by properly selected decoupling capacitors. It is recommended that a  $1\mu\text{F}$  ceramic capacitor be used on every device between  $V_{CC}$  and  $V_{SS}$ . This should be a high frequency capacitor

of low inherent inductance and should be placed as close to the device as possible. In addition, a  $4.7\mu\text{F}$  bulk electrolytic capacitor should be used between  $V_{CC}$  and GND for every eight devices. The bulk capacitor should be located near the power supply connection point. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PCB traces.

**Programming**

When delivered (and after each erasure for UV EPROM), all bits of the M27128A are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The M27128A is in the programming mode when  $V_{PP}$  input is at 12.5V and  $\bar{E}$  and  $\bar{P}$  are at TTL low. The data to be programmed is applied 8 bits in parallel, to the data output pins. The levels required for the address and data inputs are TTL.

**Fast Programming Algorithm**

Fast Programming Algorithm rapidly programs M27128A EPROMs using an efficient and reliable method suited to the production programming environment. Programming reliability is also ensured as the incremental program margin of each byte is

**Table 3. Operating Modes**

Mode	$\bar{E}$	$\bar{G}$	$\bar{P}$	A9	$V_{PP}$	Q0 - Q7
Read	$V_{IL}$	$V_{IL}$	$V_{IH}$	X	$V_{CC}$	Data Out
Output Disable	$V_{IL}$	$V_{IH}$	$V_{IH}$	X	$V_{CC}$	Hi-Z
Program	$V_{IL}$	$V_{IH}$	$V_{IL}$ Pulse	X	$V_{PP}$	Data In
Verify	$V_{IL}$	$V_{IL}$	$V_{IH}$	X	$V_{PP}$	Data Out
Program Inhibit	$V_{IH}$	X	X	X	$V_{PP}$	Hi-Z
Standby	$V_{IH}$	X	X	X	$V_{CC}$	Hi-Z
Electronic Signature	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{ID}$	$V_{CC}$	Codes Out

Note: X =  $V_{IH}$  or  $V_{IL}$ ,  $V_{ID} = 12V \pm 0.5\%$ .

**Table 4. Electronic Signature**

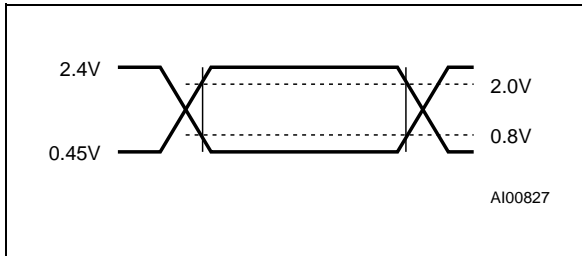
Identifier	A0	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Hex Data
Manufacturer's Code	$V_{IL}$	0	0	1	0	0	0	0	0	20h
Device Code	$V_{IH}$	1	0	0	0	1	0	0	1	89h

**AC MEASUREMENT CONDITIONS**

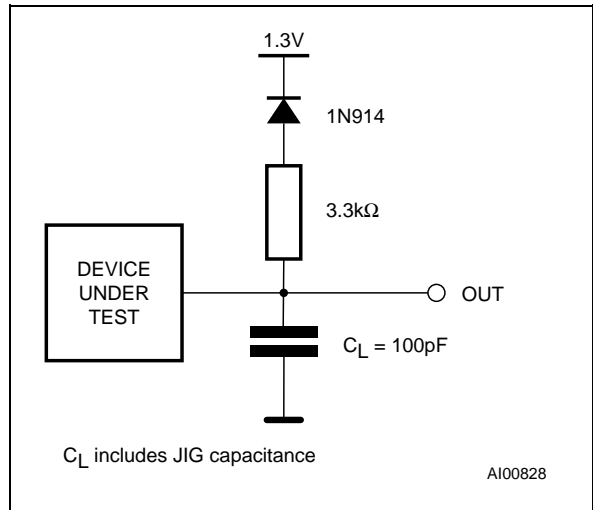
Input Rise and Fall Times  $\leq 20\text{ns}$   
 Input Pulse Voltages 0.45V to 2.4V  
 Input and Output Timing Ref. Voltages 0.8V to 2.0V

Note that Output Hi-Z is defined as the point where data is no longer driven.

**Figure 3. AC Testing Input Output Waveforms**



**Figure 4. AC Testing Load Circuit**

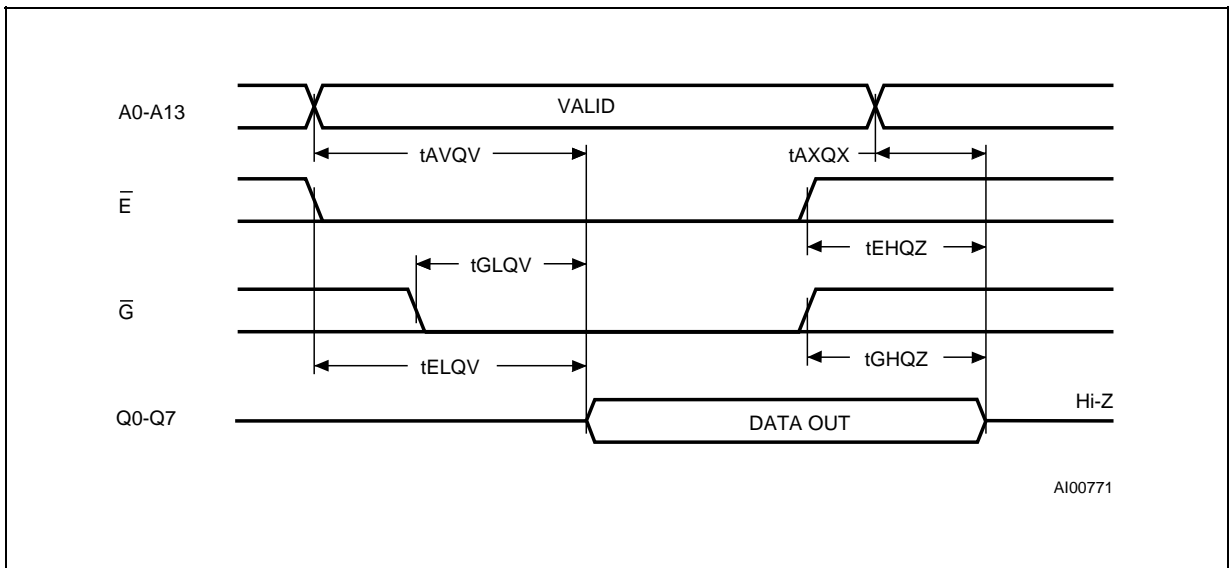


**Table 5. Capacitance <sup>(1)</sup> (T<sub>A</sub> = 25 °C, f = 1 MHz)**

Symbol	Parameter	Test Condition	Min	Max	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	=	6	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 0V	=	12	pF

**Note:** 1. Sampled only, not 100% tested.

**Figure 5. Read Mode AC Waveforms**



**Table 6. Read Mode DC Characteristics <sup>(1)</sup>**(T<sub>A</sub> = 0 to 70 °C or -40 to 85 °C; V<sub>CC</sub> = 5V ± 5% or 5V ± 10%; V<sub>PP</sub> = V<sub>CC</sub>)

Symbol	Parameter	Test Condition	Min	Max	Unit
I <sub>LI</sub>	Input Leakage Current	0 ≤ V <sub>IN</sub> ≤ V <sub>CC</sub>		±10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = V <sub>CC</sub>		±10	μA
I <sub>CC</sub>	Supply Current	$\bar{E} = V_{IL}, \bar{G} = V_{IL}$		75	mA
I <sub>CC1</sub>	Supply Current (Standby)	$\bar{E} = V_{IH}$		35	mA
I <sub>PP</sub>	Program Current	V <sub>PP</sub> = V <sub>CC</sub>		5	mA
V <sub>IL</sub>	Input Low Voltage		-0.1	0.8	V
V <sub>IH</sub>	Input High Voltage		2	V <sub>CC</sub> + 1	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA	=	0.45	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400μA	2.4		V

**Note:** 1. V<sub>CC</sub> must be applied simultaneously with or before V<sub>PP</sub> and removed simultaneously or after V<sub>PP</sub>.**Table 7. Read Mode AC Characteristics <sup>(1)</sup>**(T<sub>A</sub> = 0 to 70 °C or -40 to 85 °C; V<sub>CC</sub> = 5V ± 5% or 5V ± 10%; V<sub>PP</sub> = V<sub>CC</sub>)

Symbol	Alt	Parameter	Test Condition	M27128A								Unit
				-2, -20		blank, -25		-3, -30		-4		
				Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>AVQV</sub>	t <sub>ACC</sub>	Address Valid to Output Valid	$\bar{E} = V_{IL}, \bar{G} = V_{IL}$		200		250		300		450	ns
t <sub>ELQV</sub>	t <sub>CE</sub>	Chip Enable Low to Output Valid	$\bar{G} = V_{IL}$		200		250		300		450	ns
t <sub>GLQV</sub>	t <sub>OE</sub>	Output Enable Low to Output Valid	$\bar{E} = V_{IL}$		75		100		120		150	ns
t <sub>EHQZ</sub> <sup>(2)</sup>	t <sub>DF</sub>	Chip Enable High to Output Hi-Z	$\bar{G} = V_{IL}$	0	55	0	60	0	105	0	130	ns
t <sub>GHQZ</sub> <sup>(2)</sup>	t <sub>DF</sub>	Output Enable High to Output Hi-Z	$\bar{E} = V_{IL}$	0	55	0	60	0	105	0	130	ns
t <sub>AXQX</sub>	t <sub>OH</sub>	Address Transition to Output Transition	$\bar{E} = V_{IL}, \bar{G} = V_{IL}$	0		0		0		0		ns

**Notes:** 1. V<sub>CC</sub> must be applied simultaneously with or before V<sub>PP</sub> and removed simultaneously or after V<sub>PP</sub>.  
2. Sampled only, not 100% tested.

**Table 8. Programming Mode DC Characteristics <sup>(1)</sup>**  
 (T<sub>A</sub> = 25 °C; V<sub>CC</sub> = 6V ± 0.25V; V<sub>PP</sub> = 12.5V ± 0.3V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I <sub>LI</sub>	Input Leakage Current	V <sub>IL</sub> ≤ V <sub>IN</sub> ≤ V <sub>IH</sub>		±10	μA
I <sub>CC</sub>	Supply Current			100	mA
I <sub>PP</sub>	Program Current	$\bar{E} = V_{IL}$		50	mA
V <sub>IL</sub>	Input Low Voltage		-0.1	0.8	V
V <sub>IH</sub>	Input High Voltage		2	V <sub>CC</sub> + 1	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA		0.45	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400μA	2.4		V
V <sub>ID</sub>	A9 Voltage		11.5	12.5	V

**Note:** 1. V<sub>CC</sub> must be applied simultaneously with or before V<sub>PP</sub> and removed simultaneously or after V<sub>PP</sub>.

**Table 9. Programming Mode AC Characteristics <sup>(1)</sup>**  
 (T<sub>A</sub> = 25 °C; V<sub>CC</sub> = 6V ± 0.25V; V<sub>PP</sub> = 12.5V ± 0.3V)

Symbol	Alt	Parameter	Test Condition	Min	Max	Unit
t <sub>AVPL</sub>	t <sub>AS</sub>	Address Valid to Program Low		2		μs
t <sub>QVPL</sub>	t <sub>DS</sub>	Input Valid to Program Low		2		μs
t <sub>VPHPL</sub>	t <sub>VPS</sub>	V <sub>PP</sub> High to Program Low		2		μs
t <sub>VCHPL</sub>	t <sub>VCS</sub>	V <sub>CC</sub> High to Program Low		2		μs
t <sub>ELPL</sub>	t <sub>CES</sub>	Chip Enable Low to Program Low		2		μs
t <sub>PLPH</sub>	t <sub>PW</sub>	Program Pulse Width (Initial)	Note 2	0.95	1.05	ms
t <sub>PLPH</sub>	t <sub>OPW</sub>	Program Pulse Width (Overprogram)	Note 3	2.85	78.75	ms
t <sub>PHQX</sub>	t <sub>DH</sub>	Program High to Input Transition		2		μs
t <sub>QXGL</sub>	t <sub>OES</sub>	Input Transition to Output Enable Low		2		μs
t <sub>GLQV</sub>	t <sub>OE</sub>	Output Enable Low to Output Valid			150	ns
t <sub>GHQZ</sub> <sup>(4)</sup>	t <sub>DFP</sub>	Output Enable High to Output Hi-Z		0	130	ns
t <sub>GHAX</sub>	t <sub>AH</sub>	Output Enable High to Address Transition		0		n s

**Notes:** 1. V<sub>CC</sub> must be applied simultaneously with or before V<sub>PP</sub> and removed simultaneously or after V<sub>PP</sub>.

2. The Initial Program Pulse width tolerance is 1 ms ± 5%.

3. The length of the Over-program Pulse varies from 2.85 ms to 78.95 ms, depending on the multiplication value of the iteration counter.

4. Sampled only, not 100% tested.

Figure 6. Programming and Verify Modes AC Waveforms

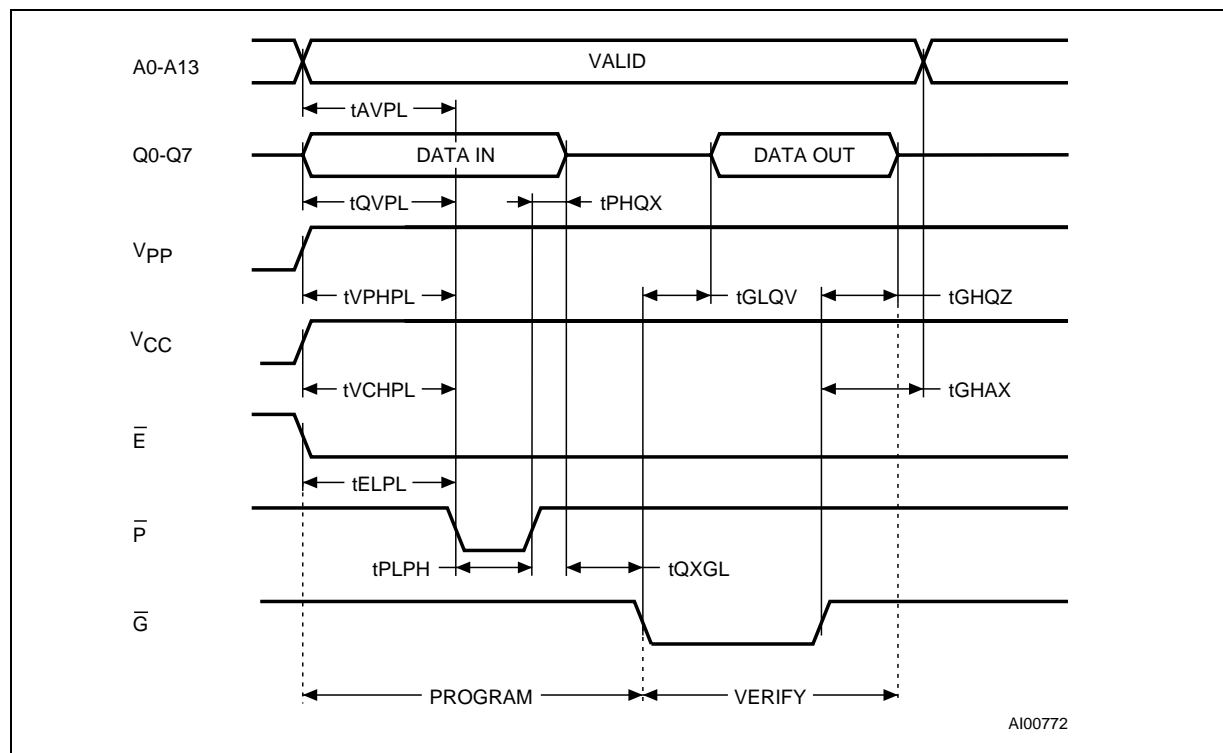
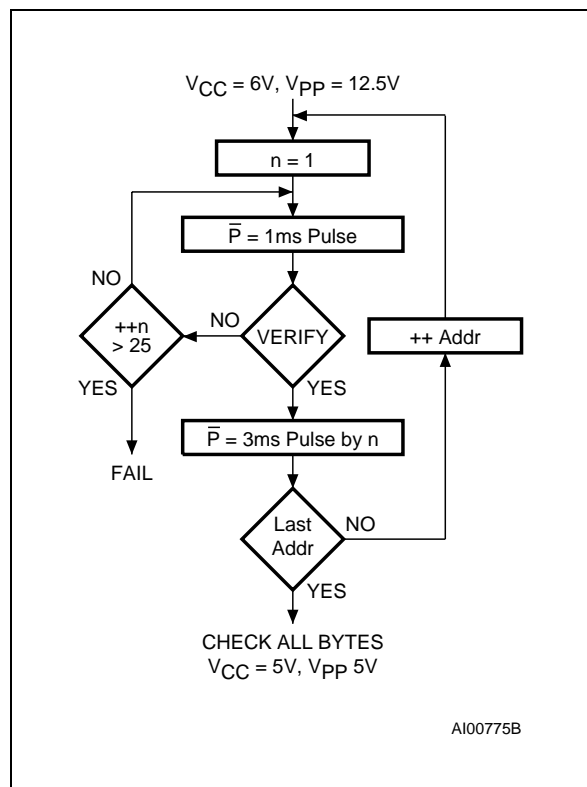


Figure 7. Programming Flowchart

**DEVICE OPERATION** (cont'd)

continually monitored to determine when it has been successfully programmed. A flowchart of the M27128A Fast Programming Algorithm is shown on the last page. The Fast Programming Algorithm utilizes two different pulse types: initial and over-program.

The duration of the initial  $\bar{P}$  pulse(s) is 1ms, which will then be followed by a longer overprogram pulse of length 3ms by n (n is equal to the number of the initial one millisecond pulses applied to a particular M27128A location), before a correct verify occurs. Up to 25 one-millisecond pulses per byte are provided for before the over program pulse is applied.

The entire sequence of program pulses and byte verifications is performed at V<sub>CC</sub> = 6V and V<sub>PP</sub> = 12.5V. When the Fast Programming cycle has been completed, all bytes should be compared to the original data with V<sub>CC</sub> = 5V and V<sub>PP</sub> = 5V.

**Program Inhibit**

Programming of multiple M27128A's in parallel with different data is also easily accomplished. Except for  $\bar{E}$ , all like inputs (including  $\bar{G}$ ) of the parallel M27128A may be common. A TTL low pulse applied to a M27128A's  $\bar{E}$  input, with V<sub>PP</sub> = 12.5V, will program that M27128A. A high level  $\bar{E}$  input inhibits the other M27128As from being programmed.

**Program Verify**

A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with  $\overline{G} = V_{IL}$ ,  $\overline{E} = V_{IL}$ ,  $\overline{P} = V_{IH}$  and  $V_{PP}$  at 12.5V.

**Electronic Signature**

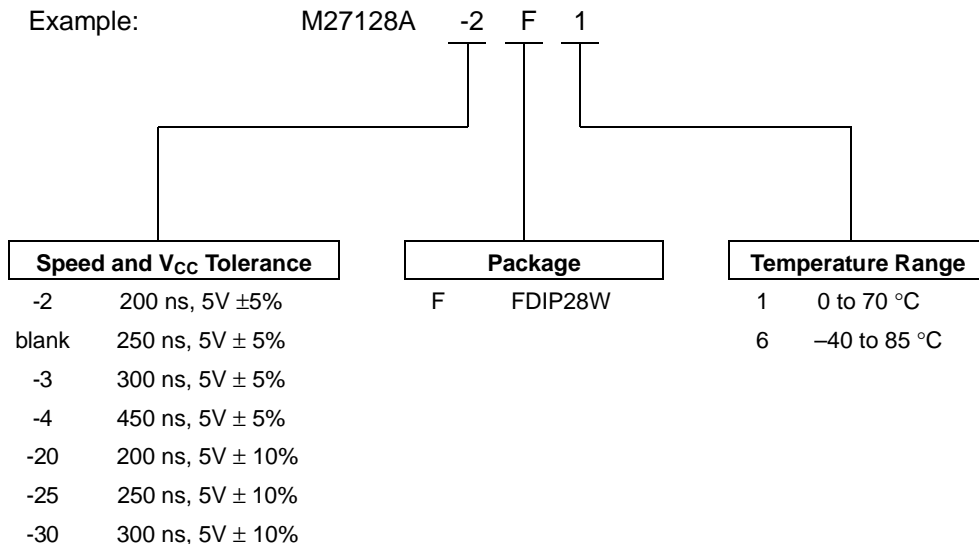
The Electronic Signature mode allows the reading out of a binary code from an EPROM that will identify its manufacturer and type. This mode is intended for use by programming equipment to automatically match the device to be programmed with its corresponding programming algorithm. This mode is functional in the  $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$  ambient temperature range that is required when programming the M27128A.

To activate this mode, the programming equipment must force 11.5V to 12.5V on address line A9 of the M27128A. Two identifier bytes may then be sequenced from the device outputs by toggling address line A0 from  $V_{IL}$  to  $V_{IH}$ . All other address lines must be held at  $V_{IL}$  during Electronic Signature mode. Byte 0 ( $A0 = V_{IL}$ ) represents the manufacturer code and byte 1 ( $A0 = V_{IH}$ ) the device identifier code. For the STMicroelectronics M27128A, these two identifier bytes are given below.

**ERASURE OPERATION (applies to UV EPROM)**

The erasure characteristic of the M27128A is such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Å. It should be noted that sunlight and some type of fluorescent lamps have wavelengths in the 3000-4000 Å range. Research shows that constant exposure to room level fluorescent lighting could erase a typical M27128A in about 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the M27128A is to be exposed to these types of lighting conditions for extended periods of time, it is suggested that opaque labels be put over the M27128A window to prevent unintentional erasure. The recommended erasure procedure for the M27128A is exposure to short wave ultraviolet light which has wavelength 2537 Å. The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm<sup>2</sup>. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 μW/cm<sup>2</sup> power rating. The M27128A should be placed within 2.5cm (1 inch) of the lamp tubes during the erasure. Some lamps have a filter on their tubes which should be removed before erasure.

**ORDERING INFORMATION SCHEME**



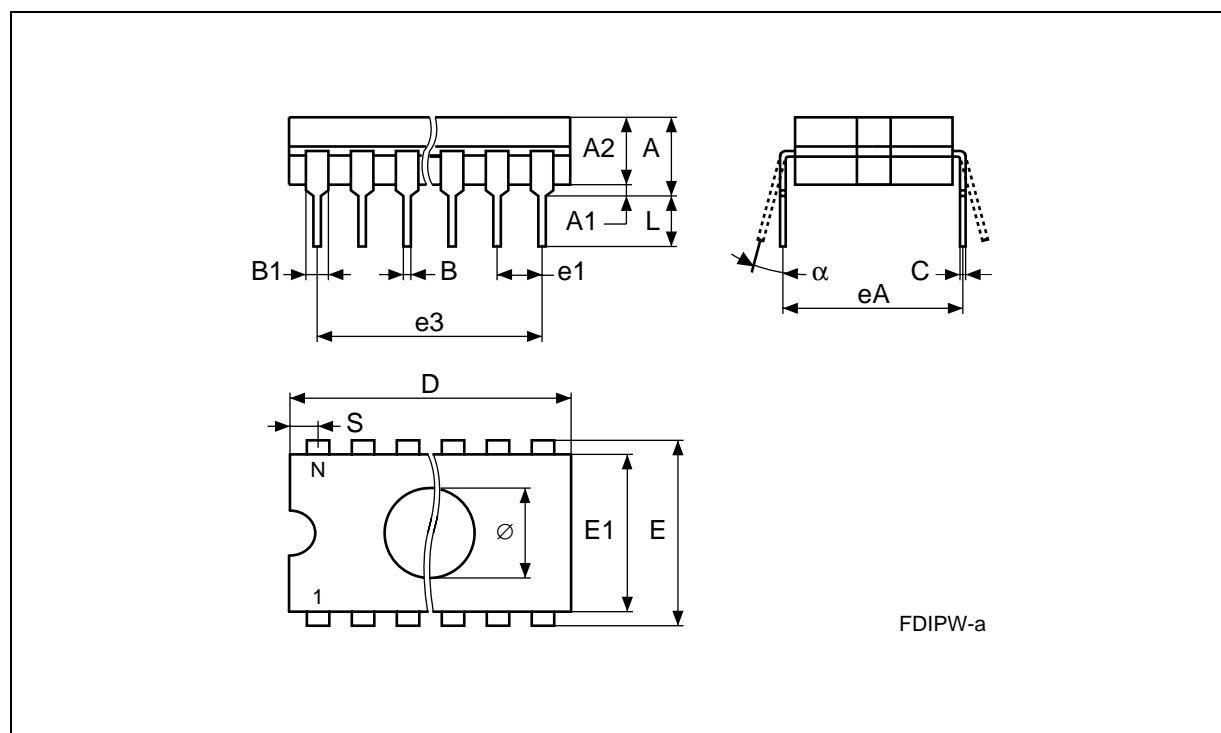
For a list of available options (Speed,  $V_{CC}$  Tolerance, Package, etc...) refer to the current Memory Shortform catalogue.

For further information on any aspect of this device, please contact STMicroelectronics Sales Office nearest to you.



### FDIP28W - 28 pin Ceramic Frit-seal DIP, with window

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			5.71			0.225
A1		0.50	1.78		0.020	0.070
A2		3.90	5.08		0.154	0.200
B		0.40	0.55		0.016	0.022
B1		1.17	1.42		0.046	0.056
C		0.22	0.31		0.009	0.012
D			38.10			1.500
E		15.40	15.80		0.606	0.622
E1		13.05	13.36		0.514	0.526
e1	2.54	–	–	0.100	–	–
e3	33.02	–	–	1.300	–	–
eA		16.17	18.32		0.637	0.721
L		3.18	4.10		0.125	0.161
S		1.52	2.49		0.060	0.098
∅	7.11	–	–	0.280	–	–
α		4°	15°		4°	15°
N	2	8		28		



Drawing is not to scale



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