M28975
ZipWirePlus™ G.shdsl Transceiver with Embedded Microprocessor
Data Sheet

500054D
November 2002

MINDSPEED™

Ordering Information

Marketing Name	Description	Package	Ambient Temperature Range
M28945-33	DSP/Framer	176-pin LQFP 48-pin ETQFP	–40 °C to +85 °C
M28945-13	DSP/Framer	13 × 13 mm FPBGA 48-pin ETQFP	–40 °C to +85 °C
M28927-29	AFE/Line Driver	6 x 6 mm 48-pin ETQFP	–40 °C to +85 °C

Revision History

Revision	Level	Date	Description
A	Advance	June 2000	Initial release.
B	Advance	August 2000	Added copyright information to footer on front page. No technical information was changed.
C	Advance	January 2001	Updated pin-out and description Major overhaul to reflect M28975 functionality
D	Advance	January 2001	Added marketing number to front page. No technical information was changed.
A	Preliminary	May 2001	New document number 500054A. Formerly known as 101083D.
B	Preliminary	October 2001	New document number 500054B. Document 500054B was separated into two documents. This document contains the hardware information. See *M28975 ZipWirePlus G.shdsl Transceiver with Embedded Microprocessor Programmer Reference Manual* for the software information. Deleted LGA package information.
C	Preliminary	November 2002	Removed erroneous operation modes.
D	Preliminary	November 2002	Corrected figures and tables.

Preliminary Information

This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

MINDSPEED™

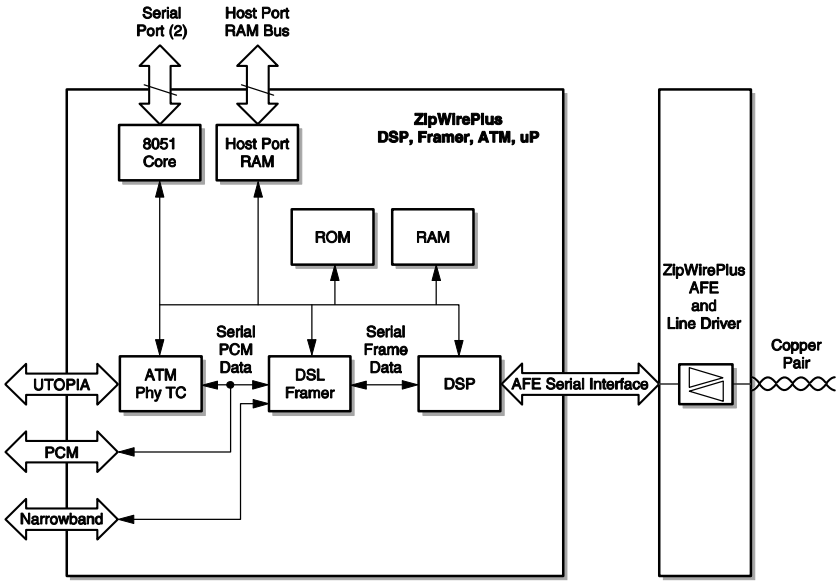
M28975

ZipWirePlus™ G.shdsl Transceiver with Embedded Microprocessor

Multimode Operation: G.shdsl+, HDSL2, SDSL, and HDSL

The ZipWirePlus multimode DSL solution goes beyond simple compliance to the ITU-T G.shdsl standard by supporting the optional Enhanced Performance Asymmetrical PSD (EPAP) mode of operation. In addition, it is compliant with the ANSI HDSL2 standard (ANSI T1.418) and provides interoperability with Mindspeed's market-leading ZipWire transceivers through operation in 2B1Q multirate mode. The 2B1Q mode includes support of AutoBaud for SDSL interoperability, rate optimization and fast connect times, as well as standards-based HDSL operation. The ZipWirePlus also supports Mindspeed's own proprietary modes, like 32-PAM, 64 kbps and 4.6 Mbps operation, which provide enhanced spectral compatibility, extended subscriber line reach, and high-speed operation. All modes are supported by a single hardware circuit (i.e., one transformer, crystal, and hybrid) and can be configured in real time via software control.

Functional Block Diagram



Distinguishing Features

- Highly integrated solution including framer, microprocessor, ROM/RAM, frequency synthesizer, DSP, AFE, and line driver
- Multimode operation including:
  - ITU-T G.shdsl including EPAP modes (ITU-T G.991.2)
  - ITU-T G.handshake (ITU-T G.994.1)
  - HDSL2 (ANSI T1.418)
  - SDSL/2B1Q (AutoBaud)
  - HDSL (ITU-T G.991.1, ETSI 101 135 and ANSI TR-28)
  - Proprietary/Extended Reach (ANSI spectrum management for loop transmission systems)
  - Proprietary/High-Speed (ANSI spectrum management for loop transmission systems)
- Low power consumption
- Two packaging options for high density and manufacturability
  - DSP/Framer = 176-pin LQFP; AFE/LD = 48-pin ETQFP
  - DSP/ Framer = 13 x 13 FPBGA; AFE/LD = 48-pin ETQFP
- Embedded microprocessor for autonomous operation and EOC processing
- Data rates from 64 kbps to 4.6 Mbps in 8 kbps increments
- Interoperable with ZipWire 2B1Q transceivers including AutoBaud
- Simultaneous operation of UTOPIA Level 2 and PCM interfaces
- Central office (COT) and remote (RT) operation
- Glueless interface to popular microprocessors
- Single hardware circuit supports all speeds and modes of operation
- +1.8 V, +3.3 V, and +12 V power supplies
- JTAG boundary scan
- Operation over full industrial temperature range (–40 to +85 °C)

Embedded Microprocessor

The ZipWirePlus chip set includes an embedded microprocessor and a full suite of software that facilitate speedy and simplified development of systems compliant with all applicable ITU, ANSI, and ETSI standards. The embedded microprocessor and software handle the EOC processing and many other functions often delegated to an external host controller in competing solutions, greatly reducing software porting efforts and eliminating real-time processing requirements for an external host controller. The host controls the ZipWirePlus through a simple and well-defined software API common to all devices in the ZipWire family.

Integrated Line Driver and Frequency Synthesizer

The ZipWirePlus includes an integrated line driver and frequency synthesizer to provide a full DSL solution. The integrated line driver can drive the high line power Enhanced Performance Asymmetrical PSDs for payload rates of 768, 1544, 2048, and 2304 kbps in accordance with the G.shdsl standard. The frequency synthesizer, along with the rest of the ZipWirePlus, supports data rates from 64 kbps to 4.6 Mbps, and requires only one external crystal. This highly integrated DSL solution enables OEMs to design and manufacture the most feature-rich, lowest power, and highest density DSL equipment in the industry.

Note:

- The M28975-13 chipset consists of the M28945-13 (CABGA package) plus integrated AFE/LD M28927-29.
- The M28975-33 chipset consists of the M28945-33 (LQFP package) plus integrated AFE/LD M28927-29.
- These devices are all part of the ZipWirePlus family of single channel SHDSL transceivers and are ordered separately.

Applications

- DSL-enabled Customer Premise Equipment (CPE)
- Integrated Access Devices (IADs)
- Digital Subscriber Line Access Multiplexers (DSLAMs)
- N-Channel DAML and Voice Pairgain Systems
- N x 64 K Data Transport
- Remote LAN Access
- T1 and E1 HDSL-enabled Transport Systems
- Cellular Base Station Data Links
- Campus Modems
- Data, Voice, and Video Transport Systems

Contents

Figures

Tables

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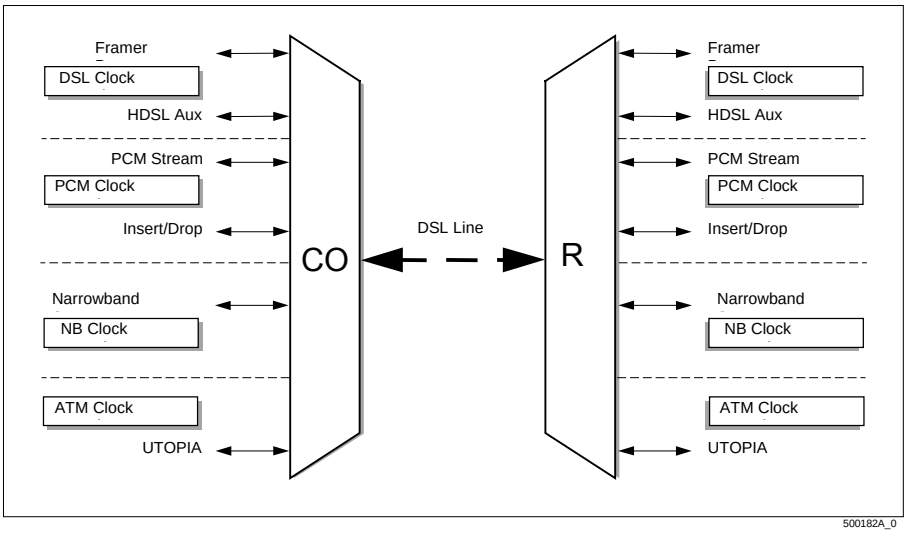
1.0 System Overview

1.1 Introduction

For most applications, the ZipWirePlus chip set can be viewed as a pair of wires: The data comes in on one terminal unit and goes out the far-end terminal unit. Figure 1-1 illustrates the ZipWirePlus data interfaces. The DSL auxiliary interface operates at the DSL line rate. The PCM and Insert/Drop interfaces operate at the PCM clock rate. The narrowband (NB) interface operates at the narrowband clock rate. The UTOPIA interface operates at the UTOPIA clock rate. The DSL line interfaces to the physical twisted pairs.

Figure 1-1. High Level Functional Diagram

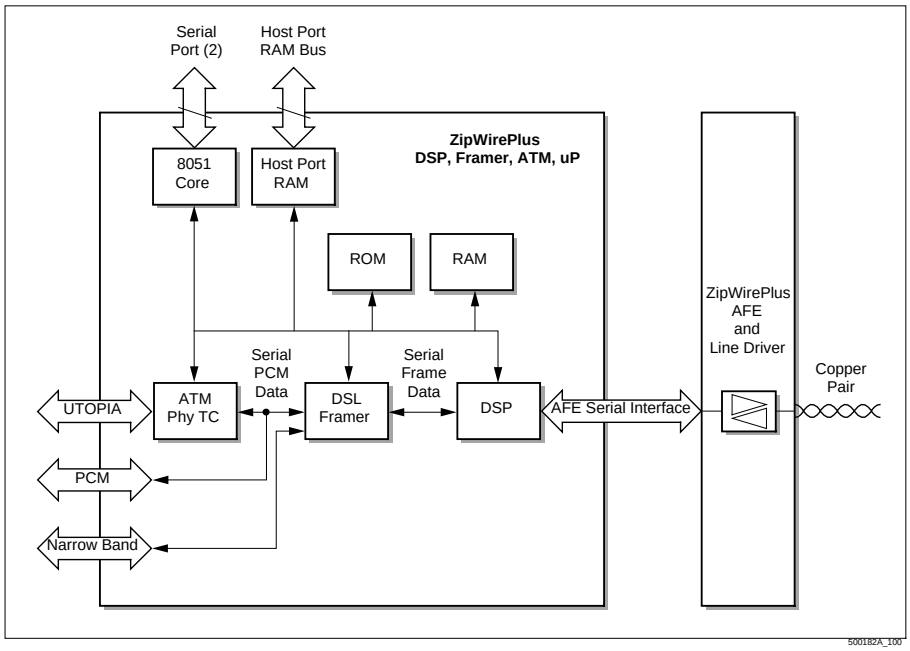


1.2 ZipWirePlus Transceiver/Framer Functional Summary

Figure 1-2 illustrates a detailed block diagram of the ZipWirePlus Transceiver/ Framer. The ZipWirePlus 8051 embedded processor core contains an internal boot-up ROM, execution program RAM (PRAM), data storage RAM, and address decoding logic. The internal 8051 performs transceiver startup, DSL framer overhead management, interrupt handling, and other functions.

A full-featured API command set allows the user to configure the ZipWirePlus system, query for status, execute loopbacks and test modes, and dictate the program flow.

Figure 1-2. ZipWirePlus Transceiver/Framer Detailed Block Diagram



1.2.1 ZipWirePlus Microprocessor Functional Summary

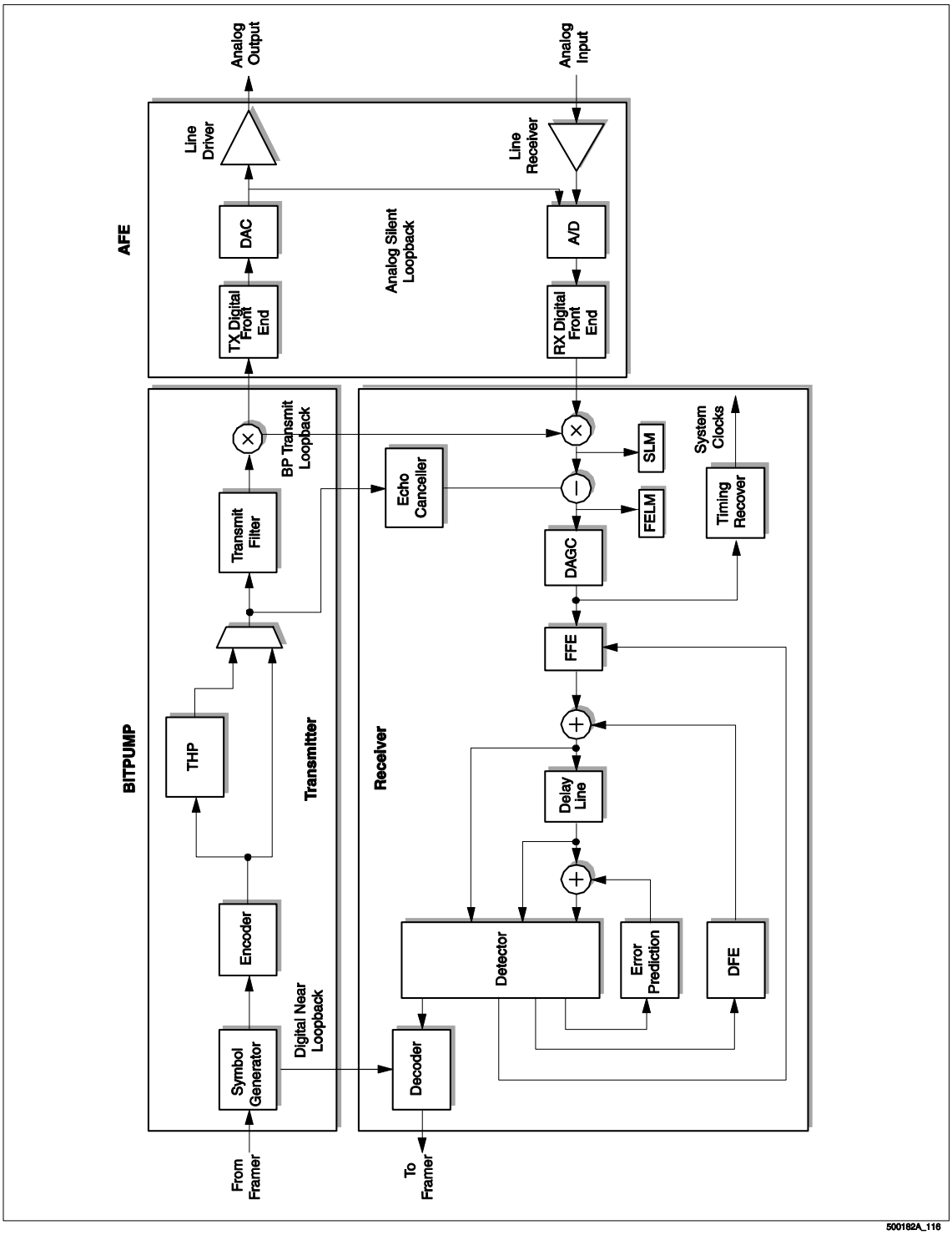
- The ZipWirePlus Transceiver/Framer has a built-in 8051 microprocessor core with the following features:
- Internal 256 bytes of direct, indirect, and bit-addressable RAM
- Internal 2 kB boot ROM
- Internal 8 kB data RAM
- Dual-port 1 kB host interface RAM
- Two asynchronous serial (RS-232) interfaces
- Internal 64 kB Program RAM. During boot load sequence the lower 2 K and upper 1 K are inaccessible because RAM and ROM, respectively, are overlaid.
- Three internal timers/counters
- Supports dual data pointers
- Executes instruction cycles in four clock cycles
- Operates at ~22 MHz

1.2.2 ZipWirePlus DSP Functional Summary

Figure 1-3 illustrates the ZipWirePlus Transceiver/DSP section. The transmitter receives a bit stream from the DSL framer and maps the data bits to the appropriate Pulse Amplitude Modulation (PAM) symbols. An optional Tomlinson-Harashima precoder (THP) follows the PAM mapper. The signal is then processed by the transmit filter to achieve the desired time and/or frequency domain characteristics before being forwarded to the Analog Front End (AFE).

The receiver receives serialized data from the AFE device and from precoded symbols from the bit pump transmitter. The precoded symbols feed into an Echo Canceller (EC) that estimates the echo response and subtracts it from the AFE samples. The signal is equalized using a Feed Forward Equalizer (FFE) and a Decision Feedback Equalizer (DFE). Finally, a Trellis Coded Modulation (TCM) decoder recovers the information bits. An error predictor is used as a part of the startup algorithm and as a precoder coefficient adaptation machine during normal operation.

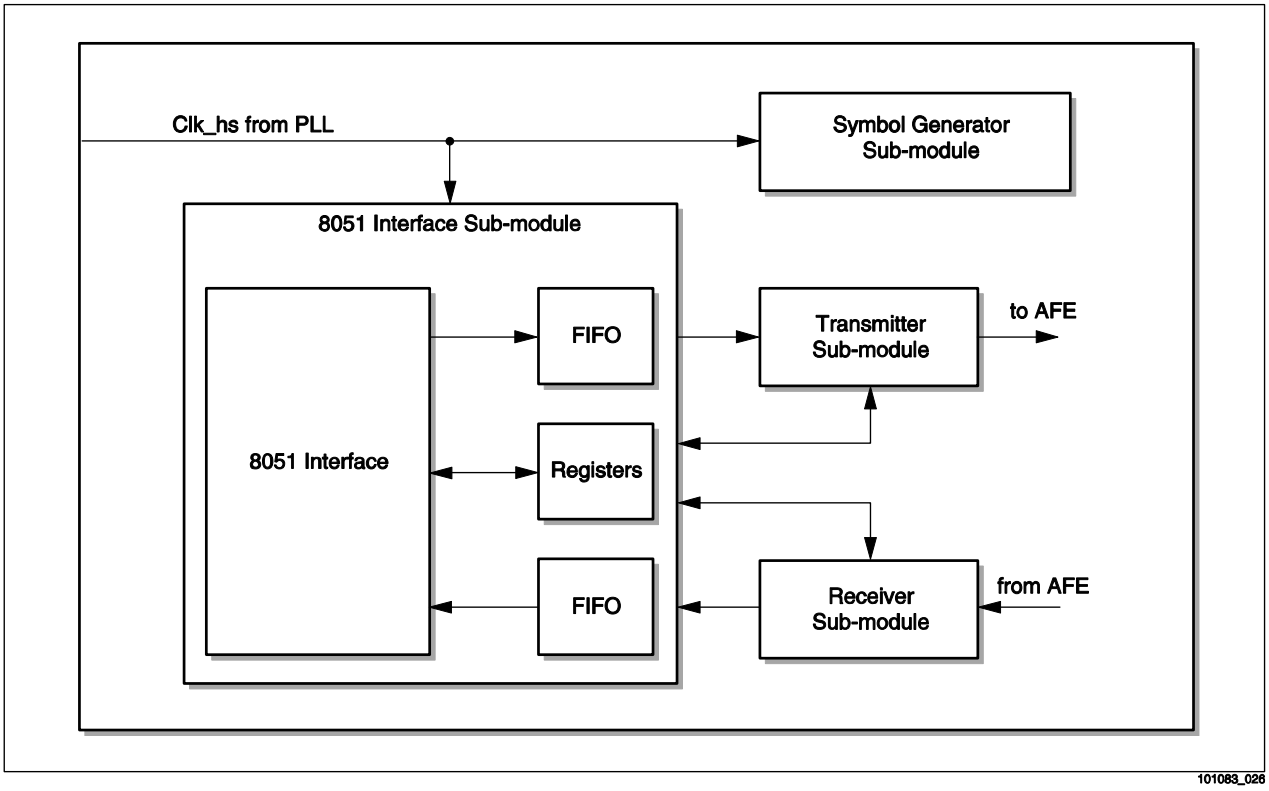
Figure 1-3. ZipWirePlus DSP Detailed Block Diagram



1.2.3 ZipWirePlus G.hs Functional Summary

Figure 1-4 illustrates the ZipWirePlus G.hs section. The G.hs block implements the G.994.1 handshaking function. The handshaking function provides a flexible mechanism for DSL transceivers to communicate before exchanging signals that are specific to a particular DSL recommendation or standard. The G.994.1 standard defines the signals, messages, and procedures for exchanging information about the capabilities of each transceiver and for selecting common modes of operation. This block implements a DPSK modem that operates at a symbol rate of 800 symbols/second. This block has interfaces to the 8051 microcontroller, the AFE, and the PLL block.

Figure 1-4. G.handshake Block Diagram

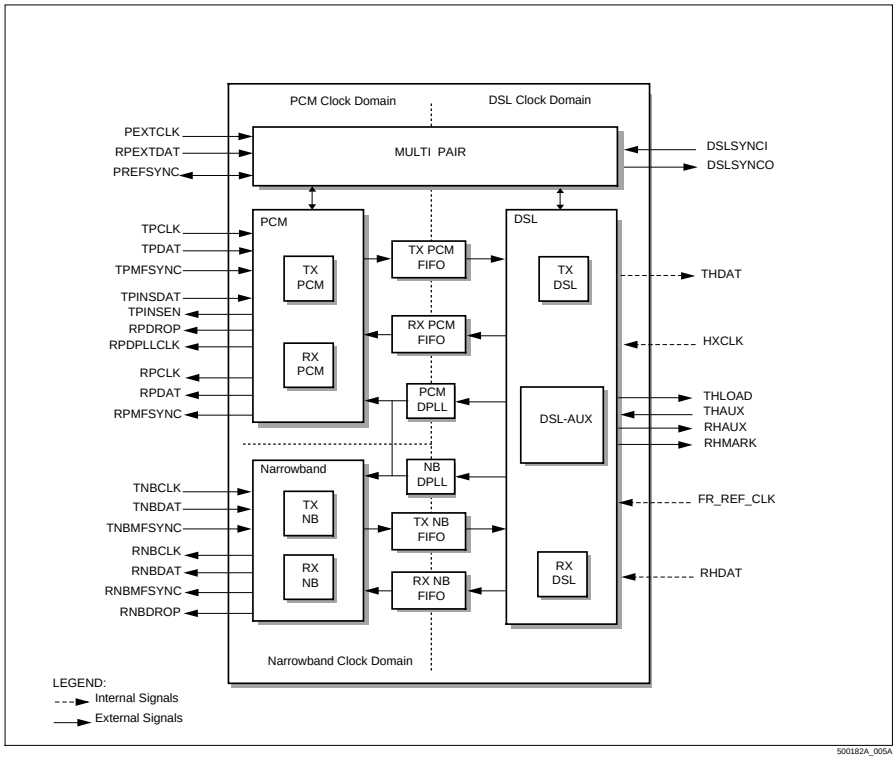


1.2.4 ZipWirePlus DSL Framer Functional Summary

Figure 1-5 illustrates the ZipWirePlus DSL framer section. The DSL framer supports G.shdsl, HDSL2, HDSL1, RADSL, and custom frame structure applications. The DSL framer provides clock, data, and frame format conversion from various PCM frame formats to various DSL applications. The DSL framer supports multi-pair configuration such as T1 two loops, E1 two and three loops, or any point-to-multipoint (P2MP) application by cascading several DSL framers. The DSL framer provides full PCM termination capabilities, including synchronization and management of E1 PRA and T1. A second independent PCM interface (narrowband) is provided to support multiservice applications. The DSL rate can vary from 64 kbps to 4.640 Mbps (2 x E1 + overhead), and the PCM rate can vary from 64 kbps up to 16.384 Mbps (8 x E1) and any custom PCM rate and frame format within this range.

The ZipWirePlus DSL framer can be configured to provide T1 path termination capabilities and thereby eliminate the need for an external T1 framer in some applications. In particular, the ZipWirePlus DSL framer is capable of generation and insertion of T1 overhead in the transmit direction as well as alignment and checking of T1 overhead in the receive direction.

Figure 1-5. DSL Framer Detailed Block Diagram

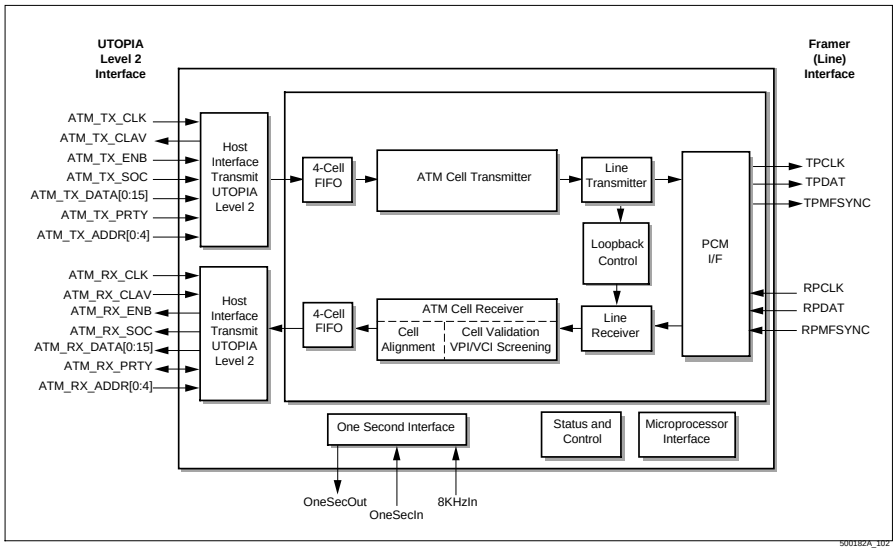


1.2.5 ZipWirePlus ATM PHY Transmission Convergence Functional Summary

Figure 1-6 illustrates the ZipWirePlus ATM Physical Layer (PHY) Transmission Convergence (TC) section. The ATM PHY supports data rates ranging from 64 kbps to 50 Mbps. A UTOPIA Level 2 multi-PHY interface connects the ZipWirePlus to the host switch or terminal system. The ATM PHY performs all cell alignment functions on the bit stream. This gives system designers a simple, modular, and low-cost architecture for supporting all UNI and NNI ATM interfaces.

NOTE: The ATM PHY TC block is a single block of Mindspeed's RS8228 octal TC PHY device.

Figure 1-6. ATM PHY TC Functional Block Diagram

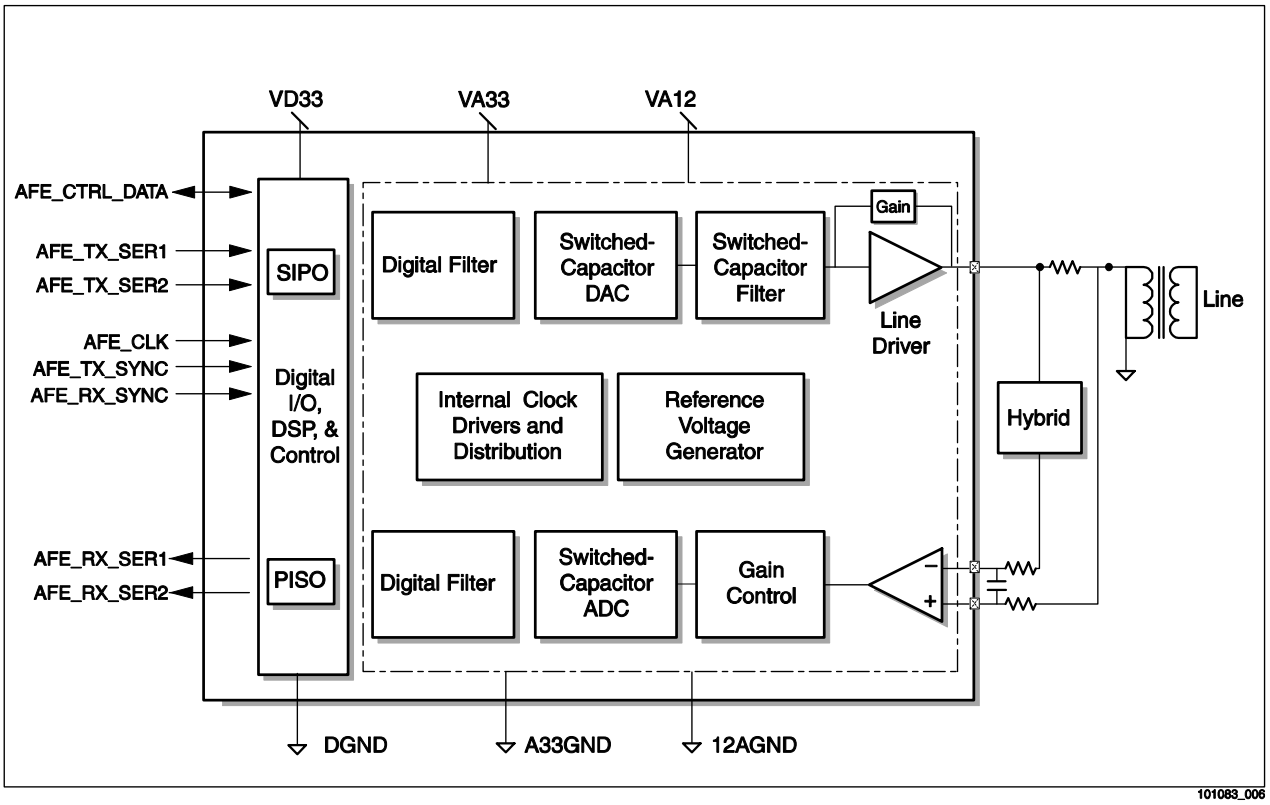


1.3 ZipWirePlus AFE Functional Summary

Figure 1-7 illustrates the ZipWirePlus AFE. The ZipWirePlus AFE performs the analog functions required for transmission and reception of G.shdsl, EPAP, OPTIS, or 2B1Q line-coded signals. The ZipWirePlus AFE includes the Digital-to-Analog (D/A) and Analog-to-Digital (A/D) data converters, anti-aliasing and post filtering circuitry, gain control blocks, and line drivers.

The ZipWirePlus AFE serial digital interface connects to the ZipWirePlus Transceiver/Framer. The serial interface protocol is proprietary. The DSP transceiver indirectly controls the AFE. The AFE interface consists of the line driver, impedance-matching resistors, external hybrid, and transformer.

Figure 1-7. ZipWirePlus AFE Block Diagram

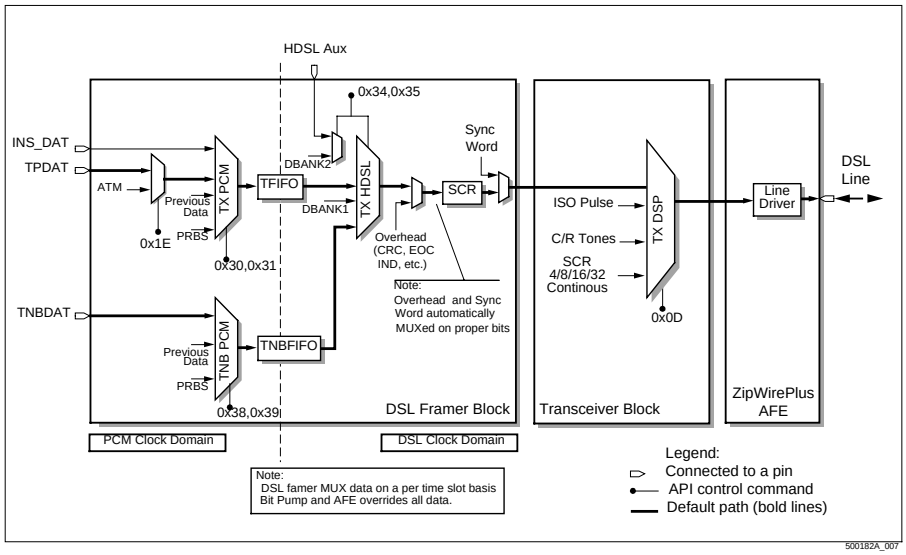


1.4 ZipWirePlus Transmit Data Path

Figure 1-8 illustrates the input data sources available to be transmitted over the ZipWirePlus link. This drawing includes all external inputs, as well as internally generated data sources.

NOTE: This figure does not show loopbacks.

Figure 1-8. Detailed Transmit Data Path Block Diagram



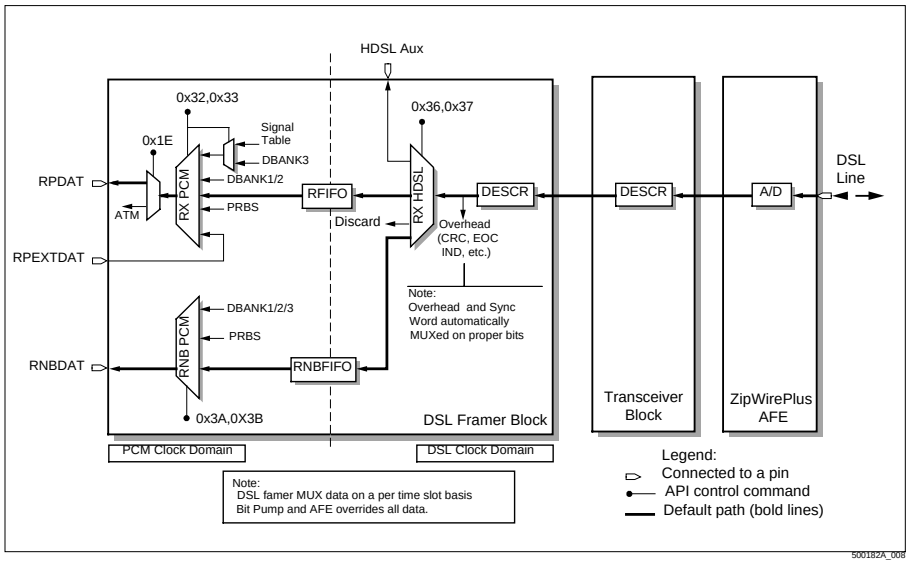
1.5 ZipWirePlus Receive Data Path

NOTE: This figure does not show loopbacks.

Figure 1-9 illustrates the data paths received from the ZipWirePlus link. This drawing includes all external inputs, as well as internally generated data sources.

NOTE: This figure does not show loopbacks.

Figure 1-9. Detailed Receive Data Path Block Diagram



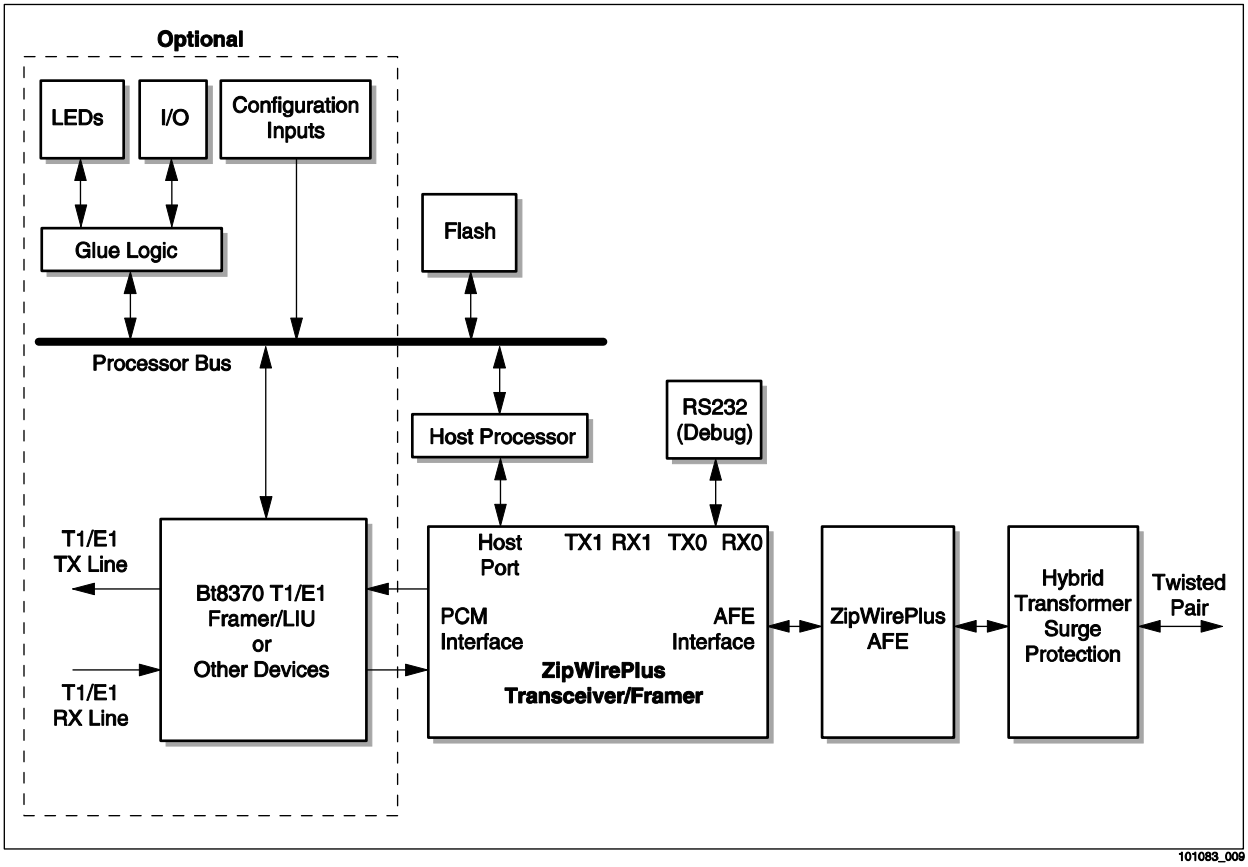
2.0 Application Interfaces

This section illustrates various application configurations. Each figure illustrates different interface configurations.

2.1 Single Device Configurations

Figure 2-1 illustrates the configuration for a single device ZipWirePlus system.

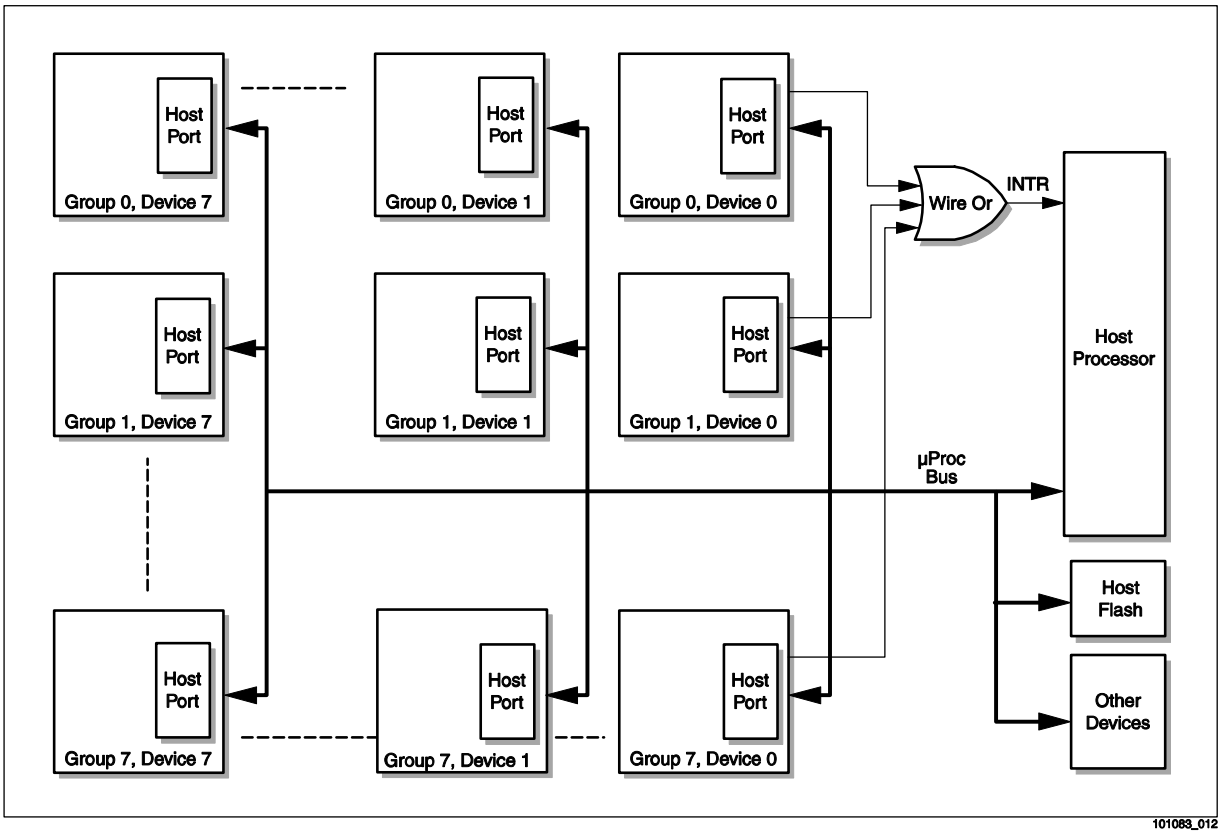
Figure 2-1. Single Pair Hardware Configuration Using Host Port



2.2 Multidevice Configurations

Figure 2-2 illustrates the hardware configuration when the host processor is connected directly to the host port of the ZipWirePlus.

Figure 2-2. Master Multipair Hardware Configuration



2.3 Multipair DSL Framer Configuration

The DSL Framer PCM bus operates up to 16 MHz by cascading multiple ZipWirePlus devices. Multipair configuration is necessary to support several applications: Point-to-Multipoint, T1 transport over two HDSL1 wire pairs (Bellcore standard), and E1 transport using two or three HDSL1 wire pairs (ETSI standard). Several cascading DSL framers support these applications.

The following pins are used in cascade mode: DSLSYNCI, DSLSYNCO, PEXTCLK, and RPEXTDAT.

Two options can be used to implement multipair configuration:

- PCM Bused (see Figure 2-3) enables the connection of an unlimited number of framers to receive the PCM highway interface in which each framer contributes and routes different time slots to and from the PCM highway. In this option, none of the framers carry a complete PCM frame; therefore, PCM framing termination (PRA) is not feasible.
- PCM Cascade (see Figure 2-4) enables transmit and receive PCM framing (PRA) by routing the receive PCM frame data from DSL framers 2 and 3 to DSL framer 1 (master) using the RPEXTDAT pin. This configuration is limited to three DSL framers.

In the transmit path direction, both configuration options behave the same and have the same capability.

The transmit PCM signal (clock, data, and sync) connects to the transmit PCM pins of each DSL framer while each framer is programmed independently to route any incoming PCM data combination to the DSL channel.

In the receive path, the master framer aligns the slaves (DSL framer 2 and DSL framer 3) receive PCM time base using the PREFSYNC bi-directional pin. The recovered PCM clock is then provided to the slave framers using RPCLK and PEXTCLK pins. This capability enables the generation of a common receive PCM time base for all DSL framer receive channels and reliably reconstructs the PCM frame.

The active DPLL (typically located in the master framer) is able to select any DSL frame reference (for the DPLL phase detector) using DSLSYNCI and DSLSYNCO pins. This allows the master to switch DSL reference sources when the selected pair becomes inactive (DSL loss-of-signal detection).

Figure 2-3. Multipair Configuration—PCM Bused

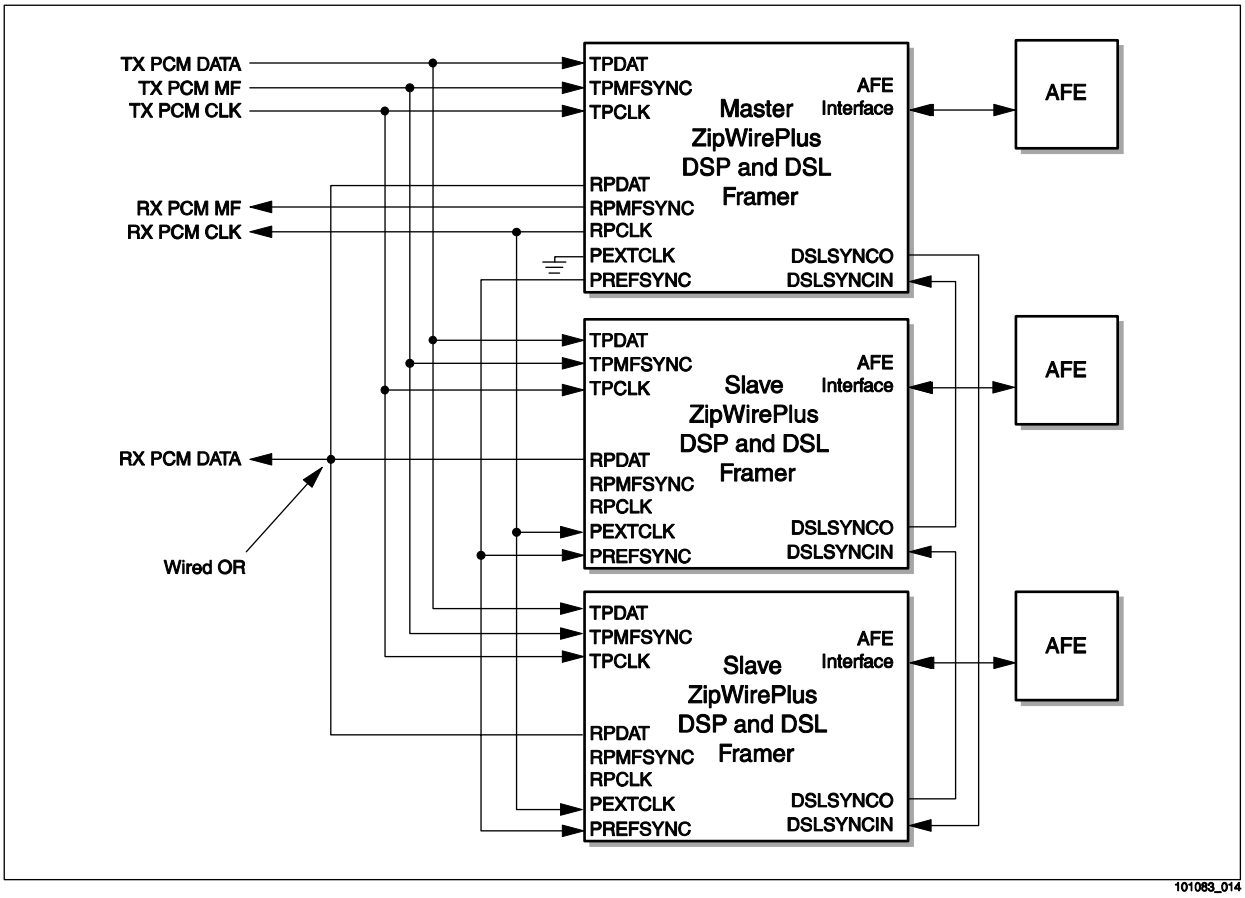
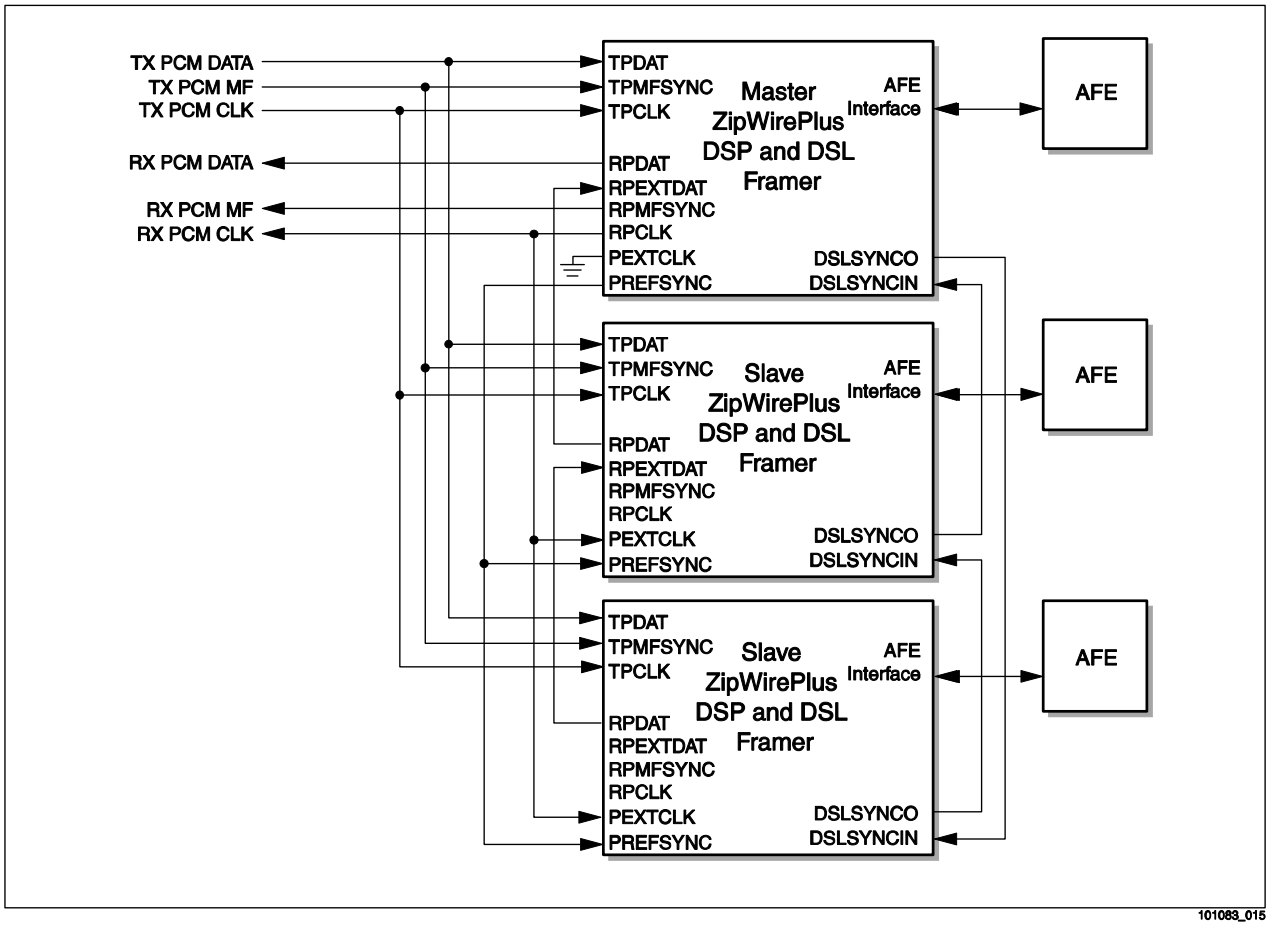


Figure 2-4. Multipair Configuration—PCM Cascade



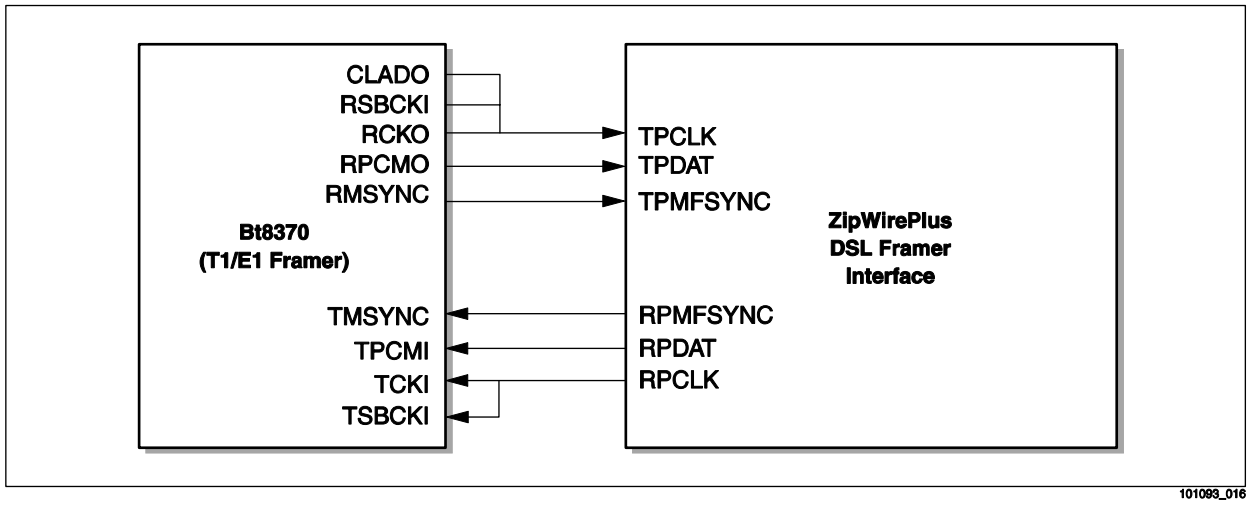
2.4 Framer Transparent Mode

Framer transparent mode would be required when the system needs to support interoperability with legacy SDSL (2B1Q) applications that do not use the DSL framer. When the DSL framer is configured to transparent mode, the data passes through the framer without adding any overhead. To configure the DSL framer for transparent mode, the frame structure parameter in the DSL_SYSTEM_CONFIG API (Opcode 0x06) should be set to _TRANSPARENT_FORMAT (value 0x05).

2.5 ZipWirePlus Transceiver/Framer to Bt8370 T1/E1 Interface

Figure 2-5 illustrates one possible configuration for the ZipWirePlus Transceiver/ Framer to Bt8370 T1/E1 Interface.

Figure 2-5. ZipWirePlus Transceiver/Framer to Bt8370 T1/E1 Interface

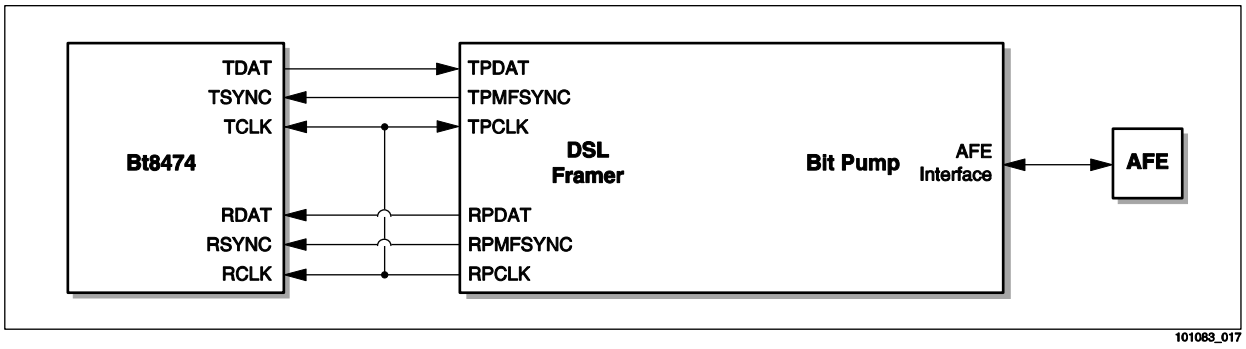


2.6 DSL Framer to Bt8474 Interface

Figure 2-6 illustrates the connection of the ZipWirePlus device to the Bt8474 device when using the ZipWirePlus DSL Framer block. In an HTU-C (central office) application, the DSL framer DPLL is programmed to open loop mode to provide the clock reference. In an HTU-R (remote terminal) application, the DSL framer DPLL is programmed to closed loop mode to recover the PCM clock reference from the HTU-C. The DSL framer generates the transmit and receive multiframe synchronization reference and feeds it to the Bt8474 device. The multiframe synchronization signals are only required in channelized applications where individual time slots are sourced from different devices.

Figure 2-6 illustrates a one-port connection.

Figure 2-6. DSL Framer to Bt8474 Interface Diagram



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3.0 ZipWirePlus Clocking Architecture

3.1 Clocking Architecture Overview

The M28975 provides a flexible clocking architecture to support a number of applications defined by various standards such as G.shdsl, HDSL2, HDSL1, SDSL. Table 3-1 lists the supported clocking modes. In general, the HTU-C clocking architecture must support the different modes while the HTU-R clock reference is derived from the received symbol clock. HTU-C clocking modes are described in Section 3.2 while HTU-R clocking modes are described in Section 3.3.

Table 3-1. Clocking Modes

Mode #	Mode Name	HTU-C Clock Reference	Application
1	Plesiosynchronous	Local oscillator (free running)	Classic HDSL
2	Plesiosynchronous with timing reference	Network reference clock	Classic HDSL
3	Synchronous	Transmit data clock or network reference clock	—
4	Hybrid	Transmit data clock	Downstream is synchronous while upstream is plesiosynchronous.

3.1.1 M28975 Clocking Architecture Implementation

Figure 3-1 illustrates the M28975 clock tree distribution. The on-chip clock synthesizer (PLL) block is responsible for generating the DSP, microprocessor, AFE, DSL framer, and ATM reference clocks. The ZipWirePlus DSL framer has two independent DPLLs to generate PCM and NB clocks. The on-chip clock synthesizer can operate in free running network timing reference, or HTU-R DSL/G.hs timing recovery mode. In free running mode, the ZipWirePlus clock synthesizer operates at the crystal (or local clock) phase offset. In network timing reference mode, the ZipWirePlus clock synthesizer will phase-lock its timing to the external reference clock. The external reference clock can be sourced from EXT_CLK_REF pin or the internal i_TPCLK signal. In HTU-R DSL/G.hs timing recovery mode, the

ZipWirePlus clock synthesizer will phase-lock its timing to the far end modem (HTU-C) via the G.hs or DSL signal.

Figure 3-1. M28975 Clock Tree Distribution

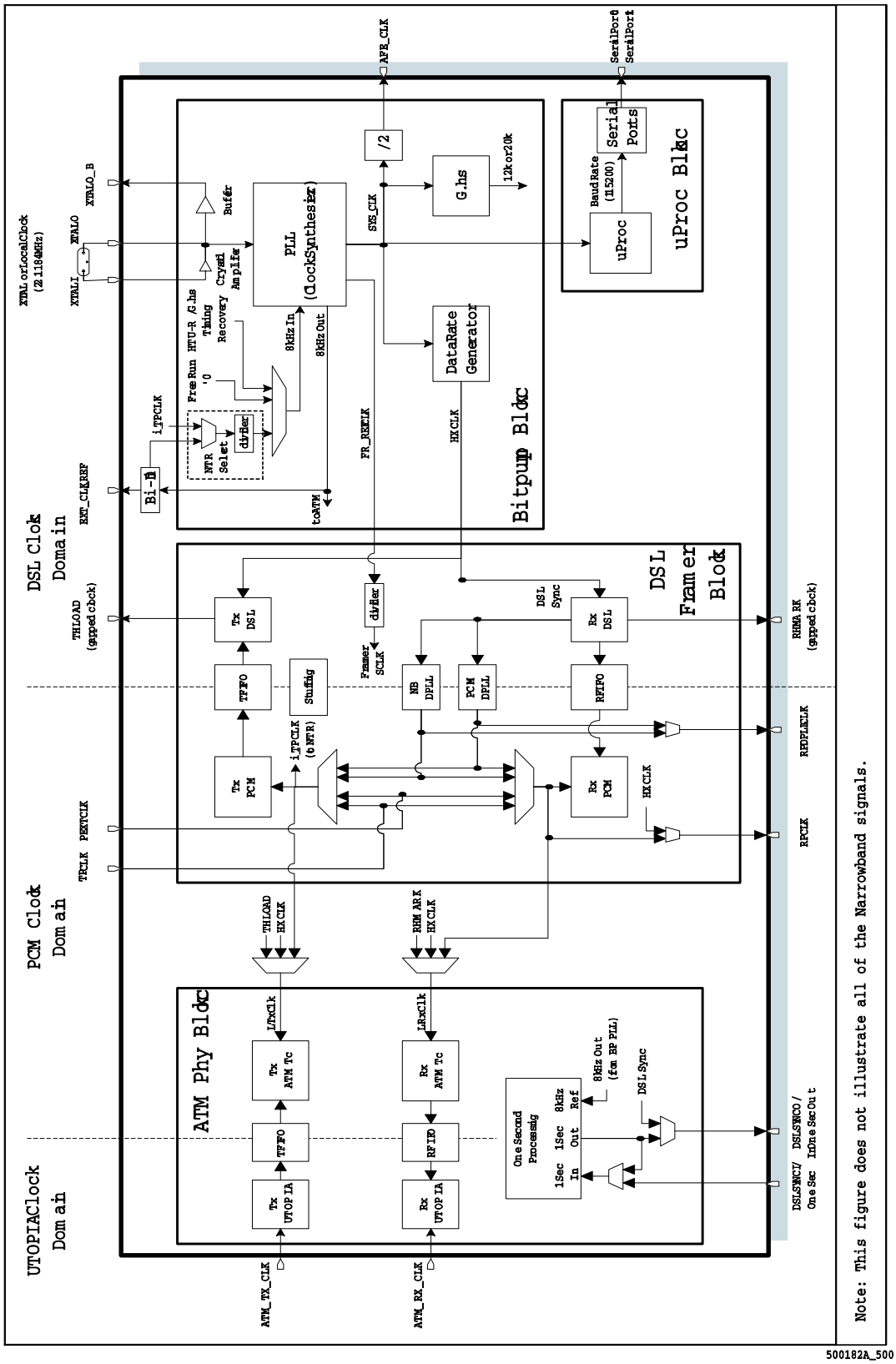


Table 3-2. ZipWirePlus Clocks

Clock	Frequency	Description
Crystal	22.1184 MHz	External crystal or clock input
XTALI / XTALO	22.1184 MHz	Crystal input/output
XTALO_B	22.1184 MHz	Buffered crystal output
EXT_CLK_REF (Input)	8 kHz–18.432 MHz	Bidirectional network timing reference clock
EXT_CLK_REF (Output)	8 kHz	Bidirectional network timing reference clock
8 kHz In	8 kHz	Internal 8 kHz input derived from EXT_CLK_REF
8 kHz Out	8 kHz	Internal 8 kHz output from PLL. Derived from 8 kHz (see Figure 3-1) when HTU-C or recovered from DSL line when HTU-R. Routed to ATM block and EXT_CLK_REF output.
SYS_CLK	43–53 MHz	Internal DSP system clock
AFE_CLK	SYS_CLK / 2	AFE clock reference
G.hs Clock	12 kHz or 20 kHz	G.hs clock – 12 kHz (HTU-R) or 20 kHz (HTU-C)
Baud Rate	115200	Baud rate that controls serial ports 0 and 1
HXCLK	64 k –4640 kbps	Data rate clock output

3.2 HTU-C Clocking Modes

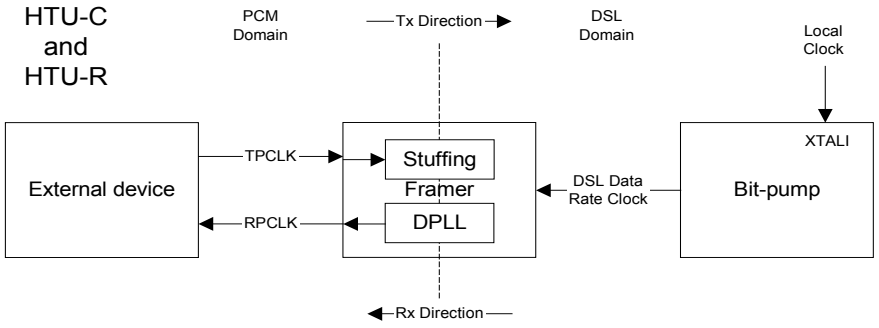
This section describes how the various clocking modes are targeted for HTU-C applications.

3.2.1 Plesiosynchronous Mode

Figure 3-2 illustrates the plesiosynchronous-clocking mode. In this mode, the transmit PCM clock and DSL clock operate independently (within appropriate PPM tolerance) and do not have any phase relationship with respect to each other. The stuffing generator is used to compensate for any phase differences between the PCM and DSL clock domains. The HTU-C locks the DSL clock to a local clock or oscillator. The transmit PCM clock (TPCLK) signal can be generated by an external device such as the Bt8370 (T1/E1 framer) or can be sourced from the PCM DPLL when operating in open loop mode. The transmit PCM and receive PCM clocks can operate at independent rates within the appropriate PPM tolerance. T1/E1 transport applications use this mode.

NOTE: Figure 3-2 applies to both the HTU-C and HTU-R.

Figure 3-2. Plesiosynchronous Mode Block Diagram

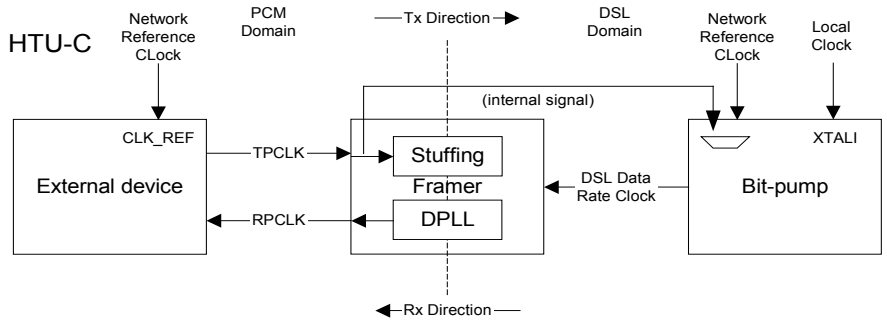


3.2.2 Plesiosynchronous Mode with External Clock Reference

Figure 3-3 illustrates the plesiosynchronous mode with external reference clock. This mode is similar to plesiosynchronous mode except that the HTU-C locks the DSL clock to an external reference clock, either from a network reference clock or the transmit PCM clock.

If the external reference clock is sourced from the TPCLK pin, the DSL and PCM clock domains are synchronized. However, the stuffing generator is still used and is therefore a slightly different configuration than the synchronous modes described in Section 3.2.3. This configuration is used when the transmit PCM clock is locked to a network reference clock and the DSL clock needs to be synchronized to the network reference clock via the transmit PCM clock.

Figure 3-3. Pesiosynchronous Mode Block Diagram



3.2.3 Synchronous Mode

In the synchronous mode, the DSL and PCM clock domains are synchronized. The stuffing generator is therefore disabled. The synchronous mode can be achieved in two following ways:

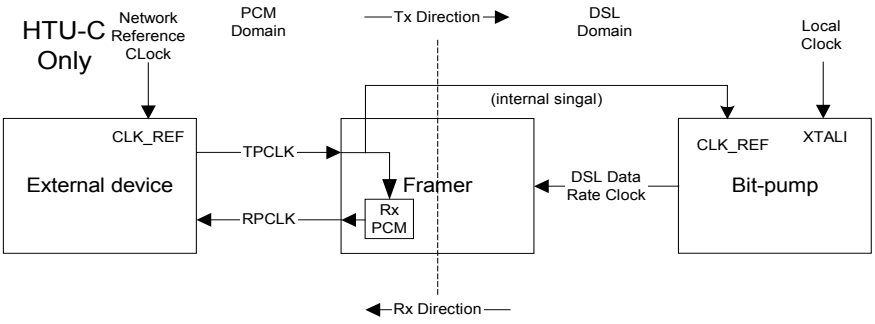
Synchronous Slave Transmit Data Clock

Synchronous Master Transmit Data Clock

3.2.3.1 Synchronous Slave Transmit Data Clock

Figure 3-4 illustrates the slave transmit data clock mode. In this configuration, the M28975's transmit PCM clock is slaved off of an external device. In this mode, the HTU-C locks the DSL clock to the transmit PCM clock (TPCLK). The transmit PCM clock (TPCLK) and receive PCM clock (RPCLK) are both sourced (slaved) from the TPCLK input pin. The TPCLK must be supplied from an external source. The PCM DPLL is disabled.

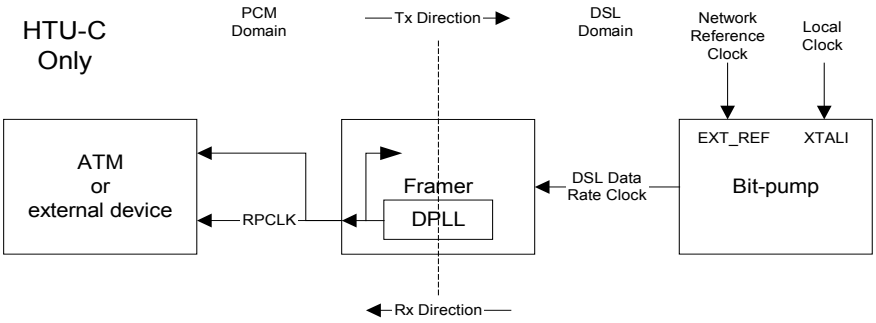
Figure 3-4. Synchronous Slave Transmit Data Clock



3.2.3.2 Synchronous Master Transmit Data Clock

Figure 3-5 illustrates the master transmit data clock mode. In this configuration, the M28975 is the PCM clock master. Any external device needs to be slaved to the M28975 clocks. The DSL clock domain is synchronized to the local oscillator or the external network reference clock. The transmit PCM clock (TPCLK) and receive PCM clock (RPCLK) are then synchronized with the DSL clock using the PCM DPLL.

Figure 3-5. Synchronous Master Transmit Data Clock



3.3 Clocking Modes for HTU-R Applications

This section describes how the various clocking modes are targeted for HTU-R applications. In general, the HTU-R will recover the DSL, PCM, and network references clocks from the incoming DSL line. The PCM clock can operate in looped timed or independent transmit/receive PCM clock modes. The network reference clock output is optional.

NOTE: When operating as an HTU-R, the device can support all of the HTU-C clocking schemes but the HTU-C modes are not required in most applications.

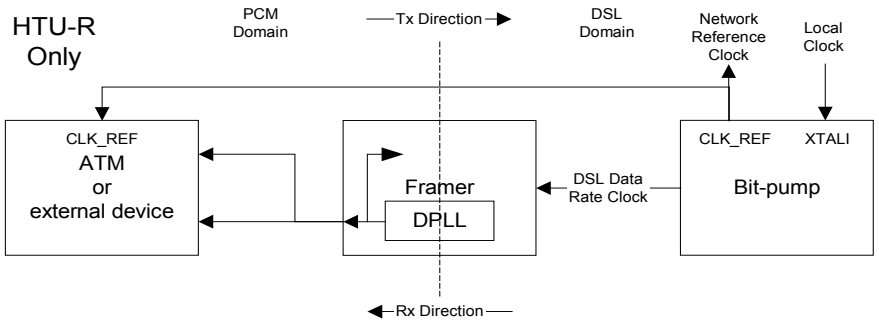
3.3.1 Independent Transmit/Receive PCM Clocks

The transmit PCM and receive PCM clocks can operate at independent rates within the appropriate PPM tolerance. This mode is the same as the HTU-C plesiosynchronous mode. See Section 3.2.1 for details and block diagram.

3.3.2 PCM Loop Timed Clocking Mode

Figure 3-6 illustrates a simplified block diagram of the HTU-R PCM loop timed clocking mode. The PCM loop timed clock mode takes the PCM DPLL recovered clock (RPCLK) and uses it for both the transmit PCM and receive PCM directions. This mode is applicable in stuffing and non-stuffing modes. This configuration is similar to Section 3.2.3.2.

Figure 3-6. Synchronous PCM Loop Timed Clocking Mode



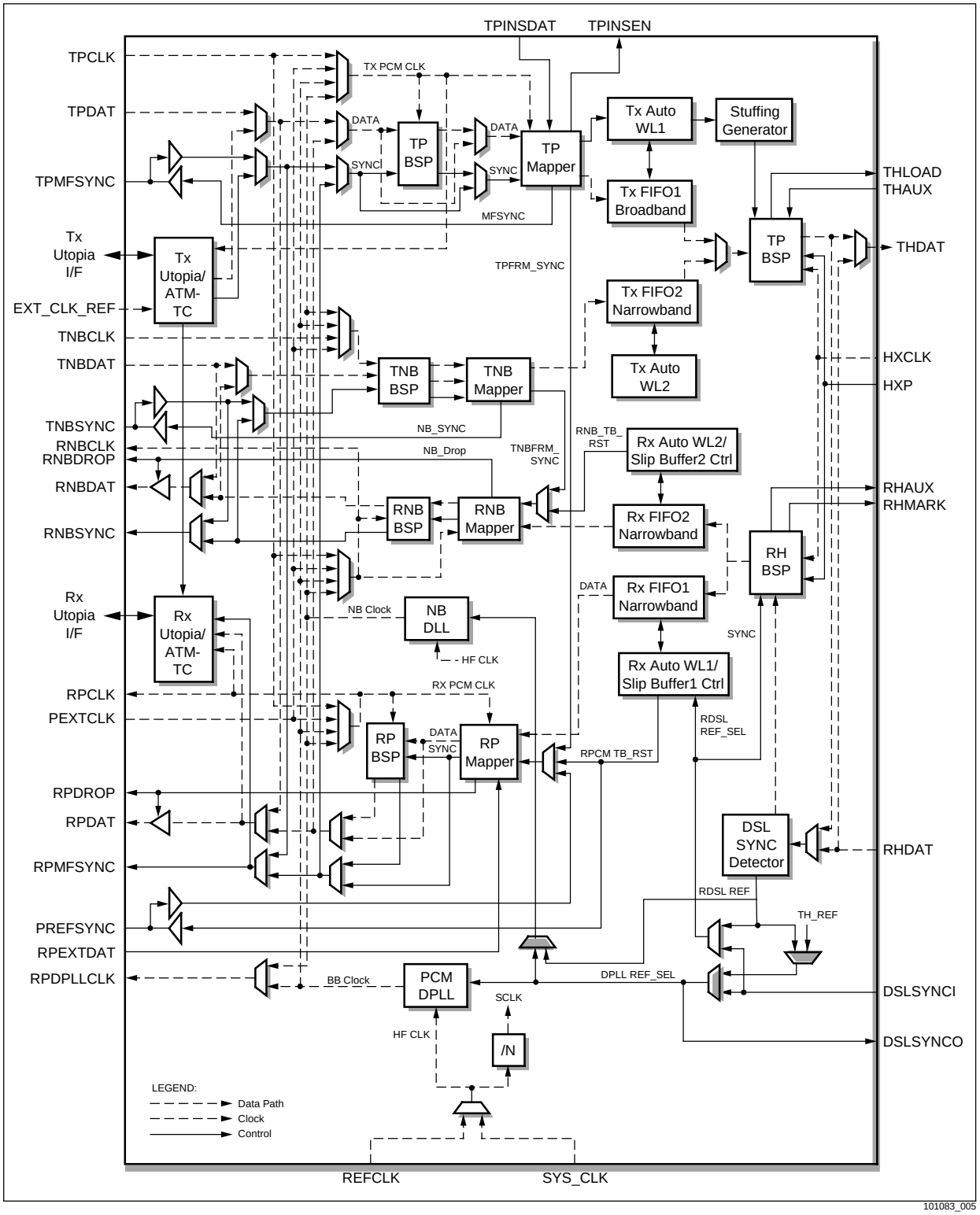
4.0 ZipWirePlus Framer Detailed Description

This section provides a detailed description of the various modules of the DSL framer block. Figure 4-1 provides a detailed block diagram of the DSL framer block.

4.1 Distinguishing Features

- Programmable frame format generator which supports G.shdsl, HDSL1, HDSL2, RADSL, and custom frame formats
- Supports all legacy features of Bt8953A and RS8953B
- Compliant with *ETSI RTS/TM-06008*
- One, two, or three pair T1/E1 ETSI and Bellcore standard application
- ISDN Primary Rate Access (PRA)
- Custom N x 64 over one, two, or three pairs
- Asymmetric PCM rate and frame format capability
- Various rates of PCM clock recovery (64 kHz to 16 MHz)
- Low jitter (wander) stuffing generator
- Flexible Stuff Bit ID (SBID) mapping, including majority vote decision (HDSL2 applications)
- Three programmable PCM and DSL synchronization detectors (supports grouped and spread sync word patterns)
- Four programmable PRBS/BER meters to both PCM and DSL sides
- Twelve programmable performance monitoring counters (can be used as CRC, BPV, or FEBE error counters)
- Three programmable CRC generators
- Programmable scrambler/descrambler
- Supports variable time slot size (eight, four, two, or one) and therefore variable PCM custom frequency (N x 64, N x 32, N x16, and N x 8, respectively)
- Two frames receive PCM and NB slip buffer
- NB port with its own DPLL
- UTOPIA Level 2 (8/16 bit mode) interface and ATM Transmission Convergence (TC)

Figure 4-1. DSL Framer Detailed Block Diagram



4.2 Common Functions

4.2.1 Data FIFO

The DSL framer contains four data FIFOs: INB TX_FIFO, INB RX_FIFO, IPCM TX_FIFO, and IPCM RX_FIFO. These FIFOs are used to provide rate buffering between the PCM side data rate and the DSL side data rate. Each FIFO is capable of storing 512 bits (two E1 frames).

4.2.2 Two-Frame Receive Slip Buffer

In order to support channelized voice applications, the transmitter and receiver time base of the framer needs to be aligned and a receive slip buffer compensates any clock differences between the central office and the remote terminal. The receive slip buffer depth has to be two full frames (E1 or T1) in order to be able to add or drop a full frame when necessary. The DSL framer has two receive slip buffers, one for each PCM port.

4.3 DSL Section

4.3.1 General DSL Function

The DSL section consists of a transmitter and receiver. The DSL transmitter frames the transmit payload data, inserts the overhead, and scrambles the DSL data. The DSL receiver unscrambles the DSL data and removes the overhead.

4.3.1.1 CRC Generator

The DSL frame contains a programmable sixteenth order CRL generator. CRC calculation can be corrupted for debugging purposes. This mode simply inverts the CRC calculation.

4.3.1.2 Scrambler/ Descrambler

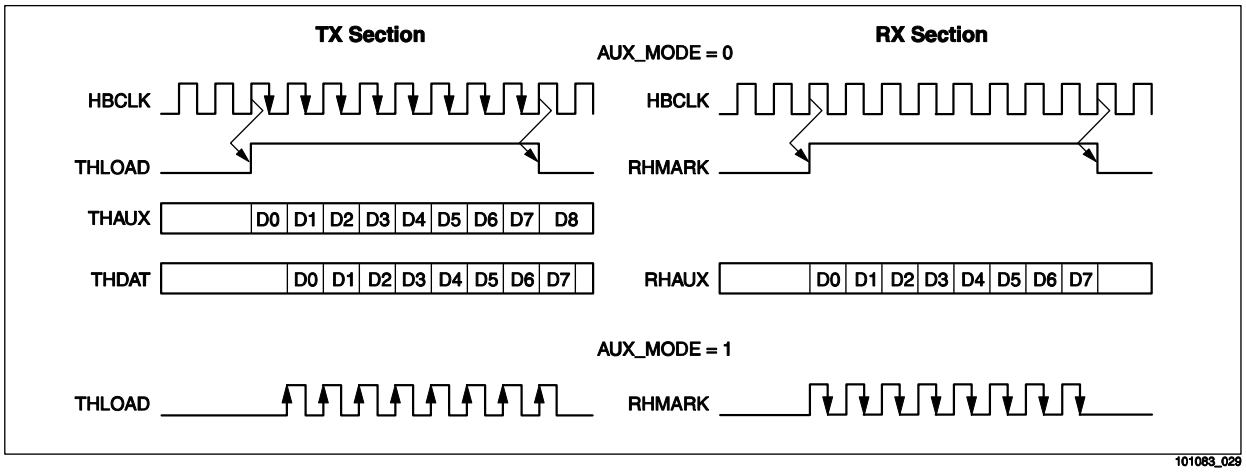
The DSL framer contains a programmable 23 tap scrambler/descrambler. The scrambler/descrambler operation can be bypassed for debugging.

4.3.1.3 Auxiliary Channel

The DSL auxiliary channel (THAUX, RHAUX) provides an alternate source of DSL payload. This channel supports any payload size and can function as an alternate source for the Z-bits or any other selected overhead. Figure 4-2 illustrates the DSL auxiliary channel timing.

The auxiliary channel interface has two operational modes. In the first mode, THLOAD and RHMARK signals simply mark high during auxiliary input mode. The second mode generates gated clock in pins THLOAD and RHMARK during auxiliary mode to clock the serial device directly. This mode prevents additional glue logic in the interface between the DSL framer and the serial device.

Figure 4-2. DSL Auxiliary Channel Timing



4.3.1.4 RX DSL Reference Phase Measurement

While working in multipair configuration, the DSL framer can measure the receiving DSL phase difference between two pairs. This phase is mainly used to determine the delta delay between two DSL channels in point to multipoint application (can also be used for debugging or link delay measurement).

4.3.2 DSL Receiver Functionality

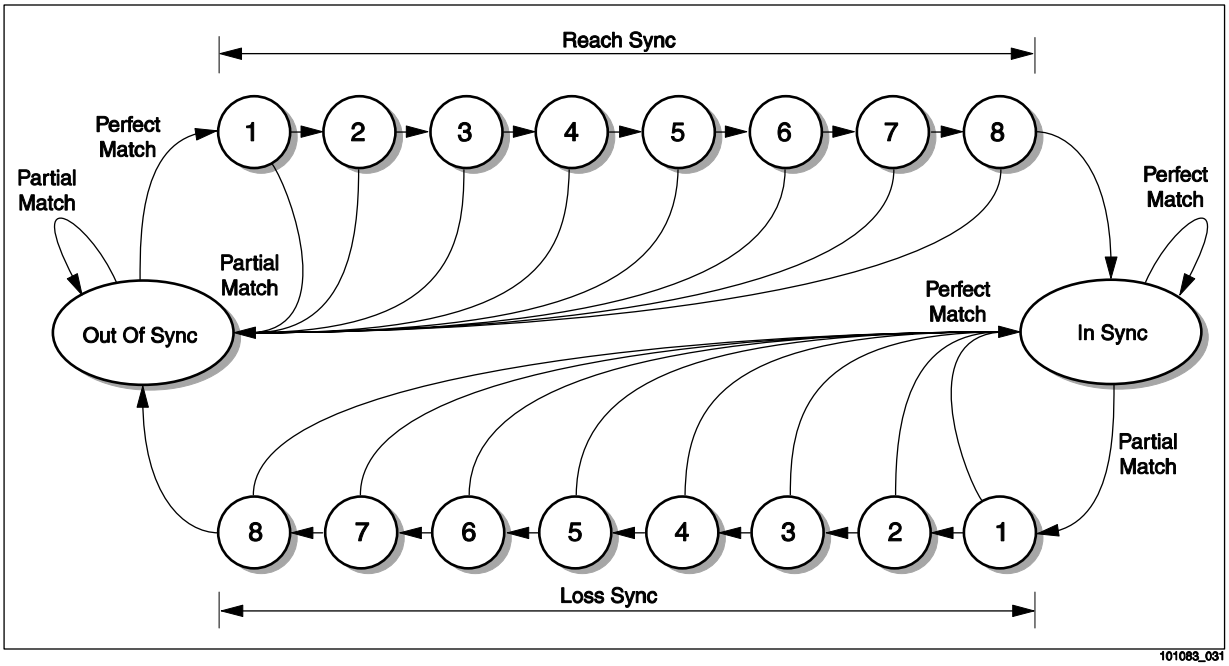
4.3.2.1 DSL Receiver Sync Detector (DSD)

The DSL Synchronization Detector (DSD) acquires and maintains synchronization of the DSL.

To support the wide variety of frame formats, the DSD is designed in a flexible way that provides the following capabilities:

- Synchronized to any grouped bit synchronization pattern up to 16 bits long
- DSL frame size (nominal) can be up to 2^{16} (65,536) bits long
- Stuff size can be two, four, six, or eight bits. For application without the necessity for stuff bits (HDLC applications), the DSD can search for the sync word without searching in variable frame length, but search for fix location instead

Figure 4-3. DSD Synchronization State Machine



4.3.2.2 DSL Receiver Tip/Ring Reversal Detection

In 2B1Q mode, Tip/Ring reversal is automatically detected and corrected by the DSD.

In G.shdsl and HDSL2 applications, the Tip/Ring reversal cannot be detected by the DSL framer due to the non-symbol alignment nature of the DSP operation. In this case, the DSP detects and corrects Tip/Ring Reversal.

4.3.3 DSL Transmitter Functionality

4.3.3.1 DSL Transmit Stuffing Generator

The stuffing generator synchronizes the DSL frame period to the PCM Frame period by adding zero, two, four, six, or eight stuff bits (zero, four in HDSL1 applications) to the DSL frame period.

The stuffing generator can be bypassed for nonvariable frame length applications and can also be used as an additional debugging tool.

4.4 PCM Section

The PCM section (receiver and transmitter) is composed of two major blocks, the PCM mapper and the Layer 3 framer.

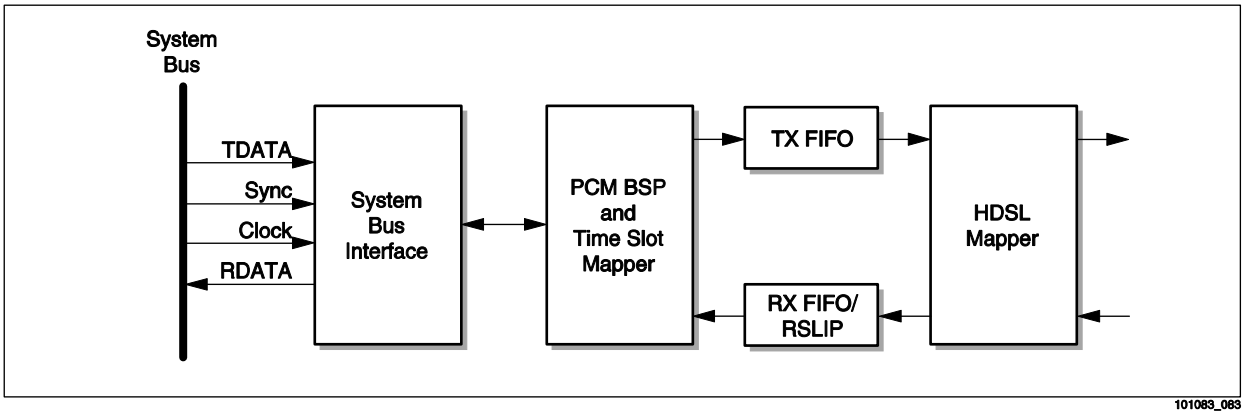
The PCM mapper functions as a formatter which maps or extracts PCM payload data into or out of the DSL channel through the FIFO. Additionally, the mapper can override the data with DBANK or generate a PRBS sequence.

The Layer 3 Framer synchronizes to PCM Frame or Multi-Frame, extracts or inserts Overhead data out of or into the PCM Frame, and checks for any block errors (such as CRC).

4.4.1 PCM Interface

In PCM highway interface applications of 8E1/8T1, the DSL framer interface is compliant with AT&T CHI and MITEL ST-BUS Interfaces up to 16 MHz. This interface enables multipair configuration or any kind of PCM aggregation mode that allows data from different sites to be aggregated onto the same PCM bus.

Figure 4-4. Integrated Slip Buffer and System Bus Interface

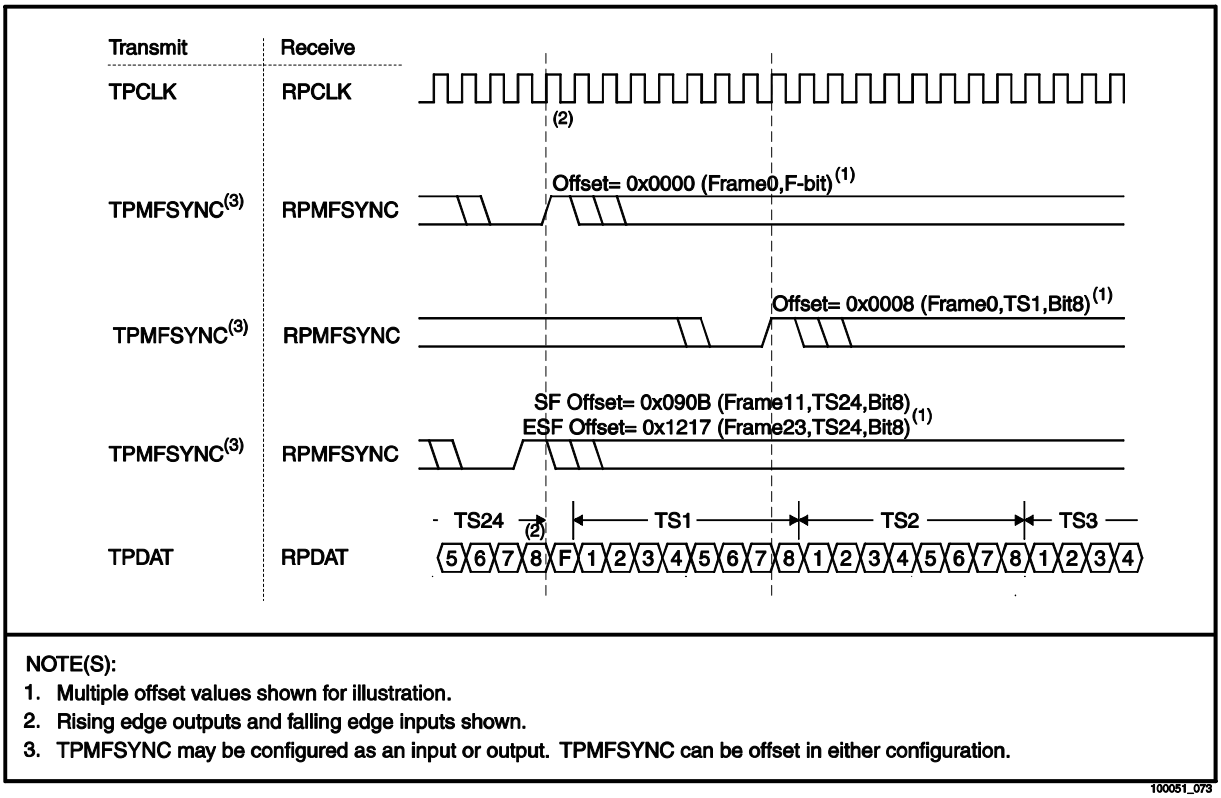


4.4.2 System Bus Timing

The M28975 system bus can be configured in many ways. The TPCLK clock edge can be selected for sampling inputs or updating outputs. The TPMFSYNC can be programmed as an input or output. The TPMFSYNC can indicate the first bit of the PCM frame or can be offset. The system bus clock rate can operate above the payload rate. The RPDAT can either output idle code during the extra timeslots, or go to high impedance.

Figure 4-5 through Figure 4-8 illustrate some of the different configurations of the system bus.

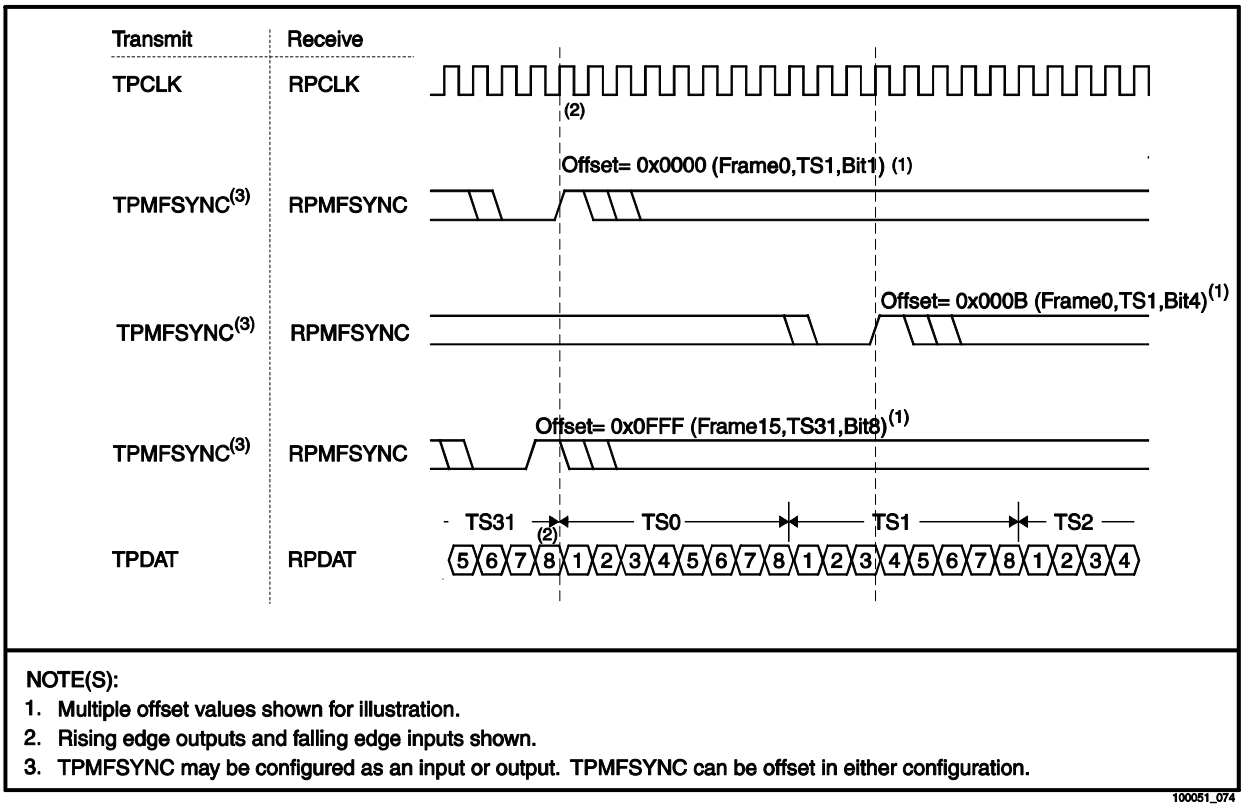
Figure 4-5. 1,544 Kbps System Bus Timing



NOTE(S):
1. Multiple offset values shown for illustration.
2. Rising edge outputs and falling edge inputs shown.
3. TPMFSYNC may be configured as an input or output. TPMFSYNC can be offset in either configuration.

100051_073

Figure 4-6. 2,048 Kbps System Bus Timing



NOTE(S):
1. Multiple offset values shown for illustration.
2. Rising edge outputs and falling edge inputs shown.
3. TPMFSYNC may be configured as an input or output. TPMFSYNC can be offset in either configuration.

100051_074

Figure 4-7. Clock Edge Options

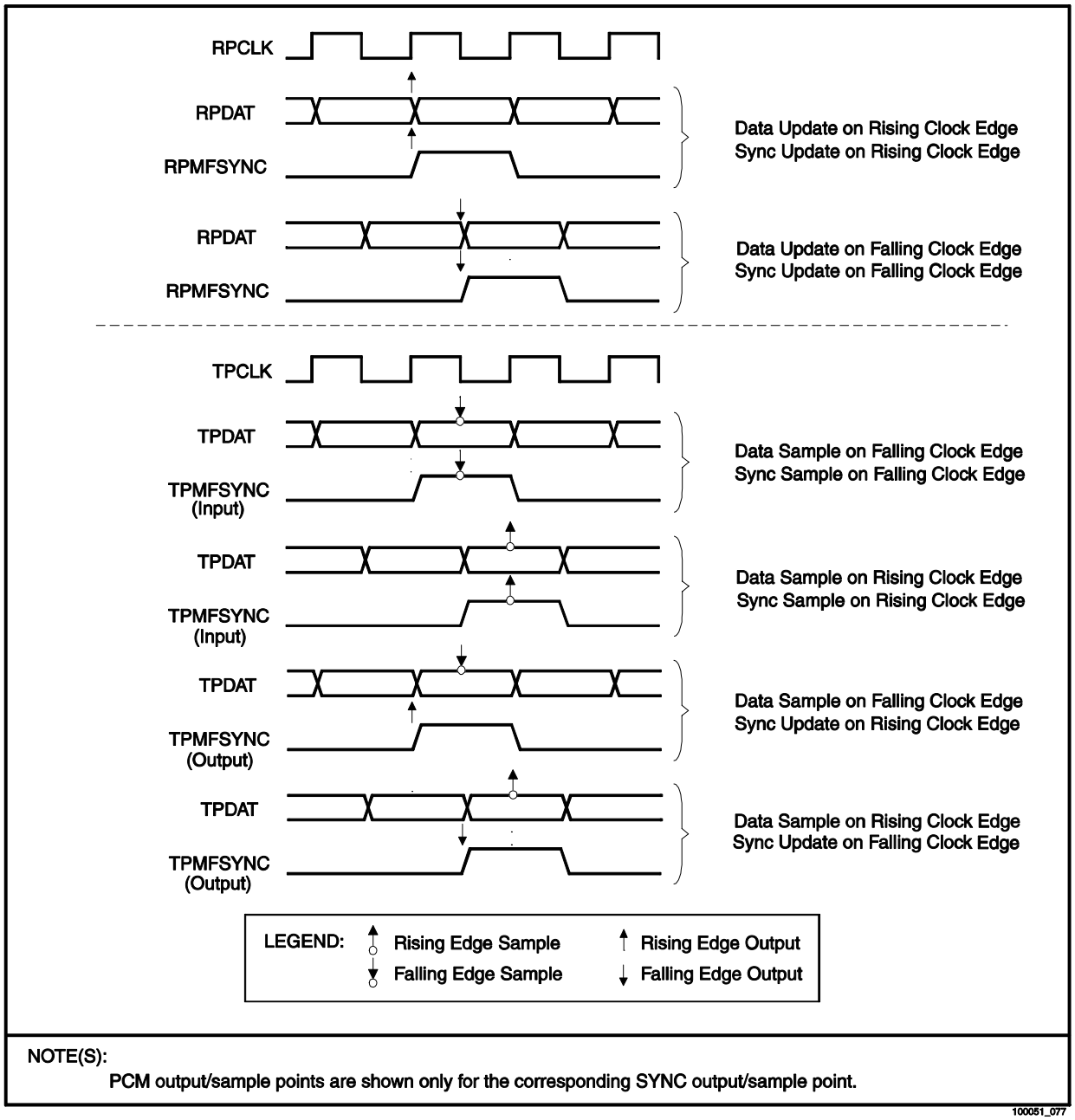
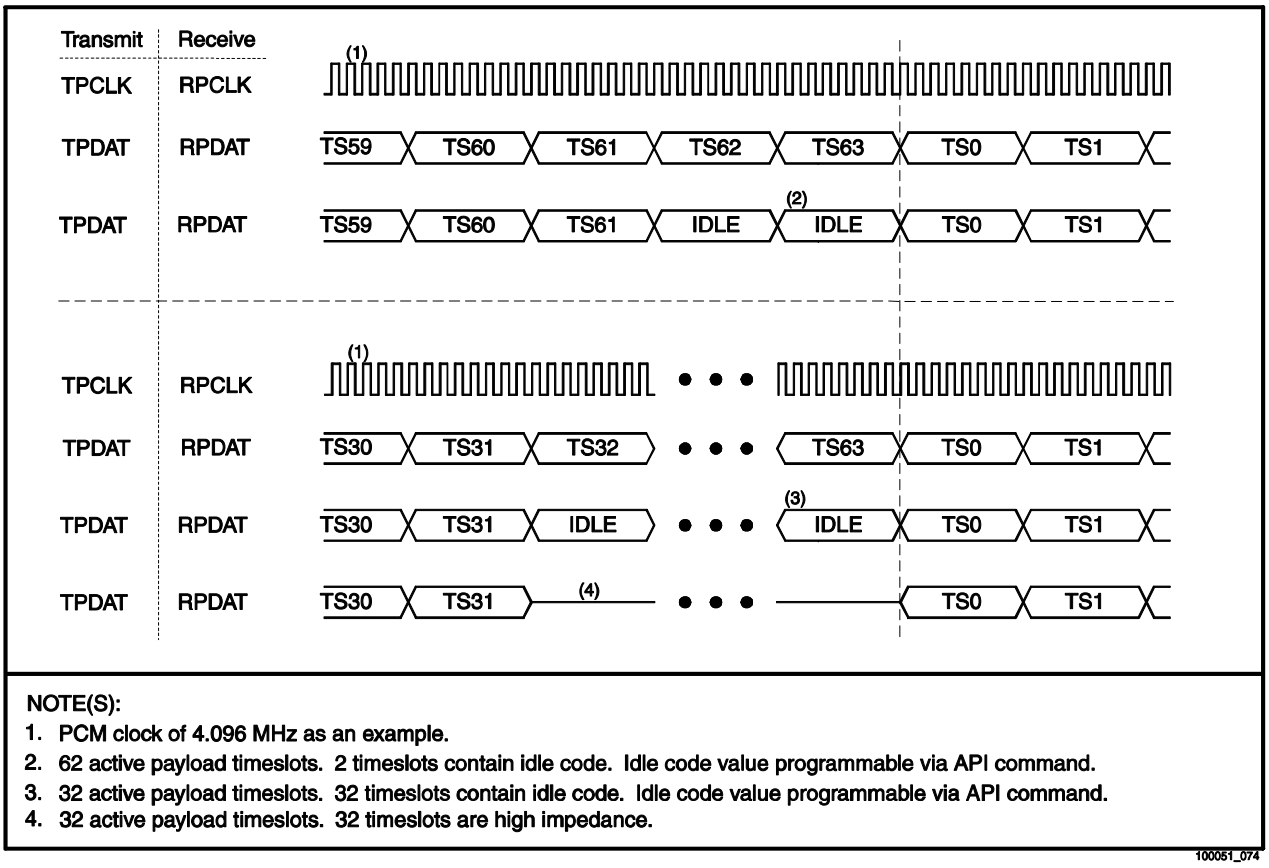


Figure 4-8. System Bus Clock Rate Greater than Payload Rate



NOTE(S):
1. PCM clock of 4.096 MHz as an example.
2. 62 active payload timeslots. 2 timeslots contain idle code. Idle code value programmable via API command.
3. 32 active payload timeslots. 32 timeslots contain idle code. Idle code value programmable via API command.
4. 32 active payload timeslots. 32 timeslots are high impedance.

4.4.3 General PCM Functions

4.4.3.1 CRC Generator

The PCM section contains two generic CRC generators functionally identical to the one located on the DSL side (see section 4.3.1.1 for more details).

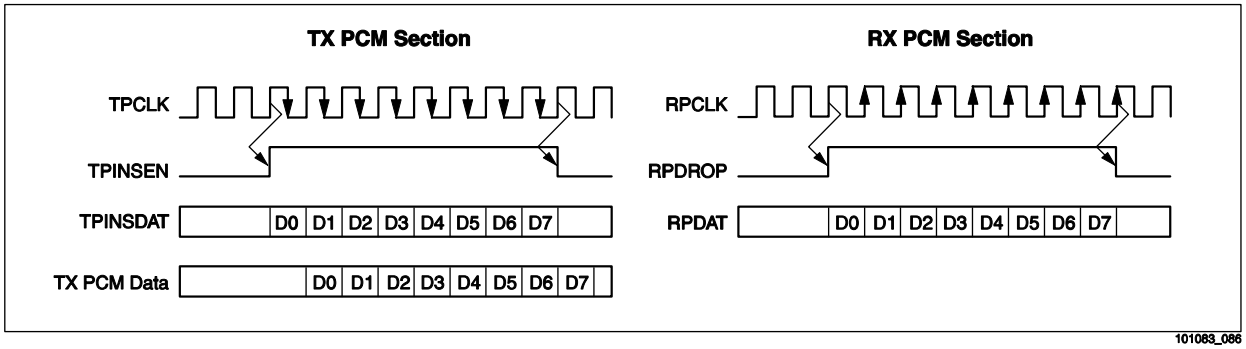
The PCM CRC calculation can be corrupted for debugging purposes. This mode simply inverts the CRC calculation. In addition, the CRC generator can be bypassed or recalculated.

Any CRC computation format can be generated. CRC computation can be enabled or disabled. Any bit in the frame can be replaced with either a 0 or 1 for CRC computation purposes. This capability enables support of any CRC operation method.

4.4.3.2 Insert/Drop

An alternate PCM source feeds into the PCM formatter using TPINSEN, TPINSDAT, and RPDROP pins (see Figure 4-9).

Figure 4-9. Insert/Drop Timing Diagram



4.4.3.3 Overhead Handling

The PCM transmitter and PCM receiver can handle up to 24 overhead (OH) bytes. These OHs can function as Sa bits, E bits, and A bits for E1 applications. They can be used to generate any in-band management.

NOTE: This option requires modifying the low-level DSL Framer code.

4.4.3.4 E1 Grooming

To support the E1 Point-to-Multi-Point (P2MP) application, it is necessary to groom Channel Associated Signaling (CAS) from different sites. Each remote site has a different PCM frame synchronization that needs to be aligned at the central site.

4.4.3.5 Multiframe Phase Measurement

During E1 (P2MP) application, PCM Multiframe phase measurement between TPMFSYNC and RPMFSYNC pins with respect to internal transmit MF Sync (MFSYNC) is necessary at the remote site to compensate for misalignment between different remote sites. This phase can then be used to internally align the DSL

transmit frame to the PCM Frame boundary in each site. It can provide the value of each site to the central office and align the receive channel signaling to the receive E1 MF.

4.4.4 PCM Receiver

The major tasks of the PCM Receiver are as follows:

1. Generate RX PCM time base aligned with the DSL reference (WL delay apart).
2. Assemble ongoing PCM frame using flexible RX PCM mapper table. Major tasks of this table are to:
    a. Assemble RX PCM frame from selectable sources: DSL payload, PRBS sequence, DATA BANK 1, 2 or 3, Signaling table (Grooming Mode), and RPEXTDAT input pin.
    b. Enable BER meteron a per time slot basis.
    c. Assert RPDROP pin to signify specific TSs in RPDAT output.
    d. Insert external PCM data (in RPEXTDAT input) to the receive PCM frame. Used in multipair configuration.
3. Generate receive user interface SYNC signals such as RPMFSYNC and PREFSYNC (multipair configuration PCM time-base synchronization).
4. Synchronize with any Layer 3 Frame/MF.
5. Check CRC (selectable) and computes CRC on the final ongoing frame.
6. Extract overhead bits.
7. Enable override of each overhead bit by the MPU.

4.4.5 PCM Transmitter

The major tasks of the PCM transmitter are to:

1. Generate transmit PCM time base aligned with the incoming frame/multiframe synchronization.
2. Map PCM frame to the TX_FIFO using TX PCM Mapper Table.
3. Enable BER meter on a per time slot basis.
4. Inserts alternate PCM channel, using TPINSDAT, TPINSEN pins.
5. Synchronizes with any Layer 3 Frame/MF.
6. Check CRC (selectable) and compute CRC on the final ongoing frame.
7. Extract overhead bits.
8. Enable override of each overhead bit by the MPU.

4.4.5.1 PCM Sync Detector

The Sync Detector can synchronize to any sync pattern, grouped or spread, up to 16 bits long. This capability allows the DSL Framer to synchronize to E1, T1, or any other frame. This requires modifying the low-level DSL framer code.

4.4.6 Primary Rate Access (PRA)

This section describes the Primary Rate Access (PRA) feature.

4.4.6.1 Distinguishing Features

The following provides a list of the PRA software features. The list is broken into the ZipWirePlus and host processor responsibilities. The software can terminate and insert the PRA functionality in both transmit and receive direction.

ZipWirePlus Responsibilities

- Align E1 frame in DSL Frame
- Transmit PCM Multiframe Self-Alignment (or use external sync reference)
- Output 2mS Multiframe in receive direction
- Automatic CRC detection and insertion
- Automatic CRC-4 error indication bits (E bits)
- Transmit remote alarm indication bits (A bits) pattern
- Process spare bits (Sa4, Sa5, Sa6, Sa7, Sa8) up to message level

Host Processor Responsibilities

- Optionally process overhead bits; A-bits, E-Bits, spare bits (Sa4, Sa5, Sa6, Sa7, Sa8) messages, etc.

4.4.6.2 PRA Overview

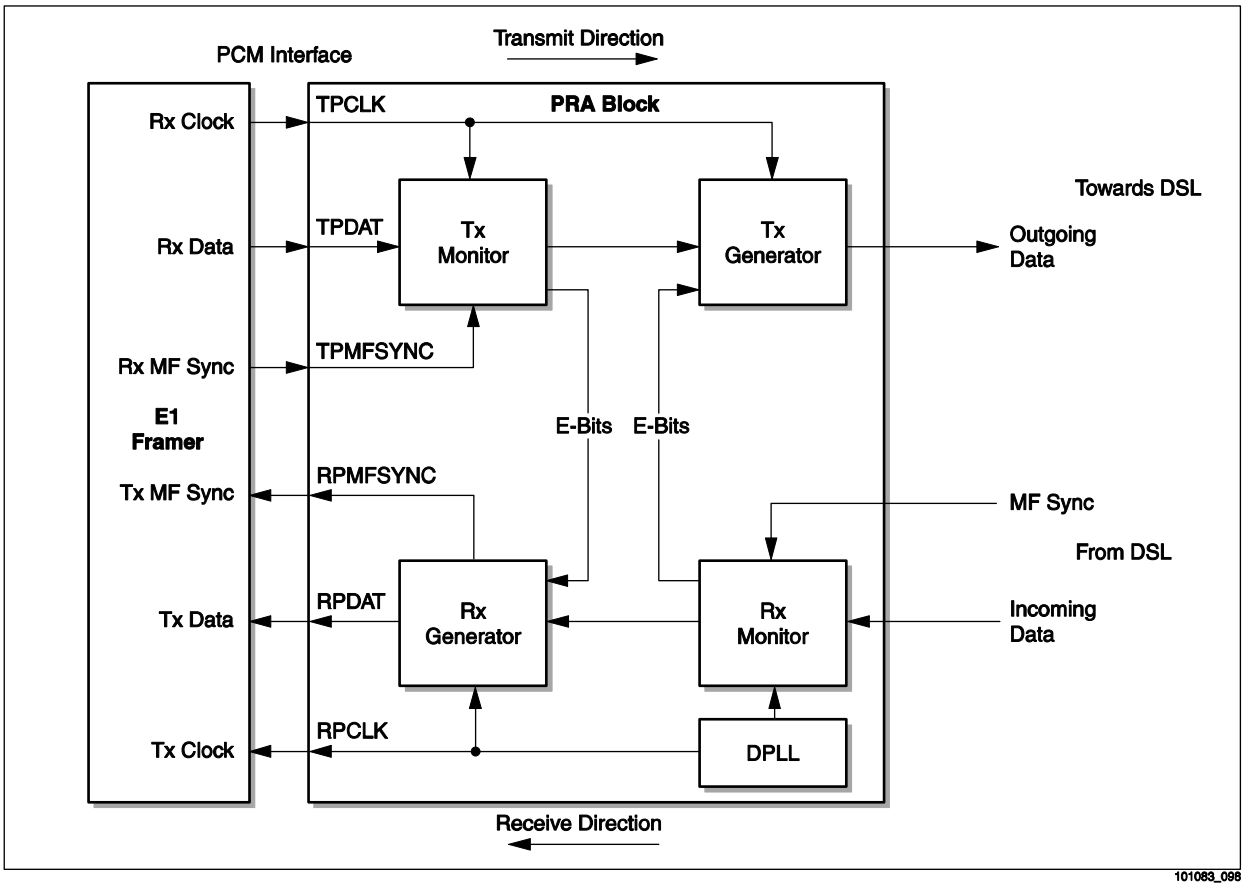
Figure 4-10 illustrates the PRA data path and terminology. The PRA functionality monitors and manipulates the overhead bits found in timeslot 0 on an E1 frame including CRC-4, E-bits, A-bits, and spare (Sa) bits. In addition, the PRA block can either automatically lock onto the incoming multiframe boundary or accept the multiframe from an external source.

The PRA functionality can be performed in both the transmit and receive directions. The transmit direction is defined as the data path from the PCM interface towards the DSL interface. The receive direction is defined as the data path from the DSL interface towards the PCM interface. Each direction consists of a monitor and generator block. The PRA functionality is identical in each direction, but each direction is independently controlled.

In general, there are three possible ways to control the various overhead bits: transparent, automatic, and manual. Refer to each overhead bit definition to determine which modes apply.

- Transparent—the generator block outputs the overhead bits unaltered from the monitor block.
- Automatic—the generator block will automatically determine and output the appropriate overhead bits value. The overhead bits are updated every multiframe sync.
- Manual—the generator block outputs the overhead bits based on an API command received from the host processor. The generator block will continuously output the new value starting on the subsequent multiframe sync.

Figure 4-10. PRA Overview



4.5 Narrowband Port

For simultaneous transport of voice and data applications with a glueless solution, a secondary port is included to transmit and receive the narrowband (NB) data stream (usually used for voice). This port has all the flexibility of a PCM port but does not have the auxiliary channel and signaling table. The narrowband channel data stream must be synchronized with the PCM data stream.

Limitations

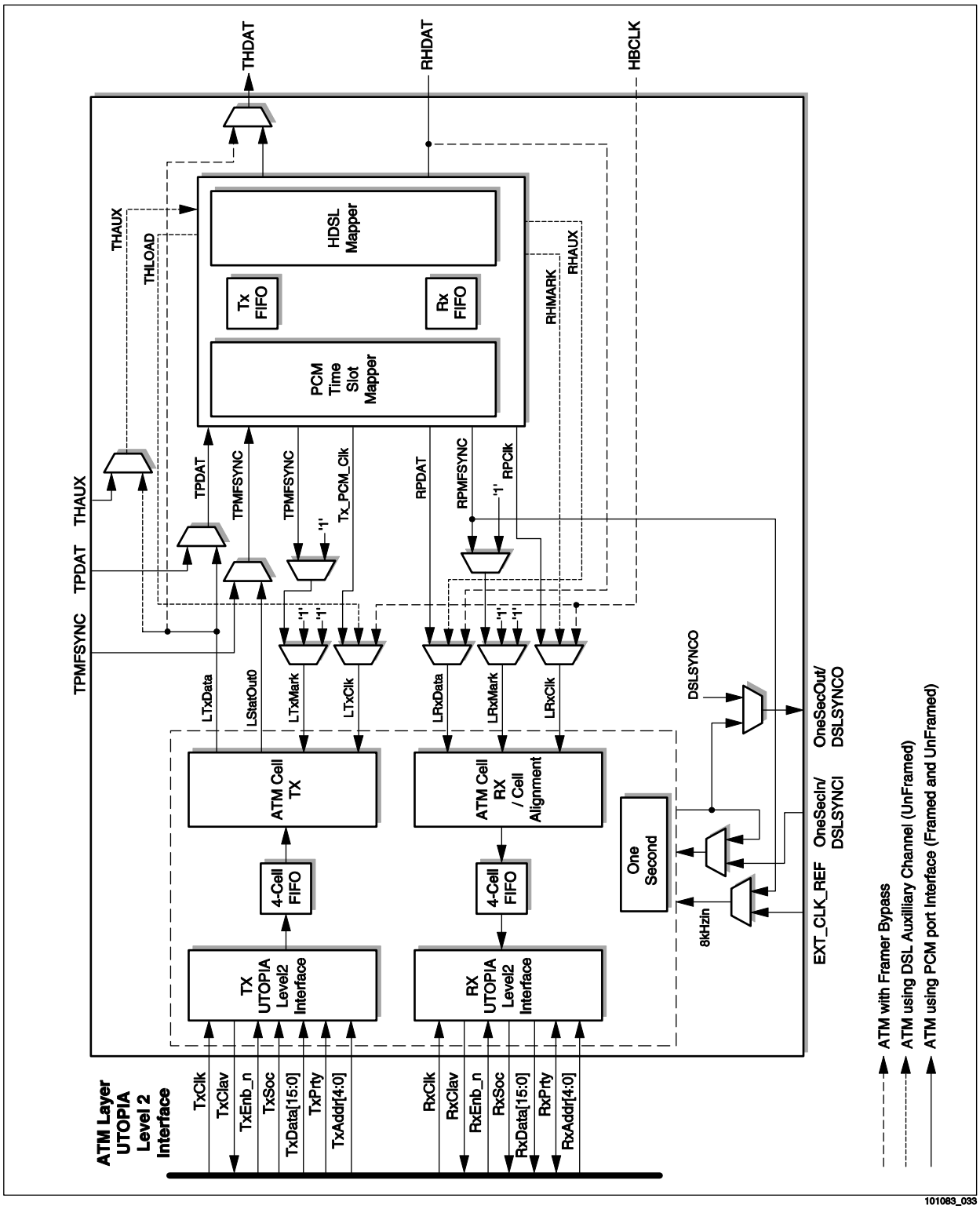
1. Narrowband clock must be synchronized with the PCM clock. This implies the same frequency offset.
2. Narrowband cannot operate independently, requires PCM
3. Narrowband only supports N x 64k operation (i-bit = 0).

4.6 ATM-TC and UTOPIA Level 2 Interface

An ATM-TC (Transmission Convergence) and UTOPIA Level 2 (or Level 1 as an option) interface are fully supported by the DSL framer, compliant with ATM Forum standards. This block is a slice of one port out of the octal ATM-TC PHY device (RS8228). See Figure 1-1.

- UTOPIA Level 2 Interface
  - PHY cell to UTOPIA interface
  - 50 MHz maximum clock rate
  - 8/16 data path interface
  - Compatible with UTOPIA Level 1
- Cell alignment framing section
  - ATM cell interface support for:
    - Circuit-based physical layer
    - Cell-based physical layer
  - Passes or rejects idle cells or selected cells based on header register configuration
  - Recovers cell alignment from HEC
  - Performs single-bit HEC error correction and multiple-bit detection
  - Generates cell status bits, cell counts, and error counts
  - Reads all data from the UTOPIA FIFO
  - Inserts headers and generates HEC
  - Inserts idle cells when no traffic is ready
- Counter/Status Information
  - One-second status latching
  - One-second counter latching

Figure 4-11. Integrated One Port of RS8228 with xDSL Framer



4.7 Test and Diagnostics

4.7.1 Performance Monitoring

The DSL framer supports up to twelve performance monitoring counters, divided equally into three sections.

Each performance-monitoring counter can function as a CRC error counter for the Severe Error Second (SES) indicator, Far End Block Error (FEBE) counter, Bipolar Violation (BPV) error counter, or any other necessary performance indicator counter. The receive DSL, receive PCM and transmit PCM support up to four performance monitoring counters.

4.7.2 PRBS and BER Meter

The DSL framer has four PRBS/BER meter modules supporting BER measurement towards the DSL, PCM, and NB sides. It can operate independently. The following description focuses on the PCM port; however, the same description applies to the NB port.

TP_PRBS (TNB_PRBS) and RP_BER (RNB_BER) function as BER meters towards the DSL side. The RP_PRBS and TP_BER function as BER meters towards the PCM side.

The PRBS sequence can override TPDAT and RPDAT on a per time slot basis, and achieve any framed or unframed test pattern examination. The PRBS pattern is programmable and selected for both RP_BER and TP_BER by PRBS_TAP_[2:0] registers, indicating up to 23rd-order PRBS (Tap[23:0]):

Example:

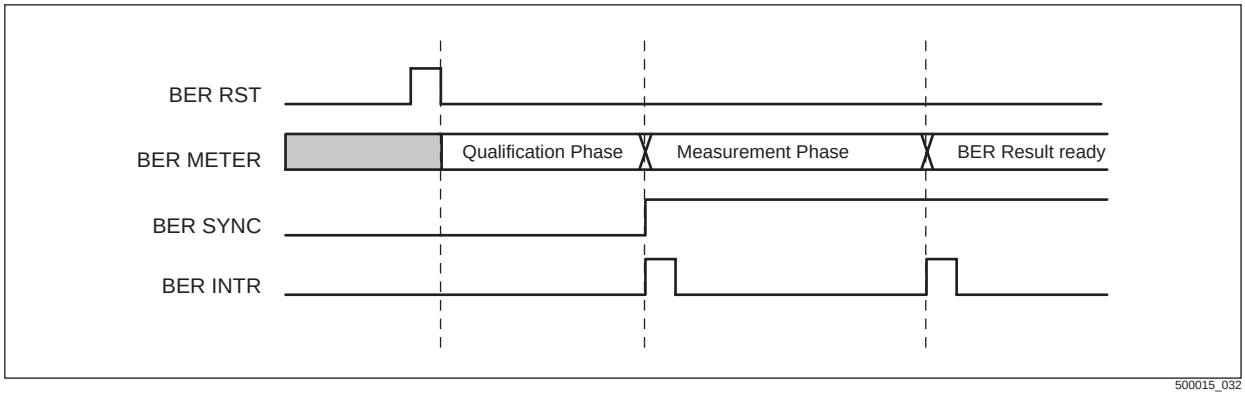
- For a PRBS pattern of $2^{15} – 1$, the polynomial is $x^{15} + x^{14} + 1$.
- For a PRBS pattern of $2^{23} – 1$, the polynomial is $x^{23} + x^{18} + 1$.
- For a QRSS $2^{20} – 1$ pattern (polynomial – $x^{20} + x^{17} + 1$), 14-bit 0 suppression is implemented.

The TP_BER and RP_BER sequence can be inverted.

The constant value per time slot basis can override TSER and RSER instead of PRBS. The MPU configures BER_SCALE to specify the test measurement interval from a range of 2^{21}— 2^{31} bit length.

Figure 4-12 illustrates the BER measurement timing.

Figure 4-12. BER Measurement Timing



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5.0 Hardware Interfaces

5.1 ZipWirePlus Clocks

The ZipWirePlus crystal amplifier provides the PLL based clock synthesizer with a stable reference. The ZipWirePlus can operate with either a crystal connected directly to the crystal amplifier input or with an external clock driving the crystal amplifier input.

The ZipWirePlus provides the XTALO_B output (which is a buffered output from the crystal amplifier) that can be used to drive the crystal amplifier input of other ZipWirePlus devices. This allows a multiport system to use only one crystal.

Figure 5-1 illustrates the high performance differential crystal amplifier.

Figure 5-1. Differential Crystal Amplifier Configuration

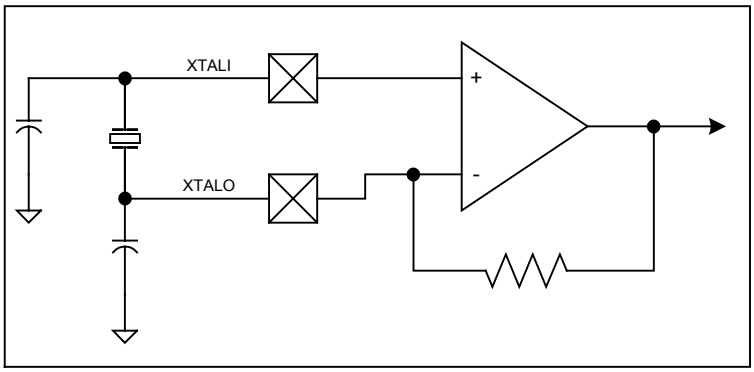


Table 5-1. Crystal Specifications

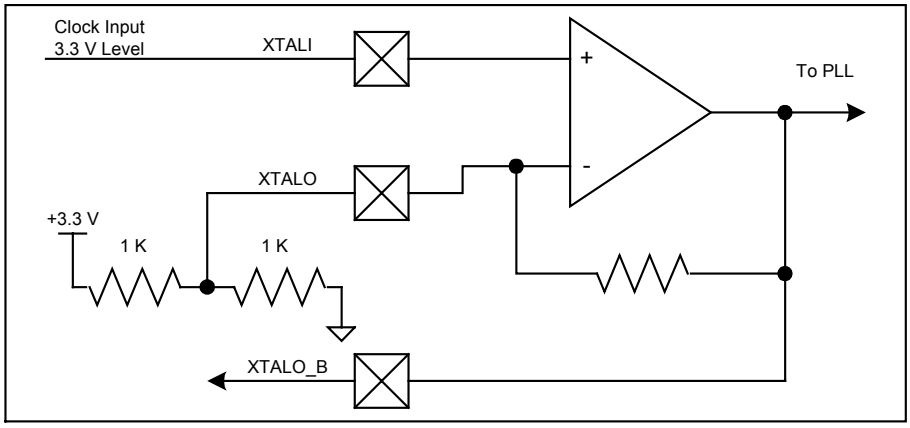
Parameter	Value
Nominal Frequency	22.1184 MHz
Frequency Tolerance at 25 °C	±10 ppm
Temperature Frequency Stability	±10 ppm
Aging	±10 ppm over 10 years
Load Capacitance	15.5 pF
Max Shunt Capacitance	7 pF
Max Drive Level	200 µW
Max ESR	25 Ω

> ***General Note:*** Individual frequency tolerance, temperature frequency stability, and aging requirements can vary as long as the total tolerance is less than ±32 ppm.

5.2 Driving the Crystal Amplifier Directly

Figure 5-2 illustrates how to drive the crystal amplifier directly. Unlike in previous designs, driving an external clock into the XTALI input alone is not sufficient. You must drive the XTALI input from an external clock and bias the XTALO input with a resistive divider from 3.3 V to ground. The XTALO pin should be biased at 1.65 V (VDDO/2). Two 1 KΩ resistors are adequate for this purpose.

Figure 5-2. Direct Clock Connection



5.3 Configuration Pins

The BOOT pin determines the start up operation mode.

0 = download the program from the serial port.

1 = download the program from the host port.

5.4 Internal 8051 Communication Interfaces

Table 5-2 lists the interfaces to communicate with external devices.

Table 5-2. Communication Interfaces

Interface	Description
Host Port RAM Interface	Used by an embedded host processor to send API commands to the ZipWirePlus system. The Host Port RAM uses a mailbox protocol to pass the API parameters.
RS-232 Serial Interface	Used by an external host processor (PC or Terminal) to send API commands to the ZipWirePlus system.

5.4.1 Host Port RAM Interface

The host port RAM interface is connected to a host processor. The host port RAM functions as a simple memory device.

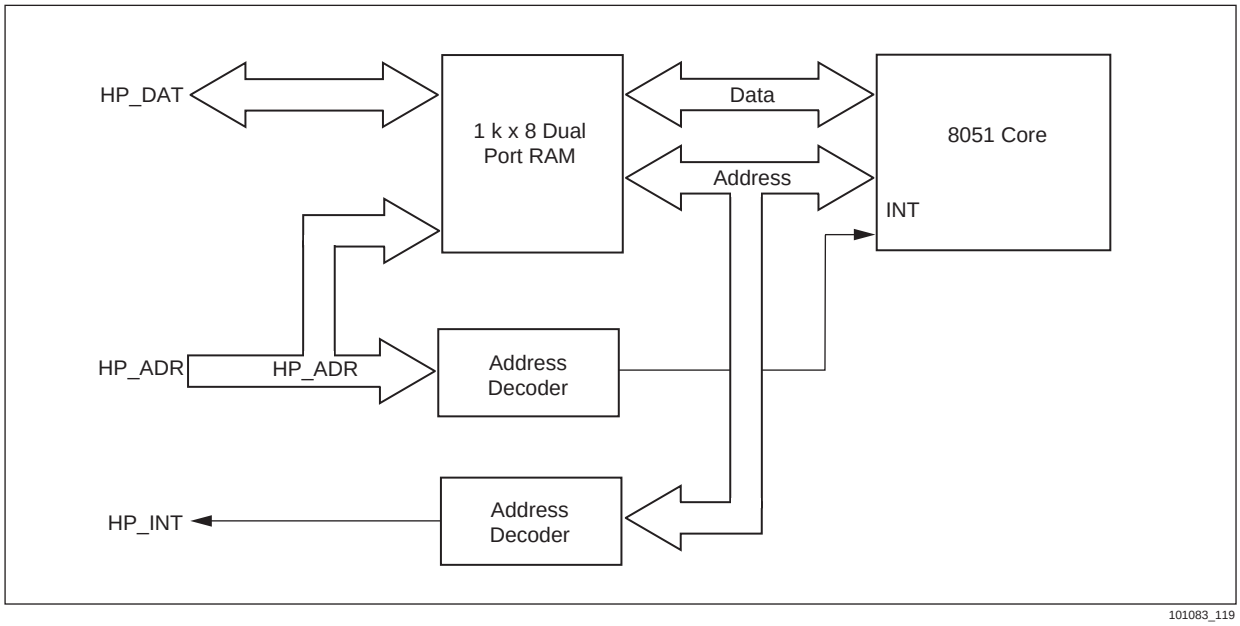
The details of the Host Port RAM protocol is described in the *M28975 ZipWirePlus G.shdsl Transceiver with Embedded Microprocessor Programmer Reference Manual* .

5.4.1.1 Host Port Hardware Implementation

Figure 5-3 illustrates the host port interface. The dual port RAM is the synchronous type.

All timing is with respect to the external HP_CLK input signal.

Figure 5-3. Host Port Interface Block Diagram—Host Port Side



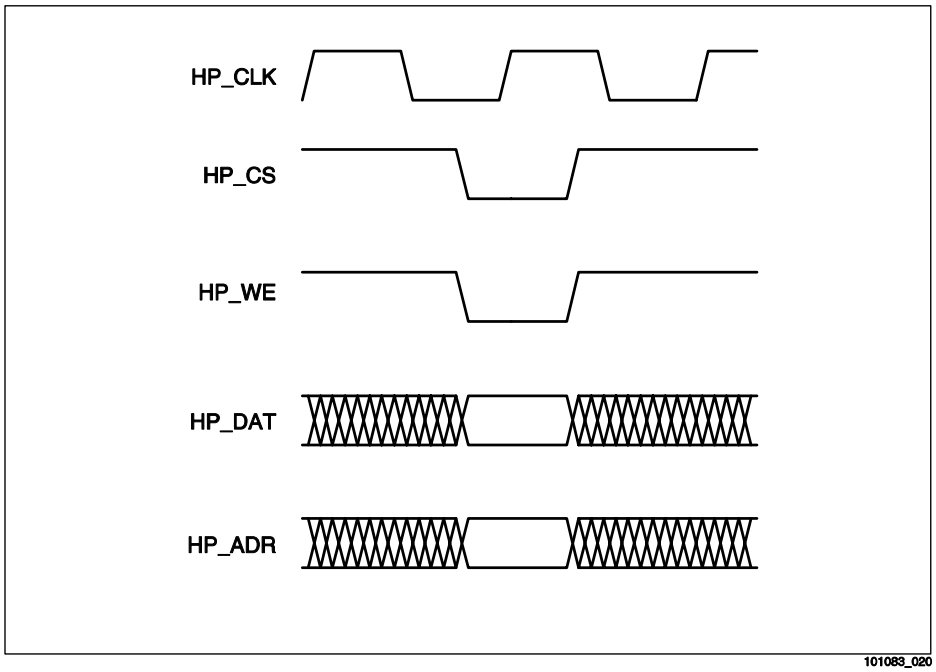
5.4.2 Host Port Timing

5.4.2.1 Host Port Write Cycle Timing

Figure 5-4 illustrates the timing of a host port write cycle. A write cycle is initiated by bringing both the host port chip select (HP_CS) and the write enable (HP_WE) low prior to the rising edge of the host port clock (HP_CLK). The host port write address (HP_ADR) and data (HP_DAT) must also be set up prior to the same clock edge. Data is written to the RAM on the rising edge of HP_CLK. A new write cycle may be performed every host port clock cycle for maximum throughput. Write cycles terminate when either the chip select or the write enable is deasserted.

A write cycle may stretch over multiple HP_CLK clock cycles as long as all hold times are met on the last clock cycle before write termination. Care should be taken to raise the chip select and/or the write enable prior to removing the address and data so that invalid data is not unintentionally written to the host port RAM.

Figure 5-4. Host Port Write Cycle Timing

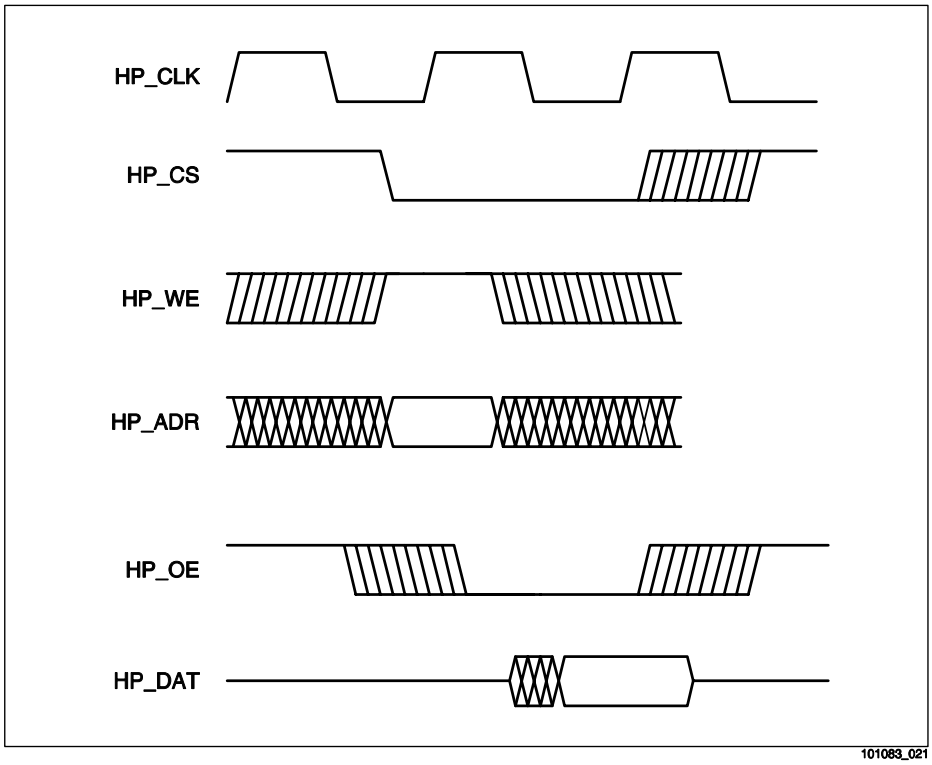


5.4.2.2 Host Port Read Cycle Timing

Figure 5-5 illustrates the timing of a Host Port, read cycle. A host port read cycle is initiated by setting the host port chip select (HP_CS) low while keeping the host port write strobe (HP_WE) high prior to the positive edge of the host port clock (HP_CLK). The host port address (HP_ADR) must be set up prior to this same clock edge.

The address is latched on the rising edge of HP_CLK. After the address settles internally, data becomes available at the output of the RAM. To access the data, the host port output enable (HP_OE) and the host port chip select must both be held low. A read cycle is terminated by bringing the host port chip select high.

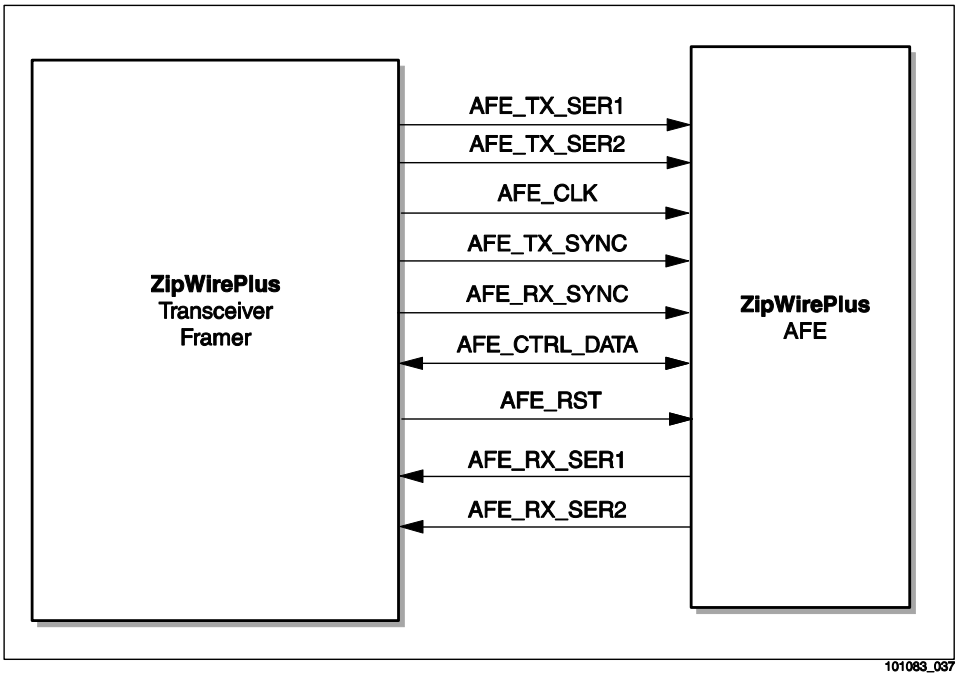
Figure 5-5. Host Port Read Cycle Timing



5.5 ZipWirePlus Transceiver/Framer to AFE Interface

Figure 5-6 illustrates the ZipWirePlus transceiver/framer to AFE interface. The two devices must be connected as shown.

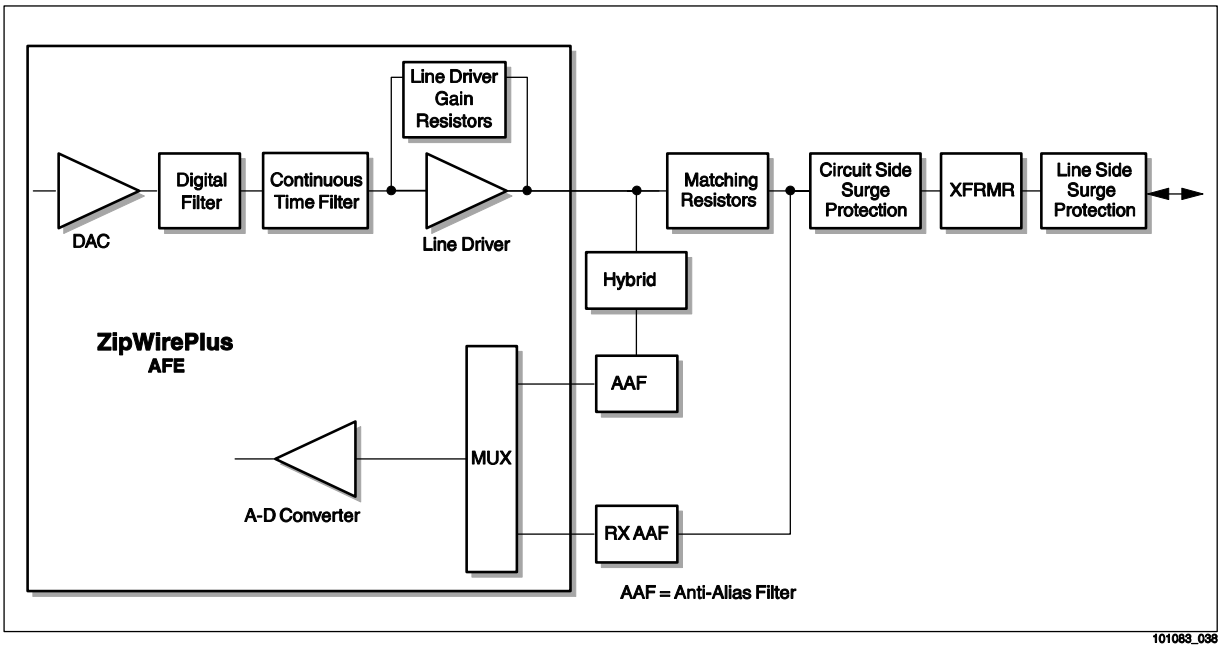
Figure 5-6. ZipWirePlus Transceiver/Framer to AFE Interface



5.6 Transmission Line Interface

Figure 5-7 illustrates a block diagram of the DSL transmission line interface. The DSL interface consists of the continuous time filter, line drive feedback resistors, impedance matching resistors, compromise hybrid, transformer, and surge protection. All signals are differential pairs. Only NPO-type capacitors should be used in the DSL transmission line interface except for the surge protection blocks. The NPO capacitors are selected because of their high degree of linearity characteristics. All capacitors should have a tolerance of 5% while the resistors should have a tolerance of 1%.

Figure 5-7. DSL Transmission Line Interface



5.6.1 Compromise Hybrid

The purpose of the compromise hybrid is to model the impedance of the transmission line. This model generates an approximation of the transmitted signal's echo. The echo replica is then subtracted from the signal on the line transformer to generate a first-order approximation of the received signal. Although the M28975 contains a digital echo canceller (EC), the hybrid is needed to reduce the signal-level input to the Analog-to-Digital Converter (ADC). This eliminates ADC overflow on short loops and increases the resolution of the digitized received signal for better digital signal processing performance.

5.6.2 Line Driver Compensation

The LD_PH/LD_PL and LD_MH/LD_ML signal pairs require that capacitors be placed between them. The LDOP/LDAOP and LDON/LDAON signal pairs require

that inductors be placed between them. These components should be placed as close as possible to the device.

5.6.3 Impedance Matching Resistors

Impedance matching resistors are placed in the transmit path so the output impedance of the line interface more closely matches the impedance of the transmission line and load. This maximizes the power transferred to the receiver on the other end of the line. The load is assumed to be 135 Ω.

5.6.4 Transformer

The line transformer provides DC isolation from the transmission line by creating a high-pass filter. The winding ratio of the transformer must be 2.0:1 (line side:circuit side) to generate the appropriate voltage level on the line. The primary inductance (L) of the line side transformer is a very critical parameter. If the inductance is too high, the cutoff frequency of the filter will be too low and the M28975 echo canceller and equalizer will not be able to cancel out the low frequency components of the echo and inter-symbol interference (ISI). If L is too low, part of the information in the signal will be filtered out, thereby decreasing the Signal-to-Noise (SNR) ratio. In addition, the line transformer must meet certain return loss requirements to maximize system performance.

5.6.5 Anti-alias Filters

Anti-aliasing filters are needed to filter out high frequencies that would be aliased back into the passband as noise. These filters are made of all passive components. The cutoff frequency (f_c) is designed to be as low as possible to achieve maximum attenuation of aliasing frequencies without filtering out the desired signal.

5.6.6 Surge Protection

Mindspeed uses the SIDACtor®, fuses, and diodes for surge protection on our EVM. Teccor Electronics (http://www.teccor.com) has an application note (*Digital Line Card Circuit Protection*) that is useful in designing surge protection.

5.7 Voltage Reference and Compensation Circuitry

Compensation capacitors must be connected between all M28975 voltage reference pins and analog ground.

In addition to compensation capacitors, external passive components are needed to set the bias current used in the M28975. Refer to the latest M28975 EVM schematics for these components.

5.8 Test and Diagnostic Interface (JTAG)

The Test and Diagnostic Interface comprises a test access port and two Serial Test Ports (STP). The test access port conforms to *IEEE Std. 1149.1-1993 (IEEE Standard Test Access Port and Boundary Scan Architecture)*. Also referred to as the Joint Test Action Group (JTAG), this interface provides direct serial access to each of the transceiver's I/O pins. This capability can be used during an in-circuit board test to increase the testability and reduce the cost of the in-circuit test process.

The serial test ports function as a real-time virtual probe for looking at the transceiver's internal signals. A majority of the receiver's signal path is accessible through these outputs.

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6.0 Pin Descriptions

The ZipWirePlus M28975 solution is available in a two-device chip set. The ZipWirePlus Transceiver/Framer/Microprocessor is packaged in one device and is marked as the CX28945. The ZipWirePlus AFE/Line Driver is packaged in a separate device and is marked as the CX28927.

The ZipWirePlus Transceiver/Framer is available in two package options. The 13 x 13 mm FPBGA option is targeted for high density while the 176-pin LQFP is targeted for ease of manufacturability.

The ZipWirePlus AFE/Line Driver is available in a 48-pin ETQFP.

6.1 ZipWirePlus Pin Assignments

This section provides the pin assignments for the ZipWirePlus devices.

6.1.1 ZipWirePlus Transceiver/Framer Pin Assignments

Table 6-1 lists the 13 × 13 mm fine pitch ball grid array (FPBGA) and 176-pin low quad flat pack (LQFP) pin assignments.

Table 6-1. Pin List for M28975 DSP/Framer—Alphabetic Order

LQFP Pin Number	FPBGA Pin Number	Signal Name
72	P9	AFE_CLK
70	N10	AFE_CTRL_DATA
69	M9	AFE_RST
78	N12	AFE_RX_SER1
77	M11	AFE_RX_SER2
68	P8	AFE_RX_SYNC
76	P10	NC1
71	R8	NC2
62	R7	AFE_TX_SER1
61	P6	AFE_TX_SER2
65	P7	AFE_TX_SYNC
153	B9	ATM_RX_ADDR0
152	D8	ATM_RX_ADDR1
151	C9	ATM_RX_ADDR2
150	A9	ATM_RX_ADDR3
146	A10	ATM_RX_ADDR4
145	B11	ATM_RX_CLAV
140	D11	ATM_RX_CLK
1	A1	ATM_RX_DATA0
176	A2	ATM_RX_DATA1
165	D5	ATM_RX_DATA10
162	C5	ATM_RX_DATA11
161	D6	ATM_RX_DATA12
160	B7	ATM_RX_DATA13
159	A8	ATM_RX_DATA14
158	C6	ATM_RX_DATA15
175	B3	ATM_RX_DATA2
174	A3	ATM_RX_DATA3
173	A4	ATM_RX_DATA4

LQFP Pin Number	CABG A Pin Number	Signal Name
172	B4	ATM_RX_DATA5
171	A5	ATM_RX_DATA6
170	C3	ATM_RX_DATA7
167	B5	ATM_RX_DATA8
166	C4	ATM_RX_DATA9
143	C11	ATM_RX_ENB
157	D7	ATM_RX_PRTY
154	C8	ATM_RX_SOC
10	D2	ATM_TX_ADDR0
7	D3	ATM_TX_ADDR1
6	D1	ATM_TX_ADDR2
5	C2	ATM_TX_ADDR3
4	C1	ATM_TX_ADDR4
39	L1	ATM_TX_CLAV
2	B2	ATM_TX_CLK
38	N3	ATM_TX_DATA0
35	L2	ATM_TX_DATA1
20	H4	ATM_TX_DATA10
19	G3	ATM_TX_DATA11
18	G1	ATM_TX_DATA12
17	F2	ATM_TX_DATA13
16	G4	ATM_TX_DATA14
13	E2	ATM_TX_DATA15
32	K2	ATM_TX_DATA2
29	K4	ATM_TX_DATA3
28	J2	ATM_TX_DATA4
27	H1	ATM_TX_DATA5
26	K3	ATM_TX_DATA6
25	J4	ATM_TX_DATA7

LQFP Pin Number	FPBGA Pin Number	Signal Name
24	H2	ATM_TX_DATA8
21	G2	ATM_TX_DATA9
3	B1	ATM_TX_ENB
12	F4	ATM_TX_PRTY
11	E3	ATM_TX_SOC
34	M3	BOOT
42	N1	TEST_AD0
41	M1	TEST_AD1
40	M2	TEST_AD2
134	B14	DSLSYNCI
129	D15	DSLSYNCO
33	L4	EXT_CLK_REF
8, 15, 22, 30, 36, 44, 58, 66, 75, 79, 97, 103, 111, 120, 124, 141, 147, 155, 164, 168, 48	P1, R3, E4, A11, C7, A6, H3, K1, N8, P11, L15, G13, F15, F3, L3, R6, R9, K13, F14, C10, B6	GND
100	K12	HP_ADR0
99	L13	HP_ADR1
96	L12	HP_ADR2
95	M13	HP_ADR3

LQFP Pin Number	CABG A Pin Number	Signal Name
94	M15	HP_ADR4
93	N14	HP_ADR5
92	N15	HP_ADR6
91	P15	HP_ADR7
85	R12	HP_ADR8
84	P12	HP_ADR9
64	M8	HP_CLK
101	L14	HP_CS
89	R15	HP_DAT0
88	R14	HP_DAT1
87	P13	HP_DAT2
86	R13	HP_DAT3
83	R11	HP_DAT4
82	N13	HP_DAT5
81	M12	HP_DAT6
73	M10	HP_DAT7
90	P14	HP_INT
105	K14	HP_OE
102	K15	HP_WE
149	B10	P12_RXD1
144	D10	P13_TXD1
130	C15	P30_RXD0
128	D14	P31_TXD0
139	C12	PEXTCLK
126	C13	PREFSYNC
133	A15	RHAUX
132	B15	RHMARK
109	J14	RNBCLK
107	J13	RNBDAT
106	J15	RNBDROP
108	H12	RNBSYNC
122	D13	RPCLK

LQFP Pin Number	CABG A Pin Number	Signal Name
118	E13	RPDAT
116	G14	RPDPLLCLK
117	F12	RPDROP
138	A12	RPEXTDAT
121	E12	RPMFSYNC
63	N7	RST
55	N5	TCK
51	N4	TDI
54	P4	TDO
57	P5	TEST_E
60	M7	TESTMODE
135	A14	THAUX
131	C14	THLOAD
56	M6	TMS
114	F13	TNBCLK
110	H13	TNBDAT
113	G12	TNBSYNC
137	B13	TPCLK
136	A13	TPDAT
127	E15	TPINSDAT
115	H15	TPINSEN
123	E14	TPMFSYNC
52	M5	TRST
14, 31, 59, 74, 104, 119, 148, 163, 43	F1, J1, N6, N11, J12, G15, D9, A7, N2	VDD (1.8 V)

LQFP Pin Number	CABG A Pin Number	Signal Name
9, 23, 37, 53, 67, 80, 98, 112, 125, 142, 156, 169, 47	E1, B12, B8, D4, J3, M4, R5, N9, R10, R2, M14, H14, D12	VDDO (3.3 V)
50	R4	VGNN
45	R1	XTALI
46	P2	XTALO
49	P3	XTALO_B

6.1.2 ZipWirePlus AFE Pin Assignments

The ZipWirePlus AFE/Line Driver is packaged as a 48-pin exposed thin Quad Flat Pack (ETQFP). The pin list is shown in Table 6-2.

Table 6-2. Pin List for M28975 AFE/Line Driver—Alphabetic Order

ETQFP	Signal Name
2	A12GND
43	A12GND
10	A33GND
12	A33GND
35	AFE_CLK
31	AFE_CTRL_DATA
36	AFE_RST
26	AFE_RX_SER1
25	AFE_RX_SER2
27	AFE_RX_SYNC
29	AFE_TX_SER1
30	AFE_TX_SER2
28	AFE_TX_SYNC
9	AVBIAS
32	DGND
40	LD_MH
39	LD_ML
46	LD_PH
47	LD_PL
42	LDAON
44	LDAOP
48	LDON
1	LDOP
24	No connect
37	No connect
8	RBIAS
4	RCDRVN
5	RCDRVP
34	SCAN_EN

ETQFP	Signal Name
3	VA12
41	VA12
45	VA12
11	VA33
13	VA33
38	VA33
16	VBGN
17	VBGP
14	VCMI
15	VCMO
23	VHN
22	VHP
33	VD33
18	VRNRX
6	VRNTX
19	VRPRX
7	VRPTX
21	VXN
20	VXP

6.2 ZipWirePlus Signal Descriptions

This section provides the signal descriptions for both the ZipWirePlus Transceiver/ Framer and ZipWirePlus AFE/Line Driver devices.

6.2.1 ZipWirePlus Transceiver/Framer Signal Descriptions

Table 6-3 lists the ZipWirePlus Transceiver/Framer signal (pin) descriptions.

Table 6-3. ZipWirePlus Transceiver/Framer Signal Definitions

Signal	Name	I/O	PU/ PD(1)	Description
Power and Ground				
VDD (VCORE)	DSP Core Voltage	—	—	Dedicated supply pins powering the DSP core. Must be connected to +1.8 V.
VDD0 (VIO)	I/O Voltage	—	—	Dedicated supply pins powering the I/O. Must be connected to +3.3 V.
VGNN (VESD)	5 V ESD Protection	—	—	Dedicated supply pins used to bias input protection diodes. If interfacing to other 5 V-powered devices, connect VGNN to +5 V; otherwise connect to +3.3 V.
GND	Ground	—	—	Common ground for ZipWirePlus device.
Clocks				
XTALI	Crystal Input	I	—	Crystal = 22.1184 MHz 3.3 V Input Level.
XTALO	Crystal Output	O	—	Connection point for the crystal.
XTALO_B	Crystal Clock Out	O	—	Buffered crystal oscillator output, 22.1184 MHz.
EXT_CLK_REF	Reference Clock	I/ O	—	8 kHz reference clock input or output.
PCM Interface				
RPCLK	Receive PCM Clock	O	—	Clocks the PCM receive outputs: RPDAT, RPMSYNC, and RPDROP. Normally derived by the internal clock recovery (DPLL). Can be derived from PEXTCLK or TPCLK.
PEXTCLK	PCM External Clock	I	(2)	Optionally sources the RPCLK or TPCLK or both RPCLK and TPCLK.
RPDPLLCLK	RX PCM DPLL Clock	O	—	DPLL clock output. This output can be used as a clock synthesizer when the DPLL is not being used for receive clock recovery. Alternately, transmit clock when operating as serial ATM interface.

Signal	Name	I/O	PU/	Description
RPDAT	Receive PCM Data	O	—	During specified time slots, data is clocked out by RPCLK. This pin can be optionally three-stated during inactive time slots or when DSL framer is bypassed. Alternately, receives data when operating as serial ATM interface.
RPEXTDAT	Receive PCM External Data	I	(2)	Used in multipair configuration, when receive PCM data from all channels needs to be routed through the master framer for PCM layer framing and overhead handling, like E1 PRA, CRC calculation, etc. Alternately, transmit start of cell when operating as serial ATM interface.
RPMFSYNC	Receive PCM Multiframe Sync	O	—	Active high output from the receive time base. Optionally, programmed to mark either frame or multi-frame boundaries during framed application. Alternately, receive start of cell when operating as serial ATM interface.
RPDROP	Drop Indicator	O	—	Active high output indicates when specific receive PCM time slots are present on RPDAT. Time slot size can be one, two, four, or eight bits long. This pin also controls the three-state output enable of RPDAT in multipair configuration.
PREFSYNC	Receive PCM Reference Sync	I/ O	—	Used in Multi-Pair configuration. When configured as a master, this output is the internal receive PCM time base reset which aligns the receive PCM time base of each slave to the master. When slave mode is selected, this signal is an RX PCM reset input (default).
TPCLK	Transmit PCM Clock	I	(2)	Normally samples the PCM transmit inputs: TPDAT, TPMSYNC, and TPINSDAT on the falling edge and clocks out TPINSEN on the rising edge. The edge transition is selectable.
TPDAT	Transmit PCM Data	I	(2)	During specified time slots, data is sampled by a selected clock source (TPCLK, PEXTCLK or DPLL recovery clock).
TPMFSYNC	Transmit PCM Multi-Frame Sync	I/ O	(4)	This input resets the transmit PCM time base during framed application and is ignored in unframed mode. This signal is internally delayed by a programmable bit and frame offset to coincide with TPDAT bit 0, frame 0. May be programmed to mark either frame or multi-frame boundaries.
TPINSDAT	Transmit PCM Insert Data	I	—	Alternate source of PCM transmits serial data. TPINSDAT replaces TPDAT when TPINSEN is active. Alternately, transmits data when operating as serial ATM interface.
TPINSEN	Transmit PCM Insert Enable	O	—	Active high output indicates when specific TPINSDAT time slots are sampled. Alternately, functions as receive clock when operating as serial ATM interface.
Narrowband Interface				
TNBDAT	Transmit NB data	I	(2)	During specified time slots, a selected clock source (TNBCLK, PEXTCLK, or DPLL recovered clock) samples data.
TNBCLK	Transmit NB clock	I	(2)	Normally, samples the NB transmits inputs: TNBDAT, TNBSYNC on the falling edge. Edge transition is selectable.

Signal	Name	I/O	PU/ PD[1]	Description
TNBSYNC	Transmit NB Multi Frame Sync	I/ O	[4]	When configured as an input, this signal resets the transmit NB time base during framed application and is ignored in unframed mode. This signal is internally delayed by a programmable bit and a frame offset to coincide with TNBDAT bit 0 frame 0. Optionally programmed to mark either frame or multiframe boundaries. When configured as an output, this signal is active high for internal transmit NB MF sync.
RNBDAT	Receive NB Data	O	—	During specified time slots, data is clocked out by RNBCLK. This pin can be optionally three-stated during inactive timeslots or when the DSL framer is bypassed.
RNBCLK	Receive NB Clock	O	—	Clocks the PCM receive outputs: RPDAT, RPHSYNC, and RPDROP. Normally derived by the internal clock recovery (DPLL). Can be derived by PEXTCLK or TNBCLK.
RNBSYNC	Receive NB Multiframe Sync	O	—	Active high output from the receive timebase. Optionally, programmed to mark either frame or multiframe boundaries during framed application.
RNBDROP	Receive NB Data Drop Indicator	0	—	Active high output indicates when specific receive NB time slots are present on RNBDAT. Time slot size can be one, two, four, or eight bits long. This pin also controls the three-state output enable of RNBDAT. Used when more than one NB port is connected to the NB system bus.
UTOPIA Interface				
ATM_RX_ADDR[0–4]	—	I	[2]	Functions as the address of the PHY device being selected for reception. Address 11111 (31 decimal) indicates a null PHY port.
ATM_RX_CLAV	—	O	—	Indicates a FIFO empty condition or cell available condition.
ATM_RX_DATA[0–15]	—	I	[2]	Functions as the address of the PHY device being selected for reception. Address 11111 (31 decimal) indicates a null PHY port.
ATM_RX_CLAV	—	O	—	Indicates a FIFO empty condition or cell available condition.
ATM_RX_DATA[0–15]	—	O	—	Receives data output to the ATM Layer.
ATM_RX_ENB	—	I	[3]	Enables data reception when asserted low.
ATM_RX_CLK	—	I	[2]	Clocks ATM_RX_DATA on the falling edge.
ATM_RX_PRTY	—	0	—	This pin is the parity calculated over the ATM_RX_DATA bus. Parity can be checked over ATM_RX_DATA [0–7] or ATM_RX_DATA [8–15]. This pin can represent either even or odd parity.
ATM_RX_SOC	—	0	—	Indicates the first byte of valid cell data transmitted when asserted high.
ATM_TX_ADDR[0–4]	—	I	[2	Functions as the address of the PHY device being selected for transmission. Address 11111 (31 decimal) indicates a null PHY port.

Signal	Name	I/O	PU/	Description
ATM_TX_CLAV	—	O	—	Indicates a FIFO full condition or cell available condition.
ATM_TX_DATA[0–15]	—	I	(2)	Transmits data from the ATM layer.
ATM_TX_ENB	—	I	(3)	Enables data transmission when asserted low.
ATM_TX_CLK	—	I	(2)	Used to sample ATM_TX_DATA on the falling edge.
ATM_TX_PRTY	—	I	(2)	This pin is the parity calculated over the ATM_TX_DATA bus. Parity can be checked over ATM_TX_DATA [0–7] or ATM_TX_DATA [8–15]. This pin can represent either even or odd parity.
ATM_TX_SOC	—	I	(2)	Indicates the first byte of valid cell data transmitted when asserted high.
HDSL Interface				
RHAUX	Receive Auxiliary Data	O	—	After descrambling, RHDAT is provided as an auxiliary channel and clocked out by HXCLK.
RHMARK	Receive Auxiliary Data Mark	O	—	Active high output indicates when specific DSL time slots are present on RHAUX. Optionally, this output provides gated HXCLK instead.
THAUX	Transmit Auxiliary Data	I	(2)	Alternate source of DSL transmit data. TAUX is mapped into selected DSL time slots when THLOAD is active.
THLOAD	Transmit Auxiliary Data Load	O	—	Active high output indicates when specific DSL time slots will be replaced by THAUX. Optionally, this pin provides gated HXCLK instead.
DSLSYNCI	DSL Reference Sync In	I	(2)	Used in multipair configuration to select the internal RDSL_REF_SEL for DPLL phase reference and RH_BSP reset. Alternatively, can be used as ATM one second input.
DSLSYNCO	DSL Reference Sync Out	O	—	The selected DSL sync for DPLL reference and RH_BSP reset is output in DSLSYNCO to allow cascading the framers in multipair configuration. Alternatively, can be used as ATM one second output.
Configuration Pins				
BOOT	BOOT Configuration Pin	I	—	See Section 5.3.
Reset				
RST	Reset	I	—	Asynchronous active-low input that places the device in an inactive state. This resets the DSP and internal 8051 blocks. This pin should be connected to the host processor's RST_OUT.
AFE Interface				
AFE_CLK	—		—	19–27 MHz AFE clock (always running). Connects directly to AFE pin AFE_CLK.

Signal	Name	I/O	PU/	Description
AFE_RST	—	O	—	Active-high output reset signal. Connects directly to AFE pin AFE_RST.
AFE_TX_SYNC	—	O	—	Tx serial data sync. Connects directly to AFE pin AFE_TX_SYNC.
AFE_RX_SYNC	—	O	—	Rx serial data sync. Connects directly to AFE pin AFE_RX_SYNC.
AFE_TX_SER1	—	O	—	Serial TX data sample one. Connects directly to AFE pin AFE_TX_SER1.
AFE_TX_SER2	—	O	—	Serial TX data sample two. Connects directly to AFE pin AFE_TX_SER2.
AFE_RX_SER1	—	I	—	Serial RX data sample one. Connects directly to AFE pin AFE_RX_SER1.
AFE_RX_SER2	—	I	—	Serial RX data sample two. Connects directly to AFE pin AFE_RX_SER2.
AFE_CTRL_DATA	—	I/ O	—	Serial control data input/output. Connects directly to AFE pin AFE_CTRL_DATA.
Host Port RAM Interface				
HP_ADR[0–9]	Host Port Address	I	—	Host port RAM address bits 0–9.
HP_DAT[0–7]	Host Port Data	I/ O	(4)	Host port RAM data bits 0–7.
HP_CS	Host Port Chip Select	I	(2)	Host port RAM chip-select. Active-low.
HP_WE	Host Port Write Enable	I	(2)	Host port RAM write enable. Active-low.
HP_OE	Host Port Output Enable	I	(2)	Host port RAM output enable. Active-low.
HP_INT	Host Port External Interrupt	O	—	Active-low interrupt that signifies the API protocol is complete. This output is totem-pole, and inactive (high) state when reset is applied to the device.
HP_CLK	Host Port Clock	I	(2)	Host port data, address, and control signal clock.
Serial Port Interface				
P12_RXD1	Debug Rx Data	I	—	Debug receive data.
P13_TXD1	Debug Tx Data	O	—	Debug transmit data.
P30_RXD0	RS232 Rx Data	I	—	UIP interface receive data.
P31_TXD0	RS232 Tx Data	O	—	UIP interface transmit data.
JTAG Interface				
TRST	Test Port Reset	I	PU	Active-low resets the TAP controller. If JTAG is not used, this pin should be tied high.

Signal	Name	I/O	PU/	Description
TDI	Test Data In	I	PU	JTAG test data input per *IEEE Std. 1149.1-1993.* Used for loading all serial instructions and data into internal test logic. Sampled on the rising edge of TCK. TDI can be left unconnected when not being used because it is internally pulled high.
TDO	Test Data Out	O	—	JTAG test data input per *IEEE Std. 1149.1-1993.* Three-state output used for reading all serial configuration and test data from internal test logic. Updated on the falling edge of TCK.
TCK	Test Clock	I	—	JTAG test data input per *IEEE Std. 1149.1-1993.* Used for all test interface and internal test logic operations. If unused, TCK should be pulled low.
TMS	Test Mode Select	I	PU	JTAG test data input per *IEEE Std. 1149.1-1993.* Input signal used to control the test logic state machine. Sampled on the rising edge of TCK. TMS can be left unconnected when not being used because it is internally pulled high.
Miscellaneous and Test Modes				
TESTMODE	—	I	—	Must be tied low (to GND).
TEST_E	—	I	—	Must be tied low (to GND).
NC1	—	I	—	Must be tied low (to GND).
TEST_AD0	—	I	—	Must be tied low with an external resistor.
TEST_AD1	—	I	—	Must be tied low with an external resistor.
TEST_AD2	—	I	—	Must be tied low with an external resistor.
NC2	—	I	—	Must be tied low (to GND).

FOOTNOTE:
(1) Internally Pulled-Up (PU) or Pulled-Down (PD) with a 50–200 KΩ resistor.
(2) When pin is not used, it should be externally tied low.
(3) When pin is not used it should be externally tied high.
(4) When pin is not used, it should be externally tied by a resister to high.

6.2.2 ZipWirePlus AFE Signal Descriptions

Table 6-4 lists the ZipWirePlus AFE signal (pin) descriptions.

Table 6-4. ZipWirePlus AFE Signal Descriptions

Signal Name	I/O	Description
Power and Ground		
VA12	—	+12 V analog supply
A12GND	—	Analog ground for +12 V analog supply
VA33	—	+3.3 V analog supply
A33GND	—	Analog ground for +3.3 V analog supply
VD33	—	+3.3 V digital I/O supply

Signal Name	I/O	Description
DGND	—	Digital I/O ground
Transmit Section		
LDOP	O	Transmit, positive (+) line driver output
LDON	O	Transmit, negative (–) line driver output
LDAOP	I	Transmit, auxiliary (+) line driver input
LDAON	I	Transmit, auxiliary (–) line driver input
RCDRVP	O	Transmit, positive (+) RC driver output
RCDRVN	O	Transmit, Negative (–) RC driver output
Transmit References		
VRPTX	REF	Transmit, positive (+) voltage reference
VRNTX	REF	Transmit, negative (–) voltage reference
Transmit Internal Signal		
LD_ML	—	Internal line driver signal
LD_MH	—	Internal line driver signal
LD_PH	—	Internal line driver signal
LD_PL	—	Internal line driver signal
Receive Section		
VXP	I	Receive, positive (+) transformer line input
VXN	I	Receive, negative (–) transformer line input
VHP	I	Receive, positive (+) hybrid analog input
VHN	I	Receive, negative (–) hybrid analog input
Receive References		
VRPRX	REF	Receive, Positive (+) Voltage Reference
VRNRX	REF	Receive, Negative (–) Voltage Reference
VBGP	REF	Reference, Positive (+) Band-gap Reference
VBGN	REF	Reference, Negative (–) Band-gap Reference
VCMO	REF	Reference, Output Common Mode Voltage
VCMI	REF	Reference, Input Common Mode Voltage
AVBIAS	REF	Reference, Compensation Capacitor
RBIAS	REF	Reference, Current Reference Resistor
DSP Interface		
AFE_CLK	I	19–27 MHz AFE clock (always running). Connects directly to DSP AFE_CLK.

Signal Name	I/O	Description
AFE_RX_SYNC	I	Rxdata strobe. Connects directly to DSP AFE_RX_SYNC.
AFE_TX_SYNC	I	Txdata strobe. Connects directly to DSP AFE_TX_SYNC.
AFE_RST	I/O	Active-high input reset signal. Connects directly to DSP AFE_RST.
AFE_CTRL_DATA	I/O	Serial control data input/output. Connects directly to DSP AFE_CTRL_DATA.
AFE_RX_SER1	O	Serial RX data sample one (LSB). Connects directly to DSP AFE_RX_SER1.
AFE_RX_SER2	O	Serial RX data sample two (MSB). Connects directly to DSP AFE_RX_SER2.
AFE_TX_SER1	I	Serial TX data sample one (LSB). Connects directly to DSP AFE_TX_SER1.
AFE_TX_SER2	I	Serial TX data sample two (MSB). Connects directly to DSP AFE_TX_SER2.
Miscellaneous and Test		
SCAN_EN	I	ASIC scan enable input, connect to logic low (GND).

7.0 Electrical and Mechanical Specifications

The following specifications apply to both the ZipWirePlus transceiver/framer and the ZipWirePlus AFE.

7.1 Specifications for the ZipWirePlus Transceiver/ Framer and ZipWirePlus AFE

7.1.1 Recommended Operating Conditions

Table 7-1. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
AFE 12.0 V Analog Supply	VA12	11.4	12.0	12.6	V
DSP 3.3 V Input/Output Supply	VIO	3.15	3.3	3.45	V
AFE 3.3 V Analog Supply	VA33	3.15	3.30	3.45	V
AFE 3.3 V Digital Supply	VD33	3.15	3.30	3.45	V
DSP 1.8 V Digital Core	VDD	1.71	1.80	1.89	V
GENERAL NOTE: A12GND = A33GND = GND = DGND = 0 V; other voltages with respect to 0 V.					

7.1.2 Recommended Power Sequencing

Power up sequencing involves the order of powering up the IO and core supplies and the period of time between powering up these supplies.

The recommended sequence for the M28975 is as follows:

5.0 V (VGNN)

3.3 V (VDDO, VD33 and VA33)

1.8 V (VDD)

There is no minimum or maximum time between supplies.

The sequencing of the 12.0 V (VA12) is not critical.

The M28975 contains power sequencing protection, which will place the output drivers in a high impedances state when the IO supply (3.3 V) is detected and place the output drivers in a low impedance state when the core supply (1.8 V) is detected. Without this power sequencing protection, when the IO supply (3.3 V) is powered up first, the output drivers can be in an indeterminate state until the core supply (1.8 V) is powered up. If this indeterminate state lasts long enough (several ms), the unknown state of the output drivers can cause system problems.

This power sequencing protection does not remove the requirement for the above power sequence. If the above power sequence is not followed, there will be potentially a large forward bias current drawn until the IO supply (3.3 V) is powered up. This can cause a reliability issue.

7.1.3 Absolute Maximum Ratings

Table 7-2. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units
VA12	VA12	—	12.0	—	V
VIO	VIO	–0.3	3.3	4.6	V
VA33	VA33	–0.3	3.30	3.45	—
VD33	VD33	–0.3	3.30	3.45	—
VDD	VDD	–0.3	1.8	2.5 V	V
Voltage on any Signal Pin	—	GND–0.3	—	VIO + 0.3	V
Input Current, any pin except supplies	IMAX	—	—	±10	mA
Analog Input Voltage	—	–0.3	—	VAA + 0.3	V
Digital Input Voltage for Transceiver and Framer	—	–0.3	—	V_{GNN} +0.3	V
Digital Input Voltage for AFE	—	–0.3	—	3.45	V
Ambient Operating Temperature	T_A	–40	25	+85	°C
Junction Temperature	T_J	—	—	125	°C
Storage Temperature (ambient)	T_{SA}	–65	—	150	°C

Parameter	Symbol	Min	Typ	Max	Units
Soldering Temperature	TSOL	–65	—	260	°C
Vapor Phase Soldering	TVSOL	–65	—	220	°C
Air Flow	0	—	0	—	L.F.P.M.

CAUTION

GENERAL NOTE: Operation beyond these limits may cause permanent damage to the device. Normal operation is not guaranteed at these extreme conditions.

7.2 Thermal Characteristics

7.2.1 ZipWirePlus AFE

For the 48-pin ETQFP (AFE) with 0 m/s of airflow, θ_{JA}~ 27 °C/W.

7.2.2 ZipWirePlus Transceiver/Framer

For the 13 × 13 mm FPBGA (transceiver/framer) with 0 m/s of airflow, θ_{JA}~ 44 °C/W.

For the 176-pin LQFP (transceiver/framer) with 0 m/s of airflow, θ_{JA}~ 32 °C/W.

7.3 Specifications for ZipWirePlus Transceiver/Framer Only

7.3.1 Power Dissipation

Table 7-3 shows the breakdown for the ZipWirePlus transceiver/framer power dissipation.

Table 7-3. ZipWirePlus Transceiver/Framer Power Dissipation

Parameter	Symbol	Min	Typ	Max	Units
DSP/Framer, +1.8 V 192 kbps 1,168 kbps 1,552 kbps 2,320 kbps	$PD_{DSP\ 1.8}$	—	 130 190 220 290	—	mW
DSP, +3.3 V 192 kbps 1,168 kbps 1,552 kbps 2,320 kbps	$PD_{DSP\ 3.3}$	—	 18 18 20 25	—	mW

7.3.2 DC Characteristics

Table 7-4 lists the transceiver's DC characteristics.

Table 7-4. Transceiver/Framer DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage	VIH	2.0	—	V_{GNN} +0.25	V
Input Low Voltage	VIL	0	—	0.8	V
Input Leakage Current	IIL/IIH	-40	—	40	nA
Input Capacitance	CIN	—	—	—	pF
Digital Outputs					
Output High Voltage	VOH	2.4	—	3.3	V
Output Low Voltage	VOL	—	—	0.4	V
Three-State Output Leakage	ILK	-40	—	40	nA
Output Capacitance	C_{OUT}	—	—	—	pF
Digital Bi-directionals					
Three-State Output Leakage	ILK	—	—	—	nA
Input/Output Capacitance	CINOUT	—	—	—	pF

7.3.3 Host Port RAM Interface Timing

Figure 7-1 and Figure 7-2 illustrate the host port RAM interface timing. Table 7-5 lists the host port RAM interface timing.

Figure 7-1. Host Port Write Cycle Timing

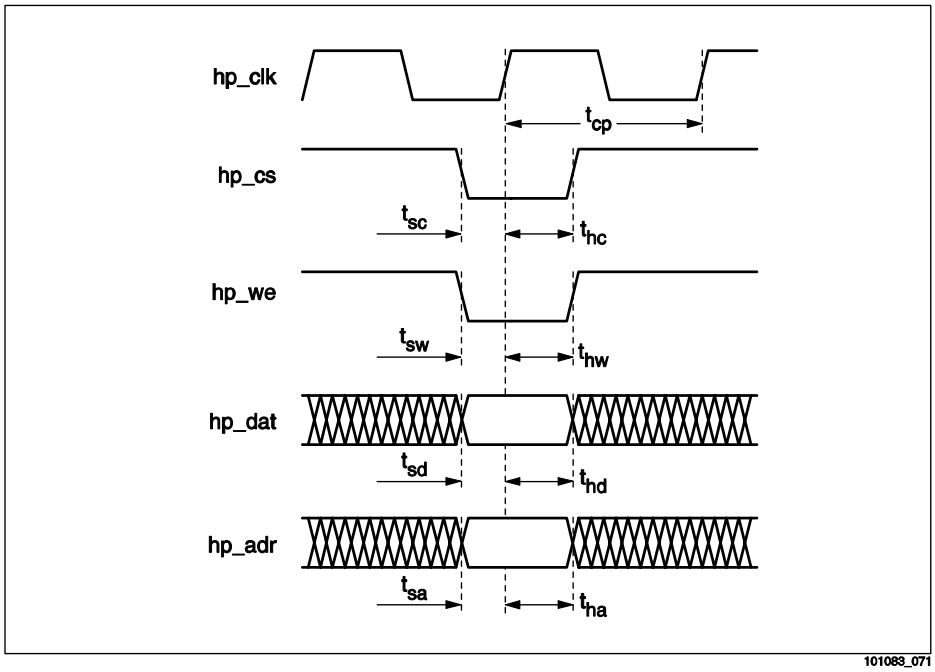


Figure 7-2. Host Port Read Cycle Timing

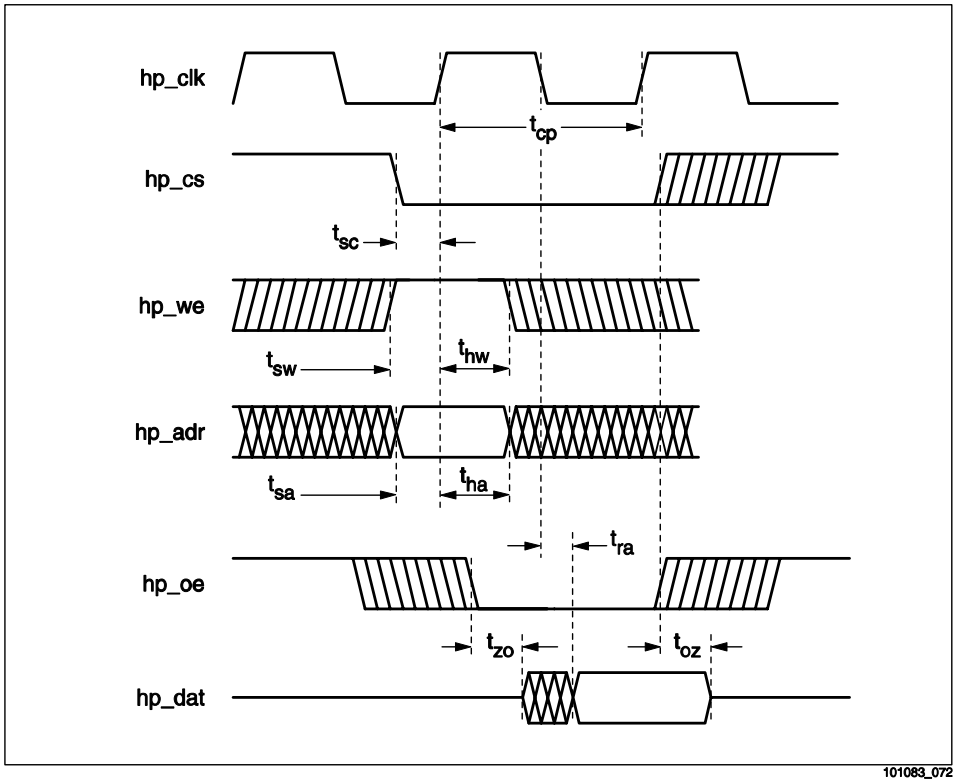


Table 7-5. Host Port Timing

Symbol	Parameter	Minimum	Maximum	Units
t_{cp}	Host port clock period	18	—	ns
t_{sc}	Chip select setup to hp_clk	1	—	ns
t_{hc}	Chip select hold after hp_clk	2	—	ns
t_{sw}	Write enable setup to hp_clk	1	—	ns
t_{hw}	Write enable hold after hp_clk	2	—	ns
t_{sd}	Data setup to hp_clk	2	—	ns
t_{hd}	Data hold after hp_clk	2	—	ns
t_{sa}	Address setup to hp_clk	1	—	ns
t_{ha}	Address hold after hp_clk	2	—	ns
T_{ra}	Read access time	—	8	ns
T_{zo}	Output enable to data driven	—	5	ns
T_{oz}	Output enable to data three-state	6	—	ns

7.3.4 DSL Framer Timing Requirements

Figure 7-3. Input Clock Requirements

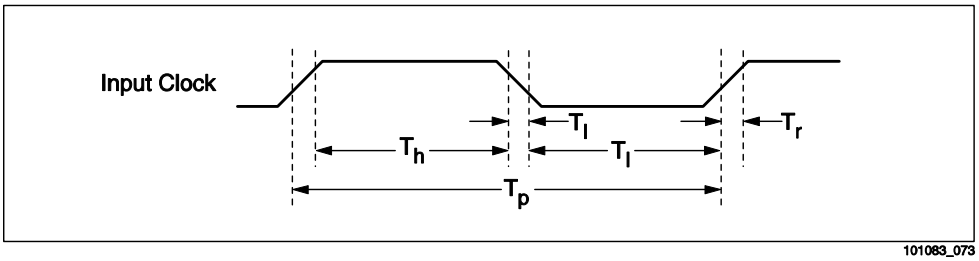


Table 7-6: Input Clock Timing

Symbol	Parameter	Minimum	Maximum	Units
—	TPCLK, PEXTCLK, TNBCLK	—	—	—
$1/T_p$	Frequency	0.064	18.432	MHz
T_h	Clock Width High	21.7	—	ns
T_1	Clock Width Low	21.7	—	ns
T_r	Clock Rise Time	—	20	ns
T_f	Clock Fall Time	—	20	ns

Figure 7-4. Input Setup and Hold Requirements

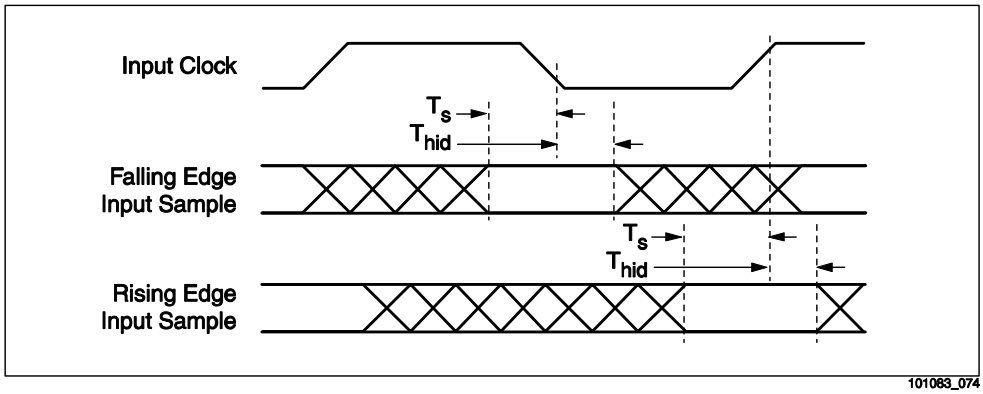


Table 7-7: Input Setup and Hold Timing

Symbol	Parameter	Minimum	Maximum	Units
—	TPDAT, TPINSDAT, TPMFSYNC, TNBDAT, TNBSYNC, SIF_TX_DATA, SIF_TX_SOC	—	—	—
T_s	Input Setup Time	35	—	ns
T_{hld}	Input Hold Time	10	—	ns

7.3.5 DSL Framer Switching Characteristics

Figure 7-5. Output Characteristics

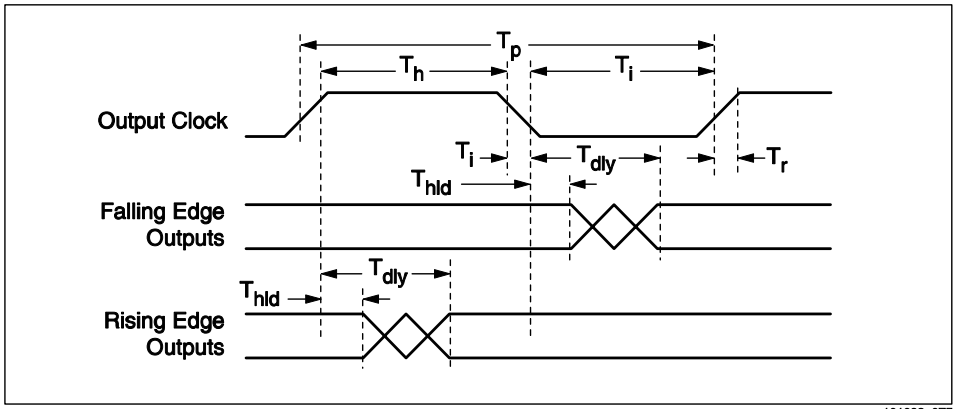


Table 7-8: Output Timing

Symbol	Parameter	Minimum	Maximum	Units
—	RPCLK, RPDPLLCLK, RNBCLK, SIF_TX_CLK, SIF_RX_CLK	—	—	—
$1/T_p$	Frequency	0.064	16.384	MHz
T_h	Clock Width High	Tp/2 – 20	Tp/2 + 20	ns
T_1	Clock Width Low	Tp/2 – 20	Tp/2 + 20	ns
T_r	Clock Rise Time	—	15	ns
T_f	Clock Fall Time	—	15	ns
—	RPDAT, RPDROP, RPMFSYNC, TPMFSYNC, SIF_RX_DATA, SIF_RX_SOC	—	—	—
T_{hld}	Output Data Hold	0	—	ns
T_{dly}	Output Data Delay	—	25	ns

7.3.6 UTOPIA Interface Timing

Figure 7-6 through Figure 7-7 and Table 7-9 through Table 7-10 show the timing requirements and characteristics of the UTOPIA interface.

Figure 7-6. UTOPIA Transmit Timing Diagram

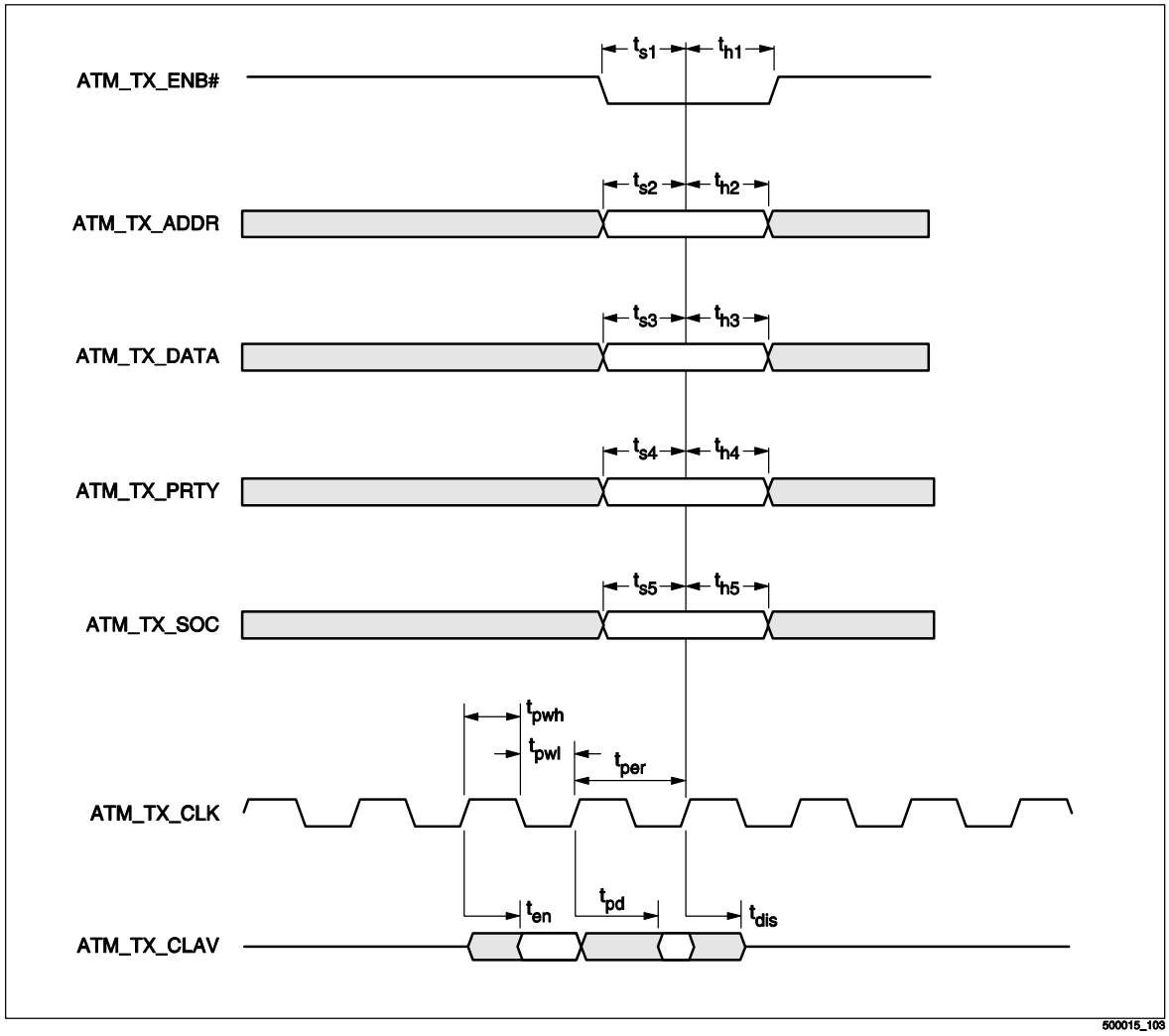


Table 7-9. UTOPIA Transmit Timing Table

Label	Parameter	Minimum	Maximum	Units
t_{pwl}	Pulse width low, ATM_TX_CLK	8	—	ns
t_{pwh}	Pulse width high, ATM_TX_CLK	8	—	ns
t_{per}	Period, ATM_TX_CLK	20	—	ns
t_{s1}	Setup, ATM_TX_ENB# to the rising edge of ATM_TX_CLK	4	—	ns
t_{h1}	Hold, ATM_TX_ENB# from the rising edge of ATM_TX_CLK	1	—	ns
t_{s2}	Setup, ATM_TX_ADDR to the rising edge of ATM_TX_CLK	4	—	ns
t_{h2}	Hold, ATM_TX_ADDR from the rising edge of ATM_TX_CLK	1	—	ns
t_{s3}	Setup, ATM_TX_DATA to the rising edge of ATM_TX_CLK	4	—	ns
t_{h3}	Hold, ATM_TX_DATA from the rising edge of ATM_TX_CLK	1	—	ns
t_{s4}	Setup, ATM_TX_PRTY to the rising edge of ATM_TX_CLK	4	—	ns
t_{h4}	Hold, ATM_TX_PRTY from the rising edge of ATM_TX_CLK	1	—	ns
t_{s5}	Setup, ATM_TX_SOC to the rising edge of ATM_TX_CLK	4	—	ns
t_{h5}	Hold, ATM_TX_SOC from the rising edge of ATM_TX_CLK	1	—	ns
t_{en}	Enable, ATM_TX_CLAV from the rising edge of ATM_TX_CLK	1	4	ns
t_{pd}	Propagation delay, ATM_TX_CLAV from the rising edge of ATM_TX_CLK	1	9	ns
t_{dis}	Disable, ATM_TX_CLAV from the rising edge of ATM_TX_CLK	1	4	ns

Figure 7-7. UTOPIA Receive Timing Diagram

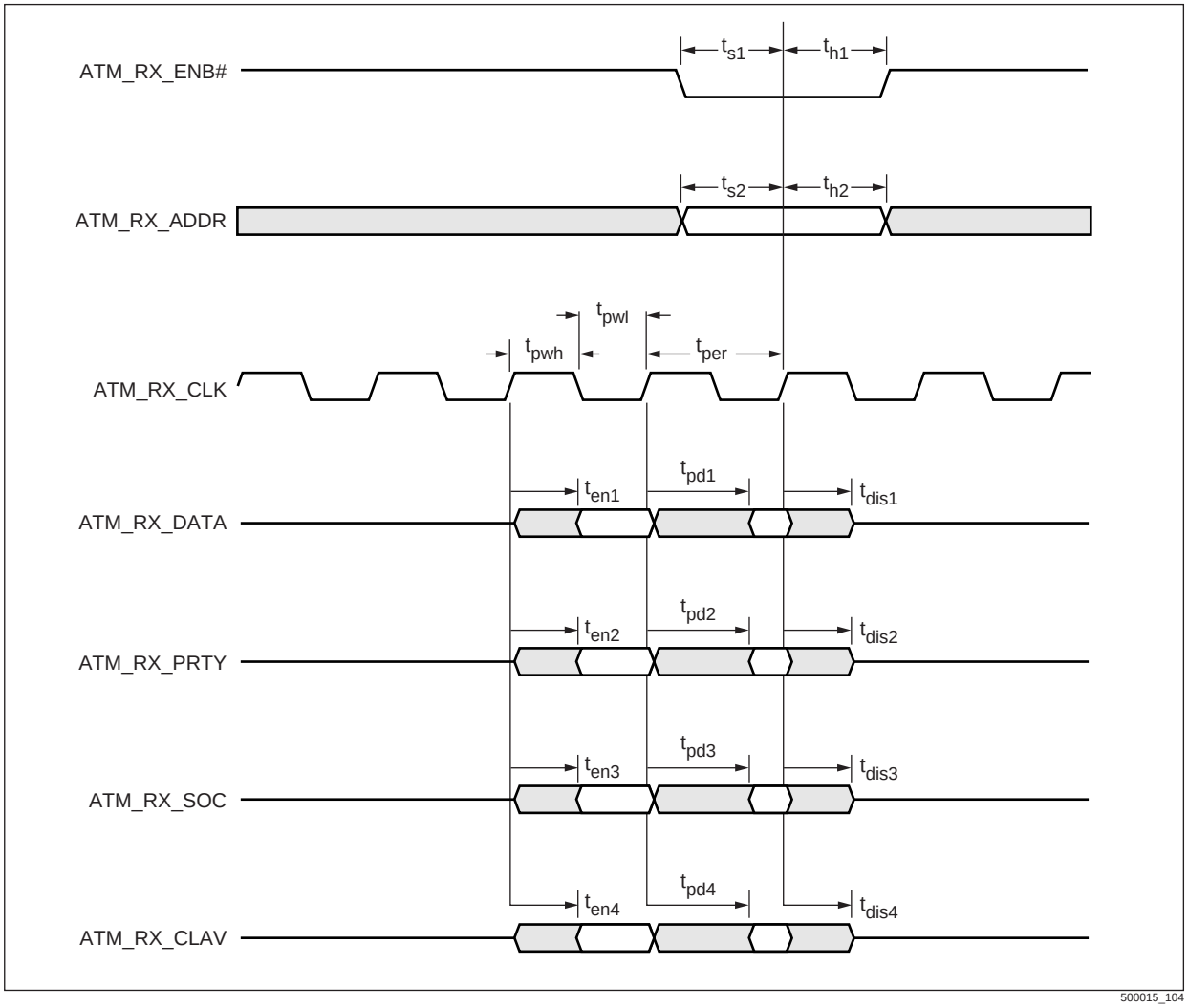


Table 7-10. UTOPIA Receive Timing Table

Label	Parameter	Minimum	Maximum	Units
t_{pwl}	Pulse width low, ATM_RX_CLK	8	—	ns
t_{pwh}	Pulse width high, ATM_RX_CLK	8	—	ns
t_{per}	Period, ATM_RX_CLK	20	—	ns
t_{s1}	Setup, ATM_RX_ENB# to the rising edge of ATM_RX_CLK	4	—	ns
t_{h1}	Hold, ATM_RX_ENB# from the rising edge of ATM_RX_CLK	1	—	ns
t_{s2}	Setup, ATM_RX_ADDR to the rising edge of ATM_RX_CLK	4	—	ns
t_{h2}	Hold, ATM_RX_ADDR from the rising edge of ATM_RX_CLK	1	—	ns
t_{en1}	Enable, ATM_RX_DATA[15:0] from the rising edge of ATM_RX_CLK	2	10	ns
t_{pd1}	Propagation Delay, ATM_RX_DATA[15:0] from the rising edge of ATM_RX_CLK	1	14	ns
t_{dis1}	Disable, ATM_RX_DATA[15:0] from the rising edge of ATM_RX_CLK	2	10	ns
t_{en2}	Enable, ATM_RX_PRTY from the rising edge of ATM_RX_CLK	2	10	ns
t_{pd2}	Propagation delay, ATM_RX_PRTY from the rising edge of ATM_RX_CLK	1	14	ns
t_{dis2}	Disable, ATM_RX_PRTY from the rising edge of ATM_RX_CLK	2	10	ns
t_{en3}	Enable, ATM_RX_SOC from the rising edge of ATM_RX_CLK	2	10	ns
t_{pd3}	Propagation delay, ATM_RX_SOC from the rising edge of ATM_RX_CLK	1	14	ns
t_{dis3}	Disable, ATM_RX_SOC from the rising edge of ATM_RX_CLK	2	10	ns
t_{en4}	Enable, ATM_RX_CLAV from the rising edge of ATM_RX_CLK	1	8	ns
t_{pd4}	Propagation delay, ATM_RX_CLAV from the rising edge of ATM_RX_CLK	1	8	ns
t_{dis4}	Disable, ATM_RX_CLAV from the rising edge of ATM_RX_CLK	1	8	ns

7.4 Specifications for ZipWirePlus AFE Only

The following specifications apply only to the ZipWirePlus AFE.

7.4.1 Power Consumption

Table 7-11 shows the breakdown for the Single Channel ZipWirePlus AFE power consumption for 1,552 kbps G.shdsl Enhanced Performance Asymmetric PSD (EPAP) and 2,320 kbps G.shdsl Symmetric PSD mode. Power consumption for other data rates will be similar.

These power values assume normal operating modes of random (scrambled) data with a 10 Kft. 26 AWG line

The maximum values are for worst case temperature, voltage, and silicon process.

The power consumption includes the power delivered to the DSL line. In EPAP mode, the power delivered to the load is ~100 mW. In symmetric PSD mode, the power delivered to the load is ~50 mW.

Figure 7-8. ZipWirePlus AFE Power Dissipation

Parameter	Condition	Symbol	Min	Typ	Max	Units
AFE, +12.0 V	EPAP	$PD_{AFE\ 12.0}$	—	420	—	mW
	Sym PSD		—	350	—	mW
AFE, +3.3 V	—	$PD_{AFE\ 3.30}$	—	410	—	mW

7.4.2 DC Characteristics

Table 7-11. AFE DC Characteristics.

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
Input High Voltage	VIH	2.50	—	3.45	V
Input Low Voltage	VIL	GND	—	0.4 V	V
Input Leakage Current	IIL/IIH	–10	—	10	µA
Input Capacitance	CIN	—	2.9	—	pF
Digital Outputs					
Output High Voltage	VOH	0.9 VIO	—	VIO	V
Output Low Voltage	VOL	GND	—	0.1 VIO	V
Three-State Output Leakage	ILK	10	—	10	µA

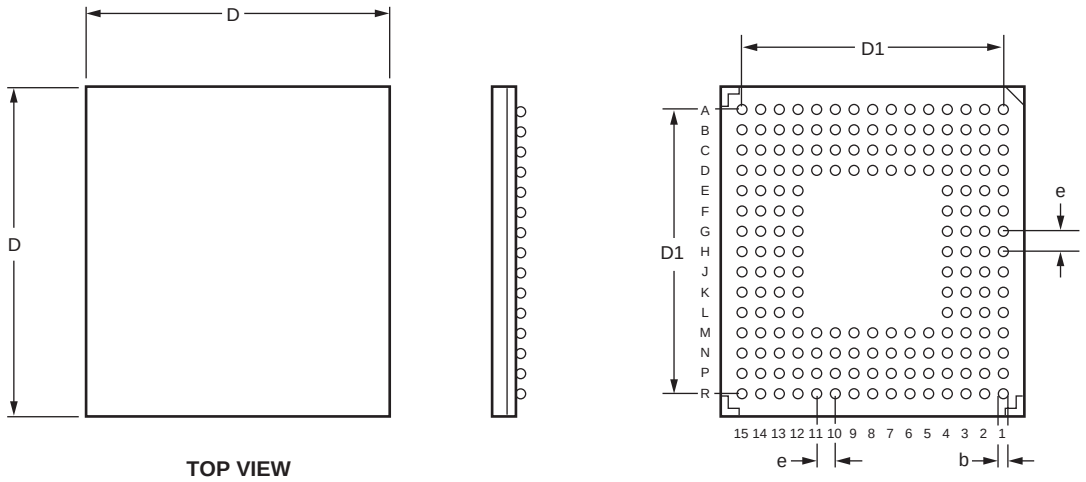
Parameter	Symbol	Min	Typ	Max	Units
Output Capacitance	CIN	—	3.1	—	pF
Digital Bidirectionals					
Three-State Output Leakage	ILK	–10	—	10	µA
Input/Output Capacitance	CINOUT	—	3.0	—	pF

7.5 Mechanical Specifications

7.5.1 The 13 x 13 mm FPBGA

Figure 7-9 illustrates the 13 × 13 FPBGA for the DSP/Framer.

Figure 7-9. Package Outline for 13 x 13 FPBGA



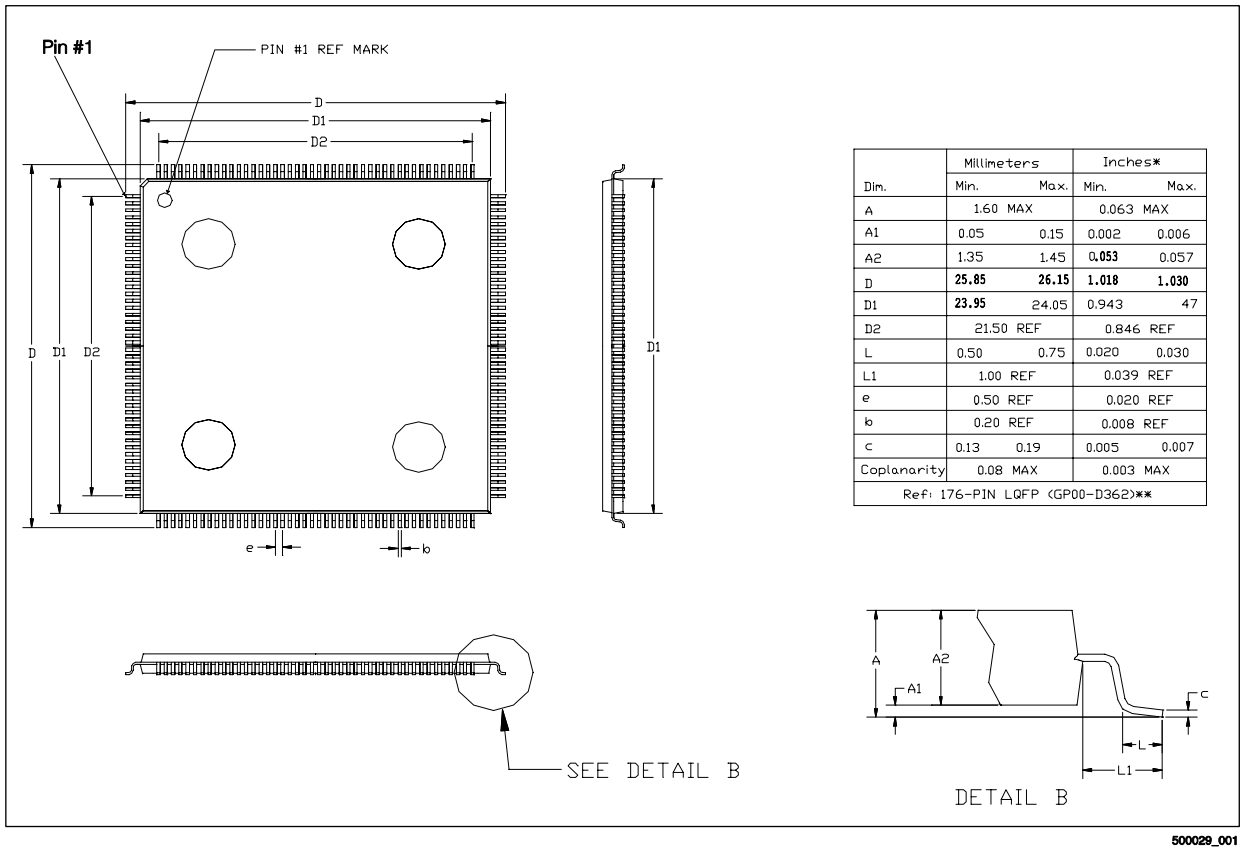
Dim.	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.41 MAX		0.056 MAX	
A1	0.31	0.41	0.012	0.016
A2	0.65	0.75	0.026	0.030
D	13.00 REF		0.512 REF	
D1	11.20 REF		0.441 REF	
M	15			
N	176			
e	0.80 REF		0.031 REF	
b	0.46 REF		0.018 REF	
c	0.29	0.39	0.011	0.015
Coplanarity	0.10 MAX		0.004 MAX	
Warpage	0.10 MAX		0.004 MAX	
Ref: 176-Pin FPBGA (GP00-D528-001)**				

101083_081

7.5.2 176-Pin LQFP

Figure 7-10 illustrates the 176-pin LQFP for the DSP/Framer.

Figure 7-10. Mechanical Drawing 176-Pin LQFP

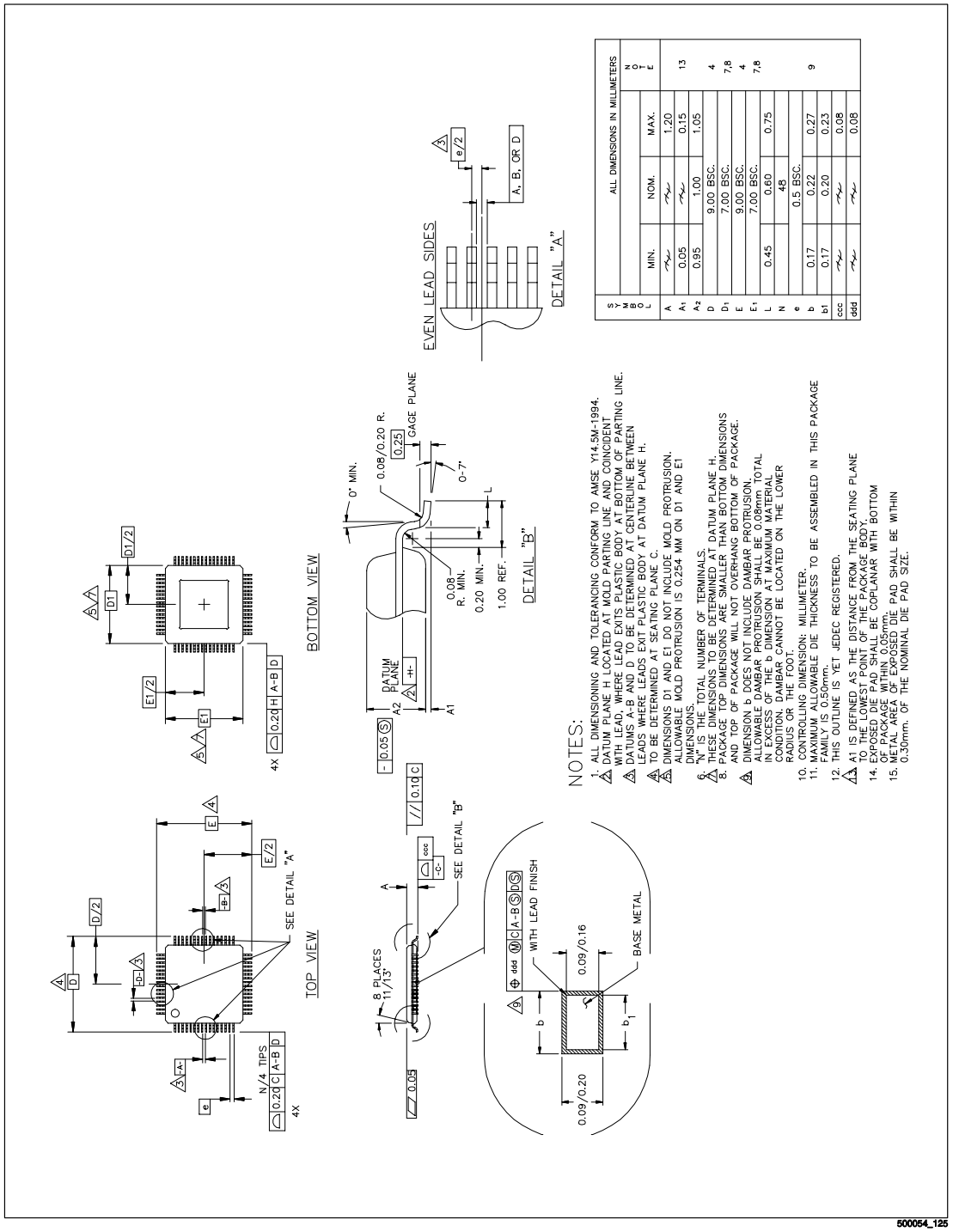


Dim.	Millimeters Min.	Millimeters Max.	Inches* Min.	Inches* Max.
A	1.60 MAX		0.063 MAX	
A1	0.05	0.15	0.002	0.006
A2	1.35	1.45	0.053	0.057
D	25.85	26.15	1.018	1.030
D1	23.95	24.05	0.943	47
D2	21.50 REF		0.846 REF	
L	0.50	0.75	0.020	0.030
L1	1.00 REF		0.039 REF	
e	0.50 REF		0.020 REF	
b	0.20 REF		0.008 REF	
c	0.13	0.19	0.005	0.007
Coplanarity	0.08 MAX		0.003 MAX	
Ref: 176-PIN LQFP (GP00-D362)**				

7.5.3 48-Pin ETQFP

Figure 7-11 illustrates the 48-pin ETQFP for the AFE/Line Driver

Figure 7-11. Top and Bottom View of a 7x7mm 48-pin ETQFP



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Appendix A: Power Consumption

Table A- 1: Power Consumption of the M28975 in Idle Mode/Reset Stage

MODE	Current (mA)				DSP Power/Port (W)	AFE Power/Port (W)	Total Power Per Port (W)
	1.8VDD DSP Core	3.3VDDO DSP I/O	3.3V AFE	12VAA AFE			
Idle	86.00	5.20	118.50	22.58	0.172	0.662	0.834
Hold Reset	80.00	4.89	87.30	0.17	0.160	0.290	0.450

Table A- 2: Power Consumption of the M28975 in HDSL2 Mode at 9 kft (26 AWG) Loop

DSL Line Rate (Kbps)	Current (mA)				DSP Power/Port (W)	AFE Power/Port (W)	Total Power Per Port (W)
	1.8VDD DSP Core	3.3VDDO DSP I/O	3.3V AFE	12VAA AFE			
1552	125.00	5.45	115.20	33.85	0.243	0.786	1.029

Table A- 3: Power Consumption of M28975 in G.hsdsl Mode at 9 kft (26 AWG) Loop in Annex A Symmetric Mode

DSL Line Rate (Kbps)	Current (mA)				DSP Power/Port (W)	AFE Power/Port (W)	Total Power Per Port (W)
	1.8VDD DSP Core	3.3VDDO DSP I/O	3.3V AFE	12VAA AFE			
144	n/a	n/a	n/a	n/a	n/a	n/a	n/a
200	65.00	4.95	113.00	30.01	0.133	0.733	0.866
208	65.00	4.95	113.10	29.85	0.133	0.731	0.865
272	68.00	4.97	113.20	29.01	0.139	0.722	0.860
392	73.00	5.01	113.20	28.44	0.148	0.715	0.863
400	73.00	5.01	113.10	28.40	0.148	0.714	0.862
528	79.00	5.05	113.30	28.17	0.159	0.712	0.871
776	90.00	5.13	113.40	28.16	0.179	0.712	0.891
784	91.00	5.15	113.70	28.21	0.181	0.714	0.895
1040	101.00	5.24	114.40	28.28	0.199	0.717	0.916
1168	105.00	5.27	114.10	28.32	0.206	0.716	0.923
1552	124.00	5.45	115.50	28.44	0.241	0.722	0.964

DSL Line Rate (Kbps)	Current (mA)				DSP Power/Port (W)	AFE Power/Port (W)	Total Power Per Port (W)
	1.8VDD DSP Core	3.3VDDO DSP I/O	3.3V AFE	12VAA AFE			
2056	144.00	5.58	115.30	28.62	0.278	0.724	1.002
2064	145.00	5.60	115.40	28.62	0.279	0.724	1.004
2312	161.00	5.80	118.50	28.62	0.309	0.734	1.043
2320	162.00	5.81	118.60	28.62	0.311	0.735	1.046

Table A- 4: CO, Annex A, Asymmetric, 9 Kft 26 AWG

DSL Line Rate (Kbps)	Current (mA)				DSP Power/Port (W)	AFE Power/Port (W)	Total Power Per Port (W)
	1.8VDD DSP Core	3.3VDDO DSP I/O	3.3V AFE	12VAA AFE			
1552	123.00	5.45	115.50	38.20	0.239	0.840	1.079

Table A- 5: CO, Annex B, Asymmetric, 9Kft 26 AWG

DSL Line Rate (Kbps)	Current (mA)				DSP Power/Port (W)	AFE Power/Port (W)	Total Power Per Port (W)
	1.8VDD DSP Core	3.3VDDO DSP I/O	3.3V AFE	12VAA AFE			
2056	142.00	5.58	116.50	35.26	0.274	0.808	1.082
2312	158.00	5.80	120.00	32.00	0.304	0.780	1.084

Appendix B: Surface Mount Application Note–FPBGA Package Family

B.1 Purpose

The Fine Pitch Ball Grid Array (FPBGA) package features a laminate BGA substrate with solder balls on a 1.0 mm or finer ball pitch. To make optimum use of this near chip scale package, the PWB must be designed with this technology in mind. This application note will focus on the specifics of integrating the FPBGA into the PWB design.

B.2 Solder Pad Geometry

For portable product applications where mechanical shock may occur, it is critical that the adhesion between the solder joint pads and the core material of the PWB does not fail. In order to overcome this failure mode, it is recommended that solder mask defined (SMD) pads be used. Table B- 1 shows the recommended solder joint pad diameter and solder mask opening diameter. Figure B- 1 shows a typical solder joint pad with dog bone trace to via. If micro via (150 µm or less) technology is available, the microvia can be placed directly in the solder joint pad. The recommended pad geometry is given in Figure B- 2.

Table B- 1: Recommended Pad Geometry

Solder Ball Pitch	Solder Ball Diameter	Solder Pad Diameter (D1)	Solder Mask Opening (D2)
1.0 mm	0.50 mm	0.53 mm	0.38 mm
0.8 mm	0.46 mm	0.45 mm	0.30 mm
0.5 mm	0.35 mm	0.35 mm	0.20 mm

Figure B- 1: Recommended SMD Pad Geometry using Standard via Technology

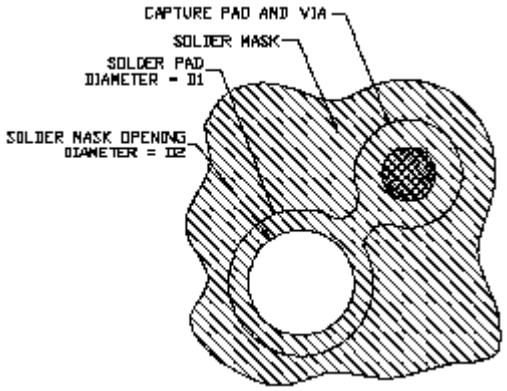
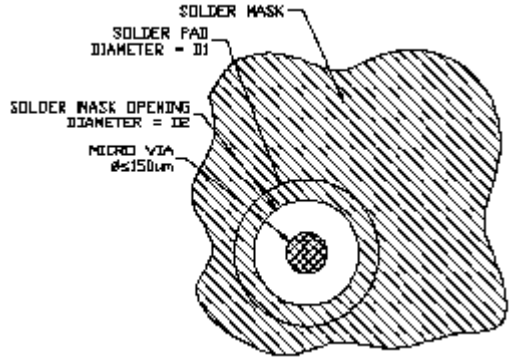


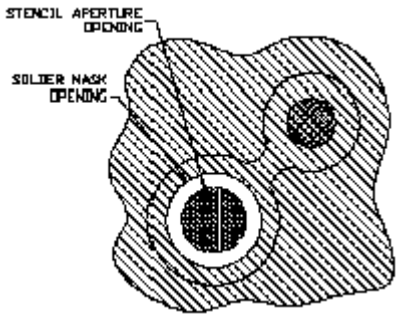
Figure B- 2: Recommended SMD Pad Geometry using Micro via Technology



B.3 Solder Stencil Determination

Solder and solder paste volume control is critical for SMT assembly of FPBGA packages onto the PWB. Stencil thickness and aperture openings should be optimized according to the optimal solder volume. In general, FPBGA packages can be reflowed on boards using a range of stencil thickness from 4 to 6 mils. Stencil thickness smaller than 4 mils should be avoided to prevent insufficient solder joint volume. To minimize the risk of shorting adjacent solder balls, it is suggested that the aperture opening for the solder pads be reduced to 2 mils smaller in diameter than the solder mask opening. See Figure B- 1 for detail. In general, the thicker the stencil, the smaller the aperture should be.

Figure B- 3: Recommended Stencil Aperture Opening for the FPBGA Solder Pad



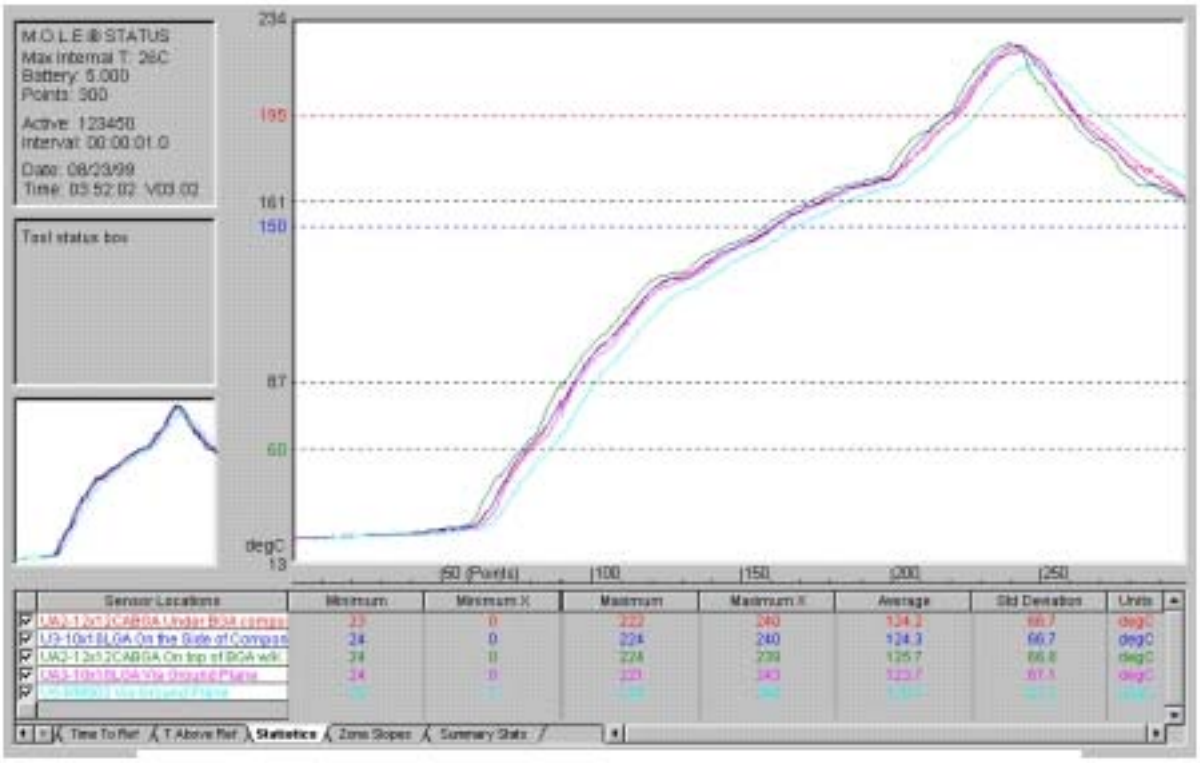
B.4 Solder Reflow Profile

Standard no-clean solder paste is generally recommended. If another type of flux is used, complete removal of flux residual may be necessary. Standard SMT reflow profiles can be used to surface mount the FPBGA packages to the PWB. A range of recommended parameters for the SMT reflow profile is listed in Table B- 2. Additional soak time and slower preheating time may be required to improve the outgassing of solder paste during SMT reflow.

Table B- 2: Recommended SMT Reflow Profile

Preheat Slope (ambient to 120 C)	1– 2 C/sec	Test Package	12x12-160 pin, 0.8 pitch
Soak Slope (120 to 183 C)	0.3– 0.6 C/sec	PWB	FR4
Time above reflow (> 183 C)	50– 80 sec	Solder Paste	No-clean Sn63Pb37
Peak Temperature	220 +/– 5 C	—	—
Cooling Rate	< 6 C/sec	—	—
Stencil	SS laser-cut, 5-mil thickness, trapezoidal	—	—

Figure B- 4: Typical Temperature Profile for Surface Mount of FPBGA



Appendix C: Surface Mount Application Note– ELQFP Package Family

C.1 Purpose

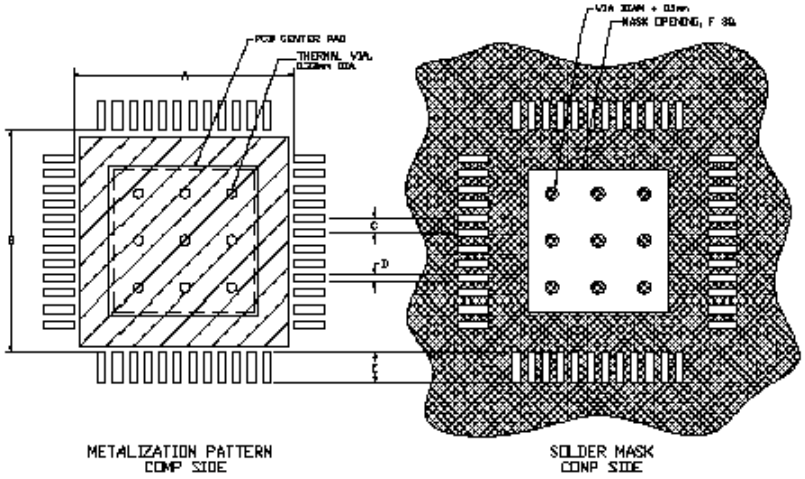
The ELQFP package features an exposed die paddle to improve both thermal and electrical performance. To make optimum use of these performance improvements, the PWB must be designed with this technology in mind. This application note focuses on the specifics of integrating the ELQFP with the PWB design.

C.2 Center Pad Geometry

To take advantage of ELQFP performance improvements, a solder-tinned-copper pad with thermal vias is required on the PWB. The pad size should be at least 0.25 mm larger on all sides than the dimensioned exposed pad on the device technical specification sheet with the solder mask opening equal to the dimensioned exposed pad on the sheet. The result is a solder mask defined pad.

An array of 0.33 mm diameter thermal vias plated with 1 oz. copper should be placed within the exposed region of the pad and shorted to the ground plane of the PWB. This thermal via pattern represents a copper cross section in the barrel of the thermal via of approximately 1% of the total center pad area. If the plating thickness is not sufficient to effectively plug the barrel of the via when plated, then solder mask should be used to cap the vias with a dimension equal to the via diameter +0.1 mm minimum. This will prevent the solder from being wicked through the thermal via and potentially creating a solder void in the region between the package bottom and the center pad on the surface of the PWB. Figure C- 1 shows the copper pad footprint, thermal vias and the solder mask opening defining the center pad.

Figure C- 1: Top Metalization and Solder Mask Definition for the 48ld ELQFP, where A = B = 7.40 mm, C = 0.50 mm, D = 0.25 mm, E = 1.00 mm, and F = 4.70 mm



C.3 Solder Stencil Determination

A general guideline would be to use the thickest solder stencil that works well for the products being assembled for the most process margin in assembling thermally enhanced packages to a PWB. A standoff height of 2.0 to 4.2 mils provides good solder joints for both the leads and the center pad. This is achieved using a stencil thickness of 5, 6, or 7 mils.

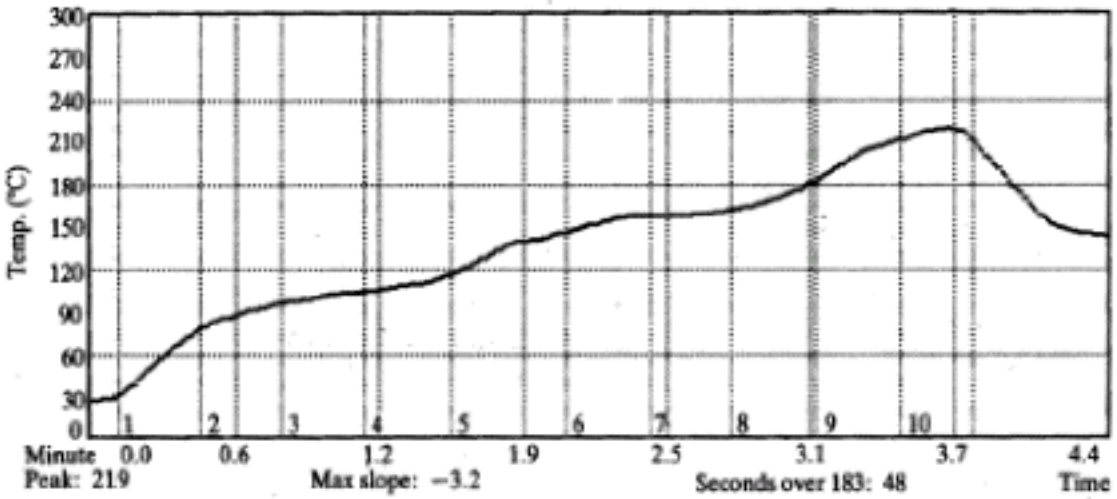
C.4 Solder Reflow Profile

The ELQFP reflow profile for board assembly does not have to be modified from the standard LQFP reflow profile because the construction of the package does not add thermal mass. Additional, the only new thermal load is due to the increased solder area between the exposed die pad on the package and the center pad on the PWB. A range of recommended parameters for the SMT reflow profile is listed in Table C- 1. Additional soak time and slower preheating time may be required to improve the outgassing of solder paste during SMT reflow. Figure C- 2 shows a typical reflow profile for the 48 pin ELQFP.

Table C- 1: Recommended SMT Reflow Profile

Preheat Slope (ambient to 120 C)	1–2 C/sec	Test Package	48 pin ELQFP
Soak Slope (120 to 183 C)	0.3–0.6 C/sec	PWB	FR4
Time above reflow (>183 C)	50–80 sec	Solder Paste	No-clean
—	Sn63Pb37	—	—
Peak Temperature	220 +/–5 C	—	—
Cooling Rate	< 6 C/sec	—	—
Stencil SS laser-cut, 5-mil thickness	—	—	—

Figure C- 2: Typical Temperature Profile for Surface Mount of ELQFP



Belt speed = 38.00 inches/minute

ZONE SETPOINTS

1	2	3	4	5	6	7	8
160	125	115	110	190	190	160	190

9	10
265	260

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Appendix D: Exposed Pad Thin Quad Flat Pack (ETQFP)

Abstract

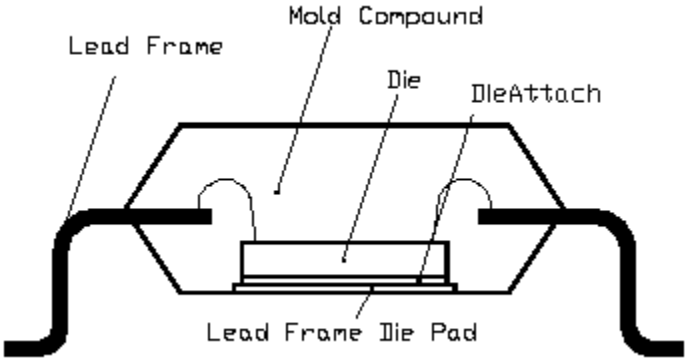
The Exposed Thin Quad Flat Pack (ETQFP) package provides greater design flexibility and increased thermal efficiency, while using a standard size IC Package. Exposed pad improved performance permits higher clock speeds, more compact systems, and more aggressive design criteria. ETQFP thermal performance is better than in standard packages. However, in order to make optimum use of the thermal efficiencies designed into the ETQFP, the PCB must be designed with this package in mind. The following sections of this document provide more information regarding the thermal performance and PWB design for Mindspeed ETQFPs.

D.1 Introduction

The ETQFP is implemented using a standard epoxy-resin package mold compound. The integrated circuit die is attached to the lead-frame die pad using a thermally conductive epoxy. The lead frame is designed with a deep downset of the die attach pad so that it is exposed on the bottom surface of the package after mold. This provides an extremely low thermal resistance between the IC junction and the exterior of the surface.

The external surface of the die pad can be attached to the PCB using standard solder reflow techniques. This allows efficient attachment to the board, and permits the board structure to be used as a heat sink for the IC. Using thermal vias, the lead frame die pad can be attached to a ground plane or special heat sink structure designed into the PCB. Figure D- 1 shows the schematic of the package components.

Figure D- 1: Schematic Representation of the Package Components



D.2 Package Thermal Characterization

D.2.1 Heat Removal Path

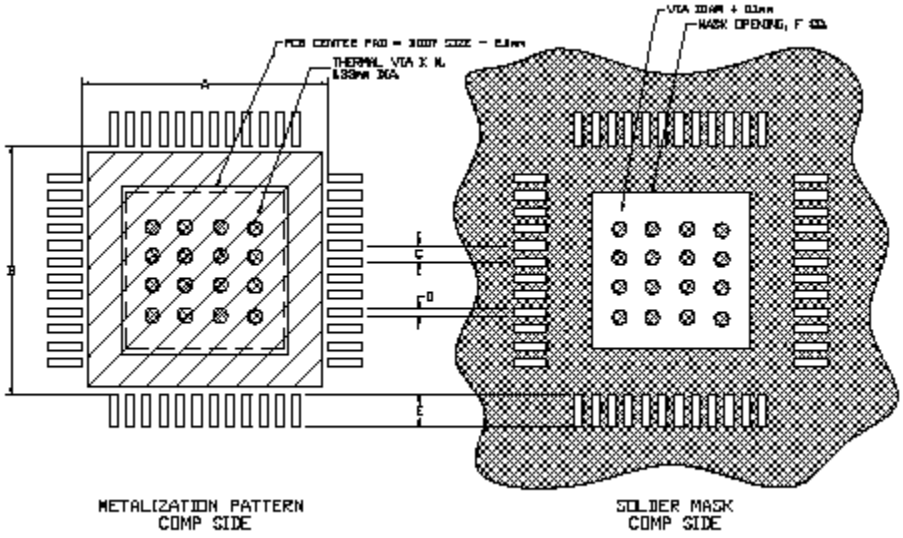
The internal heat removal path is designed to transfer heat from the top surface of the die to the die pad and then directly to the Printed Circuit Board (PCB) through a center solder pad. The PCB must be designed to remove heat from the package efficiently. At a minimum, there must be an area of solder-tinned-copper underneath the ETQFP, called a thermal land. Heat is transferred from the thermal land to the environment through thermal vias designed within the PCB structure.

D.2.2 Thermal Lands

A thermal land is required on the surface of the PCB directly underneath the body of the exposed package. During normal surface mount re-flow, the exposed pad on the underside of the package is soldered to this thermal land to create an efficient thermal path. The size of thermal path is as large as needed to dissipate the required heat.

For simple double-sided PCBs having no internal layers, the surface layers must be used to remove heat. Figure D- 2 shows a sample package detail, including required solder mask and thermal land pattern for an EQTFP. The designer may consider external means of heat conduction, such as attaching the copper planes to a convenient chassis member or other hardware convection.

Figure D- 2: Package and PCB Land Configuration



An array of 0.33 mm diameter thermal vias plated with 1 oz. copper must be placed on the pad and shorted to the ground plane of the PCB. If the plating thickness in the exposed region of the center pad is not sufficient to effectively plug the barrel of the via when plated, then solder mask should be used to cap the vias; the mask diameter should have a dimension equal to the via diameter + 0.1 mm minimum. This will prevent the solder from wicking through the thermal via, potentially creating a solder void in the region between the package bottom and the center pad on the surface of the PCB. Table D- 1 shows the dimensions for the entire ETQFP package family.

Table D- 1: Dimensional Parameters (mm)

Package Type	A	B	C	D	E	F	Recommended Array of Thermal Vias
48 pin ETQFP	7.40	7.40	0.50	0.25	1.00	25 sq.	5 x 5
64 pin ETQFP	10.40	10.40	0.50	0.25	1.0	56.25	8 x 8
80 pin ETQFP	14.40	14.40	0.50	0.25	1.0	106.09	10 x 10

D.3 PCB Design

Thermal vias are the primary method of heat transfer from the PCB thermal land to the internal copper planes or to other heat removal sinks. The number of vias, the size of the vias used, and the construction of the vias is important in obtaining the best package thermal performance and the package/PCB assembly. Thermal performance analysis shows that there is a point of diminishing returns where additional vias will not improve heat transfer through the board, which is a function of die size and the number of thermal via. The PCB internal structure plays a very important role in package thermal performance. Figure D- 3 and Figure D- 4 show the PCB structure for a 2- and a 6-layer design, respectively. PCB designs with more than two layers should have all thermal vias connected to the ground plane.

Figure D- 3: Internal Structure for a Two Layer PCB.

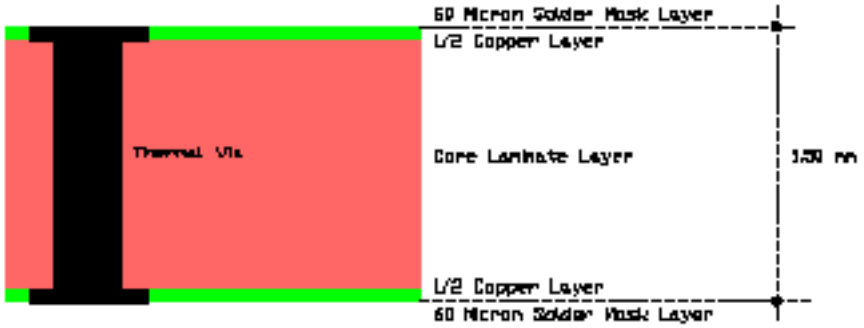
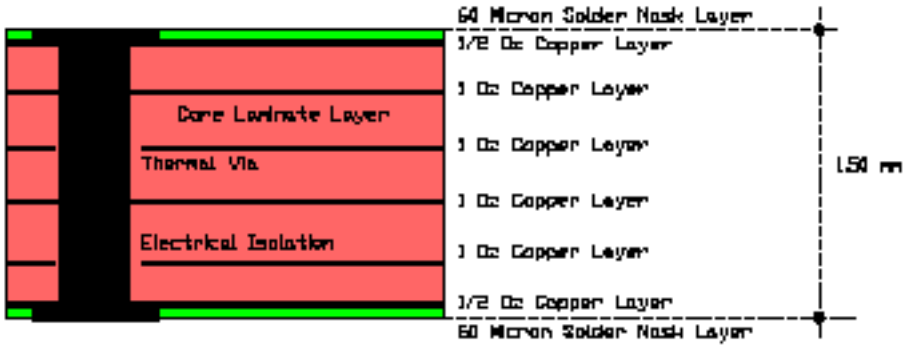


Figure D- 4: Internal Structure for a Six Layer PCB

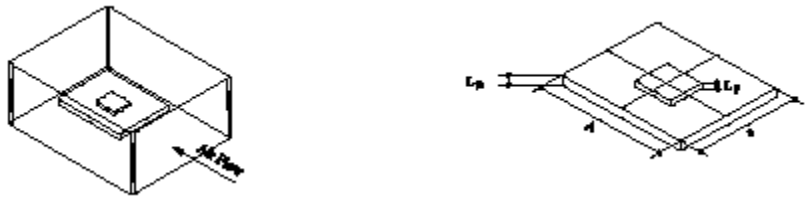


D.4 Thermal Test Structure

D.4.1 Test Environment

Package thermal performance has been tested following JEDEC standards. The ETQFP package is mounted at the center of a 100 mm x 100 mm six layer test board and is tested under different air flow velocities. Figure D- 5 shows the system configuration.

Figure D- 5: Test Performance Structure (A = 100 mm, B = 100 mm, LP = 1.40 mm, LB = 1.60 mm)



D.4.2 Thermal Test Boards

Two different test boards have been used to evaluate package thermal performance for both worst and best conditions. Table D- 1 shows the specifications of these test boards.

Table D- 2: Specification for a Two-layer Test Board

Drawing Number	TR03-T1
Substrate Material	FR-4
Thickness	1.6 mm
Stackup (# signal layers, # Cu planes)	1S0P
Cu Coverage (signal layer - top/bottom)	10%
Cu Coverage (power/gnd layer)	100%
Inner Cu Thickness (spec)	35□3.5

Table D- 3: Specification for a Four-layer Test Board

Drawing Number	TR03-T1
Substrate Material	FR-4
Thickness	1.6 mm
Stackup (# signal layers, # Cu planes)	1S2P

Drawing Number	TR03-T1
Cu Coverage (signal layer - top/bottom)	10%
Cu Coverage (power/gnd layer)	100%
Inner Cu Thickness (spec)	35□3.5

D.5 Package Thermal Performance

D.5.1 Calculation Guidelines

Maximum junction temperature can be calculated as:

$$T_j = P \times \theta_{ja} + T_a \quad (1)$$

Where:

θ_{ja} = Equivalent Package Thermal Resistance (C/W)

T_j = Maximum Junction Temperature (C)

T_a = Ambient Temperature (C)

P = Package Total Power Dissipation Value (W)

D.5.2 Package Thermal Resistance

Delco thermal test chips are used to estimate package thermal performance. Table D- 4 shows thermal die specifications

Table D- 4: Specification for Delco Thermal Test Chips

Manufacturer	Delco	Delco	Delco
Dimensions	3.81 mm x 3.81 mm	6.35 mm x 6.35 mm	7.8 mm x 7.8 mm
Thickness	0.33 mm	0.45 mm	0.5 mm

Figure D- 6 shows package thermal resistance as a function of airflow velocity for a 48 ETQFP package using two different test boards, specified in Table D- 1 and Table D- 3 and a prediction for a 6-layer PCB design. Figure D- 7 and Figure D- 8 show the similar information for a 64 and 80 ETQFP package. Table D- 5 shows the test condition for each package type.

Table D- 5: Test Conditions

Package Type	48 EQTFP	64 ETQFP	80 ETQFP
Body Size	7 mm x 7 mm	10 mm x 10 mm	14 mm x 14 mm
Die Size	3.81 mm x 3.81 mm	6.35 mm x 6.35 mm	7.8 mm x 7.8 mm
Die Pad Size	5 mm x 5 mm	7.50 mm x 7.50 mm	9.50 mm x 9.50 mm

Figure D- 6: Package Thermal Resistance as a Function of Airflow Velocity for a 48 ETQFP

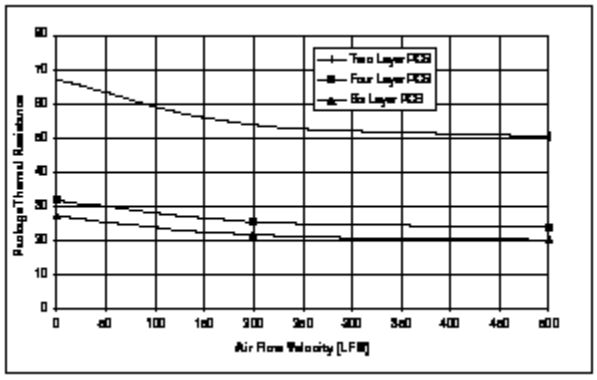


Figure D- 7: Package Thermal Resistance as a Function of Airflow Velocity for a 64 ETQFP

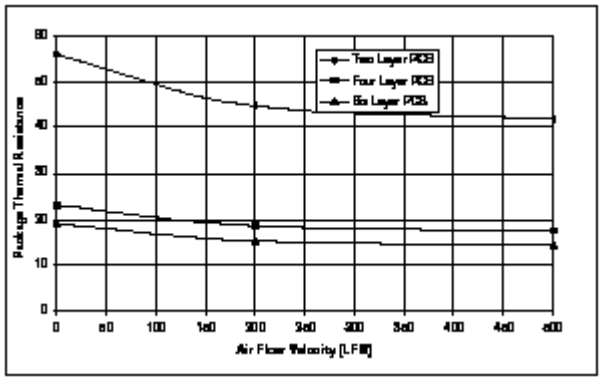
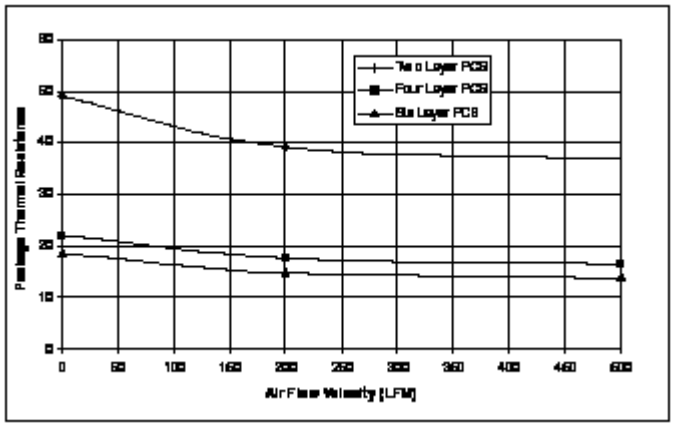


Figure D- 8 illustrates the package thermal resistance as a function of airflow velocity for a 80 ETQFP. Package. Table D- 1 shows the test conditions.

Figure D- 8: Package Thermal Resistance as a Function of Airflow Velocity for a 80 ETQFP



D.6 Solder Stencil Determination

The thickest possible solder mask, consistent with the components being assembled to the PWB and the with the PWB surface mount process, should be used. A standoff height of 2.0 to 4.2 mils provides good solder joints for both the leads and the center pad. This is achieved using a stencil thickness of 5, 6, or 7 mils.

D.7 Solder Reflow Profile

The ETQFP uses the standard TQFP re-flow profile because the ETQFP package construction does not add thermal mass. There is minimal additional thermal load due to the increased solder area between the exposed die pad on the package and the center pad on the PCB. Figure D- 9 and Figure D- 10 show typical IR reflow profiles for Sn63:Pb37 solder in the cases of natural convection and forced convection ovens.

Figure D- 9 illustrates the typical IR Reflow Profile for Eutectic Sn63:Pb37. Peak temperature should be approximately 220 °C, and the exposure time should normally be less than 1.0 minute at temperatures above 183 °C.

Figure D- 9: IR Reflow Profile

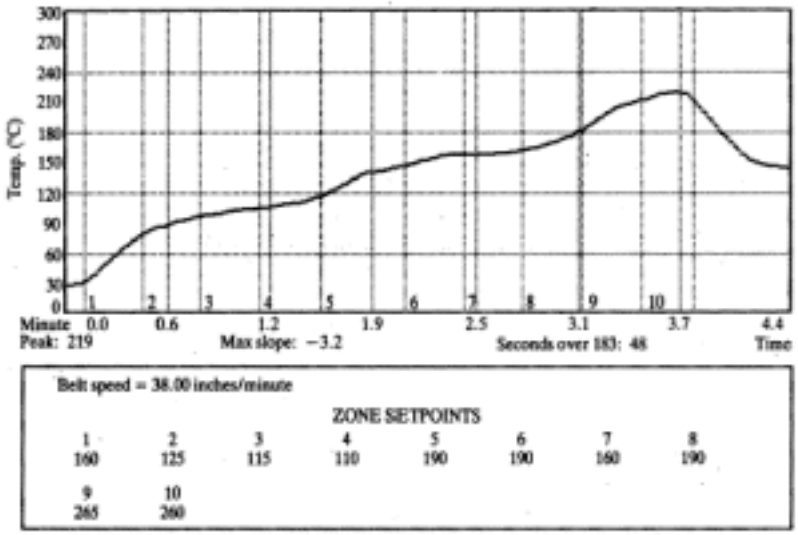
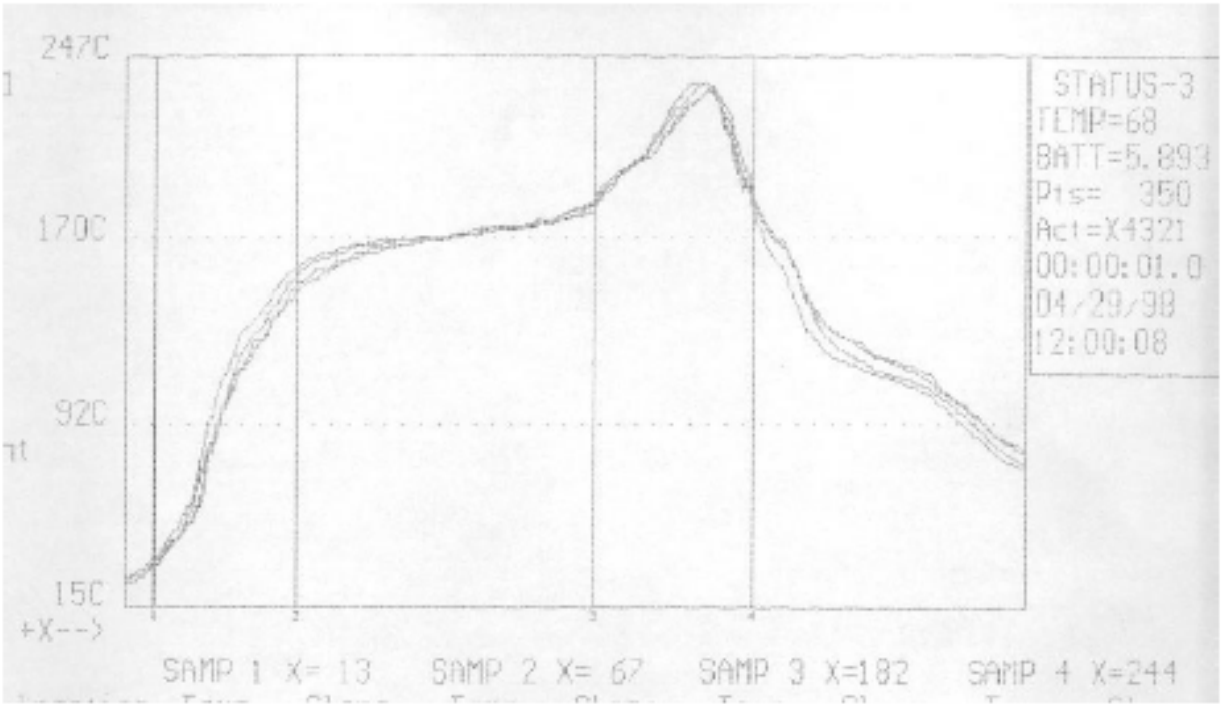


Figure D- 10 illustrates the typical Forced Convection Reflow Profile for Eutectic Sn63:Pb37. Peak temperature should be approximately 235 °C, and the exposure time should normally be less than 1.2 minutes at temperature above 183 °C. Belt speed = 30 inches/minute (top and bottom setting), fan speed = 2500 RPM, and nitrogen level = 1200 SCFH.

Figure D- 10: Forced Convection Reflow Profile



NOTE:	ZONE 1 = 185°C ZONE 2 = 185°C ZONE 3 = 175°C ZONE 4 = 175°C ZONE 5 = 180°C ZONE 6 = 190°C ZONE 7 = 230°C ZONE 8 = 270°C

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Appendix E: Acronyms and Abbreviations

ADC (A/D)	Analog-to-Digital Converter
AFE	Analog Front End
AIS	Alarm Indication Signal
ANSI	American National Standards Institute
API	Application Programming Interface
ATM-TC	Asynchronous Transfer Mode-Transmission Convergence
BER	Bit Error Rate
BGA	Ball Grid Array
BP	Bit Pump
BPV	Bipolar Violation
BT	Bit Pump Transceiver
CAS	Channel Associated Signaling
Channel Unit	HDSL Framer (name comes from HDSL1 Framer)
CRC-N	Cyclic Redundancy Check-N
CU	Channel Unit or HDSL Framer
DAC (D/A)	Digital-to-Analog Converter
DFE	Decision Feedback Equalizer
DIP	Dual In-Line Package
Downstream	From the HTU-C towards the HTU-R (includes regenerators)
DPLL	Digital Phase Lock Loop
DSD	DSL Sync Detector
DSL	Digital Subscriber Line
DSL Framer	ZipWirePlus DSL Framer Block
DSP	Digital Signal Processor
EC	Echo Canceller
EOC	Embedded Operations Channel

ETQFP	Exposed Pad Twin Quad Flat Pack
ETSI	European Telecommunications Standards Institute
EVM	Evaluation Module
FEBE	Far End Block Error (the far end reported a CRC error)
FEXT	Far End Cross Talk
FFE	Feed Forward Equalizer
FIFO	First-In First-Out
FPBGA	Fine Pitch Ball Grid Array
FR	Framer
H2TU	HDSL2 Terminal Unit
HDLC	High-Level Data Link Controller
HDSL	High-Bit-Rate Digital Subscriber Line
HEC	Head Error Control
HTU	HDSL Terminal Unit
HTU-C or COT or LTU	Central Office Terminal or Local Terminal Unit
HTU-R or RT or NTU	Remote Terminal or Network Terminal Unit
LED	Light Emitting Diode
ITU	International Telecommunications Union
LOS	Loss of Signal
LQFP	Low Profile Quad Flat Pack
MPU	Micro Processor Unit
NEXT	Near End Cross Talk
NNI	Network Node Interface
NP0	Negative Positive Zero
OOF	Out of Frame
P2MP	Point to Multipoint
PAM	Pulse Amplitude Modulation
PCM	Pulse Code Modulation
PLL	Phase Lock Loop
PPM	Parts per Million
PRA	Primary Rate Access
PRBS	Pseudo-Random Bit Sequence
PSD	Power Spectral Density
RAM	Random Access Memory

ROM	Read Only Memory
SBID	Stuff Bit ID
SES	Severe Error Second
SIF	Serial Interface
STP	Serial Test Port
TC	Transmission Convergence
TCM	Time Code Modulation
TQFP	Thin Quad Flat Pack
Transceiver	ZipWirePlus DSP/Transceiver Block
UART	Universal Asynchronous Receive Transmit
UIP	User Interface Program
UNI	User Network Interface
Upstream	From the HTU-R towards the HTU-C (includes regenerators)
UTOPIA	Universal Test and Operations PHY Interface for ATM
WL	Water Level

MINDSPEED™

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