REJ03B0002-0100Z
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# 1. Overview

The M16C/1N group consists of single-chip microcomputers that use high-performance silicon gate CMOS processes and have a on-chip M16C/60 series CPU core. The microcomputers are housed in 48-pin plastic mold QFP package. These single-chip microcomputers have both high function instructions and high instruction efficiency and feature a one-megabyte address space and the capability to execute instructions at high speed.

## 1.1 Applications

Automotive and industrial control systems, other automobile, other

## 1.2 Performance Overview

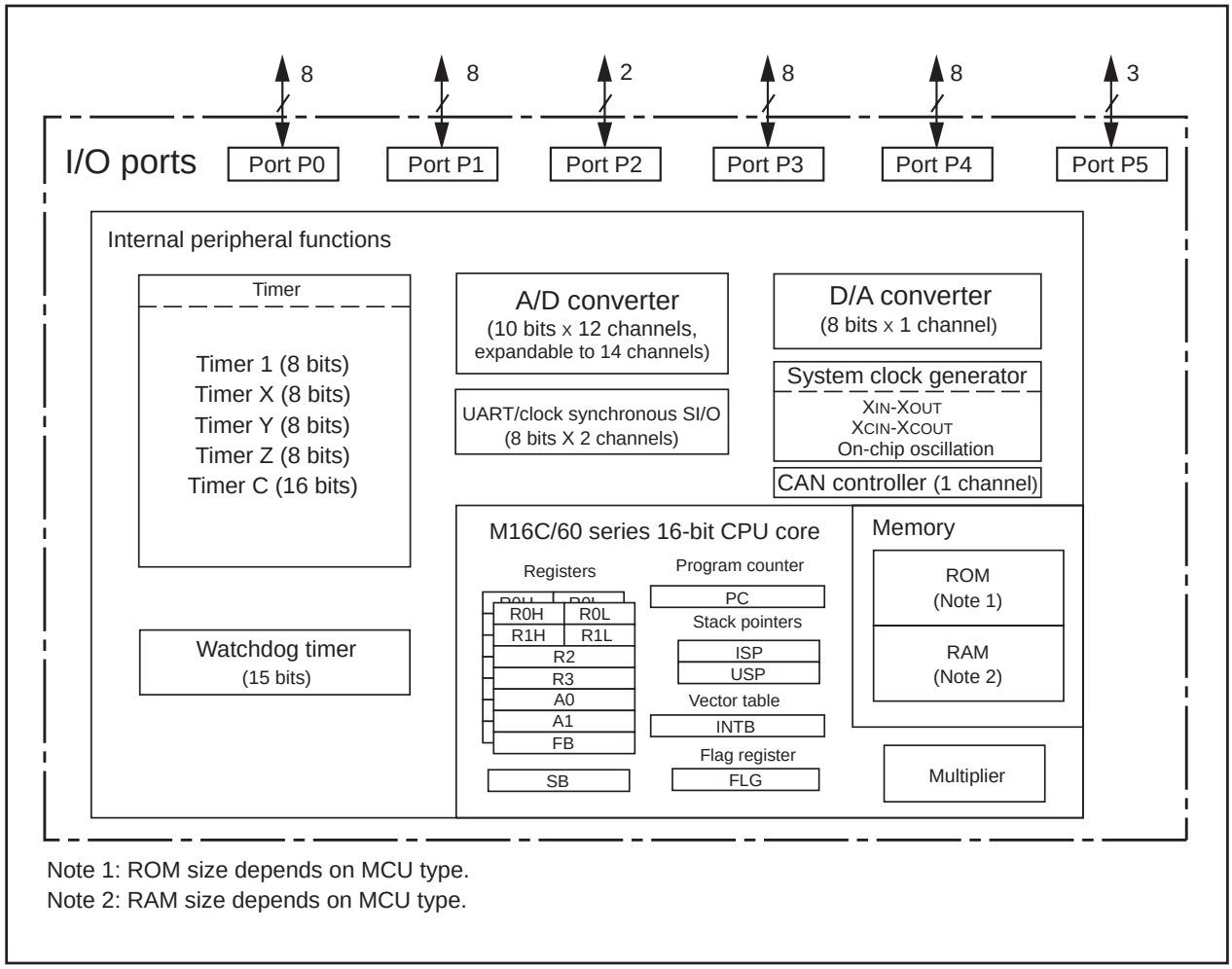
Table 1.1 gives an overview of the M16C/1N group performance specification.

**Table 1.1 Performance overview**

| Item | | Performance |
|---|---|---|
| Number of basic instructions | | 91 instructions |
| Shortest instruction execution time | | 62.5 ns (when f(XIN)=16MHz) |
| Memory size | ROM | See **Table 1.2 Performance overview** |
| | RAM | See **Table 1.2 Performance overview** |
| I/O port | | P0 to P5: 37 lines |
| Multifunction timer | T1 | 8 bits x 1 |
| | TX, TY, TZ | 8 bits x 3 |
| | TC | 16 bits x 1 |
| Serial I/O (UART or clock synchronous) | | x 2 |
| A/D converter (maximum resolution: 10 bits) | | x 12 channels (Expandable up to 14 channels) |
| D/A converter | | 8 bits x 1 |
| CAN controller | | 1 channel, 2.0B active |
| Watchdog timer | | 15 bits x 1 (with prescaler) |
| Interrupts | | 15 internal causes, 8 external causes, 4 software causes |
| Clock generating circuits | | 3 internal circuits |
| Power supply voltage | | 4.2 V to 5.5V (when f(XIN)=16MHz) |
| Power consumption | | 70mW(VCC=5.0V, f(XIN)=16MHz) |
| I/O characteristics | I/O withstand voltage | 5V |
| | Output current | 5mA (10mA:LED drive port) |
| Device configuration | | CMOS silicon gate |
| Package | | 48-pin LQFP |

## 1.3 Block Diagram

Figure 1.1 shows block diagram of the M16C/1N group.




Note 1: ROM size depends on MCU type.
Note 2: RAM size depends on MCU type.

**Figure 1.1 Block diagram**

## 1.4 Performance Overview

Table 1.2 shows performance overview.

**Table 1.2 Performance overview**

As of June 2004

| Type No. | ROM | RAM | Package | Remarks |
|---|---|---|---|---|
| M301N2M4T-XXXFP(D) | 32Kbytes | 1Kbytes | 48P6Q-A | Mask ROM |
| M301N2M8T-XXXFP(D) | 64Kbytes | 3Kbytes | | |
| M301N2F8TFP(D) | | | | Flash memory |
| M301N2F8FP(D) | | | | |

(D): Under development

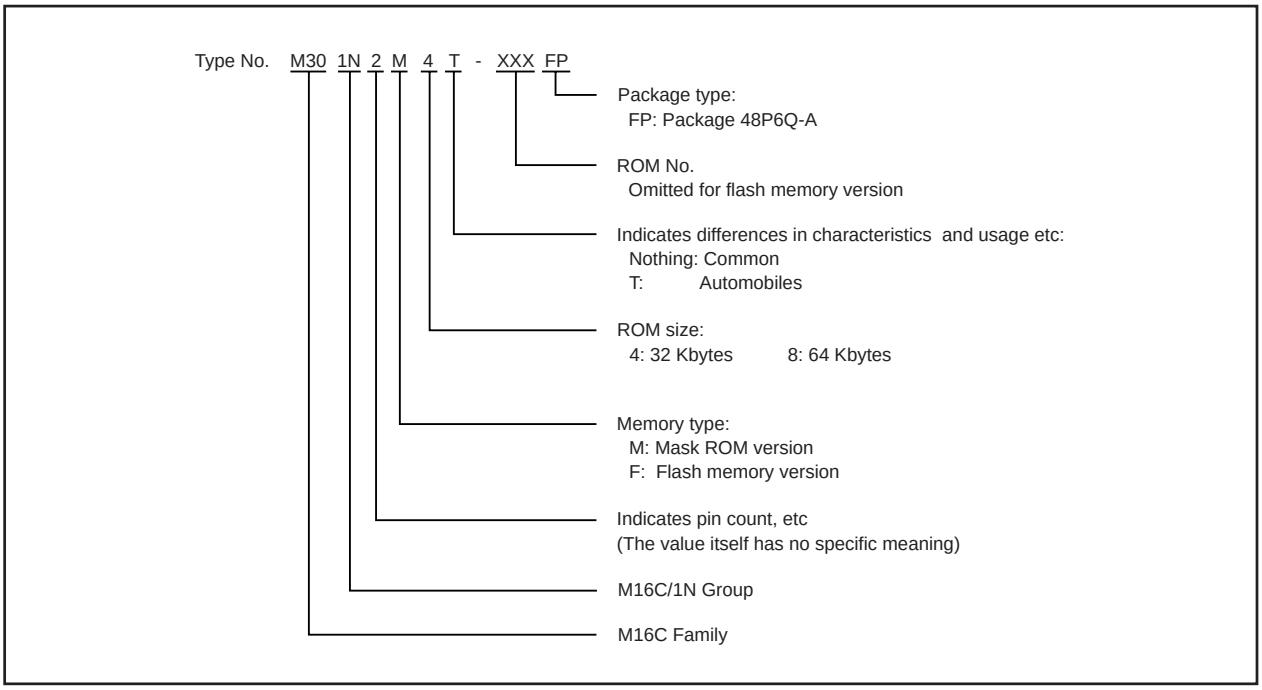
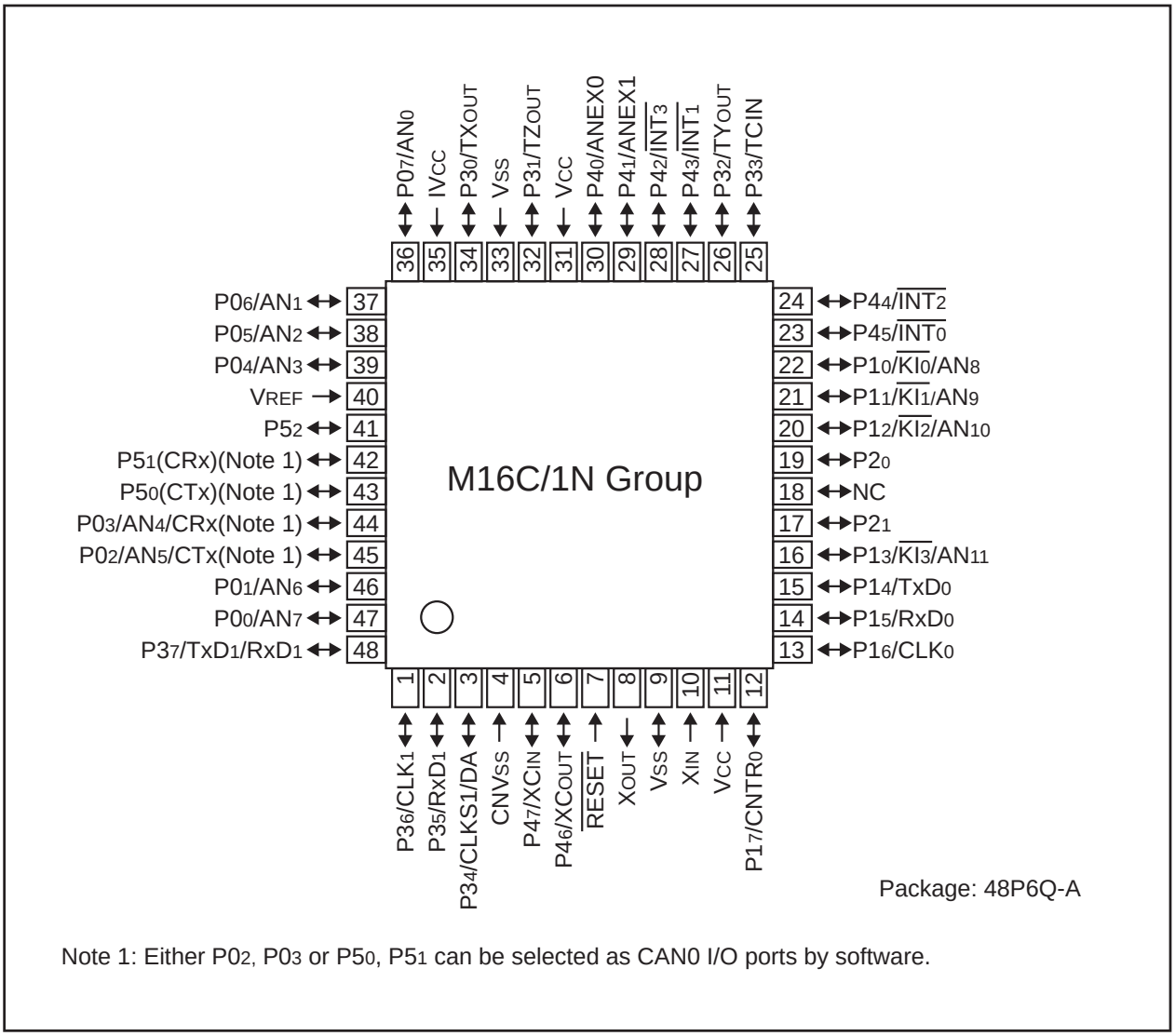



**Figure 1.2 Type No., memory size, and package**

## 1.5 Pin Configuration

Figure 1.3 shows pin configurations (top view) of the M16C/1N group.




Note 1: Either P02, P03 or P50, P51 can be selected as CAN0 I/O ports by software.

**Figure 1.3 Pin configuration diagram (top view)**

## 1.6 Pin Description

Table 1.3 shows the pin description.

**Table 1.3 Pin Description**

| Pin name | Signal name | I/O type | Function |
|---|---|---|---|
| VCC, VSS | Power supply input | Input | Supply 4.2 to 5.5 V to the VCC pin. Supply 0 V to the VSS pin. |
| IVCC | IVCC | Input | Connect a capacitor (0.1 µF) between this pin and VSS. |
| CNVSS | CNVSS | Input | Connect it to the VSS pin via resistance (about 5 kΩ). |
| $\overline{\text{RESET}}$ | Reset input | Input | A "L" on this input resets the microcomputer. |
| XIN | Clock input | Input | These pins are provided for the main clock oscillation circuit. Connect a ceramic resonator or crystal between the XIN and XOUT pins. To use an externally derived clock, input it to the XIN pin and leave the XOUT pin open. |
| XOUT | Clock output | Output | |
| VREF | Reference voltage input | Input | This pin is a reference voltage input for the A/D converter. |
| $P0_0$ to $P0_7$ | I/O port P0 | Input/output | This is an 8-bit CMOS I/O port. It has an input/output port direction register that allows the user to set each pin for input or output individually. When set for input, the user can specify in units of four bits via software whether or not they are tied to a pull-up resistor. These pins are shared with analog input pins. $P0_2$ and $P0_3$ function as CAN0 I/O pins by using software. |
| $P1_0$ to $P1_7$ | I/O port P1 | Input/output | This is an 8-bit I/O port equivalent to P0. $P1_0$ to $P1_3$ are shared with analog inputs and key input interrupts. $P1_4$ to $P1_6$ are shared with serial I/O pins. $P1_7$ is shared with timer input. Can be used as an LED drive port. |
| $P2_0$ to $P2_1$ | I/O port P2 | Input/output | This is a 2-bit I/O port equivalent to P0. |
| $P3_0$ to $P3_7$ | I/O port P3 | Input/output | This is a 8-bit I/O port equivalent to P0. $P3_0$ to $P3_3$ are shared with timer input/output. $P3_4$ to $P3_7$ are shared with serial I/O. $P3_4$ is shared with analog outputs. |
| $P4_0$ to $P4_7$ | I/O port P4 | Input/output | This is a 8-bit I/O port equivalent to P0. $P4_0$ to $4_1$ are shared with analog inputs. $P4_2$ to $P4_5$ are shared with interrupt inputs. $P4_6$ to $P4_7$ are shared with the I/O pin of the clock oscillation circuit for the clock. |
| $P5_0$ to $P5_2$ | I/O port P5 | Input/output | This is a 3-bit I/O port equivalent to P0. $P5_0$ and $P5_1$ function as CAN0 I/O pins by using software. |

## 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

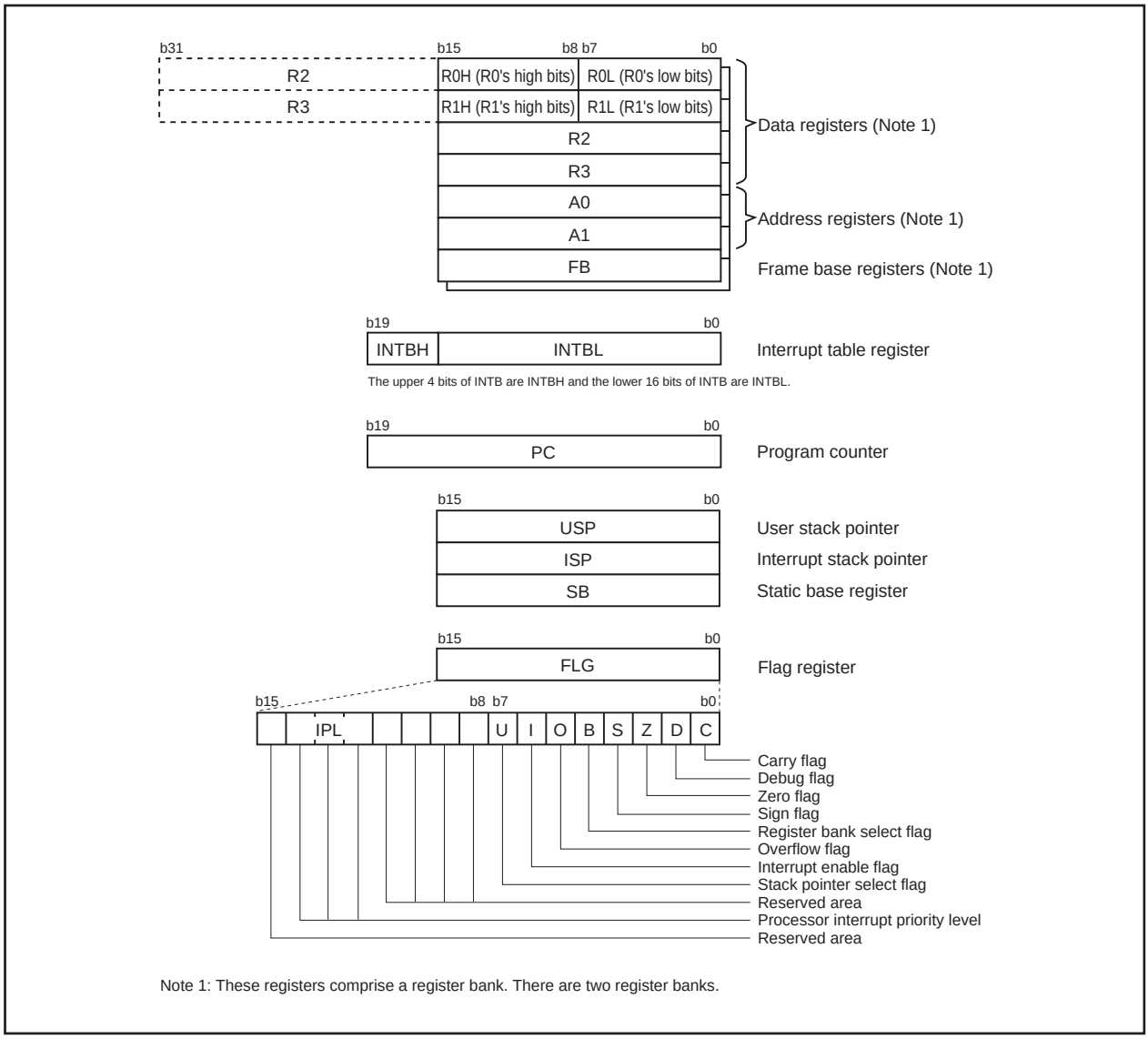



**Figure 2.1 CPU Registers**

### 2.1 Data Registers (R0, R1, R2, and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

### 2.2 Address Registers (A0 and A1)

The A0 register consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0.

In some instructions, A1 and A0 can be combined for use as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

## 2.6 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.
Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

## 2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

### 2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

### 2.8.2 Debug Flag (D Flag)

This flag is used exclusively for debugging purpose. During normal use, it must be set to “0”.

### 2.8.3 Zero Flag (Z Flag)

This flag is set to “1” when an arithmetic operation resulted in 0; otherwise, it is “0”.

### 2.8.4 Sign Flag (S Flag)

This flag is set to “1” when an arithmetic operation resulted in a negative value; otherwise, it is “0”.

### 2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is “0”; register bank 1 is selected when this flag is “1”.

### 2.8.6 Overflow Flag (O Flag)

This flag is set to “1” when the operation resulted in an overflow; otherwise, it is “0”.

### 2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.
Maskable interrupts are disabled when the I flag is “0”, and are enabled when the I flag is “1”. The I flag is set to “0” when the interrupt request is accepted.

### 2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is “0”; USP is selected when the U flag is “1”.
The U flag is set to “0” when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has priority greater than IPL, the interrupt request is enabled.

### 2.8.10 Reserved Area

When white to this bit, write “0”. When read, its content is indeterminate.

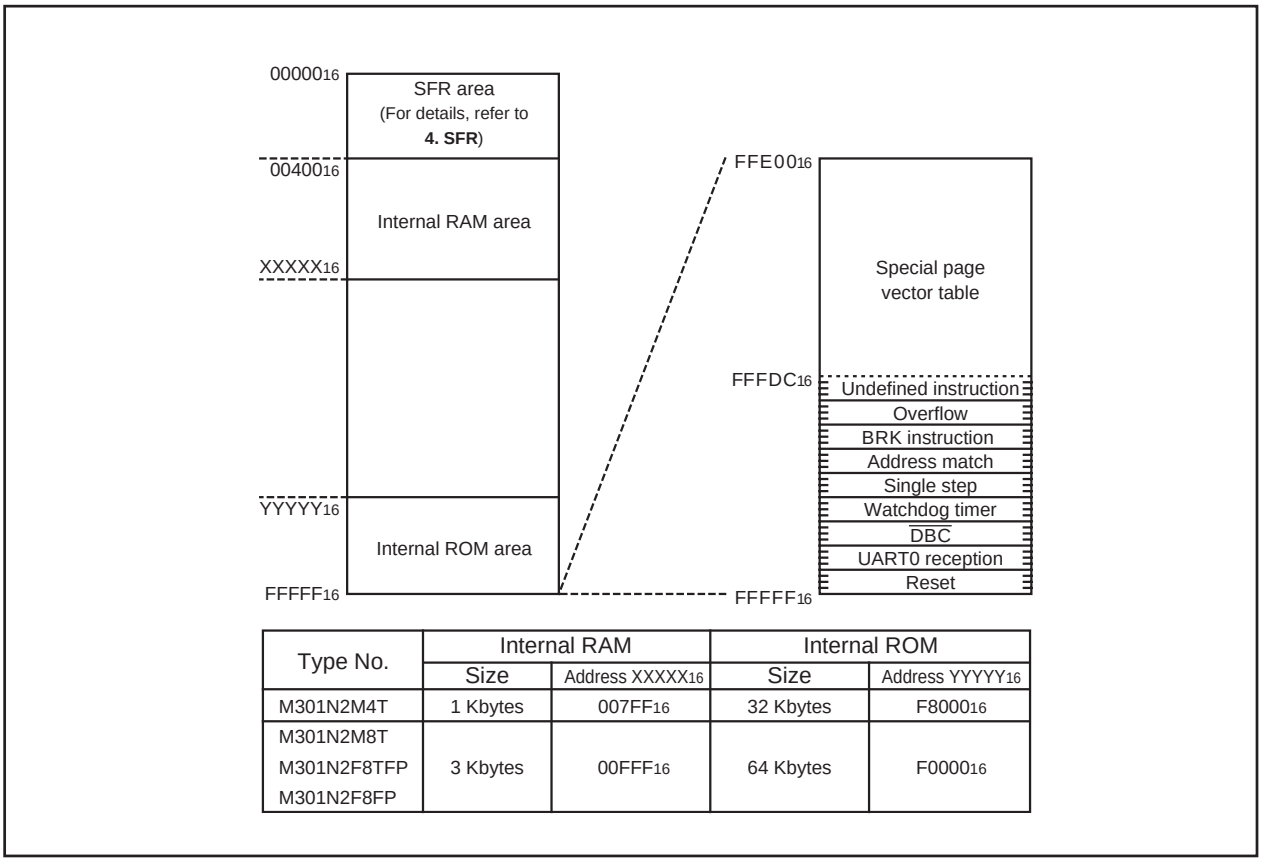
## 3. Memory

Figure 3.1 is a memory map. The address space extends the 1M bytes from address 00000$_{16}$ to FFFFF$_{16}$. From FFFFF$_{16}$ down is ROM. For example, in the M301N2M4T-XXXFP, there is 32K bytes of internal ROM from F8000$_{16}$ to FFFFF$_{16}$. The vector table for fixed interrupts such as the reset are mapped to FFFDC$_{16}$ to FFFFF$_{16}$. The starting address of the interrupt routine is stored here. The address of the vector table for timer interrupts, etc., can be set as desired using the internal register (INTB). See the section on interrupts for details.

From 00400$_{16}$ up is RAM. For example, in the M301N2M4T-XXXFP, there is 1K byte of internal RAM from 00400$_{16}$ to 007FF$_{16}$. In addition to storing data, the RAM also stores the stack used when calling subroutines and when interrupts are generated.

The SFR area is mapped to 00000$_{16}$ to 003FF$_{16}$. This area accommodates the control registers for peripheral devices such as I/O ports, A/D converter, serial I/O, and timers, etc. Any part of the SFR area that is not occupied is reserved and cannot be used for other purposes.

The special page vector table is mapped to FFE00$_{16}$ to FFFDB$_{16}$. If the starting addresses of subroutines or the destination addresses of jumps are stored here, subroutine call instructions and jump instructions can be used as 2-byte instructions, reducing the number of program steps.




| Type No. | Internal RAM | | Internal ROM | |
|---|---|---|---|---|
| | Size | Address XXXXX$_{16}$ | Size | Address YYYYY$_{16}$ |
| M301N2M4T | 1 Kbytes | 007FF$_{16}$ | 32 Kbytes | F8000$_{16}$ |
| M301N2M8T<br>M301N2F8TFP<br>M301N2F8FP | 3 Kbytes | 00FFF$_{16}$ | 64 Kbytes | F0000$_{16}$ |

**Figure 3.1 Memory map**

# 4. Special Function Registers (SFR)

| Address | Register | Symbol | After reset |
|---|---|---|---|
| $0000_{16}$ | | | |
| $0001_{16}$ | | | |
| $0002_{16}$ | | | |
| $0003_{16}$ | | | |
| $0004_{16}$ | Processor mode register 0 | PM0 | $XXXX0X00_2$ |
| $0005_{16}$ | Processor mode register 1 | PM1 | $00XXX0X0_2$ |
| $0006_{16}$ | System clock control register 0 | CM0 | $48_{16}$ |
| $0007_{16}$ | System clock control register 1 | CM1 | $20_{16}$ |
| $0008_{16}$ | | | |
| $0009_{16}$ | Address match interrupt enable register | AIER | $XXXXXX00_2$ |
| $000A_{16}$ | Protect register | PRCR | $XXXXX000_2$ |
| $000B_{16}$ | | | |
| $000C_{16}$ | Oscillation stop detection register | CM2 | $04_{16}$ |
| $000D_{16}$ | | | |
| $000E_{16}$ | Watchdog timer start register | WDTS | $XX_{16}$ |
| $000F_{16}$ | Watchdog timer control register | WDC | $000XXXXX_2$ |
| $0010_{16}$ | Address match interrupt register 0 | RMAD0 | $00000000_2$ |
| $0011_{16}$ | | | $00000000_2$ |
| $0012_{16}$ | | | $XXXX0000_2$ |
| $0013_{16}$ | | | |
| $0014_{16}$ | Address match interrupt register 1 | RMAD1 | $00000000_2$ |
| $0015_{16}$ | | | $00000000_2$ |
| $0016_{16}$ | | | $XXXX0000_2$ |
| $0017_{16}$ | | | |
| $0018_{16}$ | | | |
| $0019_{16}$ | | | |
| $001A_{16}$ | | | |
| $001B_{16}$ | | | |
| $001C_{16}$ | | | |
| $001D_{16}$ | | | |
| $001E_{16}$ | $\overline{\text{INT0}}$ input filter select register | INT0F | $XXXXX000_2$ |
| $001F_{16}$ | | | |
| $0020_{16}$ | | | |
| $0021_{16}$ | | | |
| $0022_{16}$ | | | |
| $0023_{16}$ | | | |
| $0024_{16}$ | | | |
| $0025_{16}$ | | | |
| $0026_{16}$ | | | |
| $0027_{16}$ | | | |
| $0028_{16}$ | | | |
| $0029_{16}$ | | | |
| $002A_{16}$ | | | |
| $002B_{16}$ | | | |
| $002C_{16}$ | | | |
| $002D_{16}$ | | | |
| $002E_{16}$ | | | |
| $002F_{16}$ | | | |
| $0030_{16}$ | | | |
| $0031_{16}$ | | | |
| $0032_{16}$ | | | |
| $0033_{16}$ | | | |
| $0034_{16}$ | | | |
| $0035_{16}$ | | | |
| $0036_{16}$ | | | |
| $0037_{16}$ | | | |
| $0038_{16}$ | | | |
| $0039_{16}$ | | | |
| $003A_{16}$ | | | |
| $003B_{16}$ | | | |
| $003C_{16}$ | | | |
| $003D_{16}$ | | | |
| $003E_{16}$ | | | |
| $003F_{16}$ | | | |

Note 1: Location in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

X : Undefined

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0040$_{16}$ | | | |
| 0041$_{16}$ | | | |
| 0042$_{16}$ | | | |
| 0043$_{16}$ | | | |
| 0044$_{16}$ | | | |
| 0045$_{16}$ | CAN0 wakeup interrupt control register | C01WKIC | XXXXX000$_2$ |
| 0046$_{16}$ | CAN0 state/error interrupt control register | C01ERRIC | XXXXX000$_2$ |
| 0047$_{16}$ | | | |
| 0048$_{16}$ | CAN0 reception successful interrupt control register | C0RECIC | XXXXX000$_2$ |
| 0049$_{16}$ | CAN0 transmission successful interrupt control register | C0TRMIC | XXXXX000$_2$ |
| 004A$_{16}$ | | | |
| 004B$_{16}$ | | | |
| 004C$_{16}$ | | | |
| 004D$_{16}$ | Key input interrupt control register | KUPIC | XXXXX000$_2$ |
| 004E$_{16}$ | A/D conversion interrupt control register | ADIC | XXXXX000$_2$ |
| 004F$_{16}$ | | | |
| 0050$_{16}$ | | | |
| 0051$_{16}$ | UART0 transmit interrupt control register | S0TIC | XXXXX000$_2$ |
| 0052$_{16}$ | UART0 receive interrupt control register | S0RIC | XXXXX000$_2$ |
| 0053$_{16}$ | UART1 transmit interrupt control register | S1TIC | XXXXX000$_2$ |
| 0054$_{16}$ | UART1 receive interrupt control register | S1RIC | XXXXX000$_2$ |
| 0055$_{16}$ | Timer 1 interrupt control register | T1IC | XXXXX000$_2$ |
| 0056$_{16}$ | Timer X interrupt control register | TXIC | XXXXX000$_2$ |
| 0057$_{16}$ | Timer Y interrupt control register | TYIC | XXXXX000$_2$ |
| 0058$_{16}$ | Timer Z interrupt control register | TZIC | XXXXX000$_2$ |
| 0059$_{16}$ | CNTR0 interrupt control register | CNTR0IC | XXXXX000$_2$ |
| 005A$_{16}$ | TCIN interrupt control register | TCINIC | XXXXX000$_2$ |
| 005B$_{16}$ | Timer C interrupt control register | TCIC | XXXXX000$_2$ |
| 005C$_{16}$ | INT3 interrupt control register | INT3IC | XXXXX000$_2$ |
| 005D$_{16}$ | INT0 interrupt control register | INT0IC | XX00X000$_2$ |
| 005E$_{16}$ | INT1 interrupt control register | INT1IC | XX00X000$_2$ |
| 005F$_{16}$ | INT2 interrupt control register | INT2IC | XX00X000$_2$ |
| 0060$_{16}$ | | | |
| 0061$_{16}$ | | | |
| 0062$_{16}$ | | | |
| 0063$_{16}$ | | | |
| 0064$_{16}$ | | | |
| 0065$_{16}$ | | | |
| 0066$_{16}$ | | | |
| 0067$_{16}$ | | | |
| 0068$_{16}$ | | | |
| 0069$_{16}$ | | | |
| 006A$_{16}$ | | | |
| 006B$_{16}$ | | | |
| 006C$_{16}$ | | | |
| 006D$_{16}$ | | | |
| 006E$_{16}$ | | | |
| 006F$_{16}$ | | | |
| 0070$_{16}$ | | | |
| 0071$_{16}$ | | | |
| 0072$_{16}$ | | | |
| 0073$_{16}$ | | | |
| 0074$_{16}$ | | | |
| 0075$_{16}$ | | | |
| 0076$_{16}$ | | | |
| 0077$_{16}$ | | | |
| 0078$_{16}$ | | | |
| 0079$_{16}$ | | | |
| 007A$_{16}$ | | | |
| 007B$_{16}$ | | | |
| 007C$_{16}$ | | | |
| 007D$_{16}$ | | | |
| 007E$_{16}$ | | | |
| 007F$_{16}$ | | | |

Note 1: Location in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

X : Undefined

| Address | Register | Symbol | After reset |
|---|---|---|---|
| $0080_{16}$ | Timer Y, Z mode register | TYZMR | $000000X0_2$ |
| $0081_{16}$ | Prescaler Y | PREY | $FF_{16}$ |
| $0082_{16}$ | Timer Y secondary | TYSC | $FF_{16}$ |
| $0083_{16}$ | Timer Y primary | TYPR | $FF_{16}$ |
| $0084_{16}$ | Timer Y, Z waveform output control register | PUM | $00_{16}$ |
| $0085_{16}$ | Prescaler Z | PREZ | $FF_{16}$ |
| $0086_{16}$ | Timer Z secondary | TZSC | $FF_{16}$ |
| $0087_{16}$ | Timer Z primary | TZPR | $FF_{16}$ |
| $0088_{16}$ | Prescaler 1 | PRE1 | $XX_{16}$ |
| $0089_{16}$ | Timer 1 | T1 | $XX_{16}$ |
| $008A_{16}$ | Timer Y, Z output control register | TYZOC | $XXXXX000_2$ |
| $008B_{16}$ | Timer X mode register | TXMR | $00000000_2$ |
| $008C_{16}$ | Prescaler X | PREX | $FF_{16}$ |
| $008D_{16}$ | Timer X | TX | $FF_{16}$ |
| $008E_{16}$ | Timer count source set register | TCSS | $00_{16}$ |
| $008F_{16}$ | Clock prescaler reset flag | CPSRF | $0XXXXXXX_2$ |
| $0090_{16}$ | Timer C counter | TC | $XX_{16}$ |
| $0091_{16}$ | | | $XX_{16}$ |
| $0092_{16}$ | | | |
| $0093_{16}$ | | | |
| $0094_{16}$ | | | |
| $0095_{16}$ | | | |
| $0096_{16}$ | External input enable register | INTEN | $00_{16}$ |
| $0097_{16}$ | | | |
| $0098_{16}$ | Key input enable register | KIEN | $00_{16}$ |
| $0099_{16}$ | | | |
| $009A_{16}$ | Timer C control register 0 | TCC0 | $0XX00000_2$ |
| $009B_{16}$ | Timer C control register 1 | TCC1 | $XXXXXX11_2$ |
| $009C_{16}$ | Time measurement register | TM | $XX_{16}$ |
| $009D_{16}$ | | | $XX_{16}$ |
| $009E_{16}$ | | | |
| $009F_{16}$ | | | |
| $00A0_{16}$ | UART0 transmit/receive mode register | U0MR | $00_{16}$ |
| $00A1_{16}$ | UART0 bit rate generator | U0BRG | $XX_{16}$ |
| $00A2_{16}$ | UART0 transmit buffer register | U0TB | $XX_{16}$ |
| $00A3_{16}$ | | | $XX_{16}$ |
| $00A4_{16}$ | UART0 transmit/receive control register 0 | U0C0 | $08_{16}$ |
| $00A5_{16}$ | UART0 transmit/receive control register 1 | U0C1 | $XXXX0010_2$ |
| $00A6_{16}$ | UART0 receive buffer register | U0RB | $XX_{16}$ |
| $00A7_{16}$ | | | $XX_{16}$ |
| $00A8_{16}$ | UART1 transmit/receive mode register | U1MR | $00_{16}$ |
| $00A9_{16}$ | UART1 bit rate generator | U1BRG | $XX_{16}$ |
| $00AA_{16}$ | UART1 transmit buffer register | U1TB | $XX_{16}$ |
| $00AB_{16}$ | | | $XX_{16}$ |
| $00AC_{16}$ | UART1 transmit/receive control register 0 | U1C0 | $08_{16}$ |
| $00AD_{16}$ | UART1 transmit/receive control register 1 | U1C1 | $XXXX0010_2$ |
| $00AE_{16}$ | UART1 receive buffer register | U1RB | $XX_{16}$ |
| $00AF_{16}$ | | | $XX_{16}$ |
| $00B0_{16}$ | UART transmit/receive control register 2 | UCON | $X0000000_2$ |
| $00B1_{16}$ | | | |
| $00B2_{16}$ | | | |
| $00B3_{16}$ | | | |
| $00B4_{16}$ | | | |
| $00B5_{16}$ | | | |
| $00B6_{16}$ | | | |
| $00B7_{16}$ | | | |
| $00B8_{16}$ | | | |
| $00B9_{16}$ | | | |
| $00BA_{16}$ | | | |
| $00BB_{16}$ | | | |
| $00BC_{16}$ | | | |
| $00BD_{16}$ | | | |
| $00BE_{16}$ | | | |
| $00BF_{16}$ | | | |

Note 1: Location in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

X : Undefined

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 00C0$_{16}$ | A/D register | AD | XX$_{16}$ |
| 00C1$_{16}$ | | | XX$_{16}$ |
| 00C2$_{16}$ | | | |
| 00C3$_{16}$ | | | |
| 00C4$_{16}$ | | | |
| 00C5$_{16}$ | | | |
| 00C6$_{16}$ | | | |
| 00C7$_{16}$ | | | |
| 00C8$_{16}$ | | | |
| 00C9$_{16}$ | | | |
| 00CA$_{16}$ | | | |
| 00CB$_{16}$ | | | |
| 00CC$_{16}$ | | | |
| 00CD$_{16}$ | | | |
| 00CE$_{16}$ | | | |
| 00CF$_{16}$ | | | |
| 00D0$_{16}$ | | | |
| 00D1$_{16}$ | | | |
| 00D2$_{16}$ | | | |
| 00D3$_{16}$ | | | |
| 00D4$_{16}$ | A/D control register 2 | ADCON2 | XXXX0000$_2$ |
| 00D5$_{16}$ | | | |
| 00D6$_{16}$ | A/D control register 0 | ADCON0 | 00000XXX$_2$ |
| 00D7$_{16}$ | A/D control register 1 | ADCON1 | 00$_{16}$ |
| 00D8$_{16}$ | D/A register | DA | XX$_{16}$ |
| 00D9$_{16}$ | | | |
| 00DA$_{16}$ | | | |
| 00DB$_{16}$ | | | |
| 00DC$_{16}$ | D/A control register | DACON | XXXXX0X0$_2$ |
| 00DD$_{16}$ | | | |
| 00DE$_{16}$ | | | |
| 00DF$_{16}$ | | | |
| 00E0$_{16}$ | Port P0 register | P0 | XX$_{16}$ |
| 00E1$_{16}$ | Port P1 register | P1 | XX$_{16}$ |
| 00E2$_{16}$ | Port P0 direction register | PD0 | 00$_{16}$ |
| 00E3$_{16}$ | Port P1 direction register | PD1 | 00$_{16}$ |
| 00E4$_{16}$ | Port P2 register | P2 | XX$_{16}$ |
| 00E5$_{16}$ | Port P3 register | P3 | XX$_{16}$ |
| 00E6$_{16}$ | Port P2 direction register | PD2 | XXXXXX00$_2$ |
| 00E7$_{16}$ | Port P3 direction register | PD3 | 00$_{16}$ |
| 00E8$_{16}$ | Port P4 register | P4 | XX$_{16}$ |
| 00E9$_{16}$ | Port P5 register | P5 | XX$_{16}$ |
| 00EA$_{16}$ | Port P4 direction register | PD4 | 00$_{16}$ |
| 00EB$_{16}$ | Port P5 direction register | PD5 | XXXXX000$_2$ |
| 00EC$_{16}$ | | | |
| 00ED$_{16}$ | | | |
| 00EE$_{16}$ | | | |
| 00EF$_{16}$ | | | |
| 00F0$_{16}$ | | | |
| 00F1$_{16}$ | | | |
| 00F2$_{16}$ | | | |
| 00F3$_{16}$ | | | |
| 00F4$_{16}$ | | | |
| 00F5$_{16}$ | | | |
| 00F6$_{16}$ | | | |
| 00F7$_{16}$ | | | |
| 00F8$_{16}$ | CAN0 I/O port select register | CIOSR | XXXXXXX0$_2$ |
| 00F9$_{16}$ | | | |
| 00FA$_{16}$ | | | |
| 00FB$_{16}$ | | | |
| 00FC$_{16}$ | Pull-up control register 0 | PUR0 | 00X00000$_2$ |
| 00FD$_{16}$ | Pull-up control register 1 | PUR1 | XXXXX000$_2$ |
| 00FE$_{16}$ | Port P1 drive capacity control register | DRR | 00$_{16}$ |
| 00FF$_{16}$ | | | |

Note 1: Location in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

X : Undefined

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0100₁₆ | | | |
| 0101₁₆ | | | |
| 0102₁₆ | | | |
| 0103₁₆ | | | |
| 0104₁₆ ≈ 01B0₁₆ | | | |
| 01B1₁₆ | | | |
| 01B2₁₆ | | | |
| 01B3₁₆ | Flash memory control register 4 (Note 2) | FMR4 | 01000000₂ |
| 01B4₁₆ | | | |
| 01B5₁₆ | Flash memory control register 1 (Note 2) | FMR1 | 0000XX0X₂ |
| 01B6₁₆ | | | |
| 01B7₁₆ | Flash memory control register 0 (Note 2) | FMR0 | XX000001₂ |
| 01B8₁₆ | | | |
| 01B9₁₆ | | | |
| 01BA₁₆ | | | |
| 01BB₁₆ | | | |
| 01BC₁₆ | | | |
| 01BD₁₆ | | | |
| 01BE₁₆ | | | |
| 01BF₁₆ ≈ 0215₁₆ | | | |
| 0216₁₆ | | | |
| 0217₁₆ | | | |
| 0218₁₆ | | | |
| 0219₁₆ | | | |
| 021A₁₆ | | | |
| 021B₁₆ | | | |
| 021C₁₆ | | | |
| 021D₁₆ | | | |
| 021E₁₆ | | | |
| 021F₁₆ | | | |
| 0220₁₆ | CAN0 message control register 0 | C0MCTL0 | 00₁₆ |
| 0221₁₆ | CAN0 message control register 1 | C0MCTL1 | 00₁₆ |
| 0222₁₆ | CAN0 message control register 2 | C0MCTL2 | 00₁₆ |
| 0223₁₆ | CAN0 message control register 3 | C0MCTL3 | 00₁₆ |
| 0224₁₆ | CAN0 message control register 4 | C0MCTL4 | 00₁₆ |
| 0225₁₆ | CAN0 message control register 5 | C0MCTL5 | 00₁₆ |
| 0226₁₆ | CAN0 message control register 6 | C0MCTL6 | 00₁₆ |
| 0227₁₆ | CAN0 message control register 7 | C0MCTL7 | 00₁₆ |
| 0228₁₆ | CAN0 message control register 8 | C0MCTL8 | 00₁₆ |
| 0229₁₆ | CAN0 message control register 9 | C0MCTL9 | 00₁₆ |
| 022A₁₆ | CAN0 message control register 10 | C0MCTL10 | 00₁₆ |
| 022B₁₆ | CAN0 message control register 11 | C0MCTL11 | 00₁₆ |
| 022C₁₆ | CAN0 message control register 12 | C0MCTL12 | 00₁₆ |
| 022D₁₆ | CAN0 message control register 13 | C0MCTL13 | 00₁₆ |
| 022E₁₆ | CAN0 message control register 14 | C0MCTL14 | 00₁₆ |
| 022F₁₆ | CAN0 message control register 15 | C0MCTL15 | 00₁₆ |
| 0230₁₆ | CAN0 control register | C0CTLR | X0000001₂ |
| 0231₁₆ | | | XX0X0000₂ |
| 0232₁₆ | CAN0 status register | C0STR | 00₁₆ |
| 0233₁₆ | | | X0000001₂ |
| 0234₁₆ | CAN0 slot status register | C0SSTR | 0000₁₆ |
| 0235₁₆ | | | 0000₁₆ |
| 0236₁₆ | CAN0 interrupt control register | C0ICR | 0000₁₆ |
| 0237₁₆ | | | 0000₁₆ |
| 0238₁₆ | CAN0 extended ID register | C0IDR | 0000₁₆ |
| 0239₁₆ | | | 0000₁₆ |
| 023A₁₆ | CAN0 configuration register | C0CONR | XX₁₆ |
| 023B₁₆ | | | XX₁₆ |
| 023C₁₆ | CAN0 receive error count register | C0RECR | 00₁₆ |
| 023D₁₆ | CAN0 transmit error count register | C0TECR | 00₁₆ |
| 023E₁₆ | | | |
| 023F₁₆ | | | |

Note 1: Location in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.
Note 2: These registers are available on flash memory versions only.

X : Undefined

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0240$_{16}$ | | | |
| 0241$_{16}$ | | | |
| 0242$_{16}$ | | | |
| 0243$_{16}$ | | | |
| 0244$_{16}$ | CAN0 acceptance filter support register | C0AFS | XX$_{16}$ |
| 0245$_{16}$ | | | XX$_{16}$ |
| 0246$_{16}$ | | | |
| 0247$_{16}$ | | | |
| 0248$_{16}$ | | | |
| 0249$_{16}$ | | | |
| 024A$_{16}$ | | | |
| 024B$_{16}$ | | | |
| 024C$_{16}$ | | | |
| 024D$_{16}$ | | | |
| 024E$_{16}$ | | | |
| 024F$_{16}$ | | | |
| 0250$_{16}$ | | | |
| 0251$_{16}$ | | | |
| 0252$_{16}$ | | | |
| 0253$_{16}$ | | | |
| 0254$_{16}$ | | | |
| 0255$_{16}$ | | | |
| 0256$_{16}$ | | | |
| 0257$_{16}$ | | | |
| 0258$_{16}$ | | | |
| 0259$_{16}$ | | | |
| 025A$_{16}$ | | | |
| 025B$_{16}$ | | | |
| 025C$_{16}$ | | | |
| 025D$_{16}$ | | | |
| 025E$_{16}$ | | | |
| 025F$_{16}$ | CAN0 clock select register | CCLKR | X000XXXX$_2$ |
| 0260$_{16}$ | CAN0 slot 0: Identifier / DLC | | XX$_{16}$ |
| 0261$_{16}$ | | | XX$_{16}$ |
| 0262$_{16}$ | | | XX$_{16}$ |
| 0263$_{16}$ | | | XX$_{16}$ |
| 0264$_{16}$ | | | XX$_{16}$ |
| 0265$_{16}$ | | | XX$_{16}$ |
| 0266$_{16}$ | CAN0 slot 0: Data Field | | XX$_{16}$ |
| 0267$_{16}$ | | | XX$_{16}$ |
| 0268$_{16}$ | | | XX$_{16}$ |
| 0269$_{16}$ | | | XX$_{16}$ |
| 026A$_{16}$ | | | XX$_{16}$ |
| 026B$_{16}$ | | | XX$_{16}$ |
| 026C$_{16}$ | | | XX$_{16}$ |
| 026D$_{16}$ | | | XX$_{16}$ |
| 026E$_{16}$ | CAN0 slot 0: Time Stamp | | XX$_{16}$ |
| 026F$_{16}$ | | | XX$_{16}$ |
| 0270$_{16}$ | CAN0 slot 1: Identifier / DLC | | XX$_{16}$ |
| 0271$_{16}$ | | | XX$_{16}$ |
| 0272$_{16}$ | | | XX$_{16}$ |
| 0273$_{16}$ | | | XX$_{16}$ |
| 0274$_{16}$ | | | XX$_{16}$ |
| 0275$_{16}$ | | | XX$_{16}$ |
| 0276$_{16}$ | CAN0 slot 1: Data Field | | XX$_{16}$ |
| 0277$_{16}$ | | | XX$_{16}$ |
| 0278$_{16}$ | | | XX$_{16}$ |
| 0279$_{16}$ | | | XX$_{16}$ |
| 027A$_{16}$ | | | XX$_{16}$ |
| 027B$_{16}$ | | | XX$_{16}$ |
| 027C$_{16}$ | | | XX$_{16}$ |
| 027D$_{16}$ | | | XX$_{16}$ |
| 027E$_{16}$ | CAN0 slot 1: Time Stamp | | XX$_{16}$ |
| 027F$_{16}$ | | | XX$_{16}$ |

Note 1: Location in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

X : Undefined

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0280$_{16}$ | CAN0 slot 2: Identifier / DLC | | XX$_{16}$ |
| 0281$_{16}$ | | | XX$_{16}$ |
| 0282$_{16}$ | | | XX$_{16}$ |
| 0283$_{16}$ | | | XX$_{16}$ |
| 0284$_{16}$ | | | XX$_{16}$ |
| 0285$_{16}$ | | | XX$_{16}$ |
| 0286$_{16}$ | CAN0 slot 2: Data Field | | XX$_{16}$ |
| 0287$_{16}$ | | | XX$_{16}$ |
| 0288$_{16}$ | | | XX$_{16}$ |
| 0289$_{16}$ | | | XX$_{16}$ |
| 028A$_{16}$ | | | XX$_{16}$ |
| 028B$_{16}$ | | | XX$_{16}$ |
| 028C$_{16}$ | | | XX$_{16}$ |
| 028D$_{16}$ | | | XX$_{16}$ |
| 028E$_{16}$ | CAN0 slot 2: Time Stamp | | XX$_{16}$ |
| 028F$_{16}$ | | | XX$_{16}$ |
| 0290$_{16}$ | CAN0 slot 3: Identifier / DLC | | XX$_{16}$ |
| 0291$_{16}$ | | | XX$_{16}$ |
| 0292$_{16}$ | | | XX$_{16}$ |
| 0293$_{16}$ | | | XX$_{16}$ |
| 0294$_{16}$ | | | XX$_{16}$ |
| 0295$_{16}$ | | | XX$_{16}$ |
| 0296$_{16}$ | CAN0 slot 3: Data Field | | XX$_{16}$ |
| 0297$_{16}$ | | | XX$_{16}$ |
| 0298$_{16}$ | | | XX$_{16}$ |
| 0299$_{16}$ | | | XX$_{16}$ |
| 029A$_{16}$ | | | XX$_{16}$ |
| 029B$_{16}$ | | | XX$_{16}$ |
| 029C$_{16}$ | | | XX$_{16}$ |
| 029D$_{16}$ | | | XX$_{16}$ |
| 029E$_{16}$ | CAN0 slot 3: Time Stamp | | XX$_{16}$ |
| 029F$_{16}$ | | | XX$_{16}$ |
| 02A0$_{16}$ | CAN0 slot 4: Identifier / DLC | | XX$_{16}$ |
| 02A1$_{16}$ | | | XX$_{16}$ |
| 02A2$_{16}$ | | | XX$_{16}$ |
| 02A3$_{16}$ | | | XX$_{16}$ |
| 02A4$_{16}$ | | | XX$_{16}$ |
| 02A5$_{16}$ | | | XX$_{16}$ |
| 02A6$_{16}$ | CAN0 slot 4: Data Field | | XX$_{16}$ |
| 02A7$_{16}$ | | | XX$_{16}$ |
| 02A8$_{16}$ | | | XX$_{16}$ |
| 02A9$_{16}$ | | | XX$_{16}$ |
| 02AA$_{16}$ | | | XX$_{16}$ |
| 02AB$_{16}$ | | | XX$_{16}$ |
| 02AC$_{16}$ | | | XX$_{16}$ |
| 02AD$_{16}$ | | | XX$_{16}$ |
| 02AE$_{16}$ | CAN0 slot 4: Time Stamp | | XX$_{16}$ |
| 02AF$_{16}$ | | | XX$_{16}$ |
| 02B0$_{16}$ | CAN0 slot 5: Identifier / DLC | | XX$_{16}$ |
| 02B1$_{16}$ | | | XX$_{16}$ |
| 02B2$_{16}$ | | | XX$_{16}$ |
| 02B3$_{16}$ | | | XX$_{16}$ |
| 02B4$_{16}$ | | | XX$_{16}$ |
| 02B5$_{16}$ | | | XX$_{16}$ |
| 02B6$_{16}$ | CAN0 slot 5: Data Field | | XX$_{16}$ |
| 02B7$_{16}$ | | | XX$_{16}$ |
| 02B8$_{16}$ | | | XX$_{16}$ |
| 02B9$_{16}$ | | | XX$_{16}$ |
| 02BA$_{16}$ | | | XX$_{16}$ |
| 02BB$_{16}$ | | | XX$_{16}$ |
| 02BC$_{16}$ | | | XX$_{16}$ |
| 02BD$_{16}$ | | | XX$_{16}$ |
| 02BE$_{16}$ | CAN0 slot 5: Time Stamp | | XX$_{16}$ |
| 02BF$_{16}$ | | | XX$_{16}$ |

Note 1: Location in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

X : Undefined

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 02C0$_{16}$ | CAN0 slot 6: Identifier / DLC | | XX$_{16}$ |
| 02C1$_{16}$ | | | XX$_{16}$ |
| 02C2$_{16}$ | | | XX$_{16}$ |
| 02C3$_{16}$ | | | XX$_{16}$ |
| 02C4$_{16}$ | | | XX$_{16}$ |
| 02C5$_{16}$ | | | XX$_{16}$ |
| 02C6$_{16}$ | CAN0 slot 6: Data Field | | XX$_{16}$ |
| 02C7$_{16}$ | | | XX$_{16}$ |
| 02C8$_{16}$ | | | XX$_{16}$ |
| 02C9$_{16}$ | | | XX$_{16}$ |
| 02CA$_{16}$ | | | XX$_{16}$ |
| 02CB$_{16}$ | | | XX$_{16}$ |
| 02CC$_{16}$ | | | XX$_{16}$ |
| 02CD$_{16}$ | | | XX$_{16}$ |
| 02CE$_{16}$ | CAN0 slot 6: Time Stamp | | XX$_{16}$ |
| 02CF$_{16}$ | | | XX$_{16}$ |
| 02D0$_{16}$ | CAN0 slot 7: Identifier / DLC | | XX$_{16}$ |
| 02D1$_{16}$ | | | XX$_{16}$ |
| 02D2$_{16}$ | | | XX$_{16}$ |
| 02D3$_{16}$ | | | XX$_{16}$ |
| 02D4$_{16}$ | | | XX$_{16}$ |
| 02D5$_{16}$ | | | XX$_{16}$ |
| 02D6$_{16}$ | CAN0 slot 7: Data Field | | XX$_{16}$ |
| 02D7$_{16}$ | | | XX$_{16}$ |
| 02D8$_{16}$ | | | XX$_{16}$ |
| 02D9$_{16}$ | | | XX$_{16}$ |
| 02DA$_{16}$ | | | XX$_{16}$ |
| 02DB$_{16}$ | | | XX$_{16}$ |
| 02DC$_{16}$ | | | XX$_{16}$ |
| 02DD$_{16}$ | | | XX$_{16}$ |
| 02DE$_{16}$ | CAN0 slot 7: Time Stamp | | XX$_{16}$ |
| 02DF$_{16}$ | | | XX$_{16}$ |
| 02E0$_{16}$ | CAN0 slot 8: Identifier / DLC | | XX$_{16}$ |
| 02E1$_{16}$ | | | XX$_{16}$ |
| 02E2$_{16}$ | | | XX$_{16}$ |
| 02E3$_{16}$ | | | XX$_{16}$ |
| 02E4$_{16}$ | | | XX$_{16}$ |
| 02E5$_{16}$ | | | XX$_{16}$ |
| 02E6$_{16}$ | CAN0 slot 8: Data Field | | XX$_{16}$ |
| 02E7$_{16}$ | | | XX$_{16}$ |
| 02E8$_{16}$ | | | XX$_{16}$ |
| 02E9$_{16}$ | | | XX$_{16}$ |
| 02EA$_{16}$ | | | XX$_{16}$ |
| 02EB$_{16}$ | | | XX$_{16}$ |
| 02EC$_{16}$ | | | XX$_{16}$ |
| 02ED$_{16}$ | | | XX$_{16}$ |
| 02EE$_{16}$ | CAN0 slot 8: Time Stamp | | XX$_{16}$ |
| 02EF$_{16}$ | | | XX$_{16}$ |
| 02F0$_{16}$ | CAN0 slot 9: Identifier / DLC | | XX$_{16}$ |
| 02F1$_{16}$ | | | XX$_{16}$ |
| 02F2$_{16}$ | | | XX$_{16}$ |
| 02F3$_{16}$ | | | XX$_{16}$ |
| 02F4$_{16}$ | | | XX$_{16}$ |
| 02F5$_{16}$ | | | XX$_{16}$ |
| 02F6$_{16}$ | CAN0 slot 9: Data Field | | XX$_{16}$ |
| 02F7$_{16}$ | | | XX$_{16}$ |
| 02F8$_{16}$ | | | XX$_{16}$ |
| 02F9$_{16}$ | | | XX$_{16}$ |
| 02FA$_{16}$ | | | XX$_{16}$ |
| 02FB$_{16}$ | | | XX$_{16}$ |
| 02FC$_{16}$ | | | XX$_{16}$ |
| 02FD$_{16}$ | | | XX$_{16}$ |
| 02FE$_{16}$ | CAN0 slot 9: Time Stamp | | XX$_{16}$ |
| 02FF$_{16}$ | | | XX$_{16}$ |

Note 1: Location in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

X : Undefined

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0300$_{16}$ | CAN0 slot 10: Identifier / DLC | | XX$_{16}$ |
| 0301$_{16}$ | | | XX$_{16}$ |
| 0302$_{16}$ | | | XX$_{16}$ |
| 0303$_{16}$ | | | XX$_{16}$ |
| 0304$_{16}$ | | | XX$_{16}$ |
| 0305$_{16}$ | | | XX$_{16}$ |
| 0306$_{16}$ | CAN0 slot 10: Data Field | | XX$_{16}$ |
| 0307$_{16}$ | | | XX$_{16}$ |
| 0308$_{16}$ | | | XX$_{16}$ |
| 0309$_{16}$ | | | XX$_{16}$ |
| 030A$_{16}$ | | | XX$_{16}$ |
| 030B$_{16}$ | | | XX$_{16}$ |
| 030C$_{16}$ | | | XX$_{16}$ |
| 030D$_{16}$ | | | XX$_{16}$ |
| 030E$_{16}$ | CAN0 slot 10: Time Stamp | | XX$_{16}$ |
| 030F$_{16}$ | | | XX$_{16}$ |
| 0310$_{16}$ | CAN0 slot 11: Identifier / DLC | | XX$_{16}$ |
| 0311$_{16}$ | | | XX$_{16}$ |
| 0312$_{16}$ | | | XX$_{16}$ |
| 0313$_{16}$ | | | XX$_{16}$ |
| 0314$_{16}$ | | | XX$_{16}$ |
| 0315$_{16}$ | | | XX$_{16}$ |
| 0316$_{16}$ | CAN0 slot 11: Data Field | | XX$_{16}$ |
| 0317$_{16}$ | | | XX$_{16}$ |
| 0318$_{16}$ | | | XX$_{16}$ |
| 0319$_{16}$ | | | XX$_{16}$ |
| 031A$_{16}$ | | | XX$_{16}$ |
| 031B$_{16}$ | | | XX$_{16}$ |
| 031C$_{16}$ | | | XX$_{16}$ |
| 031D$_{16}$ | | | XX$_{16}$ |
| 031E$_{16}$ | CAN0 slot 11: Time Stamp | | XX$_{16}$ |
| 031F$_{16}$ | | | XX$_{16}$ |
| 0320$_{16}$ | CAN0 slot 12: Identifier / DLC | | XX$_{16}$ |
| 0321$_{16}$ | | | XX$_{16}$ |
| 0322$_{16}$ | | | XX$_{16}$ |
| 0323$_{16}$ | | | XX$_{16}$ |
| 0324$_{16}$ | | | XX$_{16}$ |
| 0325$_{16}$ | | | XX$_{16}$ |
| 0326$_{16}$ | CAN0 slot 12: Data Field | | XX$_{16}$ |
| 0327$_{16}$ | | | XX$_{16}$ |
| 0328$_{16}$ | | | XX$_{16}$ |
| 0329$_{16}$ | | | XX$_{16}$ |
| 032A$_{16}$ | | | XX$_{16}$ |
| 032B$_{16}$ | | | XX$_{16}$ |
| 032C$_{16}$ | | | XX$_{16}$ |
| 032D$_{16}$ | | | XX$_{16}$ |
| 032E$_{16}$ | CAN0 slot 12: Time Stamp | | XX$_{16}$ |
| 032F$_{16}$ | | | XX$_{16}$ |
| 0330$_{16}$ | CAN0 slot 13: Identifier / DLC | | XX$_{16}$ |
| 0331$_{16}$ | | | XX$_{16}$ |
| 0332$_{16}$ | | | XX$_{16}$ |
| 0333$_{16}$ | | | XX$_{16}$ |
| 0334$_{16}$ | | | XX$_{16}$ |
| 0335$_{16}$ | | | XX$_{16}$ |
| 0336$_{16}$ | CAN0 slot 13: Data Field | | XX$_{16}$ |
| 0337$_{16}$ | | | XX$_{16}$ |
| 0338$_{16}$ | | | XX$_{16}$ |
| 0339$_{16}$ | | | XX$_{16}$ |
| 033A$_{16}$ | | | XX$_{16}$ |
| 033B$_{16}$ | | | XX$_{16}$ |
| 033C$_{16}$ | | | XX$_{16}$ |
| 033D$_{16}$ | | | XX$_{16}$ |
| 033E$_{16}$ | CAN0 slot 13: Time Stamp | | XX$_{16}$ |
| 033F$_{16}$ | | | XX$_{16}$ |

Note 1: Location in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

X : Undefined

| Address | Register | Symbol | After reset |
|---|---|---|---|
| 0340₁₆ | CAN0 slot 14: Identifier / DLC | | XX₁₆ |
| 0341₁₆ | | | XX₁₆ |
| 0342₁₆ | | | XX₁₆ |
| 0343₁₆ | | | XX₁₆ |
| 0344₁₆ | | | XX₁₆ |
| 0345₁₆ | | | XX₁₆ |
| 0346₁₆ | CAN0 slot 14: Data Field | | XX₁₆ |
| 0347₁₆ | | | XX₁₆ |
| 0348₁₆ | | | XX₁₆ |
| 0349₁₆ | | | XX₁₆ |
| 034A₁₆ | | | XX₁₆ |
| 034B₁₆ | | | XX₁₆ |
| 034C₁₆ | | | XX₁₆ |
| 034D₁₆ | | | XX₁₆ |
| 034E₁₆ | CAN0 slot 14: Time Stamp | | XX₁₆ |
| 034F₁₆ | | | XX₁₆ |
| 0350₁₆ | CAN0 slot 15: Identifier / DLC | | XX₁₆ |
| 0351₁₆ | | | XX₁₆ |
| 0352₁₆ | | | XX₁₆ |
| 0353₁₆ | | | XX₁₆ |
| 0354₁₆ | | | XX₁₆ |
| 0355₁₆ | | | XX₁₆ |
| 0356₁₆ | CAN0 slot 15: Data Field | | XX₁₆ |
| 0357₁₆ | | | XX₁₆ |
| 0358₁₆ | | | XX₁₆ |
| 0359₁₆ | | | XX₁₆ |
| 035A₁₆ | | | XX₁₆ |
| 035B₁₆ | | | XX₁₆ |
| 035C₁₆ | | | XX₁₆ |
| 035D₁₆ | | | XX₁₆ |
| 035E₁₆ | CAN0 slot 15: Time Stamp | | XX₁₆ |
| 035F₁₆ | | | XX₁₆ |
| 0360₁₆ | CAN0 Global mask | C0GMR | XX₁₆ |
| 0361₁₆ | | | XX₁₆ |
| 0362₁₆ | | | XX₁₆ |
| 0363₁₆ | | | XX₁₆ |
| 0364₁₆ | | | XX₁₆ |
| 0365₁₆ | | | XX₁₆ |
| 0366₁₆ | CAN0 local mask A | C0LMAR | XX₁₆ |
| 0367₁₆ | | | XX₁₆ |
| 0368₁₆ | | | XX₁₆ |
| 0369₁₆ | | | XX₁₆ |
| 036A₁₆ | | | XX₁₆ |
| 036B₁₆ | | | XX₁₆ |
| 036C₁₆ | CAN0 local mask B | C0LMBR | XX₁₆ |
| 036D₁₆ | | | XX₁₆ |
| 036E₁₆ | | | XX₁₆ |
| 036F₁₆ | | | XX₁₆ |
| 0370₁₆ | | | XX₁₆ |
| 0371₁₆ | | | XX₁₆ |
| ≈ | | | ≈ |
| 03B4₁₆ | | | |
| 03B5₁₆ | | | |
| 03B6₁₆ | | | |
| 03B7₁₆ | | | |
| 03B8₁₆ | | | |
| 03B9₁₆ | | | |
| ≈ | | | ≈ |
| 03FA₁₆ | | | |
| 03FB₁₆ | | | |
| 03FC₁₆ | | | |
| 03FD₁₆ | | | |
| 03FE₁₆ | | | |
| 03FF₁₆ | | | |

Note 1: Location in the SFR area where nothing is allocated are reserved areas. Do not access these areas for read or write.

X : Undefined

# 5. Electrical Characteristics

### Table 5.1 Absolute maximum ratings

| Symbol | Parameter | | Condition | Rated value | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | | - 0.3 to 6.5 | V |
| $V_I$ | Input voltage | $\overline{RESET}$, $V_{REF}$, $X_{IN}$<br>$P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$, $P2_1$,<br>$P3_0$ to $P3_7$, $P4_0$ to $P4_7$, $P5_0$ to $P5_2$, CNVss (Note 1) | | - 0.3 to Vcc + 0.3 | V |
| $V_O$ | Output voltage | $P0_0$ to $P0_7$, $P1_0$ to $P1_7$, $P2_0$, $P2_1$, $P3_0$ to $P3_7$,<br>$P4_0$ to $P4_7$, $P5_0$ to $P5_2$, $X_{OUT}$ | | - 0.3 to Vcc + 0.3 | V |
| | | $IV_{CC}$ | | - 0.3 to 2.8V | V |
| $P_d$ | Power dissipation | | Topr = 25 °C | 300 | mW |
| $T_{opr}$ | Operating ambient temperature | | | - 40 to 85 (Note 2) | °C |
| $T_{stg}$ | Storage temperature | | | - 65 to 150 | °C |

Note 1: CNVSS pin of flash memory version: -0.3 to 6.5 V

Note 2: When flash memory version is program/erase mode: 0 to 60 °C

**Table 5.2 Recommended operating conditions**
**(Unless otherwise noted: Vcc = 4.2V to 5.5V, Topr = -40 to 85°C)**

| Symbol | Parameter | | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ. | Max. | |
| Vcc | Supply voltage | | | 4.2 | 5.0 | 5.5 | V |
| Vss | Supply voltage | | | | 0 | | V |
| VIH | HIGH input voltage | P00 to P07, P10 to P17, P20, P21, P30 to P37, P40 to P47, P50 to P52, XIN, RESET, CNVSS | | 0.8Vcc | | Vcc | V |
| VIL | LOW input voltage | P00 to P07, P10 to P17, P20, P21, P30 to P37, P40 to P47, P50 to P52, XIN, RESET, CNVSS | | 0 | | 0.2Vcc | V |
| IOH (peak) | HIGH peak output current | P00 to P07, P10 to P17, P20, P21, P30 to P37, P40 to P47, P50 to P52 | | | | - 10.0 | mA |
| IOH (avg) | HIGH average output current | P00 to P07, P10 to P17, P20, P21, P30 to P37, P40 to P47, P50 to P52 | | | | - 5.0 | mA |
| IOL (peak) | LOW peak output current | P00 to P07, P20, P21, P30 to P37, P40 to P47, P50 to P52 | | | | 10.0 | mA |
| | | P10 to P17 | HIGH POWER | | | 20.0 | mA |
| | | | LOW POWER | | | 10.0 | |
| IOL (avg) | LOW average output current | P00 to P07, P20, P21, P30 to P37, P40 to P47, P50 to P52 | | | | 5.0 | mA |
| | | P10 to P17 | HIGH POWER | | | 10.0 | mA |
| | | | LOW POWER | | | 5.0 | |
| f (XIN) | Main clock input oscillation frequency (Note 3) | | Vcc=4.2V to 5.5V | 0 | | 16 | MHz |
| f (XCIN) | Subclock oscillation frequency | | | | 32.768 | 50 | kHz |

Note 1: The average output current is an average value measured over 100ms.

Note 2: Keep output current as follows:

The sum of port P00 to P03, P13 to P17, P21, P34 to P37, P46, P47, P50 to P52 IOL (peak) is under 60 mA. The sum of port P00 to P03, P13 to P17, P21, P34 to P37, P46, P47, P50 to P52 IOH (peak) is under 60 mA. The sum of port P04 to P07, P10 to P12, P20, P30 to P33, P40 to P45 IOL (peak) is under 60 mA. The sum of port P04 to P07, P10 to P12, P20, P30 to P33, P40 to P45 IOH (peak) is under 60 mA.

Note 3: Relationship between main clock oscillation frequency and supply voltage is shown as below.

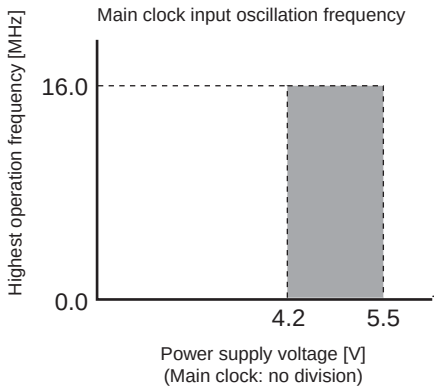


**Table 5.3 Electrical characteristics (1)**
**(Unless otherwise noted: $V_{CC}$ = 5V, $V_{SS}$ = 0V at Topr = -40 to 85°C, f($X_{IN}$) = 16MHz)**

| Symbol | Parameter | | Measuring condition | Standard | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| $V_{OH}$ | HIGH output voltage $P0_0$ to $P0_7$,$P1_0$ to $P1_7$,$P2_0$ to $P2_1$, $P3_0$ to $P3_7$,$P4_0$ to $P4_7$,$P5_0$ to $P5_2$ | | $I_{OH}$ = - 5 mA | 3.0 | | | V |
| | | | $I_{OH}$ = - 200 µA | 4.7 | | | |
| $V_{OH}$ | HIGH output voltage $X_{OUT}$ | HIGH POWER | $I_{OH}$ = - 1 mA | 3.0 | | | V |
| | | LOW POWER | $I_{OH}$ = - 0.5 mA | 3.0 | | | |
| $V_{OH}$ | HIGH output voltage $X_{COUT}$ | HIGH POWER | No load | | 2.5 | | V |
| | | LOW POWER | No load | | 1.6 | | |
| $V_{OL}$ | LOW output voltage $P0_0$ to $P0_7$,$P2_0$,$P2_1$,$P3_0$ to $P3_7$, $P4_0$ to $P4_7$,$P5_0$ to $P5_2$ | | $I_{OL}$ = 5 mA | | | 2.0 | V |
| | | | $I_{OL}$ = 200 µA | | | 0.45 | |
| $V_{OL}$ | LOW output voltage $P1_0$ to $P1_7$ | HIGH POWER | $I_{OL}$ = 10 mA | | | 2.0 | V |
| | | LOW POWER | $I_{OL}$ = 5 mA | | | 2.0 | |
| $V_{OL}$ | LOW output voltage $X_{OUT}$ | HIGH POWER | $I_{OH}$ = 1 mA | | | 2.0 | V |
| | | LOW POWER | $I_{OH}$ = 0.5 mA | | | 2.0 | |
| $V_{OL}$ | LOW output voltage $X_{COUT}$ | HIGH POWER | No load | | 0 | | V |
| | | LOW POWER | No load | | 0 | | |
| $V_{T+}$ -$V_{T-}$ | Hysteresis $\overline{CNTR_0}$,$\overline{TCIN}$, $\overline{INT_0}$ to $\overline{INT_3}$,$\overline{CLK_0}$,$\overline{CLK_1}$,$P4_5$ $RxD_0$,$RxD_1$,$\overline{KI_0}$ to $\overline{KI_3}$,$CRX_0$ | | | 0.2 | | 0.8 | V |
| $V_{T+}$ -$V_{T-}$ | Hysteresis $\overline{RESET}$ | | | 0.2 | | 1.8 | V |
| $I_{IH}$ | HIGH input current $P0_0$ to $P0_7$,$P1_0$ to $P1_7$,$P2_0$,$P2_1$, $P3_0$ to $\overline{P3_7}$,$P4_0$ to $P4_7$,$P5_0$ to $P5_2$, $X_{IN}$,$\overline{RESET}$,CNVss | | $V_I$ = 5V | | | 5.0 | µA |
| $I_{IL}$ | LOW input current $P0_0$ to $P0_7$,$P1_0$ to $P1_7$,$P2_0$,$P2_1$, $P3_0$ to $\overline{P3_7}$,$P4_0$ to $P4_7$,$P5_0$ to $P5_2$, $X_{IN}$,$\overline{RESET}$,CNVss | | $V_I$ = 0V | | | -5.0 | µA |
| $R_{PULLUP}$ | Pull-up resistor $P0_0$ to $P0_7$,$P1_0$ to $P1_7$,$P2_0$,$P2_1$, $P3_0$ to $P3_7$,$P4_0$ to $P4_7$,$P5_0$ to $P5_2$ | | $V_I$ = 0V | 30.0 | 50.0 | 167.0 | kΩ |
| $R_{fXIN}$ | Feedback resistor $X_{IN}$ | | | | 1.0 | | MΩ |
| $R_{fXCIN}$ | Feedback resistor $X_{CIN}$ | | | | 15.0 | | MΩ |
| $V_{RAM}$ | RAM retention voltage | | When clock is stopped | 2.0 | | | V |
| $R_{OSC}$ | Oscillation frequency of On-chip oscillator | Mask ROM | | 300 | 600 | 1200 | kHz |
| | | Flash memory | | | | | |

**Table 5.4 Electrical characteristics (2)**
**(Unless otherwise noted: $V_{CC}$ = 5V, $V_{SS}$ = 0V at Topr = 25°C, f($X_{IN}$) = 16MHz)**

| Symbol | Parameter | Measuring condition | | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| Icc | Power supply current | I/O pin has no load | Mask ROM | f($X_{IN}$) = 16 MHz Square wave, no division | | 12.0 | 22.0 | mA |
| | | | Flash memory | | | 14.0 | 24.0 | mA |
| | | | Mask ROM | On-chip oscillator mode No division | | 300 | | µA |
| | | | Flash memory | | | 800 | | µA |
| | | | Mask ROM | On-chip oscillator mode When a WAIT instruction is executed | | 60 | | µA |
| | | | Flash memory | | | 100 | | µA |
| | | | Mask ROM | f($X_{CIN}$) = 32 kHz Square wave | | 20 | | µA |
| | | | Flash memory | | | 450 | | µA |
| | | | Mask ROM | f($X_{CIN}$) = 32 kHz When a WAIT instruction is executed | | 2 | | µA |
| | | | Flash memory | f($X_{CIN}$) = 32 kHz When a WAIT instruction is executed | | 2 | | µA |
| | | | Mask ROM | Topr = 25 °C when clock is stopped | | 0.8 | 3 | µA |
| | | | Flash memory | | | 0.8 | 3 | µA |

**Table 5.5 Power supply timing circuit characteristics**

| Symbol | Parameter | Measuring condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| td(P-R) | Timer for internal power supply stabilization during powering-on | $V_{CC}$ = 4.2 to 5.5 V | | | 2 | ms |
| td(R-S) | Stop release time | | | | 150 | µs |
| td(W-S) | Wait release time during low power dissipation mode | | | | 150 | µs |
| td(M-L) | Timer for internal power supply stabilization when main clock oscillation starts | | | | 150 | µs |

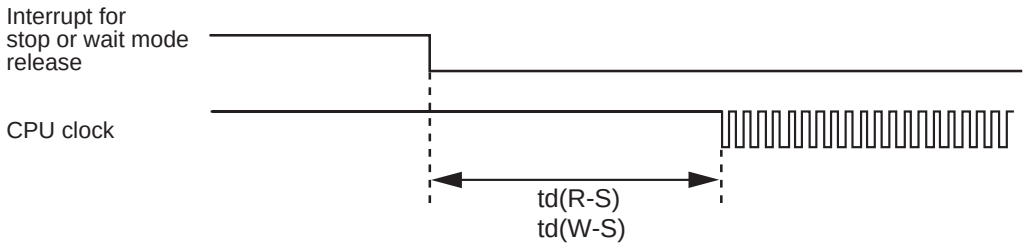


**Table 5.6 Flash memory version electrical characteristics**
**(Unless otherwise noted: Vcc = 4.2 to 5.5 V, Topr= 0 to 60°C)**

| Symbol | Parameter | | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. (Note 1) | Max. | |
| - | Erase/write cycle (Note 2) | | 100 (Note 3) | | | cycle |
| - | Word programming time | | | 75 | 600 | µs |
| - | Block erasing time | 2Kbyte block | | 0.2 | 9 | s |
| | | 8Kbyte block | | 0.4 | 9 | s |
| | | 16Kbyte block | | 0.7 | 9 | s |
| | | 32Kbyte block | | 1.2 | 9 | s |
| td(SR-ES) | Transition time from erasure operation to erase-suspend | | | | 20 | ms |
| - | Data retention | | 10 | | | year |

Note1: Vcc=5.0V, Topr=25°C
Note2: Definition of Programming and erasure times
The Programming and erasure times are defined to be per-block erasure times. For example a case where a 2K-byte block is programmed in 1,024 operations by writing one word at a time and erased thereafter. Performing multiple programs to the same address before an erase operation is prohibited.
Note 3: Minimum number of programming/erasure for which operation is guaranteed.

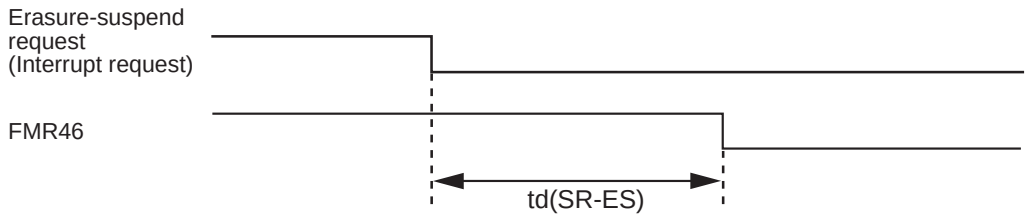


**Table 5.7 A/D conversion characteristics**
**(Unless otherwise noted: $V_{CC}$ = $V_{REF}$ = 5V, $V_{SS}$ = 0V at Topr = 25°C, f($X_{IN}$) = 16MHz)**

| Symbol | Parameter | | Measuring condition | | Standard | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| – | Resolution | | $V_{REF}$ =$V_{CC}$ | | | | 10 | Bits |
| – | Absolute accuracy | Sample & hold function not available | $V_{REF}$ =$V_{CC}$ = 5V | | | | ±3 | LSB |
| | | Sample & hold function available(10bit) | $V_{REF}$ =$V_{CC}$ = 5V | $AN_0$ to $AN_{11}$ input | | | ±3 | LSB |
| | | | | $ANEX_0$, $ANEX_1$ input, external op-amp connected mode | | | ±7 | LSB |
| | | Sample & hold function available(8bit) | $V_{REF}$ =$V_{CC}$ = 5V | | | | ±2 | LSB |
| $R_{LADDER}$ | Ladder resistance | | $V_{REF}$ =$V_{CC}$ | | 10 | | 40 | kΩ |
| $t_{CONV}$ | Conversion time(10bit) | | f($X_{IN}$)=10MHz, $Ø_{AD}$=$f_{AD}$=10MHz | | 3.3 | | | µs |
| $t_{CONV}$ | Conversion time(8bit) | | f($X_{IN}$)=10MHz, $Ø_{AD}$=$f_{AD}$=10MHz | | 2.8 | | | µs |
| $t_{SAMP}$ | Sampling time | | f($X_{IN}$)=10MHz, $Ø_{AD}$=$f_{AD}$=10MHz | | 0.3 | | | µs |
| $V_{REF}$ | Reference voltage | | f($X_{IN}$)=10MHz, $Ø_{AD}$=$f_{AD}$=10MHz | | 2 | | $V_{CC}$ | V |
| $V_{IA}$ | Analog input voltage | | f($X_{IN}$)=10MHz, $Ø_{AD}$=$f_{AD}$=10MHz | | 0 | | $V_{REF}$ | V |

Note 1: Divide the $f_{AD}$ if f($X_{IN}$) exceeds 10MHz, and make AD operation clock frequency ($Ø_{AD}$) equal to or lower than 10MHz.

**Table 5.8 D/A conversion characteristics**
**(Unless otherwise noted: $V_{CC}$ = $V_{REF}$ = 5V, $V_{SS}$ = 0V at Topr = 25°C, f($X_{IN}$) = 16MHz)**

| Symbol | Parameter | Measuring condition | Standard | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| – | Resolution | | | | 8 | Bits |
| – | Absolute accuracy | | | | 1.0 | % |
| $t_{su}$ | Setup time | | | | 3 | µs |
| $R_O$ | Output resistance | | 4 | 10 | 20 | kΩ |
| $I_{VREF}$ | Reference power supply input current | (Note 1) | | | 1.5 | mA |

Note 1: The A/D converter's ladder resistance is not included.
When D/A register contents are not "00$_{16}$", the current $I_{VREF}$ always flows even though $V_{REF}$ may have been set to be unconnected by the A/D control register.

## 5.1 Timing requirements

**(Unless otherwise noted: $V_{CC}$ = 5V, $V_{SS}$ = 0V at Topr = -40 to 85°C)**

**Table 5.9 $X_{IN}$ input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(XIN)}$ | $X_{IN}$ input cycle time | 62.5 | | ns |
| $t_{wH(XIN)}$ | $X_{IN}$ input HIGH pulse width | 30 | | ns |
| $t_{wL(XIN)}$ | $X_{IN}$ input LOW pulse width | 30 | | ns |

**Table 5.10 $CNTR_0$ input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CNTR0)}$ | $CNTR_0$ input cycle time | 100 | | ns |
| $t_{wH(CNTR0)}$ | $CNTR_0$ input HIGH pulse width | 40 | | ns |
| $t_{wL(CNTR0)}$ | $CNTR_0$ input LOW pulse width | 40 | | ns |

**Table 5.11 TCIN input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(TCIN)}$ | TCIN input cycle time | 400(Note 1) | | ns |
| $t_{wH(TCIN)}$ | TCIN input HIGH pulse width | 200(Note 2) | | ns |
| $t_{wL(TCIN)}$ | TCIN input LOW pulse width | 200(Note 2) | | ns |

Note 1: Use the greater value, either (1/digital filter clock frequency X 6) or min. value.

Note 2: Use the greater value, either (1/digital filter clock frequency X 3) or min. value.

**Table 5.12 Serial I/O**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 200 | | ns |
| $t_{w(CKH)}$ | CLKi input HIGH pulse width | 100 | | ns |
| $t_{w(CKL)}$ | CLKi input LOW pulse width | 100 | | ns |
| $t_{d(C-Q)}$ | TxDi output delay time | | 80 | ns |
| $t_{h(C-Q)}$ | TxDi hold time | 0 | | ns |
| $t_{su(D-C)}$ | RxDi input setup time | 30 | | ns |
| $t_{h(C-D)}$ | RxDi input hold time | 90 | | ns |

**Table 5.13 External interrupt $\overline{INTi}$ input**

| Symbol | Parameter | Standard | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| $t_{w(INH)}$ | $\overline{INTi}$ input HIGH pulse width | 250(Note 1) | | ns |
| $t_{w(INL)}$ | $\overline{INTi}$ input LOW pulse width | 250(Note 2) | | ns |

Note 1: When the $\overline{INT0}$ input filter select bit selects the digital filter, use the $\overline{INT0}$ input HIGH pulse width to the greater value, either (1/digital filter clock frequency X 3) or min. value.

Note 2: When the $\overline{INT0}$ input filter select bit selects the digital filter, use the $\overline{INT0}$ input LOW pulse width to the greater value, either (1/digital filter clock frequency X 3) or min. value.

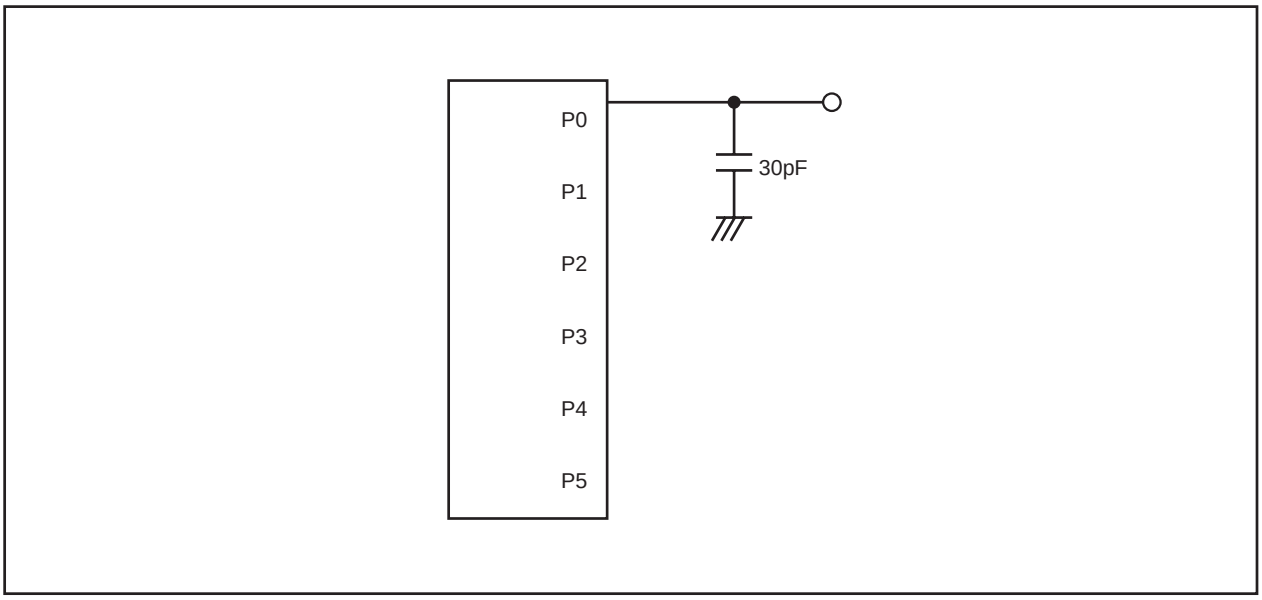



**Figure 5.1 Port P0 to P5 measurement circuit**

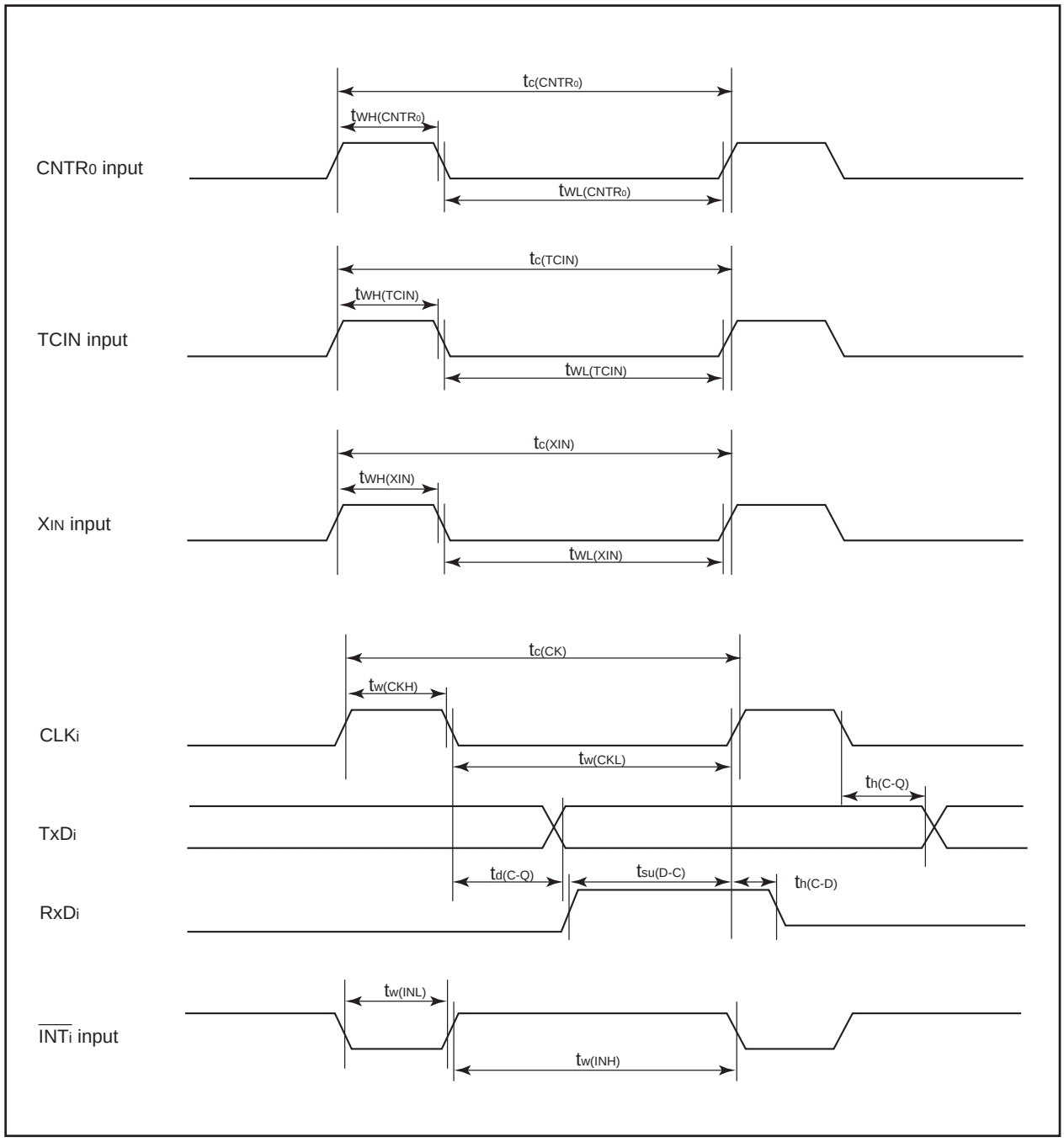


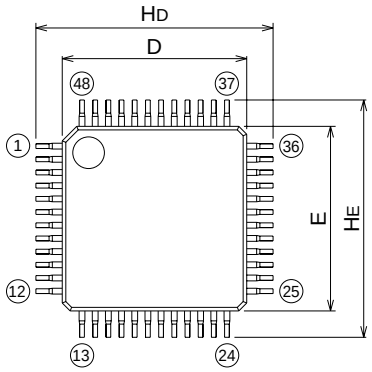

**Figure 5.2 Vcc=5V timing diagram**

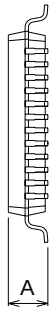
## Package Dimension

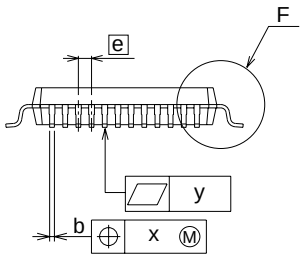
**48P6Q-A** Recommended

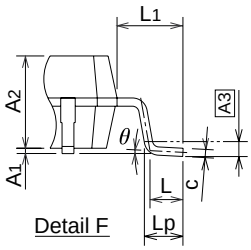
**Plastic 48pin 7×7mm body LQFP**

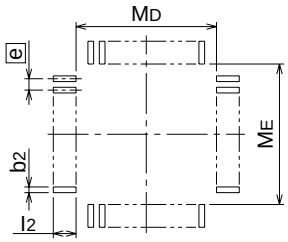
| EIAJ Package Code | JEDEC Code | Weight(g) | Lead Material |
|---|---|---|---|
| LQFP48-P-77-0.50 | – | – | Cu Alloy |




Recommended Mount Pad

| Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | – | – | 1.7 |
| A1 | 0 | 0.1 | 0.2 |
| A2 | – | 1.4 | – |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.105 | 0.125 | 0.175 |
| D | 6.9 | 7.0 | 7.1 |
| E | 6.9 | 7.0 | 7.1 |
| e | – | 0.5 | – |
| HD | 8.8 | 9.0 | 9.2 |
| HE | 8.8 | 9.0 | 9.2 |
| L | 0.35 | 0.5 | 0.65 |
| L1 | – | 1.0 | – |
| Lp | 0.45 | 0.6 | 0.75 |
| A3 | – | 0.25 | – |
| x | – | – | 0.08 |
| y | – | – | 0.1 |
| θ | 0° | – | 8° |
| b2 | – | 0.225 | – |
| I2 | 1.0 | – | – |
| MD | – | 7.4 | – |
| ME | – | 7.4 | – |

| REVISION HISTORY | M16C/1N Group Data Sheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | Oct 20, 2004 | – | First edition issued (Renesas Technology version) |

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