

M320C50 DSP



Digital Soft Megacells

Features

- Functionally compatible with the industry standard
- 32-bit ALU/accumulator
- 16 X 16 parallel multiplier
- 16-bit shifter
- 16-bit parallel logic space
- Up to 64k words each of program and data memory
- 64K I/O space
- Interrupt controller
- Serial port and TDM serial port
- Equivalent gates: 40,000

Description

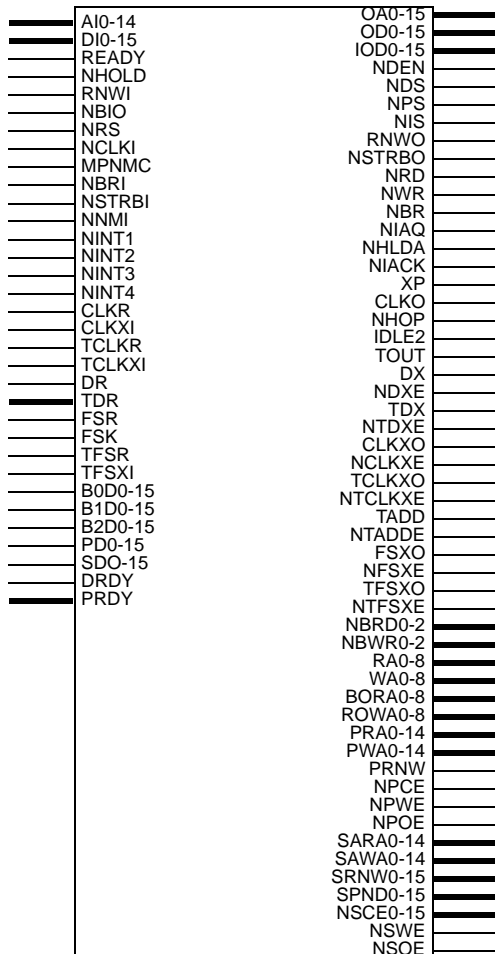
M320C50 is a digital signal processor with separate data and program memory. The program memory may be up to 64k words. The data memory may be up to 64k words, up to 32 words of which may be global access. It has 64k 16-bit I/O ports, sixteen of which are memory mapped. The central ALU has a 32-bit arithmetic logic unit, a 32-bit accumulator and accumulator buffer, a 16-bit scaling shifter, and a 16 X 16 parallel multiplier. A separate parallel logic unit can perform bit manipulations on any data memory location or control/status register. It has eight auxiliary registers, an eight level hardware stack, and a four stage instruction pipeline. The M320C50 contains no ROM or RAM but provides functional interconnect signals for connecting to memory blocks.

Peripherals are controlled through 28 memory-mapped registers and consists of: a timer, a serial port, a time-divison-multiplexed serial port, a programmable wait-state generator, an interrupt controller, and the I/O ports.

The M320C50 is compatible, including instructions execution times, with industry standard devices.

LOGIC SYMBOL

M320C50



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