M320x Series 9x14 mm, 3.3/2.5/1.8 Volt, PECL/LVDS/CML, VCXO



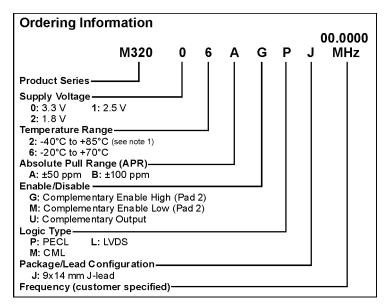


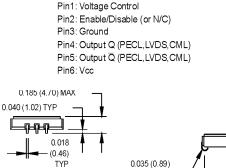


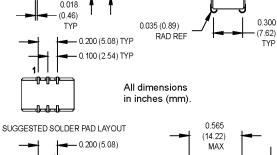
- Featuring *QiK Chip*[™] Technology
- Superior Jitter Performance (comparable to SAW based)
- APR of ±50 or ±100ppm over industrial temperature range
- Frequencies from 150 MHz to 1.4 GHz
- Designed for a short 2 week cycle time

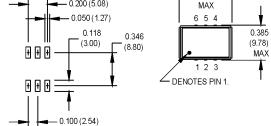
Phase Lock Loop Applications:

- Telecommunications such as SONET / SDH / DWDM / FEC / SERDES / OC-3 thru OC-192
- Wireless base stations / WLAN / Gigabit Ethernet
- Avionic flight controls and military communications









MtronPTI reserves the right to make changes to the product(s) and service(s) described herein without notice. No liability is assumed as a result of their use or application.

Please see www.mtronpti.com for our complete offering and detailed datasheets. Contact us for your application specific requirements: MtronPTI 1-800-762-8800.





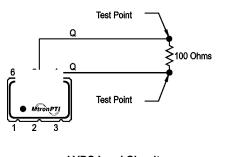
	PARAMETER	Symbol	Min.	Тур.	Max.	Units	Condition/Notes
Electrical Specifications	Frequency Range	F	150		1400	MHz	See Note 2
	Operating Temperature	TA	(See ordering information)			See Note 1	
	Storage Temperature	Ts	-55		+125	°C	
	Frequency Stability	$\Delta F/F$		±25		ppm	
	Aging 1st Year Thereafter (per year)		-3 -1		+3 +1	ppm ppm	
	Pullability/APR		(See ordering information)			See Note 3	
	Control Voltage	Vc	0.18 0.25 0.30	0.90 1.25 1.65	1.62 2.25 3.0	V V V	@ 1.8V Vcc @ 2.5V Vcc @ 3.3V Vcc
	Linearity			1	5	%	Positive Monotonic
	Modulation Bandwidth	fm	20			KHz	-3 dB bandwidth
	Input Impedance	Zin	500k	1M		Ohms	@ DC
	Supply Voltage	Vcc	1.71	1.8	1.89	V	
			2.375	2.5	2.625	V	
			3.135	3.3	3.465	V	
	Input Current	lcc			125	mA	PECL/LVDS/CML
	Load		50 Ohms to (Vcc –2) Vdc 100 Ohm differential load			See Note 4 PECL Waveform LVDS/CML Waveform	
	Symmetry (Duty Cycle)		45		55	%	@ 50% of waveform
	Output Skew			TBD			
	Differential Voltage		350	425 TBD	500	mVppd	LVDS CML
	Common Mode Output Voltage	Vcm		1.2		V	LVDS
	Logic "1" Level	Voh	Vcc -1.02			V	LVPECL
	Logic "0" Level	Vol			Vcc -1.63	V	LVPECL
	Rise/Fall Time	Tr/Tf		0.23	0.50	ns	@ 20/80% LVPECL
	Enable Function		80% Vcc min. or N/C: output active 20% Vcc max: output disables to high-Z				Output Option G
			20% Vcc max: output active 80% Vcc min: output disables to high-Z			Output Option M	
	Start up Time			10		ms	
	Phase Jitter @ 622.08 MHz	φJ		0.50		ps RMS	Integrated 12 kHz – 20 MHz

Note 1: If the device is powered up below -20°C and then the ambient temperature rises 105°C during normal operation, the output will be interrupted for approximately 2-3 ms. A correction is in process an will be available Q1 2007

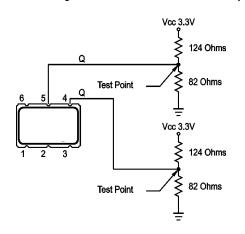
Note 2: Contact factory for exact frequency availability over 945 MHz.

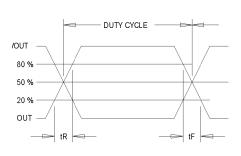
Note 3: APR specification is inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging for one year at 50°C mean ambient temperature.

Note 4: See Load Circuit Diagram in this Datasheet. Consult factory with nonstandard output load requirements.



LVDS Load Circuit





Output Waveform: LVDS/CML/PECL

3.3V LVPECL Load Circuit

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