

1. Overview

The M32C/82 group microcomputer is a single-chip control unit that utilizes high-performance silicon gate CMOS technology with the M32C/80 series CPU core. The M32C/82 group is available in 144-pin and 100-pin plastic molded LQFP/QFP packages.

With a 16-Mbyte address space, this microcomputer combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

It incorporates a multiplier and DMAC adequate for office automation, communication devices and industrial equipments and other high-speed processing applications.

1.1 Applications

Audio, cameras, office equipment, communications equipment, portable equipment, etc.

1.2 Difference between the M32C/82 Group and the M32C/83 Group

The M32C/82 group microcomputer has less peripheral functions than the M32C/83 group microcomputer. The intelligent I/O group 3, CAN and the A/D1 converter are not provided in the M32C/82 group. Interrupt requests, and as a result interrupts, DMAC, and DMACII, caused by these peripheral functions are not available in the M32C/82 group.

1.2 Performance Outline

Tables 1.1 and 1.2 list performance outlines of the M32C/82 group.

Table 1.1 M32C/82 Group Performance (144-Pin Package)

Item		Performance
CPU	Basic instructions	108 instructions
	Shortest instruction execution time	33 ns (f(BCLK)=30 MHz, Vcc=4.2 V to 5.5 V) 50 ns (f(BCLK)=20 MHz, Vcc=3.0 V to 5.5 V)
	Operation mode	Single-chip mode, Memory expansion mode and Microprocessor mode
	Address space	16 Mbytes
	Memory capacity	See Table 1.3
Peripheral function	Port	123 I/O pins and 1 input pin
	Multifunction timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit
	Intelligent I/O	Time measurement function: 16 bits x 12 channels Waveform generating function: 16 bits x 20 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing, Clock synchronous variable length serial I/O, IEBus ⁽¹⁾)
	Serial I/O	5 channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus ⁽¹⁾ , I ² C bus ⁽²⁾
	A/D converter	10-bit A/D converter: 1 circuit, 34 channels
	D/A converter	8 bits x 2 channels
	DMAC	4 channels
	DMAC II	Can be activated by all peripheral function interrupt factors Immediate transfer, Calculation transfer and Chain transfer functions
	DRAMC	$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh, self-refresh, EDO, FP
	CRC calculation circuit	CRC-CCITT
	XY converter	16 bits x 16 bits
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupt	41 internal and 8 external sources, 5 software sources Interrupt priority level: 7
	Clock generating circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally
	Oscillation stop detect function	Main clock oscillation stop detect function
Electric characteristics	Supply voltage	4.2 V to 5.5 V (f(BCLK)=30 MHz) 3.0 V to 5.5 V (f(BCLK)=20 MHz, through VDC) 3.0 V to 3.6 V (f(BCLK)=20 MHz, not through VDC)
	Power consumption	28 mA (Vcc=5 V, f(BCLK)=30 MHz) 17 mA (Vcc=3.3 V, f(BCLK)=20 MHz) 470 μ A (Vcc=5 V, f(XCIN)=32 kHz, in wait mode) 340 μ A (Vcc=3.3 V, f(XCIN)=32 kHz, through VDC in wait mode) 5.0 μ A (Vcc=3.3 V, f(XCIN)=32 kHz, not through VDC in wait mode) 0.4 μ A (Vcc=5 V, f(XCIN)=32 kHz, in stop mode) 0.4 μ A (Vcc=3.3 V, f(XCIN)=32 kHz, in stop mode)
Operating ambient temperature		-20 to 85°C, -40 to 85°C (optional)
Package		144-pin plastic molded LQFP

NOTES:

- IEBus is a trademark of NEC Electronics Corporation.
 - I²C bus is a trademark of Koninklijke Philips Electronics N. V.
- All options are on a request basis.

Table 1.2 M32C/82 Group Performance (100-Pin Package)

Item		Performance
CPU	Basic instructions	108 instructions
	Shortest instruction execution time	33 ns (f(BCLK)=30 MHz, Vcc=4.2 V to 5.5 V) 50 ns (f(BCLK)=20 MHz, Vcc=3.0 V to 5.5 V)
	Operation mode	Single-chip mode, Memory expansion mode and Microprocessor mode
	Address space	16 Mbytes
	Memory capacity	See Table 1.3
Peripheral function	Port	87 I/O pins and 1 input pin
	Multifunction timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit
	Intelligent I/O	Time measurement function: 16 bits x 5 channels Waveform generating function: 16 bits x 8 channels Communication function (Clock synchronous serial I/O, Clock asynchronous serial I/O, HDLC data processing, Clock synchronous variable length serial I/O, IEBus ⁽¹⁾)
	Serial I/O	5 channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus ⁽¹⁾ , I ² C bus ⁽²⁾
	A/D converter	10-bit A/D converter: 1 circuit, 26 channels
	D/A converter	8 bits x 2 channels
	DMAC	4 channels
	DMAC II	Can be activated by all peripheral function interrupt factors Immediate transfer, Calculation transfer and Chain transfer functions
	DRAMC	CAS-before-RAS refresh, self-refresh, EDO, FP
	CRC calculation circuit	CRC-CCITT
	X Y converter	16 bits x 16 bits
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupt	41 internal and 8 external sources, 5 software sources Interrupt priority level: 7
	Clock generating circuit	4 circuits Main clock oscillation circuit(*), Sub clock oscillation circuit(*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor. Ceramic resonator or crystal oscillator must be connected externally
	Oscillation stop detect function	Main clock oscillation stop detect function
Electric characteristics	Supply voltage	4.2 V to 5.5 V (f(BCLK)=30 MHz) 3.0 V to 5.5 V (f(BCLK)=20 MHz, through VDC) 3.0 V to 3.6 V (f(BCLK)=20 MHz, not through VDC)
	Power consumption	28 mA (Vcc=5 V, f(BCLK)=30 MHz) 17 mA (Vcc=3.3 V, f(BCLK)=20 MHz) 470 μ A (Vcc=5 V, f(XCIN)=32 kHz, in wait mode) 340 μ A (Vcc=3.3 V, f(XCIN)=32 kHz, through VDC in wait mode) 5.0 μ A (Vcc=3.3 V, f(XCIN)=32 kHz, not through VDC in wait mode) 0.4 μ A (Vcc=5 V, f(XCIN)=32 kHz, in stop mode) 0.4 μ A (Vcc=3.3 V, f(XCIN)=32 kHz, in stop mode)
Operating ambient temperature		-20 to 85°C, -40 to 85°C (optional)
Package		100-pin plastic molded LQFP/QFP

NOTES:

1. IEBus is a trademark of NEC Electronics Corporation.
 2. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
- All options are on a request basis.

1.3 Block Diagram

Figure 1.1 shows a block diagram of the M32C/82 group microcomputer.

The M32C/82 group microcomputer contains ROM and RAM as memory to store instructions and data, CPU to execute calculations and peripheral functions such as interrupt, timer, serial I/O, DMAC, CRC calculation circuit, A/D converter, D/A converter, DRAMC, intelligent I/O and ports.

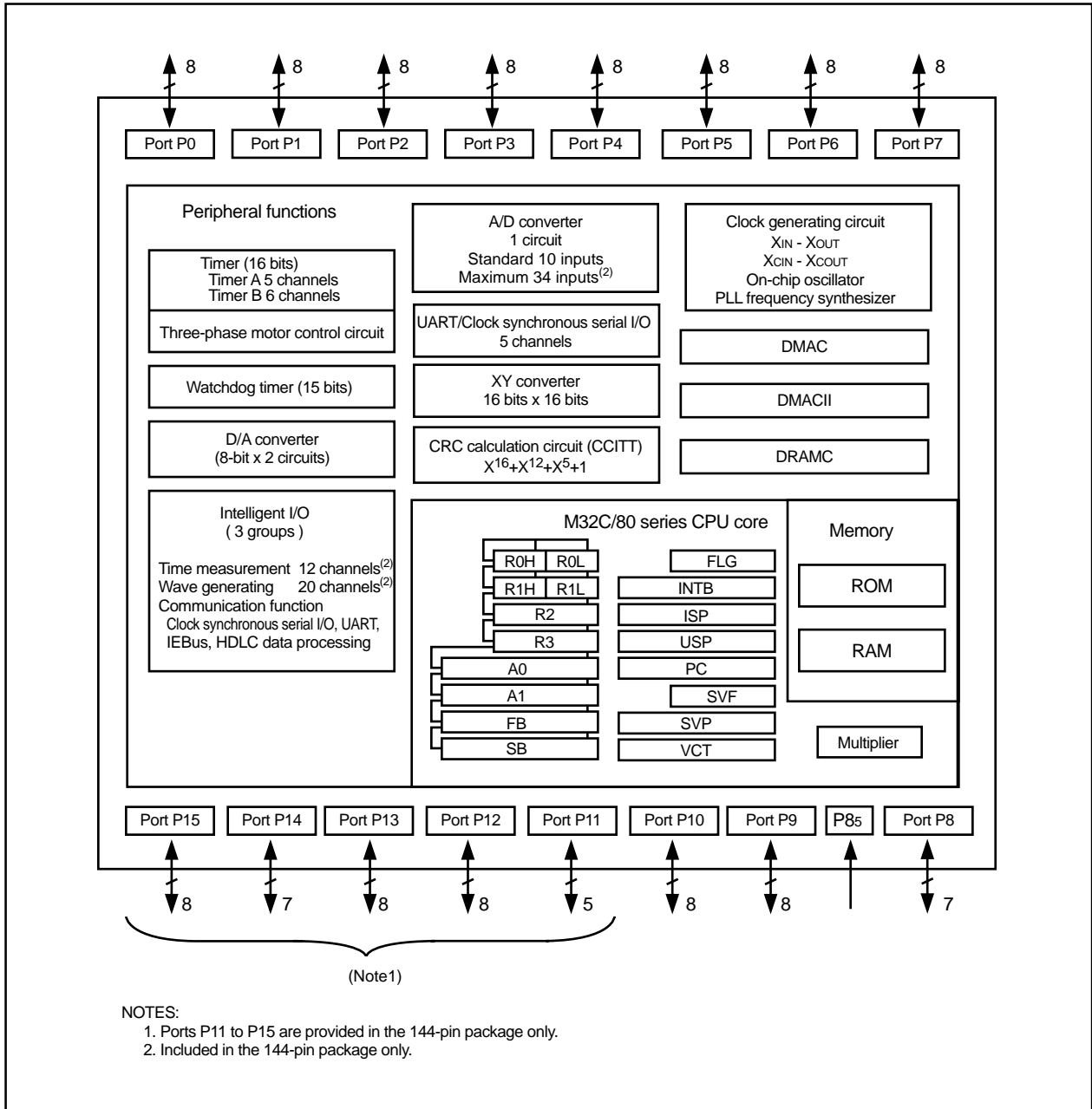


Figure 1.1 M32C/82 Group Block Diagram

1.4 Product Information

Renesas plans to release the following products in the M32C/82 group:

- (1) Support for the masked ROM version
- (2) ROM/RAM capacity
- (3) Package

100P6S-A : Plastic molded QFP
 100P6Q-A : Plastic molded LQFP
 144P6Q-A : Plastic molded LQFP

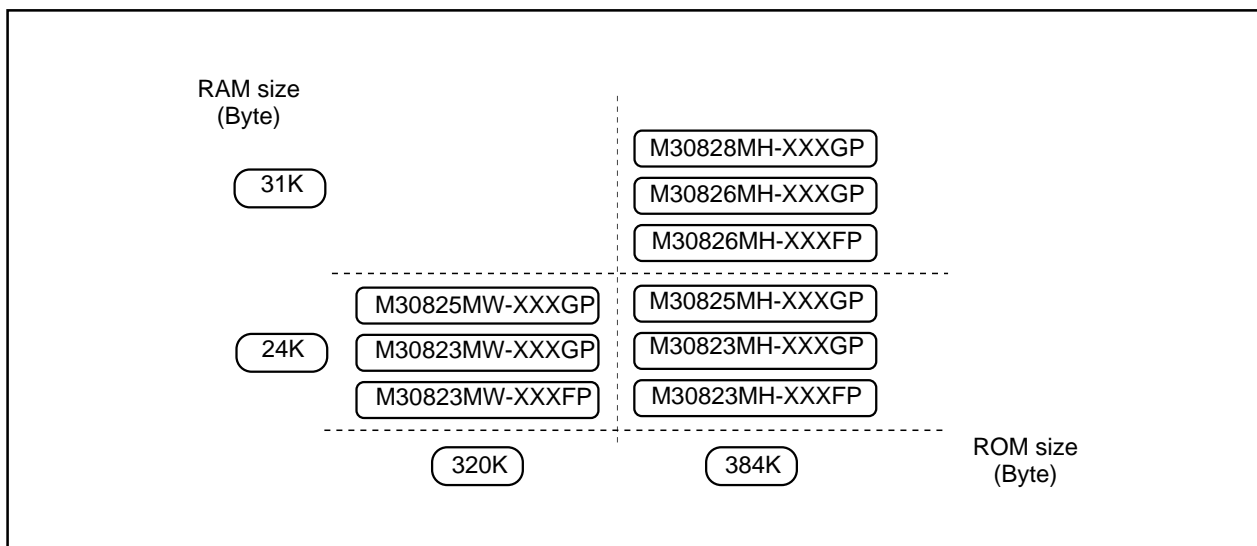


Figure 1.2 ROM/RAM

Table 1.3 M32C/82 Group

Type number	ROM capacity	RAM capacity	Package type	Remarks
M30825MW-XXXGP	320 Kbytes	24 Kbytes	144P6Q-A	Masked ROM
M30823MW-XXXGP			100P6Q-A	
M30823MW-XXXFP			100P6S-A	
M30825MH-XXXGP	384 Kbytes	24 Kbytes	144P6Q-A	
M30823MH-XXXGP			100P6Q-A	
M30823MH-XXXFP			100P6S-A	
M30828MH-XXXGP	384 Kbytes	31 Kbytes	144P6Q-A	
M30826MH-XXXGP			100P6Q-A	
M30826MH-XXXFP			100P6S-A	

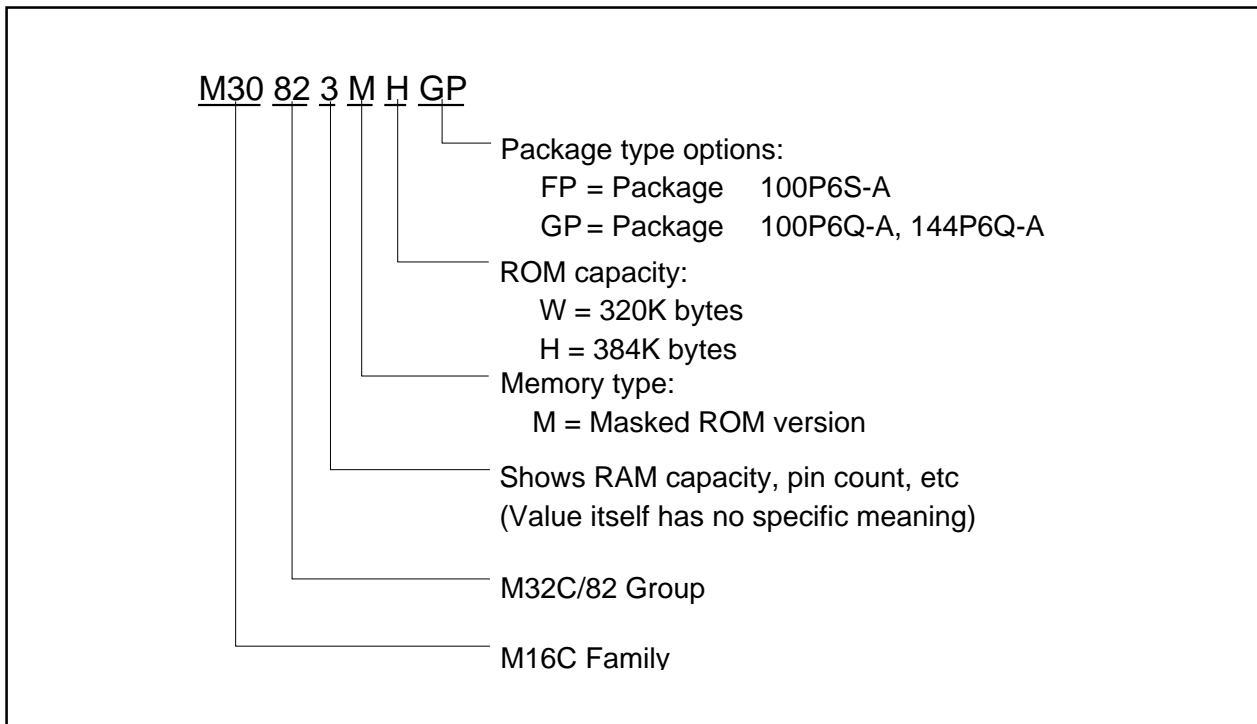


Figure 1.3 Product Numbering System

1.5 Pin Assignments

Figures 1.4 to 1.6 show pin assignments (top view).

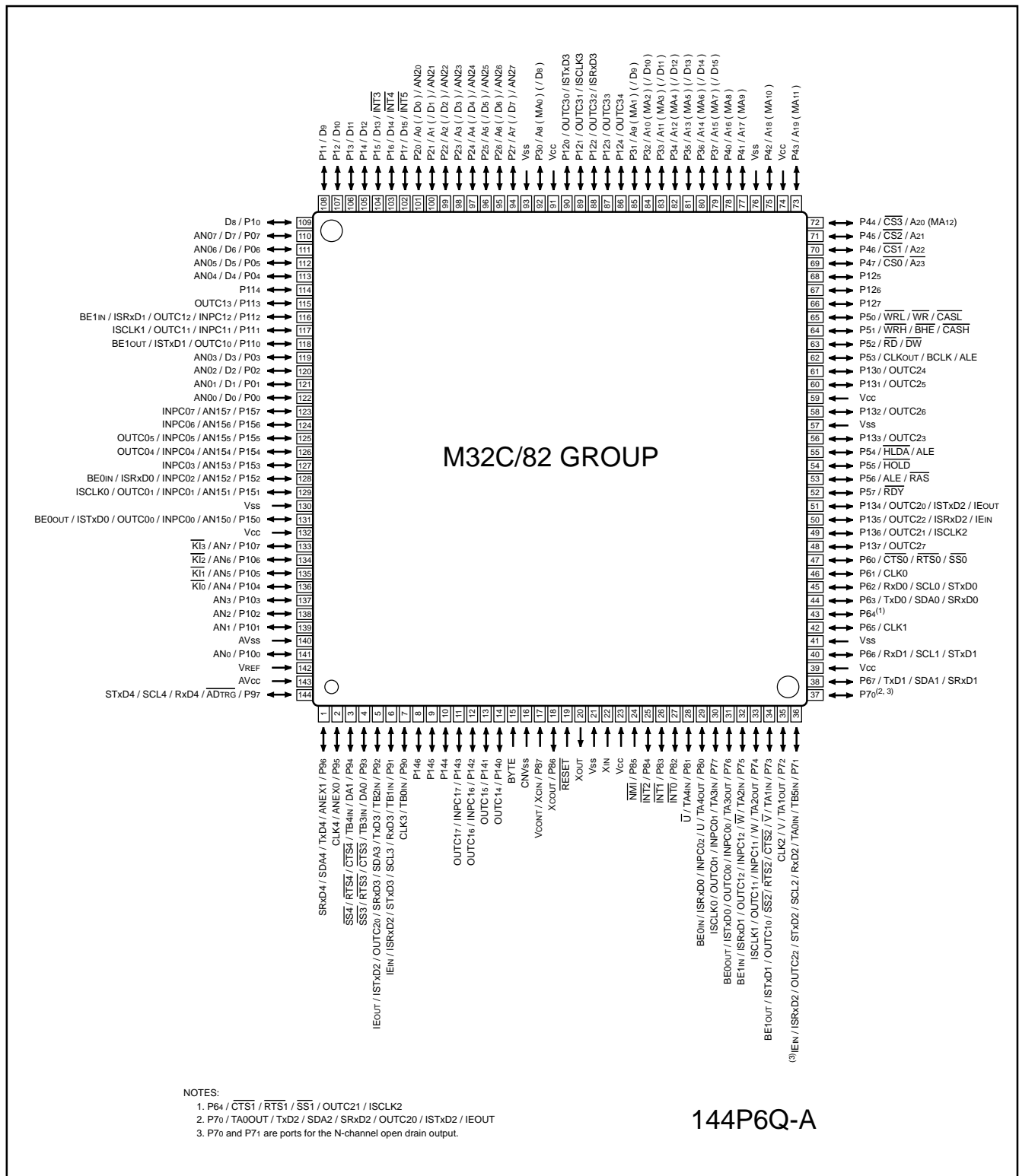


Figure 1.4 Pin Assignment for 144-Pin Package

Table 1.4 Pin Characteristics for 144-Pin Package

Pin No	Control pin	Port	Interrupt pin	Timer pin	UART pin	Intelligent I/O pin	Analog pin	Bus control pin
1		P96			TxD4/SDA4/SRxD4		ANEX1	
2		P95			CLK4		ANEX0	
3		P94		TB4IN	CTS4/RTS4/SS4		DA1	
4		P93		TB3IN	CTS3/RTS3/SS3		DA0	
5		P92		TB2IN	TxD3/SDA3/SRxD3	OUTC2 ₀ /IE _{OUT} /ISTxD2		
6		P91		TB1IN	RxD3/SCL3/STxD3	IE _{IN} /ISRxD2		
7		P90		TB0IN	CLK3			
8		P146						
9		P145						
10		P144						
11		P143				INPC17/OUTC17		
12		P142				INPC16/OUTC16		
13		P141				OUTC15		
14		P140				OUTC14		
15	BYTE							
16	CNVSS							
17	X _{CIN} /V _{CONT}	P87						
18	X _{COU} T	P86						
19	RESET							
20	X _{OUT}							
21	V _{SS}							
22	X _{IN}							
23	V _{CC}							
24		P85	NMI					
25		P84	INT2					
26		P83	INT1					
27		P82	INT0					
28		P81		TA4 _{IN} /U				
29		P80		TA4 _{OUT} /U		INPC02/ISRxD0/BE0 _{IN}		
30		P77		TA3 _{IN}		INPC01/OUTC01/ISCLK0		
31		P76		TA3 _{OUT}		INPC00/OUTC00/ISTxD0/BE0 _{OUT}		
32		P75		TA2 _{IN} /W		INPC12/OUTC12/ISRxD1/BE1 _{IN}		
33		P74		TA2 _{OUT} /W		INPC11/OUTC11/ISCLK1		
34		P73		TA1 _{IN} /V	CTS2/RTS2/SS2	OUTC10/ISTxD1/BE1 _{OUT}		
35		P72		TA1 _{OUT} /V	CLK2			
36		P71		TB5 _{IN} /TA0 _{IN}	RxD2/SCL2/STxD2	OUTC22/ISRxD2/IE _{IN}		
37		P70		TA0 _{OUT}	TxD2/SDA2/SRxD2	OUTC20/ISTxD2/IE _{OUT}		
38		P67			TxD1/SDA1/SRxD1			
39	V _{CC}							
40		P66			RxD1/SCL1/STxD1			
41	V _{SS}							
42		P65			CLK1			
43		P64			CTS1/RTS1/SS1	OUTC21/ISCLK2		
44		P63			TxD0/SDA0/SRxD0			
45		P62			RxD0/SCL0/STxD0			
46		P61			CLK0			
47		P60			CTS0/RTS0/SS0			
48		P137				OUTC27		

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No	Control pin	Port	Interrupt pin	Timer pin	UART pin	Intelligent I/O pin	Analog pin	Bus control pin
49		P136				OUTC21/ISCLK2		
50		P135				OUTC22/ISRxD2/IE _{IN}		
51		P134				OUTC20/ISTxD2/IE _{OUT}		
52		P57						$\overline{\text{RDY}}$
53		P56						$\overline{\text{ALE/RAS}}$
54		P55						$\overline{\text{HOLD}}$
55		P54						$\overline{\text{HLDA/ALE}}$
56		P133				OUTC23		
57	V _{SS}							
58		P132				OUTC26		
59	V _{CC}							
60		P131				OUTC25		
61		P130				OUTC24		
62		P53						$\overline{\text{CLK}_{\text{OUT}}/\text{BCLK/ALE}}$
63		P52						$\overline{\text{RD/DW}}$
64		P51						$\overline{\text{WRH/BHE/CASH}}$
65		P50						$\overline{\text{WRL/WR/CASL}}$
66		P127						
67		P126						
68		P125						
69		P47						$\overline{\text{CS0/A23}}$
70		P46						$\overline{\text{CS1/A22}}$
71		P45						$\overline{\text{CS2/A21}}$
72		P44						$\overline{\text{CS3/A20(MA12)}}$
73		P43						A _{19(MA11)}
74	V _{CC}							
75		P42						A _{18(MA10)}
76	V _{SS}							
77		P41						A _{17(MA9)}
78		P40						A _{16(MA8)}
79		P37						A _{15(MA7)/(D15)}
80		P36						A _{14(MA6)/(D14)}
81		P35						A _{13(MA5)/(D13)}
82		P34						A _{12(MA4)/(D12)}
83		P33						A _{11(MA3)/(D11)}
84		P32						A _{10(MA2)/(D10)}
85		P31						A _{9(MA1)/(D9)}
86		P124						
87		P123						
88		P122						
89		P121						
90		P120						
91	V _{CC}							
92		P30						A _{8(MA0)/(D8)}
93	V _{SS}							
94		P27					AN27	A _{7/(D7)}
95		P26					AN26	A _{6/(D6)}
96		P25					AN25	A _{5/(D5)}

Table 1.4 Pin Characteristics for 144-Pin Package (Continued)

Pin No	Control pin	Port	Interrupt pin	Timer pin	UART pin	Intelligent I/O pin	Analog pin	Bus control pin
97		P24					AN24	A4(/D4)
98		P23					AN23	A3(/D3)
99		P22					AN22	A2(/D2)
100		P21					AN21	A1(/D1)
101		P20					AN20	A0(/D0)
102		P17	$\overline{\text{INT5}}$					D15
103		P16	$\overline{\text{INT4}}$					D14
104		P15	$\overline{\text{INT3}}$					D13
105		P14						D12
106		P13						D11
107		P12						D10
108		P11						D9
109		P10						D8
110		P07					AN07	D7
111		P06					AN06	D6
112		P05					AN05	D5
113		P04					AN04	D4
114		P114						
115		P113				OUTC13		
116		P112				INPC12/OUTC12/ISRxD1/BE1IN		
117		P111				INPC11/OUTC11/ISCLK1		
118		P110				OUTC10/ISTxD1/BE1OUT		
119		P03					AN03	D3
120		P02					AN02	D2
121		P01					AN01	D1
122		P00					AN00	D0
123		P157				INPC07	AN157	
124		P156				INPC06	AN156	
125		P155				INPC05/OUTC05	AN155	
126		P154				INPC04/OUTC04	AN154	
127		P153				INPC03	AN153	
128		P152				INPC02/ISRxD0/BE0IN	AN152	
129		P151				INPC01/OUTC01/ISCLK0	AN151	
130	Vss							
131		P150				INPC00/OUTC00/ISTxD0/BE0OUT	AN150	
132	Vcc							
133		P107	$\overline{\text{KI3}}$				AN7	
134		P106	$\overline{\text{KI2}}$				AN6	
135		P105	$\overline{\text{KI1}}$				AN5	
136		P104	$\overline{\text{KI0}}$				AN4	
137		P103					AN3	
138		P102					AN2	
139		P101					AN1	
140	AVss							
141		P100					AN0	
142	VREF							
143	AVcc							
144		P97			RxD4/SCL4/STxD4		$\overline{\text{ADTRG}}$	

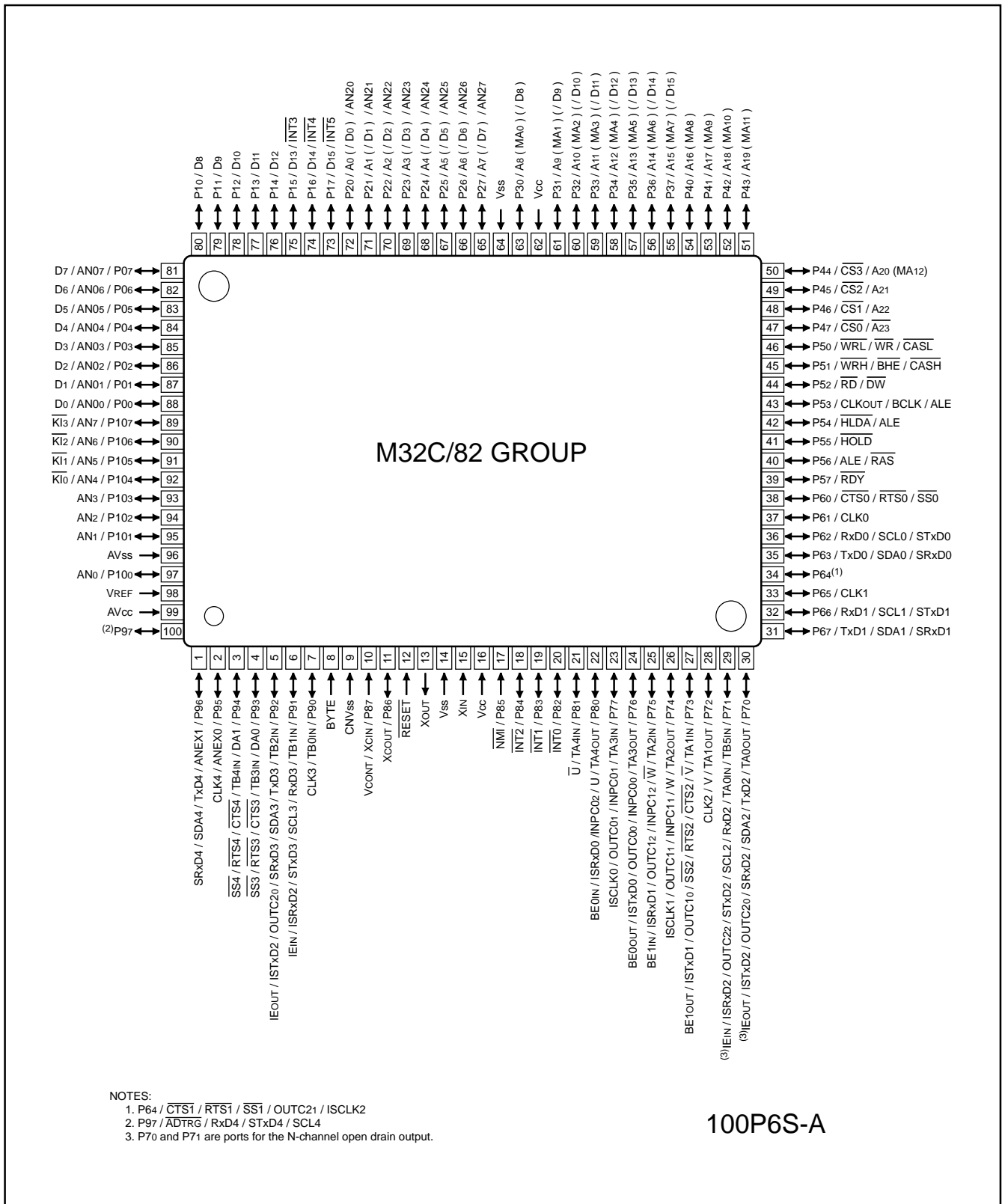


Figure 1.5 Pin assignment for 100-Pin Package

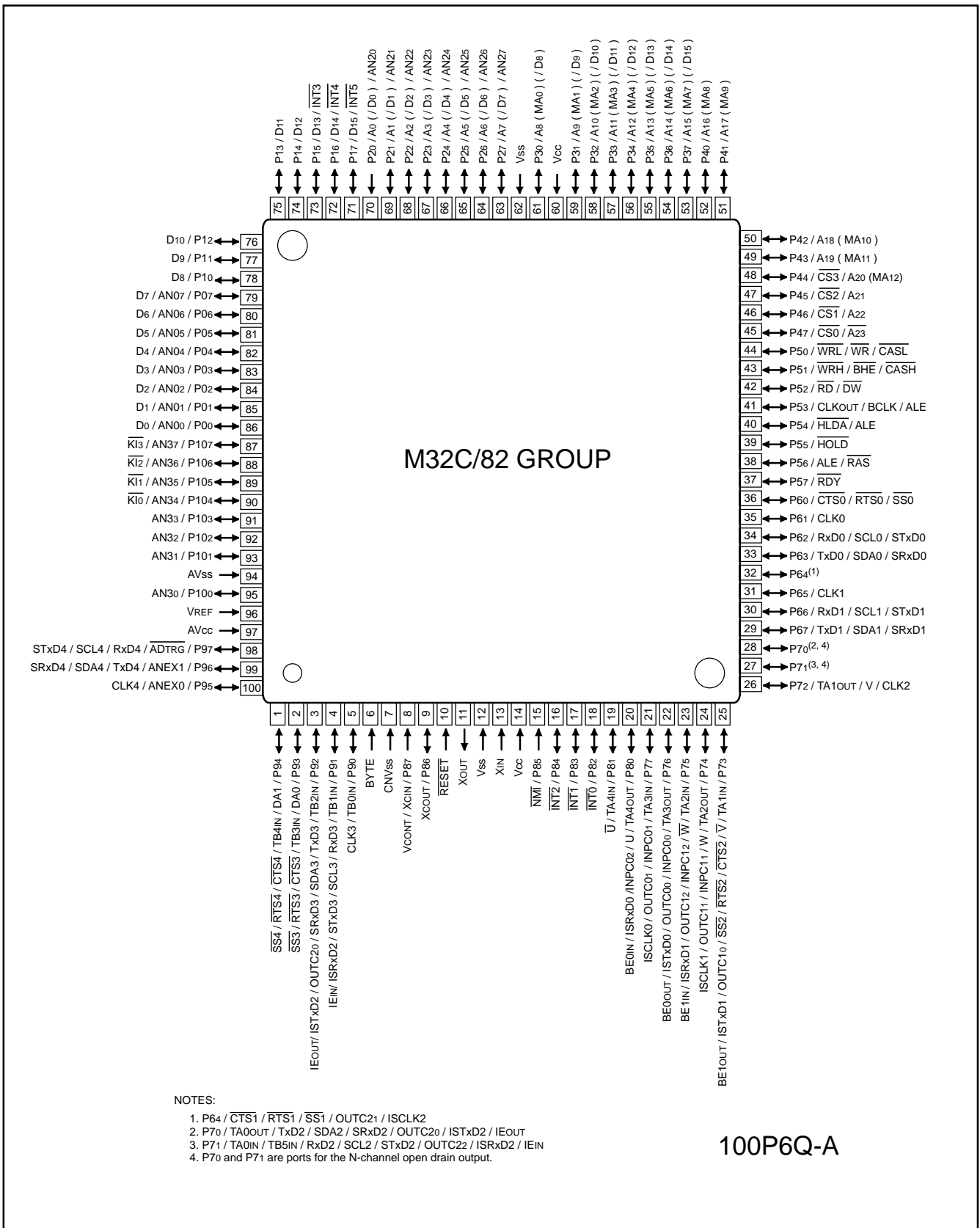


Figure 1.6 Pin Assignment for 100-Pin Package

Table 1.5 Pin Characteristics for 100-Pin Package

Package Pin No		Control pin	Port	Interrupt pin	Timer pin	UART pin	Intelligent I/O pin	Analog pin	Bus control pin
FP	GP								
1	99		P96			TxD4/SDA4/SRxD4		ANEX1	
2	100		P95			CLK4		ANEX0	
3	1		P94		TB4IN	CTS4/RTS4/SS4		DA1	
4	2		P93		TB3IN	CTS3/RTS3/SS3		DA0	
5	3		P92		TB2IN	TxD3/SDA3/SRxD3	OUTC2 ₀ /IE _{OUT} /ISTxD2		
6	4		P91		TB1IN	RxD3/SCL3/STxD3	IE _{IN} /ISRxD2		
7	5		P90		TB0IN	CLK3			
8	6	BYTE							
9	7	CNV _{SS}							
10	8	X _{CIN} /V _{CONT}	P87						
11	9	X _{COU} T	P86						
12	10	RESET							
13	11	X _{OUT}							
14	12	V _{SS}							
15	13	X _{IN}							
16	14	V _{CC}							
17	15		P85	NMI					
18	16		P84	INT ₂					
19	17		P83	INT ₁					
20	18		P82	INT ₀					
21	19		P81		TA4IN/ \bar{U}				
22	20		P80		TA4OUT/U		INPC0 ₂ /ISRxD0/BE0 _{IN}		
23	21		P77		TA3IN		INPC0 ₁ /OUTC0 ₁ /ISCLK0		
24	22		P76		TA3OUT		INPC0 ₀ /OUTC0 ₀ /ISTxD0/BE0 _{OUT}		
25	23		P75		TA2IN/ \bar{W}		INPC1 ₂ /OUTC1 ₂ /ISRxD1/BE1 _{IN}		
26	24		P74		TA2OUT/W		INPC1 ₁ /OUTC1 ₁ /ISCLK1		
27	25		P73		TA1IN/ \bar{V}	CTS2/RTS2/SS2	OUTC1 ₀ /ISTxD1/BE1 _{OUT}		
28	26		P72		TA1OUT/V	CLK2			
29	27		P71		TB5IN/TA0IN	RxD2/SCL2/STxD2	OUTC2 ₂ /ISRxD2/IE _{IN}		
30	28		P70		TA0OUT	TxD2/SDA2/SRxD2	OUTC2 ₀ /ISTxD2/IE _{OUT}		
31	29		P67			TxD1/SDA1/SRxD1			
32	30		P66			RxD1/SCL1/STxD1			
33	31		P65			CLK1			
34	32		P64			CTS1/RTS1/SS1	OUTC2 ₁ /ISCLK2		
35	33		P63			TxD0/SDA0/SRxD0			
36	34		P62			RxD0/SCL0/STxD0			
37	35		P61			CLK0			
38	36		P60			CTS0/RTS0/SS0			
39	37		P57						RDY
40	38		P56						ALE/RAS
41	39		P55						HOLD
42	40		P54						HLD \bar{A} /ALE
43	41		P53						CLK _{OUT} /BCLK/ALE
44	42		P52						RD/DW
45	43		P51						WRH/BHE/CASH
46	44		P50						WRL/WR/CASL
47	45		P47						CS0/A23
48	46		P46						CS1/A22
49	47		P45						CS2/A21
50	48		P44						CS3/A20(MA ₁₂)

Table 1.5 Pin Characteristics for 100-Pin Package (Continued)

Package pin No		Control pin	Port	Interrupt pin	Timer pin	UART pin	Intelligent I/O pin	Analog pin	Bus control pin
FP	GP								
51	49		P4 ₃						A19(MA11)
52	50		P4 ₂						A18(MA10)
53	51		P4 ₁						A17(MA9)
54	52		P4 ₀						A16(MA8)
55	53		P3 ₇						A15(MA7)/(D15)
56	54		P3 ₆						A14(MA6)/(D14)
57	55		P3 ₅						A13(MA5)/(D13)
58	56		P3 ₄						A12(MA4)/(D12)
59	57		P3 ₃						A11(MA3)/(D11)
60	58		P3 ₂						A10(MA2)/(D10)
61	59		P3 ₁						A9(MA1)/(D9)
62	60	Vcc							
63	61		P3 ₀						A8(MA0)/(D8)
64	62	Vss							
65	63		P2 ₇				AN2 ₇	A7(D7)	
66	64		P2 ₆				AN2 ₆	A6(D6)	
67	65		P2 ₅				AN2 ₅	A5(D5)	
68	66		P2 ₄				AN2 ₄	A4(D4)	
69	67		P2 ₃				AN2 ₃	A3(D3)	
70	68		P2 ₂				AN2 ₂	A2(D2)	
71	69		P2 ₁				AN2 ₁	A1(D1)	
72	70		P2 ₀				AN2 ₀	A0(D0)	
73	71		P1 ₇	INT5					D15
74	72		P1 ₆	INT4					D14
75	73		P1 ₅	INT3					D13
76	74		P1 ₄						D12
77	75		P1 ₃						D11
78	76		P1 ₂						D10
79	77		P1 ₁						D9
80	78		P1 ₀						D8
81	79		P0 ₇				AN0 ₇	D7	
82	80		P0 ₆				AN0 ₆	D6	
83	81		P0 ₅				AN0 ₅	D5	
84	82		P0 ₄				AN0 ₄	D4	
85	83		P0 ₃				AN0 ₃	D3	
86	84		P0 ₂				AN0 ₂	D2	
87	85		P0 ₁				AN0 ₁	D1	
88	86		P0 ₀				AN0 ₀	D0	
89	87		P10 ₇	KI ₃			AN7		
90	88		P10 ₆	KI ₂			AN6		
91	89		P10 ₅	KI ₁			AN5		
92	90		P10 ₄	KI ₀			AN4		
93	91		P10 ₃				AN3		
94	92		P10 ₂				AN2		
95	93		P10 ₁				AN1		
96	94	AVss							
97	95		P10 ₀				AN0		
98	96	VREF							
99	97	AVcc							
100	98		P9 ₇			RxD4/SCL4/STxD4		ADTRG	

1.6 Pin Description

Table 1.6 Pin Description (100-Pin and 144-Pin Packages)

Symbol	Function	I/O type	Description
Vcc	Power supply input	I	Apply 3.0 to 5.5 V to the Vcc pins.
Vss		I	Apply 0 V to the Vss pin.
CNVss	CNVss	I	Switches processor mode. Connect this pin to Vss to start up in single-chip mode (memory expansion mode). Connect this pin to Vcc to start up in microprocessor mode.
RESET	Reset input	I	The microcomputer is in a reset state when applying "L" to the RESET pin.
XIN	Clock input	I	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To use an external clock, input the clock to XIN and leave XOUT open.
XOUT	Clock output	O	
BYTE	Input to switch external data bus width	I	Switches the data bus in external memory space 3. The data bus is 16 bits wide when the BYTE pin is held "L" and 8 bits wide when the BYTE pin is held "H". Set to either. Connect this pin to Vss when an external bus is not used.
AVcc	Analog power supply input	I	Applies power supply for the A/D converter and D/A converter. Connect this pin to Vcc.
AVss	Analog power supply input	I	Applies power supply for the A/D converter and D/A converter. Connect this pin to Vss.
VREF	Reference voltage input	I	Applies reference voltage for the A/D converter.
P00 to P07	I/O port P0	I/O	8-bit I/O ports in CMOS having a direction register to select input or output. Each pin is set as an input port or output port. An input port in single-chip mode can be set for a pull-up or for no pull-up in 4-bit unit by program. When these pins are used as bus control pins in memory expansion mode and microprocessor mode, internal pull-up resistor cannot be selected. Ports used as input ports can be set for a pull-up or for no pull-up in the modes above.
D0 to D7	Data bus	I/O	Inputs and outputs data (D0 to D7) when these pins are set as the separate bus.
AN00 to AN07	Analog input pin	I	Analog input pins for the A/D converter
P10 to P17	I/O port P1	I/O	8-bit I/O ports having equivalent functions to P0
INT3 to INT5	INT interrupt input pin	I	Input pins for the INT interrupt
D8 to D15	Data bus	I/O	Inputs and outputs data (D8 to D15) when these pins are set as the separate bus.
P20 to P27	I/O port P2	I/O	8-bit I/O ports having equivalent functions to P0
A0 to A7	Address bus	O	Outputs 8 low-order address bits (A0 to A7).
A0/D0 to A7/D7	Address bus/data bus	I/O	Inputs and outputs data (D0 to D7) and outputs 8 low-order address bits (A0 to A7) by time-sharing when these pins are set as the multiplexed bus.
AN20 to AN27	Analog input pin	I	Analog input pins for A/D converter
P30 to P37	I/O port P3	I/O	8-bit I/O ports having equivalent functions to P0
A8 to A15	Address bus	O	Outputs 8 middle-order address bits (A8 to A15).
A8/D8 to A15/D15	Address bus/data bus	I/O	Inputs and outputs data (D8 to D15) and outputs 8 middle-order address bits (A8 to A15) by time-sharing when external 16-bit data bus is set as the multiplexed bus.
MA0 to MA7	Address bus	O	Outputs row addresses and column addresses by time-sharing when accessing the DRAM area.

I : Input O : Output I/O : Input and output

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Symbol	Function	I/O type	Description
P40 to P47	I/O port P4	I/O	8-bit I/O ports having equivalent functions to P0
A16 to A22, A23	Address bus	O	Outputs 8 high-order address bits (A16 to A22, A23). The highest-order bit (A23) inverted is also output.
CS0 to CS3	Chip-select	O	Outputs CS0 to CS3 signals. CS0 to CS3 are chip-select signals specifying an external space.
MA8 to MA12	Address bus	O	Outputs row addresses and column addresses by time-sharing when accessing the DRAM area.
P50 to P57	I/O port P5	I/O	8-bit I/O ports having equivalent functions to P0
CLKOUT	Clock output	O	Outputs the main clock divided by 8 or divided by 32 or the clock having the same frequency as the sub clock from P53.
WRL WR WRH BHE RD BCLK HLDA HOLD ALE RDY	Bus control pin	O O O O O O O I O I	Outputs WRL, WRH, (WR, BHE), RD, BCLK, HLDA and ALE signals. WRL and WRH or BHE and WR can be switched by program. ■ WRL, WRH and RD are selected The WRL signal becomes "L" by writing data to an even address in an external memory space. The WRH signal becomes "L" by writing data to an odd address in an external memory space. The RD pin signal becomes "L" by reading data in an external memory space. ■ WR, BHE and RD are selected The WR signal becomes "L" by writing data to an external memory space. The RD signal becomes "L" by reading data in an external memory space. The BHE signal becomes "L" by accessing an odd address. Select WR, BHE and RD for an external 8-bit data bus. While the HOLD pin is held "L", the microcomputer is placed in a hold state. In a hold state, HLDA outputs a "L" signal. ALE is a signal latching the address. While the RDY pin is held "L", the microcomputer is placed in a wait state.
DW CASL CASH RAS	DRAM bus control pin	O O O O	The DW signal becomes "L" by writing data to the DRAM area. CASL and CASH are signals indicating a timing to latch column addresses. The CASL signal becomes "L" by accessing an even address. The CASH signal becomes "L" by accessing an odd address. RAS is a signal latching row addresses.
P60 to P67	I/O port P6	I/O	8-bit I/O ports having equivalent functions to P0
CTS0, CTS1 RTS0, RTS1 SS0, SS1 CLK0, CLK1 RxD0, RxD1 SCL0, SCL1 STxD0, STxD1 TxD0, TxD1 SDA0, SDA1 SRxD0, SRxD1	UART pin	I O I I/O I I/O O O I/O I	I/O pins for UART0 (P60 to P63) and UART1 (P64 to P67)
ISCLK2 OUTC21	Intelligent I/O pin	I/O O	ISCLK2 inputs and outputs the clock for the intelligent I/O communication function. OUTC21 outputs the clock for the waveform generating function.

I : Input O : Output I/O : Input and output

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Symbol	Function	I/O type	Description
P70 to P77	I/O port P7	I/O	8-bit I/O ports having equivalent functions to P0 (P70 and P71 are ports for the N-channel open drain output.)
TA0OUT to TA3OUT TA0IN to TA3IN	Timer A pin	I/O I	I/O pins for timer A0 to A3
TB5IN	Timer B pin	I	Input pin for timer B5
V, \bar{V}	Three-phase motor	O	V-phase output pin
W, \bar{W}	control output pin	O	W-phase output pin
CTS2 RTS2 SS2 CLK2 RxD2 SCL2 STxD2 TxD2 SDA2 SRxD2	UART pin	I O I I/O I I/O O O I/O I	I/O pins for UART2
INPC00, INPC01 INPC11, INPC12 OUTC00, OUTC01 OUTC10 to OUTC12 OUTC20, OUTC22 ISCLK0, ISCLK1 ISTxD0 to ISTxD2 ISRxD1, ISRxD2 IEOUT IEIN BE0OUT BE1OUT BE1IN	Intelligent I/O pin	I O I/O O I O I O O I	INPC00, INPC01, INPC11 and INPC12 are input pins for the time measurement function. OUTC00, OUTC01, OUTC10 to OUTC12, OUTC20 and OUTC22 are output pins for the waveform generating function. ISCLK0 and ISCLK1 input and output the clock for the intelligent I/O communication function. ISRxD1, ISRxD2, IEIN and BE1IN input received data for the intelligent I/O communication function. ISTxD0 to ISTxD2, IEOUT, BE0OUT and BE1OUT output transmit data for the intelligent I/O communication function.

I : Input O : Output I/O : Input and output

Table 1.6 Pin Description (100-Pin and 144-Pin Packages) (Continued)

Symbol	Function	I/O type	Description
P80 to P84, P86, P87	I/O port P8	I/O	I/O ports having equivalent functions to P0
XCIN XCOUT	Sub clock	I O	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT.
VCONT	Low-pass filter connect pin for PLL frequency synthesizer pin		Connects the low-pass filter to the VCONT pin when using the PLL frequency synthesizer. Connect P86 to VSS to stabilize the PLL frequency.
TA4OUT TA4IN	Timer A pin	I/O I	I/O pins for timer A4
U, \bar{U}	Three-phase motor control output pin	O	U-phase output pins
INT0 to INT2	INT interrupt input pin	I	Input pins for the INT interrupt
INPC02 ISRxD0 BE0IN	Intelligent I/O pin	I I I	INPC02 is an input pin for the time measurement function. ISRxD0 and BE0IN input received data for the intelligent I/O communication function.
P85/ $\overline{\text{NMI}}$	NMI interrupt input pin	I	Input pin for the NMI interrupt. Pin states can be read by the P8_5 bit in the P8 register.
P90 to P97	I/O port P9	I/O	8-bit I/O ports having equivalent functions P0. The PRCR register prevents PD9 and PS3 registers from rewriting.
TB0IN to TB4IN	Timer B pin	I	Input pins for timers B0 to B4
$\overline{\text{CTS3}}$, $\overline{\text{CTS4}}$ $\overline{\text{RTS3}}$, $\overline{\text{RTS4}}$ $\overline{\text{SS3}}$, $\overline{\text{SS4}}$ CLK3, CLK4 RxD3, RxD4 SCL3, SCL4 STxD3, STxD4 TxD3, TxD4 SDA3, SDA4 SRxD3, SRxD4	UART pin	I O I I/O I I/O O O I/O I	I/O pins for UART3 (P90 to P93) and UART4 (P94 to P97)
DA0, DA1	D/A output pin	O	Output pins for the D/A converter
ANEX0, ANEX1, $\overline{\text{ADTRG}}$	A/D related pin	I/O I I	ANEX0 is an extended analog I/O pin for the A/D converter. ANEX1 is an extended analog input pin for the A/D converter. $\overline{\text{ADTRG}}$ is an A/D trigger input pin.
OUTC20 ISTxD2 IEOUT IEIN ISRxD2	Intelligent I/O pin	O O O I I	OUTC20 is an output pin for the waveform generating function. ISTxD2 and IEOUT output transmit data for the intelligent I/O communication function. ISRxD2 and IEIN input received data for the intelligent I/O communication function.
P100 to P107	I/O port P10	I/O	8-bit I/O ports having equivalent functions to P0
$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	Key input interrupt pin	I	Input pins for the key input interrupt
AN0 to AN7	Analog input pin	I	Analog input pins for the A/D converter

I : Input O : Output I/O : Input and output

Table 1.6 Pin Description (144-Pin Package only) (Continued)

Symbol	Function	I/O type	Description
P11 ₀ to P11 ₄	I/O port P11	I/O	5-bit I/O ports having equivalent functions to P0.
INPC11, INPC12	Intelligent I/O pin	I	INPC11 and INPC12 are input pins for the time measurement function.
OUTC1 ₀ to OUTC1 ₃		O	OUTC1 ₀ to OUTC1 ₃ are output pins for the waveform generating function.
ISCLK1		I/O	ISCLK1 inputs and outputs the clock for the intelligent I/O communication function.
ISRxD1		I	ISRxD1 and BE1IN input received data for the intelligent I/O communication function.
BE1IN		I	ISRxD1 and BE1IN input received data for the intelligent I/O communication function.
ISTxD1		O	ISTxD1 and BE1OUT output transmit data for the intelligent I/O communication function.
BE1OUT		O	ISTxD1 and BE1OUT output transmit data for the intelligent I/O communication function.
P12 ₀ to P12 ₇	I/O port P12	I/O	8-bit I/O ports having equivalent functions to P0
P13 ₀ to P13 ₇	I/O port P13	I/O	8-bit I/O ports having equivalent functions to P0
OUTC2 ₀ to OUTC2 ₇	Intelligent I/O pin	O	OUTC2 ₀ to OUTC2 ₇ are output pins for the waveform generating function.
ISCLK2		I/O	ISCLK2 inputs and outputs the clock for the intelligent I/O communication function.
ISRxD2		I	ISRxD2 and IEIN input received data for the intelligent I/O communication function.
IEIN		I	ISRxD2 and IEIN input received data for the intelligent I/O communication function.
ISTxD2		O	ISTxD2 and IEOUT output transmit data for the intelligent I/O communication function.
IEOUT		O	ISTxD2 and IEOUT output transmit data for the intelligent I/O communication function.
P14 ₀ to P14 ₆		I/O port P14	I/O
INPC16, INPC17	Intelligent I/O pin	I	INPC16 and INPC17 are input pins for the time measurement function.
OUTC14 to OUTC17		O	OUTC14 to OUTC17 are output pins for the waveform generating function.
P15 ₀ to P15 ₇	I/O port P15	I/O	8-bit I/O ports having equivalent functions to P0
INPC0 ₀ to INPC0 ₇	Intelligent I/O pin	I	INPC0 ₀ to INPC0 ₇ are input pins for the time measurement function.
OUTC0 ₀ , OUTC0 ₁		O	OUTC0 ₀ , OUTC0 ₁ , OUTC0 ₄ and OUTC0 ₅ are output pins for the waveform generating function.
OUTC0 ₄ , OUTC0 ₅		O	OUTC0 ₀ , OUTC0 ₁ , OUTC0 ₄ and OUTC0 ₅ are output pins for the waveform generating function.
ISCLK0		I/O	ISCLK0 inputs and outputs the clock for the intelligent I/O communication function.
ISRxD0		I	ISRxD0 and BE0IN input received data for the intelligent I/O communication function.
BE0IN		I	ISRxD0 and BE0IN input received data for the intelligent I/O communication function.
ISTxD0		O	ISTxD0 and BE0OUT output transmit data for the intelligent I/O communication function.
BE0OUT		O	ISTxD0 and BE0OUT output transmit data for the intelligent I/O communication function.
AN15 ₀ to AN15 ₇	Analog input port	I	Analog input pins for the A/D converter

I : Input O : Output I/O : Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.

A register bank comprises 8 registers (R0, R1, R2, R3, A0, A1, SB and FB) out of 28 CPU registers. Two sets of register banks are provided.

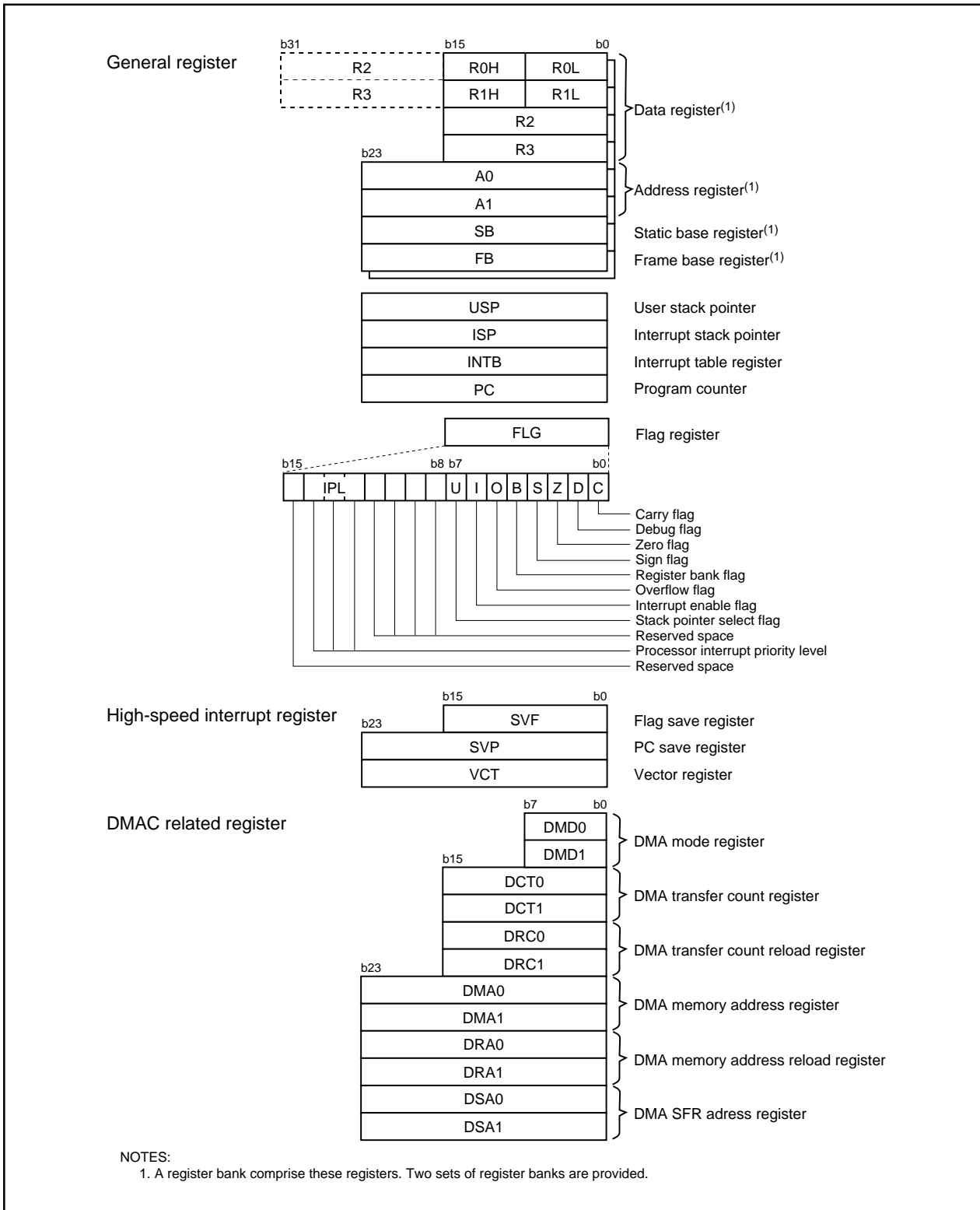


Figure 2.1 CPU Register

2.1 General Register

2.1.1 Data Registers (R0, R1, R2 and R3)

R0, R1, R2 and R3 are 16-bit registers for transfer, arithmetic and logic operations. R0 and R1 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R3R1.

2.1.2 Address Registers (A0 and A1)

A0 and A1 are 24-bit registers for A0-/A1-indirect addressing, A0-/A1-relative addressing, transfer, arithmetic and logic operations.

2.1.3 Static Base Register (SB)

SB is a 24-bit register for SB-relative addressing.

2.1.4 Frame Base Register (FB)

FB is a 24-bit register for FB-relative addressing.

2.1.5 Program Counter (PC)

PC is 24 bits wide. It indicates an address of an instruction to be executed.

2.1.6 Interrupt Table Register (INTB)

INTB is a 24-bit register indicating a starting address of an interrupt vector table.

2.1.7 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

USP and ISP as the stack pointer are 24 bits wide. The U flag can switch USP to ISP and vice versa. Refer to "2.1.8 Flag Register (FLG)" about the U flag. Set USP and ISP to even addresses to execute an interrupt sequence efficiently.

2.1.8 Flag Register (FLG)

FLG is a 16-bit register indicating a CPU state.

2.1.8.1 Carry Flag (C)

The C flag indicates whether carry or borrow occurs after an instruction is executed.

2.1.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

2.1.8.3 Zero Flag (Z)

The Z flag is set to "1" when the value of zero is obtained from an arithmetic calculation; otherwise "0".

2.1.8.4 Sign Flag (S)

The S flag is set to "1" when a negative value is obtained from an arithmetic calculation; otherwise "0".

2.1.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is set to "0". The register bank 1 is selected when this flag is set to "1".

2.1.8.6 Overflow Flag (O)

The O flag is set to "1" when a result of an arithmetic operation overflows; otherwise "0".

2.1.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.

An interrupt is disabled when the I flag is set to "0" and is enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt is acknowledged.

2.1.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0". USP is selected when this flag is set to "1".

The U flag is set to "0" when a hardware interrupt is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.1.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide. It assigns an interrupt priority levels from level 0 to level 7.

If a requested interrupt has a greater priority than IPL, the interrupt is enabled.

2.1.8.10 Reserved Space

When writing to the reserved space, set to "0". When read, its content is indeterminate.

2.2 High-Speed Interrupt Registers

Registers associated with the high-speed interrupt are as follows.

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

2.3 DMAC-associated Registers

Registers associated with DMAC are as follows.

- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA SFR address register (DSA0, DSA1)
- DMA memory address reload register (DRA0, DRA1)

3. Memory

Figure 3.1 shows a memory map of the M32C/82 group.

The M32C/82 provides 16-Mbyte address space from addresses 000000₁₆ to FFFFFFF₁₆.

The internal ROM is allocated in lower addresses beginning with address FFFFFFF₁₆. For example, a 64-Kbyte internal ROM is allocated in addresses FF0000₁₆ to FFFFFFF₁₆.

The fixed interrupt vectors are allocated in addresses FFFFDC₁₆ to FFFFFFF₁₆. It stores the starting address of each interrupt routine.

The internal RAM is allocated in higher addresses beginning with address 000400₁₆. For example, a 10-Kbyte internal RAM is allocated in addresses 000400₁₆ to 002BFF₁₆. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

The SFR is allocated in addresses 000000₁₆ to 0003FF₁₆. The control registers for peripheral functions such as I/O port, A/D conversion, serial I/O, timer are allocated here. All addresses, which have nothing allocated within the SFR, are reserved space and cannot be accessed by users.

The special page vectors are allocated in addresses FFFE00₁₆ to FFFFDB₁₆. It is used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **Software Manual** for details.

In memory expansion mode and microprocessor mode, some space are reserved and cannot be accessed by users.

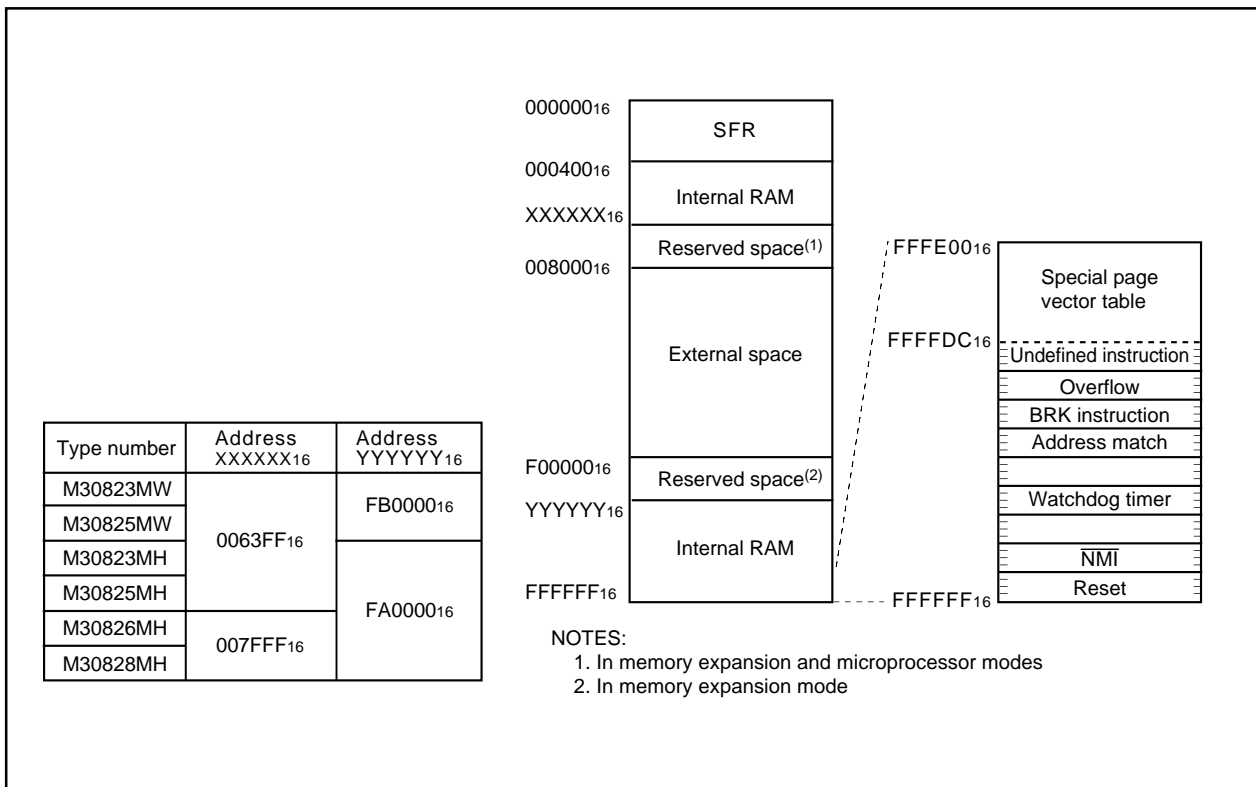


Figure 3.1 Memory Map

4. Special Function Registers (SFR)

Address	Register	Symbol	Value after RESET
0000 ₁₆			
0001 ₁₆			
0002 ₁₆			
0003 ₁₆			
0004 ₁₆	Processor mode register 0	PM0	1000 0000 ₂ (CNVss pin ="L") 0000 0011 ₂ (CNVss pin ="H")
0005 ₁₆	Processor mode register 1	PM1	0X00 0000 ₂
0006 ₁₆	System clock control register 0	CM0	0000 X000 ₂
0007 ₁₆	System clock control register 1	CM1	0010 0000 ₂
0008 ₁₆	Wait control register	WCR	1111 1111 ₂
0009 ₁₆	Address match interrupt enable register	AIER	XXXX 0000 ₂
000A ₁₆	Protect register	PRCR	XXXX 0000 ₂
000B ₁₆	External data bus width control register	DS	XXXX 1000 ₂ (BYTE pin ="L") XXXX 0000 ₂ (BYTE pin ="H")
000C ₁₆	Main clock division register	MCD	XXX0 1000 ₂
000D ₁₆	Oscillation stop detect register	CM2	00 ₁₆
000E ₁₆	Watchdog timer start register	WDTS	XX ₁₆
000F ₁₆	Watchdog timer control register	WDC	000X XXXX ₂
0010 ₁₆			
0011 ₁₆	Address match interrupt register 0	RMAD0	000000 ₁₆
0012 ₁₆			
0013 ₁₆			
0014 ₁₆			
0015 ₁₆	Address match interrupt register 1	RMAD1	000000 ₁₆
0016 ₁₆			
0017 ₁₆	VDC control register for PLL	PLV	XXXX XX01 ₂
0018 ₁₆			
0019 ₁₆	Address match interrupt register 2	RMAD2	000000 ₁₆
001A ₁₆			
001B ₁₆	VDC control register 0	VDC0	00 ₁₆
001C ₁₆			
001D ₁₆	Address match interrupt register 3	RMAD3	000000 ₁₆
001E ₁₆			
001F ₁₆			
0020 ₁₆			
0021 ₁₆			
0022 ₁₆			
0023 ₁₆			
0024 ₁₆			
0025 ₁₆			
0026 ₁₆			
0027 ₁₆			
0028 ₁₆			
0029 ₁₆			
002A ₁₆			
002B ₁₆			
002C ₁₆			
002D ₁₆			
002E ₁₆			
002F ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0030 ₁₆			
0031 ₁₆			
0032 ₁₆			
0033 ₁₆			
0034 ₁₆			
0035 ₁₆			
0036 ₁₆			
0037 ₁₆			
0038 ₁₆			
0039 ₁₆			
003A ₁₆			
003B ₁₆			
003C ₁₆			
003D ₁₆			
003E ₁₆			
003F ₁₆			
0040 ₁₆	DRAM control register	DRAMCONT	XX ₁₆
0041 ₁₆	DRAM refresh interval set register	REFCNT	XX ₁₆
0042 ₁₆			
0043 ₁₆			
0044 ₁₆			
0045 ₁₆			
0046 ₁₆			
0047 ₁₆			
0048 ₁₆			
0049 ₁₆			
004A ₁₆			
004B ₁₆			
004C ₁₆			
004D ₁₆			
004E ₁₆			
004F ₁₆			
0050 ₁₆			
0051 ₁₆			
0052 ₁₆			
0053 ₁₆			
0054 ₁₆			
0055 ₁₆			
0056 ₁₆			
0057 ₁₆			
0058 ₁₆			
0059 ₁₆			
005A ₁₆			
005B ₁₆			
005C ₁₆			
005D ₁₆			
005E ₁₆			
005F ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0060 ₁₆			
0061 ₁₆			
0062 ₁₆			
0063 ₁₆			
0064 ₁₆			
0065 ₁₆			
0066 ₁₆			
0067 ₁₆			
0068 ₁₆	DMA0 interrupt control register	DM0IC	XXXX X000 ₂
0069 ₁₆	Timer B5 interrupt control register	TB5IC	XXXX X000 ₂
006A ₁₆	DMA2 interrupt control register	DM2IC	XXXX X000 ₂
006B ₁₆	UART2 receive /ACK interrupt control register	S2RIC	XXXX X000 ₂
006C ₁₆	Timer A0 interrupt control register	TA0IC	XXXX X000 ₂
006D ₁₆	UART3 receive /ACK interrupt control register	S3RIC	XXXX X000 ₂
006E ₁₆	Timer A2 interrupt control register	TA2IC	XXXX X000 ₂
006F ₁₆	UART4 receive /ACK interrupt control register	S4RIC	XXXX X000 ₂
0070 ₁₆	Timer A4 interrupt control register	TA4IC	XXXX X000 ₂
0071 ₁₆	UART0/UART3 bus conflict detect interrupt control register	BCN0IC/BCN3IC	XXXX X000 ₂
0072 ₁₆	UART0 receive/ACK interrupt control register	S0RIC	XXXX X000 ₂
0073 ₁₆	A/D0 conversion interrupt control register	AD0IC	XXXX X000 ₂
0074 ₁₆	UART1 receive/ACK interrupt control register	S1RIC	XXXX X000 ₂
0075 ₁₆	Intelligent I/O interrupt control register 0	IIO0IC	XXXX X000 ₂
0076 ₁₆	Timer B1 interrupt control register	TB1IC	XXXX X000 ₂
0077 ₁₆	Intelligent I/O interrupt control register 2	IIO2IC	XXXX X000 ₂
0078 ₁₆	Timer B3 interrupt control register	TB3IC	XXXX X000 ₂
0079 ₁₆	Intelligent I/O interrupt control register 4	IIO4IC	XXXX X000 ₂
007A ₁₆	INT5 interrupt control register	INT5IC	XX00 X000 ₂
007B ₁₆	Intelligent I/O interrupt control register 6	IIO6IC	XXXX X000 ₂
007C ₁₆	INT3 interrupt control register	INT3IC	XX00 X000 ₂
007D ₁₆	Intelligent I/O interrupt control register 8	IIO8IC	XXXX X000 ₂
007E ₁₆	INT1 interrupt control register	INT1IC	XX00 X000 ₂
007F ₁₆	Intelligent I/O interrupt control register 10	IIO10IC	XXXX X000 ₂
0080 ₁₆			
0081 ₁₆	Intelligent I/O interrupt control register 11	IIO11IC	XXXX X000 ₂
0082 ₁₆			
0083 ₁₆			
0084 ₁₆			
0085 ₁₆			
0086 ₁₆			
0087 ₁₆			
0088 ₁₆	DMA1 interrupt control register	DM1IC	XXXX X000 ₂
0089 ₁₆	UART2 transmit /NACK interrupt control register	S2TIC	XXXX X000 ₂
008A ₁₆	DMA3 interrupt control register	DM3IC	XXXX X000 ₂
008B ₁₆	UART3 transmit /NACK interrupt control register	S3TIC	XXXX X000 ₂
008C ₁₆	Timer A1 interrupt control register	TA1IC	XXXX X000 ₂
008D ₁₆	UART4 transmit /NACK interrupt control register	S4TIC	XXXX X000 ₂
008E ₁₆	Timer A3 interrupt control register	TA3IC	XXXX X000 ₂
008F ₁₆	UART2 bus conflict detect interrupt control register	BCN2IC	XXXX X000 ₂

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0090 ₁₆	UART0 transmit /NACK interrupt control register	S0TIC	XXXX X000 ₂
0091 ₁₆	UART1/UART4 bus conflict detect interrupt control register	BCN11C/BCN41C	XXXX X000 ₂
0092 ₁₆	UART1 transmit/NACK interrupt control register	S1TIC	XXXX X000 ₂
0093 ₁₆	Key input interrupt control register	KUPIC	XXXX X000 ₂
0094 ₁₆	Timer B0 interrupt control register	TB01C	XXXX X000 ₂
0095 ₁₆	Intelligent I/O interrupt control register 1	IIO11C	XXXX X000 ₂
0096 ₁₆	Timer B2 interrupt control register	TB21C	XXXX X000 ₂
0097 ₁₆	Intelligent I/O interrupt control register 3	IIO31C	XXXX X000 ₂
0098 ₁₆	Timer B4 interrupt control register	TB41C	XXXX X000 ₂
0099 ₁₆	Intelligent I/O interrupt control register 5	IIO51C	XXXX X000 ₂
009A ₁₆	INT4 interrupt control register	INT41C	XX00 X000 ₂
009B ₁₆	Intelligent I/O interrupt control register 7	IIO71C	XXXX X000 ₂
009C ₁₆	INT2 interrupt control register	INT21C	XX00 X000 ₂
009D ₁₆	Intelligent I/O interrupt control register 9	IIO91C	XXXX X000 ₂
009E ₁₆	INT0 interrupt control register	INT01C	XX00 X000 ₂
009F ₁₆	Exit priority control register	RLVL	XXXX 0000 ₂
00A0 ₁₆	Interrupt request register 0	IIO01R	0000 000X ₂
00A1 ₁₆	Interrupt request register 1	IIO11R	0000 000X ₂
00A2 ₁₆	Interrupt request register 2	IIO21R	0000 000X ₂
00A3 ₁₆	Interrupt request register 3	IIO31R	0000 000X ₂
00A4 ₁₆	Interrupt request register 4	IIO41R	0000 000X ₂
00A5 ₁₆	Interrupt request register 5	IIO51R	0000 000X ₂
00A6 ₁₆	Interrupt request register 6	IIO61R	0000 000X ₂
00A7 ₁₆	Interrupt request register 7	IIO71R	0000 000X ₂
00A8 ₁₆	Interrupt request register 8	IIO81R	0000 000X ₂
00A9 ₁₆	Interrupt request register 9	IIO91R	0000 000X ₂
00AA ₁₆	Interrupt request register 10	IIO101R	0000 000X ₂
00AB ₁₆	Interrupt request register 11	IIO111R	0000 000X ₂
00AC ₁₆			
00AD ₁₆			
00AE ₁₆			
00AF ₁₆			
00B0 ₁₆	Interrupt enable register 0	IIO01E	00 ₁₆
00B1 ₁₆	Interrupt enable register 1	IIO11E	00 ₁₆
00B2 ₁₆	Interrupt enable register 2	IIO21E	00 ₁₆
00B3 ₁₆	Interrupt enable register 3	IIO31E	00 ₁₆
00B4 ₁₆	Interrupt enable register 4	IIO41E	00 ₁₆
00B5 ₁₆	Interrupt enable register 5	IIO51E	00 ₁₆
00B6 ₁₆	Interrupt enable register 6	IIO61E	00 ₁₆
00B7 ₁₆	Interrupt enable register 7	IIO71E	00 ₁₆
00B8 ₁₆	Interrupt enable register 8	IIO81E	00 ₁₆
00B9 ₁₆	Interrupt enable register 9	IIO91E	00 ₁₆
00BA ₁₆	Interrupt enable register 10	IIO101E	00 ₁₆
00BB ₁₆	Interrupt enable register 11	IIO111E	00 ₁₆
00BC ₁₆			
00BD ₁₆			
00BE ₁₆			
00BF ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00C0 ₁₆ 00C1 ₁₆	Group 0 time measurement/waveform generating register 0	G0TM0/G0PO0	XX ₁₆ XX ₁₆
00C2 ₁₆ 00C3 ₁₆	Group 0 time measurement/waveform generating register 1	G0TM1/G0PO1	XX ₁₆ XX ₁₆
00C4 ₁₆ 00C5 ₁₆	Group 0 time measurement/waveform generating register 2	G0TM2/G0PO2	XX ₁₆ XX ₁₆
00C6 ₁₆ 00C7 ₁₆	Group 0 time measurement/waveform generating register 3	G0TM3/G0PO3	XX ₁₆ XX ₁₆
00C8 ₁₆ 00C9 ₁₆	Group 0 time measurement/waveform generating register 4	G0TM4/G0PO4	XX ₁₆ XX ₁₆
00CA ₁₆ 00CB ₁₆	Group 0 time measurement/waveform generating register 5	G0TM5/G0PO5	XX ₁₆ XX ₁₆
00CC ₁₆ 00CD ₁₆	Group 0 time measurement/waveform generating register 6	G0TM6/G0PO6	XX ₁₆ XX ₁₆
00CE ₁₆ 00CF ₁₆	Group 0 time measurement/waveform generating register 7	G0TM7/G0PO7	XX ₁₆ XX ₁₆
00D0 ₁₆	Group 0 waveform generating control register 0	G0POCR0	0X00 X0002
00D1 ₁₆	Group 0 waveform generating control register 1	G0POCR1	0X00 X0002
00D2 ₁₆	Group 0 waveform generating control register 2	G0POCR2	0X00 X0002
00D3 ₁₆	Group 0 waveform generating control register 3	G0POCR3	0X00 X0002
00D4 ₁₆	Group 0 waveform generating control register 4	G0POCR4	0X00 X0002
00D5 ₁₆	Group 0 waveform generating control register 5	G0POCR5	0X00 X0002
00D6 ₁₆	Group 0 waveform generating control register 6	G0POCR6	0X00 X0002
00D7 ₁₆	Group 0 waveform generating control register 7	G0POCR7	0X00 X0002
00D8 ₁₆	Group 0 time measurement control register 0	G0TMCR0	00 ₁₆
00D9 ₁₆	Group 0 time measurement control register 1	G0TMCR1	00 ₁₆
00DA ₁₆	Group 0 time measurement control register 2	G0TMCR2	00 ₁₆
00DB ₁₆	Group 0 time measurement control register 3	G0TMCR3	00 ₁₆
00DC ₁₆	Group 0 time measurement control register 4	G0TMCR4	00 ₁₆
00DD ₁₆	Group 0 time measurement control register 5	G0TMCR5	00 ₁₆
00DE ₁₆	Group 0 time measurement control register 6	G0TMCR6	00 ₁₆
00DF ₁₆	Group 0 time measurement control register 7	G0TMCR7	00 ₁₆
00E0 ₁₆ 00E1 ₁₆	Group 0 base timer register	G0BT	XX ₁₆ XX ₁₆
00E2 ₁₆	Group 0 base timer control register 0	G0BCR0	00 ₁₆
00E3 ₁₆	Group 0 base timer control register 1	G0BCR1	00 ₁₆
00E4 ₁₆	Group 0 time measurement prescaler register 6	G0TPR6	00 ₁₆
00E5 ₁₆	Group 0 time measurement prescaler register 7	G0TPR7	00 ₁₆
00E6 ₁₆	Group 0 function enable register	G0FE	00 ₁₆
00E7 ₁₆	Group 0 function select register	G0FS	00 ₁₆
00E8 ₁₆ 00E9 ₁₆	Group 0 SI/O receive buffer register	G0RB	XXXX XXXX ₂ XX00 XXXX ₂
00EA ₁₆	Group 0 transmit buffer/receive data register	G0TB/G0DR	XX ₁₆
00EB ₁₆			
00EC ₁₆	Group 0 receive input register	G0RI	XX ₁₆
00ED ₁₆	Group 0 SI/O communication mode register	G0MR	00 ₁₆
00EE ₁₆	Group 0 transmit output register	G0TO	XX ₁₆
00EF ₁₆	Group 0 SI/O communication control register	G0CR	0000 X0002

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00F0 ₁₆	Group 0 data compare register 0	G0CMP0	XX ₁₆
00F1 ₁₆	Group 0 data compare register 1	G0CMP1	XX ₁₆
00F2 ₁₆	Group 0 data compare register 2	G0CMP2	XX ₁₆
00F3 ₁₆	Group 0 data compare register 3	G0CMP3	XX ₁₆
00F4 ₁₆	Group 0 data mask register 0	G0MSK0	XX ₁₆
00F5 ₁₆	Group 0 data mask register 1	G0MSK1	XX ₁₆
00F6 ₁₆			
00F7 ₁₆			
00F8 ₁₆ 00F9 ₁₆	Group 0 receive CRC code register	G0RCRC	XX ₁₆ XX ₁₆
00FA ₁₆ 00FB ₁₆	Group 0 transmit CRC code register	G0TCRC	00 ₁₆ 00 ₁₆
00FC ₁₆	Group 0 SI/O extended mode register	G0EMR	00 ₁₆
00FD ₁₆	Group 0 SI/O extended receive control register	G0ERC	00 ₁₆
00FE ₁₆	Group 0 SI/O special communication interrupt detect register	G0IRF	0000 00XX ₂
00FF ₁₆	Group 0 SI/O extended transmit control register	G0ETC	0000 0XXX ₂
0100 ₁₆ 0101 ₁₆	Group 1 time measurement/waveform generating register 0	G1TM0/G1PO0	XX ₁₆ XX ₁₆
0102 ₁₆ 0103 ₁₆	Group 1 time measurement/waveform generating register 1	G1TM1/G1PO1	XX ₁₆ XX ₁₆
0104 ₁₆ 0105 ₁₆	Group 1 time measurement/waveform generating register 2	G1TM2/G1PO2	XX ₁₆ XX ₁₆
0106 ₁₆ 0107 ₁₆	Group 1 time measurement/waveform generating register 3	G1TM3/G1PO3	XX ₁₆ XX ₁₆
0108 ₁₆ 0109 ₁₆	Group 1 time measurement/waveform generating register 4	G1TM4/G1PO4	XX ₁₆ XX ₁₆
010A ₁₆ 010B ₁₆	Group 1 time measurement/waveform generating register 5	G1TM5/G1PO5	XX ₁₆ XX ₁₆
010C ₁₆ 010D ₁₆	Group 1 time measurement/waveform generating register 6	G1TM6/G1PO6	XX ₁₆ XX ₁₆
010E ₁₆ 010F ₁₆	Group 1 time measurement/waveform generating register 7	G1TM7/G1PO7	XX ₁₆ XX ₁₆
0110 ₁₆	Group 1 waveform generating control register 0	G1POCR0	0X00 X000 ₂
0111 ₁₆	Group 1 waveform generating control register 1	G1POCR1	0X00 X000 ₂
0112 ₁₆	Group 1 waveform generating control register 2	G1POCR2	0X00 X000 ₂
0113 ₁₆	Group 1 waveform generating control register 3	G1POCR3	0X00 X000 ₂
0114 ₁₆	Group 1 waveform generating control register 4	G1POCR4	0X00 X000 ₂
0115 ₁₆	Group 1 waveform generating control register 5	G1POCR5	0X00 X000 ₂
0116 ₁₆	Group 1 waveform generating control register 6	G1POCR6	0X00 X000 ₂
0117 ₁₆	Group 1 waveform generating control register 7	G1POCR7	0X00 X000 ₂
0118 ₁₆	Group 1 time measurement control register 0	G1TMCR0	00 ₁₆
0119 ₁₆	Group 1 time measurement control register 1	G1TMCR1	00 ₁₆
011A ₁₆	Group 1 time measurement control register 2	G1TMCR2	00 ₁₆
011B ₁₆	Group 1 time measurement control register 3	G1TMCR3	00 ₁₆
011C ₁₆	Group 1 time measurement control register 4	G1TMCR4	00 ₁₆
011D ₁₆	Group 1 time measurement control register 5	G1TMCR5	00 ₁₆
011E ₁₆	Group 1 time measurement control register 6	G1TMCR6	00 ₁₆
011F ₁₆	Group 1 time measurement control register 7	G1TMCR7	00 ₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0120 ₁₆ 0121 ₁₆	Group 1 base timer register	G1BT	XX ₁₆ XX ₁₆
0122 ₁₆	Group 1 base timer control register 0	G1BCR0	00 ₁₆
0123 ₁₆	Group 1 base timer control register 1	G1BCR1	00 ₁₆
0124 ₁₆	Group 1 time measurement prescaler register 6	G1TPR6	00 ₁₆
0125 ₁₆	Group 1 time measurement prescaler register 7	G1TPR7	00 ₁₆
0126 ₁₆	Group 1 function enable register	G1FE	00 ₁₆
0127 ₁₆	Group 1 function select register	G1FS	00 ₁₆
0128 ₁₆ 0129 ₁₆	Group 1 SI/O receive buffer register	G1RB	XXXX XXXX ₂ XX00 XXXX ₂
012A ₁₆ 012B ₁₆	Group 1 transmit buffer/receive data register	G1TB/G1DR	XX ₁₆
012C ₁₆	Group 1 receive input register	G1RI	XX ₁₆
012D ₁₆	Group 1 SI/O communication mode register	G1MR	00 ₁₆
012E ₁₆	Group 1 transmit output register	G1TO	XX ₁₆
012F ₁₆	Group 1 SI/O communication control register	G1CR	0000 X000 ₂
0130 ₁₆	Group 1 data compare register 0	G1CMP0	XX ₁₆
0131 ₁₆	Group 1 data compare register 1	G1CMP1	XX ₁₆
0132 ₁₆	Group 1 data compare register 2	G1CMP2	XX ₁₆
0133 ₁₆	Group 1 data compare register 3	G1CMP3	XX ₁₆
0134 ₁₆	Group 1 data mask register 0	G1MSK0	XX ₁₆
0135 ₁₆	Group 1 data mask register 1	G1MSK1	XX ₁₆
0136 ₁₆			
0137 ₁₆			
0138 ₁₆ 0139 ₁₆	Group 1 receive CRC code register	G1RCRC	XX ₁₆ XX ₁₆
013A ₁₆ 013B ₁₆	Group 1 transmit CRC code register	G1TCRC	00 ₁₆ 00 ₁₆
013C ₁₆	Group 1 SI/O extended mode register	G1EMR	00 ₁₆
013D ₁₆	Group 1 SI/O extended receive control register	G1ERC	00 ₁₆
013E ₁₆	Group 1 SI/O special communication interrupt detect register	G1IRF	0000 00XX ₂
013F ₁₆	Group 1 SI/O extended transmit control register	G1ETC	0000 0XXX ₂
0140 ₁₆ 0141 ₁₆	Group 2 waveform generating register 0	G2PO0	XX ₁₆ XX ₁₆
0142 ₁₆ 0143 ₁₆	Group 2 waveform generating register 1	G2PO1	XX ₁₆ XX ₁₆
0144 ₁₆ 0145 ₁₆	Group 2 waveform generating register 2	G2PO2	XX ₁₆ XX ₁₆
0146 ₁₆ 0147 ₁₆	Group 2 waveform generating register 3	G2PO3	XX ₁₆ XX ₁₆
0148 ₁₆ 0149 ₁₆	Group 2 waveform generating register 4	G2PO4	XX ₁₆ XX ₁₆
014A ₁₆ 014B ₁₆	Group 2 waveform generating register 5	G2PO5	XX ₁₆ XX ₁₆
014C ₁₆ 014D ₁₆	Group 2 waveform generating register 6	G2PO6	XX ₁₆ XX ₁₆
014E ₁₆ 014F ₁₆	Group 2 waveform generating register 7	G2PO7	XX ₁₆ XX ₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0150 ₁₆	Group 2 waveform generating control register 0	G2POCR0	00 ₁₆
0151 ₁₆	Group 2 waveform generating control register 1	G2POCR1	00 ₁₆
0152 ₁₆	Group 2 waveform generating control register 2	G2POCR2	00 ₁₆
0153 ₁₆	Group 2 waveform generating control register 3	G2POCR3	00 ₁₆
0154 ₁₆	Group 2 waveform generating control register 4	G2POCR4	00 ₁₆
0155 ₁₆	Group 2 waveform generating control register 5	G2POCR5	00 ₁₆
0156 ₁₆	Group 2 waveform generating control register 6	G2POCR6	00 ₁₆
0157 ₁₆	Group 2 waveform generating control register 7	G2POCR7	00 ₁₆
0158 ₁₆			
0159 ₁₆			
015A ₁₆			
015B ₁₆			
015C ₁₆			
015D ₁₆			
015E ₁₆			
015F ₁₆			
0160 ₁₆ 0161 ₁₆	Group 2 base timer register	G2BT	XX ₁₆ XX ₁₆
0162 ₁₆	Group 2 base timer control register 0	G2BCR0	00 ₁₆
0163 ₁₆	Group 2 base timer control register 1	G2BCR1	00 ₁₆
0164 ₁₆	Base timer start register	BTSR	XXXX 0000 ₂
0165 ₁₆			
0166 ₁₆	Group 2 function enable register	G2FE	00 ₁₆
0167 ₁₆	Group 2 RTP output buffer register	G2RTP	00 ₁₆
0168 ₁₆			
0169 ₁₆			
016A ₁₆	Group 2 SI/O communication mode register	G2MR	00XX X000 ₂
016B ₁₆	Group 2 SI/O communication control register	G2CR	0000 X000 ₂
016C ₁₆ 016D ₁₆	Group 2 SI/O transmit buffer register	G2TB	XX ₁₆ XX ₁₆
016E ₁₆ 016F ₁₆	Group 2 SI/O receive buffer register	G2RB	XX ₁₆ XX ₁₆
0170 ₁₆ 0171 ₁₆	Group 2 IEBus address register	IEAR	XX ₁₆ XX ₁₆
0172 ₁₆	Group 2 IEBus control register	IECR	00XX X000 ₂
0173 ₁₆	Group 2 IEBus transmit interrupt cause detect register	IETIF	XXX0 0000 ₂
0174 ₁₆	Group 2 IEBus receive interrupt cause detect register	IERIF	XXX0 0000 ₂
0175 ₁₆			
0176 ₁₆			
0177 ₁₆			
0178 ₁₆	Input function select register	IPS	00 ₁₆
0179 ₁₆			
017A ₁₆ to 01D3 ₁₆			
01D4 ₁₆	A/D1 control register 2	AD1CON2	X00X X000 ₂
01D5 ₁₆			
01D6 ₁₆	A/D1 control register 0	AD1CON0	00 ₁₆
01D7 ₁₆	A/D1 control register 1	AD1CON1	XX00 0000 ₂
01D8 ₁₆ to 02BF ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
02C0 ₁₆ 02C1 ₁₆	X0 register Y0 register	X0R,Y0R	XX ₁₆ XX ₁₆
02C2 ₁₆ 02C3 ₁₆	X1 register Y1 register	X1R,Y1R	XX ₁₆ XX ₁₆
02C4 ₁₆ 02C5 ₁₆	X2 register Y2 register	X2R,Y2R	XX ₁₆ XX ₁₆
02C6 ₁₆ 02C7 ₁₆	X3 register Y3 register	X3R,Y3R	XX ₁₆ XX ₁₆
02C8 ₁₆ 02C9 ₁₆	X4 register Y4 register	X4R,Y4R	XX ₁₆ XX ₁₆
02CA ₁₆ 02CB ₁₆	X5 register Y5 register	X5R,Y5R	XX ₁₆ XX ₁₆
02CC ₁₆ 02CD ₁₆	X6 register Y6 register	X6R,Y6R	XX ₁₆ XX ₁₆
02CE ₁₆ 02CF ₁₆	X7 register Y7 register	X7R,Y7R	XX ₁₆ XX ₁₆
02D0 ₁₆ 02D1 ₁₆	X8 register Y8 register	X8R,Y8R	XX ₁₆ XX ₁₆
02D2 ₁₆ 02D3 ₁₆	X9 register Y9 register	X9R,Y9R	XX ₁₆ XX ₁₆
02D4 ₁₆ 02D5 ₁₆	X10 register Y10 register	X10R,Y10R	XX ₁₆ XX ₁₆
02D6 ₁₆ 02D7 ₁₆	X11 register Y11 register	X11R,Y11R	XX ₁₆ XX ₁₆
02D8 ₁₆ 02D9 ₁₆	X12 register Y12 register	X12R,Y12R	XX ₁₆ XX ₁₆
02DA ₁₆ 02DB ₁₆	X13 register Y13 register	X13R,Y13R	XX ₁₆ XX ₁₆
02DC ₁₆ 02DD ₁₆	X14 register Y14 register	X14R,Y14R	XX ₁₆ XX ₁₆
02DE ₁₆ 02DF ₁₆	X15 register Y15 register	X15R,Y15R	XX ₁₆ XX ₁₆
02E0 ₁₆	XY control register	XYC	XXXX XX00 ₂
02E1 ₁₆			
02E2 ₁₆			
02E3 ₁₆			
02E4 ₁₆	UART1 special mode register 4	U1SMR4	00 ₁₆
02E5 ₁₆	UART1 special mode register 3	U1SMR3	00 ₁₆
02E6 ₁₆	UART1 special mode register 2	U1SMR2	00 ₁₆
02E7 ₁₆	UART1 special mode register	U1SMR	00 ₁₆
02E8 ₁₆	UART1 transmit/receive mode register	U1MR	00 ₁₆
02E9 ₁₆	UART1 baud rate register	U1BRG	XX ₁₆
02EA ₁₆ 02EB ₁₆	UART1 transmit buffer register	U1TB	XX ₁₆ XX ₁₆
02EC ₁₆	UART1 transmit/receive control register 0	U1C0	0000 1000 ₂
02ED ₁₆	UART1 transmit/receive control register 1	U1C1	0000 0010 ₂
02EE ₁₆ 02EF ₁₆	UART1 receive buffer register	U1RB	XX ₁₆ XX ₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
02F0 ₁₆			
02F1 ₁₆			
02F2 ₁₆			
02F3 ₁₆			
02F4 ₁₆	UART4 special mode register 4	U4SMR4	00 ₁₆
02F5 ₁₆	UART4 special mode register 3	U4SMR3	00 ₁₆
02F6 ₁₆	UART4 special mode register 2	U4SMR2	00 ₁₆
02F7 ₁₆	UART4 special mode register	U4SMR	00 ₁₆
02F8 ₁₆	UART4 transmit/receive mode register	U4MR	00 ₁₆
02F9 ₁₆	UART4 baud rate register	U4BRG	XX ₁₆
02FA ₁₆	UART4 transmit buffer register	U4TB	XX ₁₆
02FB ₁₆			XX ₁₆
02FC ₁₆	UART4 transmit/receive control register 0	U4C0	0000 1000 ₂
02FD ₁₆	UART4 transmit/receive control register 1	U4C1	0000 0010 ₂
02FE ₁₆	UART4 receive buffer register	U4RB	XX ₁₆
02FF ₁₆			XX ₁₆
0300 ₁₆	Timer B3,B4,B5 count start flag	TBSR	000X XXXX ₂
0301 ₁₆			
0302 ₁₆	Timer A1-1 register	TA11	XX ₁₆
0303 ₁₆			XX ₁₆
0304 ₁₆	Timer A2-1 register	TA21	XX ₁₆
0305 ₁₆			XX ₁₆
0306 ₁₆	Timer A4-1 register	TA41	XX ₁₆
0307 ₁₆			XX ₁₆
0308 ₁₆	Three-phase PWM control register 0	INVC0	00 ₁₆
0309 ₁₆	Three-phase PWM control register 1	INVC1	00 ₁₆
030A ₁₆	Three-phase output buffer register 0	IDB0	XX ₁₁ 1111 ₂
030B ₁₆	Three-phase output buffer register 1	IDB1	XX ₁₁ 1111 ₂
030C ₁₆	Dead time timer	DTT	XX ₁₆
030D ₁₆	Timer B2 interrupt generating frequency set counter	ICTB2	XX ₁₆
030E ₁₆			
030F ₁₆			
0310 ₁₆	Timer B3 register	TB3	XX ₁₆
0311 ₁₆			XX ₁₆
0312 ₁₆	Timer B4 register	TB4	XX ₁₆
0313 ₁₆			XX ₁₆
0314 ₁₆	Timer B5 register	TB5	XX ₁₆
0315 ₁₆			XX ₁₆
0316 ₁₆			
0317 ₁₆			
0318 ₁₆			
0319 ₁₆			
031A ₁₆			
031B ₁₆	Timer B3 mode register	TB3MR	00XX 0000 ₂
031C ₁₆	Timer B4 mode register	TB4MR	00XX 0000 ₂
031D ₁₆	Timer B5 mode register	TB5MR	00XX 0000 ₂
031E ₁₆			
031F ₁₆	External interrupt cause select register	IFSR	00 ₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0320 ₁₆			
0321 ₁₆			
0322 ₁₆			
0323 ₁₆			
0324 ₁₆	UART3 special mode register 4	U3SMR4	00 ₁₆
0325 ₁₆	UART3 special mode register 3	U3SMR3	00 ₁₆
0326 ₁₆	UART3 special mode register 2	U3SMR2	00 ₁₆
0327 ₁₆	UART3 special mode register	U3SMR	00 ₁₆
0328 ₁₆	UART3 transmit/receive mode register	U3MR	00 ₁₆
0329 ₁₆	UART3 baud rate register	U3BRG	XX ₁₆
032A ₁₆	UART3 transmit buffer register	U3TB	XX ₁₆
032B ₁₆			XX ₁₆
032C ₁₆	UART3 transmit/receive control register 0	U3C0	0000 1000 ₂
032D ₁₆	UART3 transmit/receive control register 1	U3C1	0000 0010 ₂
032E ₁₆	UART3 receive buffer register	U3RB	XX ₁₆
032F ₁₆			XX ₁₆
0330 ₁₆			
0331 ₁₆			
0332 ₁₆			
0333 ₁₆			
0334 ₁₆	UART2 special mode register 4	U2SMR4	00 ₁₆
0335 ₁₆	UART2 special mode register 3	U2SMR3	00 ₁₆
0336 ₁₆	UART2 special mode register 2	U2SMR2	00 ₁₆
0337 ₁₆	UART2 special mode register	U2SMR	00 ₁₆
0338 ₁₆	UART2 transmit/receive mode register	U2MR	00 ₁₆
0339 ₁₆	UART2 baud rate register	U2BRG	XX ₁₆
033A ₁₆	UART2 transmit buffer register	U2TB	XX ₁₆
033B ₁₆			XX ₁₆
033C ₁₆	UART2 transmit/receive control register 0	U2C0	0000 1000 ₂
033D ₁₆	UART2 transmit/receive control register 1	U2C1	0000 0010 ₂
033E ₁₆	UART2 receive buffer register	U2RB	XX ₁₆
033F ₁₆			XX ₁₆
0340 ₁₆	Count start flag	TABSR	00 ₁₆
0341 ₁₆	Clock prescaler reset flag	CPSRF	0XXX XXXX ₂
0342 ₁₆	One-shot start flag	ONSF	00 ₁₆
0343 ₁₆	Trigger select register	TRGSR	00 ₁₆
0344 ₁₆	Up-down flag	UDF	00 ₁₆
0345 ₁₆			
0346 ₁₆	Timer A0 register	TA0	XX ₁₆
0347 ₁₆			XX ₁₆
0348 ₁₆	Timer A1 register	TA1	XX ₁₆
0349 ₁₆			XX ₁₆
034A ₁₆	Timer A2 register	TA2	XX ₁₆
034B ₁₆			XX ₁₆
034C ₁₆	Timer A3 register	TA3	XX ₁₆
034D ₁₆			XX ₁₆
034E ₁₆	Timer A4 register	TA4	XX ₁₆
034F ₁₆			XX ₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0350 ₁₆ 0351 ₁₆	Timer B0 register	TB0	XX ₁₆ XX ₁₆
0352 ₁₆ 0353 ₁₆	Timer B1 register	TB1	XX ₁₆ XX ₁₆
0354 ₁₆ 0355 ₁₆	Timer B2 register	TB2	XX ₁₆ XX ₁₆
0356 ₁₆	Timer A0 mode register	TA0MR	0000 0X00 ₂
0357 ₁₆	Timer A1 mode register	TA1MR	0000 0X00 ₂
0358 ₁₆	Timer A2 mode register	TA2MR	0000 0X00 ₂
0359 ₁₆	Timer A3 mode register	TA3MR	0000 0X00 ₂
035A ₁₆	Timer A4 mode register	TA4MR	0000 0X00 ₂
035B ₁₆	Timer B0 mode register	TB0MR	00XX 0000 ₂
035C ₁₆	Timer B1 mode register	TB1MR	00XX 0000 ₂
035D ₁₆	Timer B2 mode register	TB2MR	00XX 0000 ₂
035E ₁₆	Timer B2 special mode register	TB2SC	XXXX XXX0 ₂
035F ₁₆	Count source prescaler register	TCSPR	0XXX 0000 ₂
0360 ₁₆			
0361 ₁₆			
0362 ₁₆			
0363 ₁₆			
0364 ₁₆	UART0 special mode register 4	U0SMR4	00 ₁₆
0365 ₁₆	UART0 special mode register 3	U0SMR3	00 ₁₆
0366 ₁₆	UART0 special mode register 2	U0SMR2	00 ₁₆
0367 ₁₆	UART0 special mode register	U0SMR	00 ₁₆
0368 ₁₆	UART0 transmit/receive mode register	U0MR	00 ₁₆
0369 ₁₆	UART0 baud rate register	U0BRG	XX ₁₆
036A ₁₆ 036B ₁₆	UART0 transmit buffer register	U0TB	XX ₁₆ XX ₁₆
036C ₁₆	UART0 transmit/receive control register 0	U0C0	0000 1000 ₂
036D ₁₆	UART0 transmit/receive control register 1	U0C1	0000 0010 ₂
036E ₁₆ 036F ₁₆	UART0 receive buffer register	U0RB	XX ₁₆ XX ₁₆
0370 ₁₆			
0371 ₁₆			
0372 ₁₆			
0373 ₁₆			
0374 ₁₆			
0375 ₁₆			
0376 ₁₆	PLL control register 0	PLC0	0011 X100 ₂
0377 ₁₆	PLL control register 1	PLC1	XXXX 0000 ₂
0378 ₁₆	DMA0 cause select register	DM0SL	0X00 0000 ₂
0379 ₁₆	DMA1 cause select register	DM1SL	0X00 0000 ₂
037A ₁₆	DMA2 cause select register	DM2SL	0X00 0000 ₂
037B ₁₆	DMA3 cause select register	DM3SL	0X00 0000 ₂
037C ₁₆ 037D ₁₆	CRC data register	CRCD	XX ₁₆ XX ₁₆
037E ₁₆ 037F ₁₆	CRC input register	CRCIN	XX ₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0380 ₁₆ 0381 ₁₆	A/D0 register 0	AD00	XX ₁₆ XX ₁₆
0382 ₁₆ 0383 ₁₆	A/D0 register 1	AD01	XX ₁₆ XX ₁₆
0384 ₁₆ 0385 ₁₆	A/D0 register 2	AD02	XX ₁₆ XX ₁₆
0386 ₁₆ 0387 ₁₆	A/D0 register 3	AD03	XX ₁₆ XX ₁₆
0388 ₁₆ 0389 ₁₆	A/D0 register 4	AD04	XX ₁₆ XX ₁₆
038A ₁₆ 038B ₁₆	A/D0 register 5	AD05	XX ₁₆ XX ₁₆
038C ₁₆ 038D ₁₆	A/D0 register 6	AD06	XX ₁₆ XX ₁₆
038E ₁₆ 038F ₁₆	A/D0 register 7	AD07	XX ₁₆ XX ₁₆
0390 ₁₆			
0391 ₁₆			
0392 ₁₆			
0393 ₁₆			
0394 ₁₆ 0395 ₁₆	A/D0 control register 2	AD0CON2	X000 0000 ₂
0396 ₁₆	A/D0 control register 0	AD0CON0	00 ₁₆
0397 ₁₆	A/D0 control register 1	AD0CON1	00 ₁₆
0398 ₁₆ 0399 ₁₆	D/A register 0	DA0	XX ₁₆
039A ₁₆ 039B ₁₆	D/A register 1	DA1	XX ₁₆
039C ₁₆ 039D ₁₆	D/A control register	DACON	XXXX XX00 ₂
039E ₁₆			
039F ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<144-pin package>

Address	Register	Symbol	Value after RESET
03A0 ₁₆	Function select register A8	PS8	X000 0000 ₂
03A1 ₁₆	Function select register A9	PS9	00 ₁₆
03A2 ₁₆			
03A3 ₁₆			
03A4 ₁₆			
03A5 ₁₆			
03A6 ₁₆			
03A7 ₁₆			
03A8 ₁₆			
03A9 ₁₆			
03AA ₁₆			
03AB ₁₆			
03AC ₁₆			
03AD ₁₆			
03AE ₁₆			
03AF ₁₆	Function select register C	PSC	00X0 0000 ₂
03B0 ₁₆	Function select register A0	PS0	00 ₁₆
03B1 ₁₆	Function select register A1	PS1	00 ₁₆
03B2 ₁₆	Function select register B0	PSL0	00 ₁₆
03B3 ₁₆	Function select register B1	PSL1	00 ₁₆
03B4 ₁₆	Function select register A2	PS2	00X0 0000 ₂
03B5 ₁₆	Function select register A3	PS3	00 ₁₆
03B6 ₁₆	Function select register B2	PSL2	00X0 0000 ₂
03B7 ₁₆	Function select register B3	PSL3	00 ₁₆
03B8 ₁₆			
03B9 ₁₆	Function select register A5	PS5	XXX0 0000 ₂
03BA ₁₆			
03BB ₁₆			
03BC ₁₆			
03BD ₁₆	Function select register A7	PS7	00 ₁₆
03BE ₁₆			
03BF ₁₆			
03C0 ₁₆	Port P6 register	P6	XX ₁₆
03C1 ₁₆	Port P7 register	P7	XX ₁₆
03C2 ₁₆	Port P6 direction register	PD6	00 ₁₆
03C3 ₁₆	Port P7 direction register	PD7	00 ₁₆
03C4 ₁₆	Port P8 register	P8	XX ₁₆
03C5 ₁₆	Port P9 register	P9	XX ₁₆
03C6 ₁₆	Port P8 direction register	PD8	00X0 0000 ₂
03C7 ₁₆	Port P9 direction register	PD9	00 ₁₆
03C8 ₁₆	Port P10 register	P10	XX ₁₆
03C9 ₁₆	Port P11 register	P11	XX ₁₆
03CA ₁₆	Port P10 direction register	PD10	00 ₁₆
03CB ₁₆	Port P11 direction register	PD11	XXX0 0000 ₂
03CC ₁₆	Port P12 register	P12	XX ₁₆
03CD ₁₆	Port P13 register	P13	XX ₁₆
03CE ₁₆	Port P12 direction register	PD12	00 ₁₆
03CF ₁₆	Port P13 direction register	PD13	00 ₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

<144-pin package>

Address	Register	Symbol	Value after RESET
03D0 ₁₆	Port P14 register	P14	XX ₁₆
03D1 ₁₆	Port P15 register	P15	XX ₁₆
03D2 ₁₆	Port P14 direction register	PD14	X000 0000 ₂
03D3 ₁₆	Port P15 direction register	PD15	00 ₁₆
03D4 ₁₆			
03D5 ₁₆			
03D6 ₁₆			
03D7 ₁₆			
03D8 ₁₆			
03D9 ₁₆			
03DA ₁₆	Pull-up control register 2	PUR2	00 ₁₆
03DB ₁₆	Pull-up control register 3	PUR3	00 ₁₆
03DC ₁₆	Pull-up control register 4	PUR4	XXXX 0000 ₂
03DD ₁₆			
03DE ₁₆			
03DF ₁₆			
03E0 ₁₆	Port P0 register	P0	XX ₁₆
03E1 ₁₆	Port P1 register	P1	XX ₁₆
03E2 ₁₆	Port P0 direction register	PD0	00 ₁₆
03E3 ₁₆	Port P1 direction register	PD1	00 ₁₆
03E4 ₁₆	Port P2 register	P2	XX ₁₆
03E5 ₁₆	Port P3 register	P3	XX ₁₆
03E6 ₁₆	Port P2 direction register	PD2	00 ₁₆
03E7 ₁₆	Port P3 direction register	PD3	00 ₁₆
03E8 ₁₆	Port P4 register	P4	XX ₁₆
03E9 ₁₆	Port P5 register	P5	XX ₁₆
03EA ₁₆	Port P4 direction register	PD4	00 ₁₆
03EB ₁₆	Port P5 direction register	PD5	00 ₁₆
03EC ₁₆			
03ED ₁₆			
03EE ₁₆			
03EF ₁₆			
03F0 ₁₆	Pull-up control register 0	PUR0	00 ₁₆
03F1 ₁₆	Pull-up control register 1	PUR1	XXXX 0000 ₂
03F2 ₁₆			
03F3 ₁₆			
03F4 ₁₆			
03F5 ₁₆			
03F6 ₁₆			
03F7 ₁₆			
03F8 ₁₆			
03F9 ₁₆			
03FA ₁₆			
03FB ₁₆			
03FC ₁₆			
03FD ₁₆			
03FE ₁₆			
03FF ₁₆	Port control register	PCR	XXXX XXX0 ₂

X: Indeterminate

Blank spaces are reserved. No access is allowed.



<100-pin package>

Address	Register	Symbol	Value after RESET	
03A0 ₁₆				(Note 2)
03A1 ₁₆				
03A2 ₁₆				
03A3 ₁₆				
03A4 ₁₆				
03A5 ₁₆				
03A6 ₁₆				
03A7 ₁₆				
03A8 ₁₆				
03A9 ₁₆				
03AA ₁₆				
03AB ₁₆				
03AC ₁₆				
03AD ₁₆				
03AE ₁₆				
03AF ₁₆	Function select register C	PSC	0X00 0000 ₂	
03B0 ₁₆	Function select register A0	PS0	00 ₁₆	
03B1 ₁₆	Function select register A1	PS1	00 ₁₆	
03B2 ₁₆	Function select register B0	PSL0	00 ₁₆	
03B3 ₁₆	Function select register B1	PSL1	00 ₁₆	
03B4 ₁₆	Function select register A2	PS2	00X0 0000 ₂	
03B5 ₁₆	Function select register A3	PS3	00 ₁₆	
03B6 ₁₆	Function select register B2	PSL2	00X0 0000 ₂	
03B7 ₁₆	Function select register B3	PSL3	00 ₁₆	
03B8 ₁₆				
03B9 ₁₆				(Note 2)
03BA ₁₆				
03BB ₁₆				
03BC ₁₆				(Note 2)
03BD ₁₆				
03BE ₁₆				
03BF ₁₆				
03C0 ₁₆	Port P6 register	P6	XX ₁₆	
03C1 ₁₆	Port P7 register	P7	XX ₁₆	
03C2 ₁₆	Port P6 direction register	PD6	00 ₁₆	
03C3 ₁₆	Port P7 direction register	PD7	00 ₁₆	
03C4 ₁₆	Port P8 register	P8	XX ₁₆	
03C5 ₁₆	Port P9 register	P9	XX ₁₆	
03C6 ₁₆	Port P8 direction register	PD8	00X0 0000 ₂	
03C7 ₁₆	Port P9 direction register	PD9	00 ₁₆	
03C8 ₁₆	Port P10 register	P10	XX ₁₆	
03C9 ₁₆				(Note 2)
03CA ₁₆	Port P10 direction register	PD10	00 ₁₆	
03CB ₁₆				(Note 1)
03CC ₁₆				(Note 2)
03CD ₁₆				
03CE ₁₆				(Note 1)
03CF ₁₆				

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1.  Set address spaces 03CB₁₆, 03CE₁₆ and 03CF₁₆ to "FF₁₆" in the 100-pin package.
2.  Address spaces 03A0₁₆, 03A1₁₆, 03B9₁₆, 03BC₁₆, 03BD₁₆, 03C9₁₆, 03CC₁₆ and 03CD₁₆ are not provided in the 100-pin package.




<100-pin package>

Address	Register	Symbol	Value after RESET	
03D0 ₁₆				(Note 3)
03D1 ₁₆				
03D2 ₁₆				(Note 1)
03D3 ₁₆				
03D4 ₁₆				
03D5 ₁₆				
03D6 ₁₆				
03D7 ₁₆				
03D8 ₁₆				
03D9 ₁₆				
03DA ₁₆	Pull-up control register 2	PUR2	00 ₁₆	
03DB ₁₆	Pull-up control register 3	PUR3	00 ₁₆	
03DC ₁₆				(Note 2)
03DD ₁₆				
03DE ₁₆				
03DF ₁₆				
03E0 ₁₆	Port P0 register	P0	XX ₁₆	
03E1 ₁₆	Port P1 register	P1	XX ₁₆	
03E2 ₁₆	Port P0 direction register	PD0	00 ₁₆	
03E3 ₁₆	Port P1 direction register	PD1	00 ₁₆	
03E4 ₁₆	Port P2 register	P2	XX ₁₆	
03E5 ₁₆	Port P3 register	P3	XX ₁₆	
03E6 ₁₆	Port P2 direction register	PD2	00 ₁₆	
03E7 ₁₆	Port P3 direction register	PD3	00 ₁₆	
03E8 ₁₆	Port P4 register	P4	XX ₁₆	
03E9 ₁₆	Port P5 register	P5	XX ₁₆	
03EA ₁₆	Port P4 direction register	PD4	00 ₁₆	
03EB ₁₆	Port P5 direction register	PD5	00 ₁₆	
03EC ₁₆				
03ED ₁₆				
03EE ₁₆				
03EF ₁₆				
03F0 ₁₆	Pull-up control register 0	PUR0	00 ₁₆	
03F1 ₁₆	Pull-up control register 1	PUR1	XXXX 0000 ₂	
03F2 ₁₆				
03F3 ₁₆				
03F4 ₁₆				
03F5 ₁₆				
03F6 ₁₆				
03F7 ₁₆				
03F8 ₁₆				
03F9 ₁₆				
03FA ₁₆				
03FB ₁₆				
03FC ₁₆				
03FD ₁₆				
03FE ₁₆				
03FF ₁₆	Port control register	PCR	XXXX XXX0 ₂	

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTES:

1.  Set address spaces 03D2₁₆ and 03D3₁₆ to "FF₁₆" in the 100-pin package.
2.  Set address spaces 03DC₁₆ to "00₁₆" in the 100-pin package.
3.  Address spaces 03D0₁₆ and 03D1₁₆ are not provided in the 100-pin package.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Value	Unit
V _{cc}	Supply voltage	V _{cc} =AV _{cc}	-0.3 to 6.0	V
AV _{cc}	Analog supply voltage	V _{cc} =AV _{cc}	-0.3 to 6.0	V
V _i	Input voltage	RESET, CNV _{ss} , BYTE, P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₂ -P7 ₇ , P8 ₀ -P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾ , V _{REF} , X _{IN}	-0.3 to V _{cc} +0.3	V
		P7 ₀ , P7 ₁	-0.3 to 6.0	
V _o	Output voltage	P0 ₀ -P0 ₇ , P1 ₀ -P1 ₇ , P2 ₀ -P2 ₇ , P3 ₀ -P3 ₇ , P4 ₀ -P4 ₇ , P5 ₀ -P5 ₇ , P6 ₀ -P6 ₇ , P7 ₂ -P7 ₇ , P8 ₀ -P8 ₄ , P8 ₆ , P8 ₇ , P9 ₀ -P9 ₇ , P10 ₀ -P10 ₇ , P11 ₀ -P11 ₄ , P12 ₀ -P12 ₇ , P13 ₀ -P13 ₇ , P14 ₀ -P14 ₆ , P15 ₀ -P15 ₇ ⁽¹⁾ , X _{OUT}	-0.3 to V _{cc} +0.3	V
		P7 ₀ , P7 ₁	-0.3 to 6.0	V
P _d	Power Dissipation	T _{opr} =25° C	500	mW
T _{opr}	Operating ambient temperature		-20 to 85/-40 to 85 ⁽²⁾	° C
T _{stg}	Storage temperature		-65 to 150	° C

NOTES:

1. P11 to P15 are provided in the 144-pin package.
2. This is an option that is on request basis.

Table 5.2 Recommended Operating Conditions ($V_{CC} = 3.0V$ to $5.5V$ at $T_{opr} = -20$ to $85^{\circ}C/-40$ to $85^{\circ}C^{(3)}$)

Symbol	Parameter		Standard			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage (Through VDC)		3.0	5.0	5.5	V
	Supply voltage (Not through VDC)		3.0	3.3	3.6	V
AV_{CC}	Analog supply voltage			V_{CC}		V
V_{SS}	Supply voltage			0		V
AV_{SS}	Analog supply voltage			0		V
V_{IH}	Input high ("H") voltage	P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P87 ⁽⁴⁾ , P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁵⁾ , X_{IN} , \overline{RESET} , CNV_{SS} , BYTE	$0.8V_{CC}$		V_{CC}	V
		P70, P71	$0.8V_{CC}$		6.0	
		P00-P07, P10-P17 (In single-chip mode)	$0.8V_{CC}$		V_{CC}	V
		P00-P07, P10-P17 (In memory expansion mode and microprocessor mode)	$0.5V_{CC}$		V_{CC}	V
V_{IL}	Input low ("L") voltage	P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87 ⁽⁴⁾ , P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁵⁾ , X_{IN} , \overline{RESET} , CNV_{SS} , BYTE	0		$0.2V_{CC}$	V
		P00-P07, P10-P17 (In single-chip mode)	0		$0.2V_{CC}$	V
		P00-P07, P10-P17 (In memory expansion mode and microprocessor mode)	0		$0.16V_{CC}$	V
$I_{OH(peak)}$	Peak output high ("H") current ⁽²⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁵⁾			-10.0	mA
$I_{OH(avg)}$	Average output high ("H") current ⁽¹⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁵⁾			-5.0	mA
$I_{OL(peak)}$	Peak output low ("L") current ⁽²⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁵⁾			10.0	mA
$I_{OL(avg)}$	Average output low ("L") current ⁽¹⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽⁵⁾			5.0	mA
$f(X_{IN})$	Main clock input frequency	Through VDC	$V_{CC}=4.2$ to $5.5V$	0	30	MHz
			$V_{CC}=3.0$ to $5.5V$	0	20	MHz
		Not through VDC	$V_{CC}=3.0$ to $3.6V$	0	20	MHz
$f(X_{CIN})$	Sub clock oscillation frequency			32.768	50	kHz

NOTES:

- Output current is averaged with 100ms.
- Total $I_{OL(peak)}$ for P0, P1, P2, P86, P87, P9, P10, P11, P14 and P15 must be less than or equal to 80mA.
Total $I_{OH(peak)}$ for P0, P1, P2, P86, P87, P9, P10, P11, P14 and P15 must be less than or equal to -80mA.
Total $I_{OL(peak)}$ for P3, P4, P5, P6, P7, P80 to P84, P12 and P13 must be less than or equal to 80mA.
Total $I_{OH(peak)}$ for P3, P4, P5, P6, P72 to P77, P80 to P84, P12 and P13 must be less than or equal to -80mA.
- This is an option that is on request basis.
- V_{IH} and V_{IL} reference for P87 applies to P87 used as a programmable input ports. It does not apply to P87 used as X_{CIN} .
- P11 to P15 are provided in the 144-pin package only.

VCC = 5V

Table 5.3 Electrical Characteristics (VCC=4.2 to 5.5V, VSS=0V at Topr= -20 to 85°C unless otherwise specified)

Symbol	Parameter		Condition	Standard			Unit
				Min	Typ	Max	
VOH	Output high ("H") voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	VCC=5V IOH=-5mA	3.0			V
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	VCC=5V IOH=-200μA	4.7			V
		XOUT	VCC=5V IOH=-1mA	3.0			V
		XCOU	No load applied		3.3		V
VOL	Output low ("L") voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	IOA=5mA			2.0	V
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	IOA=200μA			0.45	V
		XOUT	IOA=1mA			2.0	V
		XCOU	No load applied		0		V
VT+ - VT-	Hysteresis	HOLD, RDY, TA0IN-TA4IN, TB0IN-TB5IN, INT0-INT5, ADTRG, CTS0-CTS4, CLK0-CLK4, TA0OUT-TA4OUT, NMI, KI0-KI3, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		RESET		0.2		1.8	V
I _{IH}	Input high ("H") current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNVSS, BYTE	VI=VCC			5.0	μA
I _{IL}	Input low ("L") current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNVSS, BYTE	VI=0V			-5.0	μA
R _{PULLUP}	Pull-up resistance	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	VI=0V	30	50	167	kΩ
R _{fXIN}	Feedback resistance	X _{IN}			1.5		MΩ
R _{fXCIN}	Feedback resistance	X _{CIN}			10		MΩ
V _{RAM}	RAM standby voltage	Through VDC		2.5			V
I _{CC}	Power supply current	Measurement conditions: In single-chip mode, output pins are left open and other pins are connected to VSS.	f(X _{IN})=30 MHz, square wave, no division		28	54	mA
			f(X _{CIN})=32 kHz, with a wait state, Topr=25° C		470		μA
			Topr=25° C when the clock stops		0.4	20	μA

NOTES:

1. P11 to P15 are provided in the 144-pin package only.

VCC = 5V**Table 5.4 A/D Conversion Characteristics (VCC = AVCC = VREF = 4.2 to 5.5V, VSS = AVSS = 0V at Topr = -20 to 85°C unless otherwise specified)**

Symbol	Parameter	Measurement condition	Standard			Unit	
			Min	Typ	Max		
-	Resolution	VREF=VCC			10	Bits	
INL	Integral nonlinearity error	VREF=VCC=5V	AN0 to AN7 ANEX0, ANEX1			±3	LSB
							LSB
						±7	LSB
	External op-amp connection mode					LSB	
DNL	Differential nonlinearity error				±1	LSB	
-	Offset error				±3	LSB	
-	Gain error				±3	LSB	
RLADDER	Resistor ladder	VREF=VCC	8		40	kΩ	
tCONV	10-bit conversion time		3.3			μs	
tCONV	8-bit conversion time		2.8			μs	
tSAMP	Sample time		0.3			μs	
VREF	Reference voltage		2		VCC	V	
VIA	Analog input voltage		0		VREF	V	

NOTES:

1. Divide f(XIN), if exceeding 10 MHz, to keep φAD frequency less than or equal to 10 MHz.

Table 5.5 D/A Conversion Characteristics (VCC = VREF = 4.2 to 5.5V, VSS = AVSS = 0V at Topr = -20 to 85°C unless otherwise specified)

Symbol	Parameter	Measurement condition	Standard			Unit
			Min	Typ	Max	
-	Resolution				8	Bits
-	Absolute accuracy				1.0	%
tSU	Setup time				3	μs
Ro	Output resistance		4	10	20	kΩ
IVREF	Reference power supply input current	(Note 1)			1.5	mA

NOTES:

1. Measurement condition is that one of two D/A converters is used and the DAi register (i=0, 1) for the unused D/A converter to "0016". The resistor ladder in the A/D converter is excluded. IVREF flows even if the ADiCON1 register is set to "0" (no VREF connection).

VCC = 5V

Timing Requirements (VCC = 4.2 to 5.5V, VSS = 0V at Topr = -20 to 85°C unless otherwise specified)

Table 5.6 External Clock Input

Symbol	Parameter	Standard		Unit
		Min	Max	
tc	External clock input cycle time	33		ns
tw(H)	External clock input high ("H") pulse width	13		ns
tw(L)	External clock input low ("L") pulse width	13		ns
tr	External clock rising edge time		5	ns
tf	External clock falling edge time		5	ns

Table 5.7 Memory Expansion and Microprocessor Modes

Symbol	Parameter	Standard		Unit
		Min	Max	
tac1(RD-DB)	Data input access time (RD standard, with no wait state)		(Note 1)	ns
tac1(AD-DB)	Data input access time (AD standard, CS standard, with no wait state)		(Note 1)	ns
tac2(RD-DB)	Data input access time (RD standard, with a wait state)		(Note 1)	ns
tac2(AD-DB)	Data input access time (AD standard, CS standard, with a wait state)		(Note 1)	ns
tac3(RD-DB)	Data input access time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
tac3(AD-DB)	Data input access time (AD standard, CS standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
tac4(RAS-DB)	Data input access time (RAS standard, when accessing a DRAM space)		(Note 1)	ns
tac4(CAS-DB)	Data input access time (CAS standard, when accessing a DRAM space)		(Note 1)	ns
tac4(CAD-DB)	Data input access time (CAD standard, when accessing a DRAM space)		(Note 1)	ns
tsu(DB-BCLK)	Data input setup time	26		ns
tsu(RDY-BCLK)	RDY input setup time	26		ns
tsu(HOLD-BCLK)	HOLD input setup time	30		ns
th(RD-DB)	Data input hold time	0		ns
th(CAS-DB)	Data input hold time	0		ns
th(BCLK-RDY)	RDY input hold time	0		ns
th(BCLK-HOLD)	HOLD input hold time	0		ns
td(BCLK-HLDA)	HLDA output delay time		25	ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency. Insert a wait state or use lower f(BCLK) as an operation frequency if a calculated value is negative.

$$tac1(RD - DB) = \frac{10^9}{f(BCLK) \times 2} - 35 \quad [ns]$$

$$tac1(AD - DB) = \frac{10^9}{f(BCLK)} - 35 \quad [ns]$$

$$tac2(RD - DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns] \quad (m=3 \text{ with 1 wait state, } m=5 \text{ with 2 wait states and } m=7 \text{ with 3 wait states})$$

$$tac2(AD - DB) = \frac{10^9 \times n}{f(BCLK)} - 35 \quad [ns] \quad (n=2 \text{ with 1 wait state, } n=3 \text{ with 2 wait states and } n=4 \text{ with 3 wait states})$$

$$tac3(RD - DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$tac3(AD - DB) = \frac{10^9 \times n}{f(BCLK) \times 2} - 35 \quad [ns] \quad (n=5 \text{ with 2 wait states and } n=7 \text{ with 3 wait states})$$

$$tac4(RAS - DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns] \quad (m=3 \text{ with 1 wait state and } m=5 \text{ with 2 wait states})$$

$$tac4(CAS - DB) = \frac{10^9 \times n}{f(BCLK) \times 2} - 35 \quad [ns] \quad (n=1 \text{ with 1 wait state and } n=3 \text{ when 2 wait states})$$

$$tac4(CAD - DB) = \frac{10^9 \times l}{f(BCLK)} - 35 \quad [ns] \quad (l=1 \text{ with 1 wait state and } l=2 \text{ with 2 wait states})$$

VCC = 5V

Timing Requirements

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = -20 to 85°C unless otherwise specified)

Table 5.8 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TAiIn input cycle time	100		ns
tw(TAH)	TAiIn input high ("H") pulse width	40		ns
tw(TAL)	TAiIn input low ("L") pulse width	40		ns

Table 5.9 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TAiIn input cycle time	400		ns
tw(TAH)	TAiIn input high ("H") pulse width	200		ns
tw(TAL)	TAiIn input low ("L") pulse width	200		ns

Table 5.10 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TAiIn input cycle time	200		ns
tw(TAH)	TAiIn input high ("H") pulse width	100		ns
tw(TAL)	TAiIn input low ("L") pulse width	100		ns

Table 5.11 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tw(TAH)	TAiIn input high ("H") pulse width	100		ns
tw(TAL)	TAiIn input low ("L") pulse width	100		ns

Table 5.12 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(UP)	TAiOUT input cycle time	2000		ns
tw(UPH)	TAiOUT input high ("H") pulse width	1000		ns
tw(UPL)	TAiOUT input low ("L") pulse width	1000		ns
tsu(UP-TIN)	TAiOUT input setup time	400		ns
th(TIN-UP)	TAiOUT input hold time	400		ns

VCC = 5V

Timing Requirements

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = -20 to 85°C unless otherwise specified)

Table 5.13 Timer B Input (Count Source Input in eEvent Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TB)	TBiIN input cycle time (counted on one edge)	100		ns
tw(TBH)	TBiIN input high ("H") pulse width (counted on one edge)	40		ns
tw(TBL)	TBiIN input low ("L") pulse width (counted on one edge)	40		ns
tc(TB)	TBiIN input cycle time (counted on both edges)	200		ns
tw(TBH)	TBiIN input high ("H") pulse width (counted on both edges)	80		ns
tw(TBL)	TBiIN input low ("L") pulse width (counted on both edges)	80		ns

Table 5.14 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high ("H") pulse width	200		ns
tw(TBL)	TBiIN input low ("L") pulse width	200		ns

Table 5.15 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TB)	TBiIN input cycle time	400		ns
tw(TBH)	TBiIN input high ("H") pulse width	200		ns
tw(TBL)	TBiIN input low ("L") pulse width	200		ns

Table 5.16 A/D trigger Input

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(AD)	\overline{ADTRG} input high ("H") pulse width (trigger available at minimum)	1000		ns
tw(ADL)	\overline{ADTRG} input low ("L") pulse width	125		ns

Table 5.17 Serial I/O

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(CLK)	CLKi input cycle time	200		ns
tw(CLKH)	CLKi input high ("H") pulse width	100		ns
tw(CLKL)	CLKi input low ("L") pulse width	100		ns
td(C-Q)	TxDi output delay time		80	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input hold time	30		ns
th(C-Q)	RxDi input hold time	90		ns

Table 5.18 External Interrupt \overline{INTi} Input

Symbol	Parameter	Standard		Unit
		Min	Max	
tw(INH)	\overline{INTi} input high ("H") pulse width	250		ns
tw(INL)	\overline{INTi} input low ("L") pulse width	250		ns

VCC = 5V

Switching Characteristics

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = -20 to 85°C unless otherwise specified)

Table 5.19 Memory Expansion Mode and Microprocessor Mode (with No Wait State)

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address output delay time	See Figure 5.1		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
th(RD-AD)	Address output hold time (RD standard)		0		ns
th(WR-AD)	Address output hold time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)		0		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE signal output delay time			18	ns
th(BCLK-ALE)	ALE signal output hold time		-2		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-RD)	RD signal output hold time		-5		ns
td(BCLK-WR)	WR signal output delay time			18	ns
td(BCLK-WR)	WR signal outpu hold time		-3		ns
td(DB-WR)	Data output delay time (WR standard)		(Note 1)		ns
th(WR-DB)	Data outpu hold time (WR standard)		(Note 1)		ns
tw(WR)	Write pulse width		(Note 1)		ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$td(DB - WR) = \frac{10^9}{f(BCLK)} - 20 \quad [ns]$$

$$th(WR - DB) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$tw(WR) = \frac{10^9}{f(BCLK) \times 2} - 15 \quad [ns]$$

VCC = 5V

Switching Characteristics

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = -20 to 85°C unless otherwise specified)

**Table 5.20 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory)**

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address output delay time	See Figure 5.1		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
th(RD-AD)	Address output hold time (RD standard)		0		ns
th(WR-AD)	Address output hold time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)		0		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE signal output delay time			18	ns
th(BCLK-ALE)	ALE signal output hold time		-2		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-RD)	RD signal output hold time		-5		ns
td(BCLK-WR)	WR signal output delay time			18	ns
td(BCLK-WR)	WR signal output hold time		-3		ns
td(DB-WR)	Data output delay time (WR standard)		(Note 1)		ns
th(WR-DB)	Data output hold time (WR standard)		(Note 1)		ns
tw(WR)	Write pulse width		(Note 1)		ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$td(DB - WR) = \frac{10^9 \times n}{f(BCLK)} - 20 \quad [ns] \quad (n=1 \text{ with 1 wait state, } n=2 \text{ with 2 wait states} \\ \text{and } n=3 \text{ with 3 wait states})$$

$$th(WR - DB) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$tw(WR) = \frac{10^9 \times n}{f(BCLK) \times 2} - 15 \quad [ns] \quad (n=1 \text{ with 1 wait state, } n=3 \text{ with 2 wait states} \\ \text{and } n=5 \text{ with 3 wait states})$$

VCC = 5V

Switching Characteristics

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = -20 to 85°C unless otherwise specified)

**Table 5.21 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory and Selecting a Space with the
Multiplexed Bus)**

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address output delay time	See Figure 5.1		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		-3		ns
th(RD-AD)	Address output hold time (RD standard)		(Note 1)		ns
th(WR-AD)	Address output hold time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		-3		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)		(Note 1)		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)		(Note 1)		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-AD)	RD signal output hold time		-5		ns
td(BCLK-WR)	WR signal output delay time			18	ns
th(BCLK-WR)	WR signal output hold time		-3		ns
td(DB-WR)	Data output delay time (WR standard)		(Note 1)		ns
th(WR-DB)	Data output hold time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE signal output delay time (BCLK standard)			18	ns
th(BCLK-ALE)	ALE signal output hold time (BCLK standard)		-2		ns
td(AD-ALE)	ALE signal output delay time (address standard)		(Note 1)		ns
th(ALE-AD)	ALE signal output hold time (address standard)		(Note 1)		ns
tdZ(RD-AD)	Address output high-impedance time			8	ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$th(RD - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(RD - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$td(DB - WR) = \frac{10^9 \times m}{f(BCLK) \times 2} - 25 \quad [ns] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$th(WR - DB) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$td(AD - ALE) = \frac{10^9}{f(BCLK) \times 2} - 20 \quad [ns]$$

$$th(ALE - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

VCC = 5V

Switching Characteristics

(VCC = 4.2 to 5.5V, VSS = 0V at Topr = -20 to 85°C unless otherwise specified)

**Table 5.22 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory and Selecting the DRAM Area)**

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Row address output delay time	See Figure 5.1		18	ns
th(BCLK-AD)	Row address output hold time (BCLK standard)		-3		ns
th(BCLK-CAD)	Column address output delay time			18	ns
td(BCLK-CAD)	Column address output hold time (BCLK standard)		-3		ns
th(RAS-RAD)	Row address output hold time after RAS output		(Note 1)		ns
td(BCLK-RAS)	RAS output delay time (BCLK standard)			18	ns
th(BCLK-RAS)	RAS output hold time (BCLK standard)		-3		ns
trp	RAS high ("H") hold time		(Note 1)		ns
td(BCLK-CAS)	CAS output delay time (BCLK standard)			18	ns
th(BCLK-CAS)	CAS output hold time (BCLK standard)		-3		ns
td(BCLK-DW)	DW output delay time (BCLK standard)			18	ns
th(BCLK-DW)	DW output hold time (BCLK standard)		-5		ns
tsu(DB-CAS)	CAS output setup time after DB output		(Note 1)		ns
th(BCLK-DB)	DB signal output hold time (BCLK standard)		-7		ns
tsu(CAS-RAS)	CAS output setup time before RAS output (refresh)		(Note 1)		ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$th(RAS - RAD) = \frac{10^9}{f(BCLK) \times 2} - 13 \quad [ns]$$

$$trp = \frac{10^9}{f(BCLK) \times 2} \times 3 - 20 \quad [ns]$$

$$tsu(DB - CAS) = \frac{10^9}{f(BCLK)} - 20 \quad [ns]$$

$$tsu(CAS - RAS) = \frac{10^9}{f(BCLK) \times 2} - 13 \quad [ns]$$

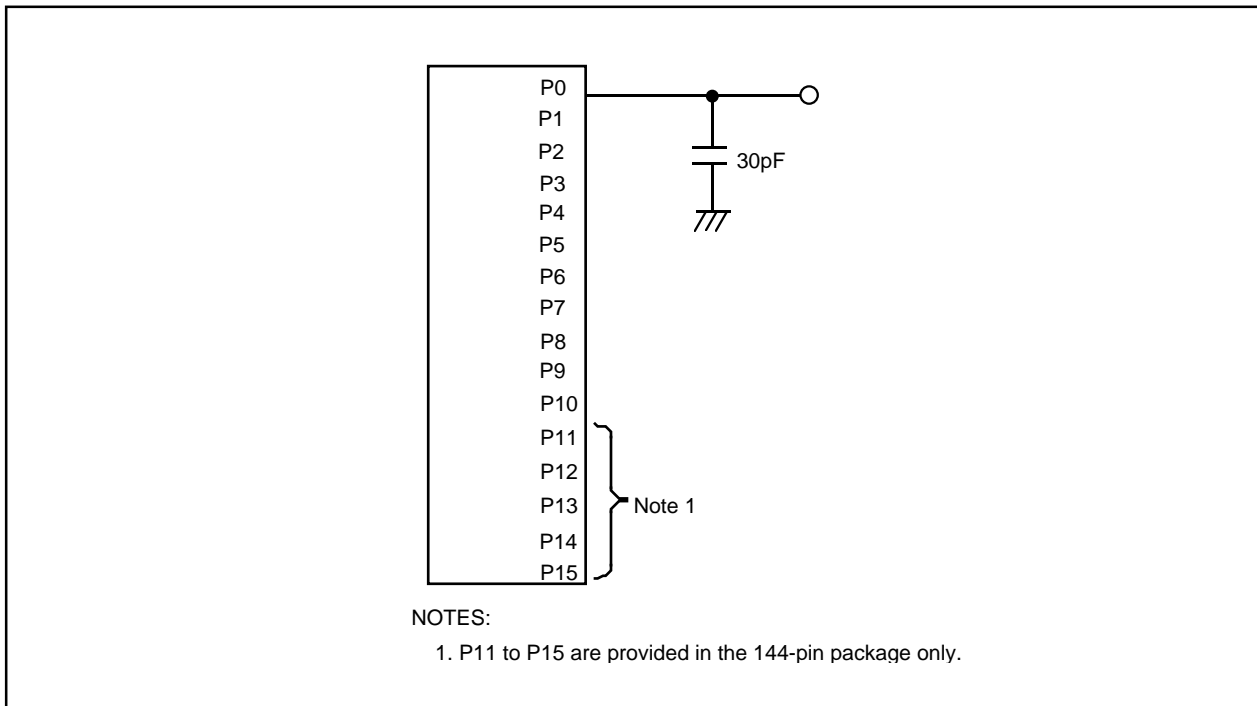


Figure 5.1 P0 to P15 Measurement Circuit

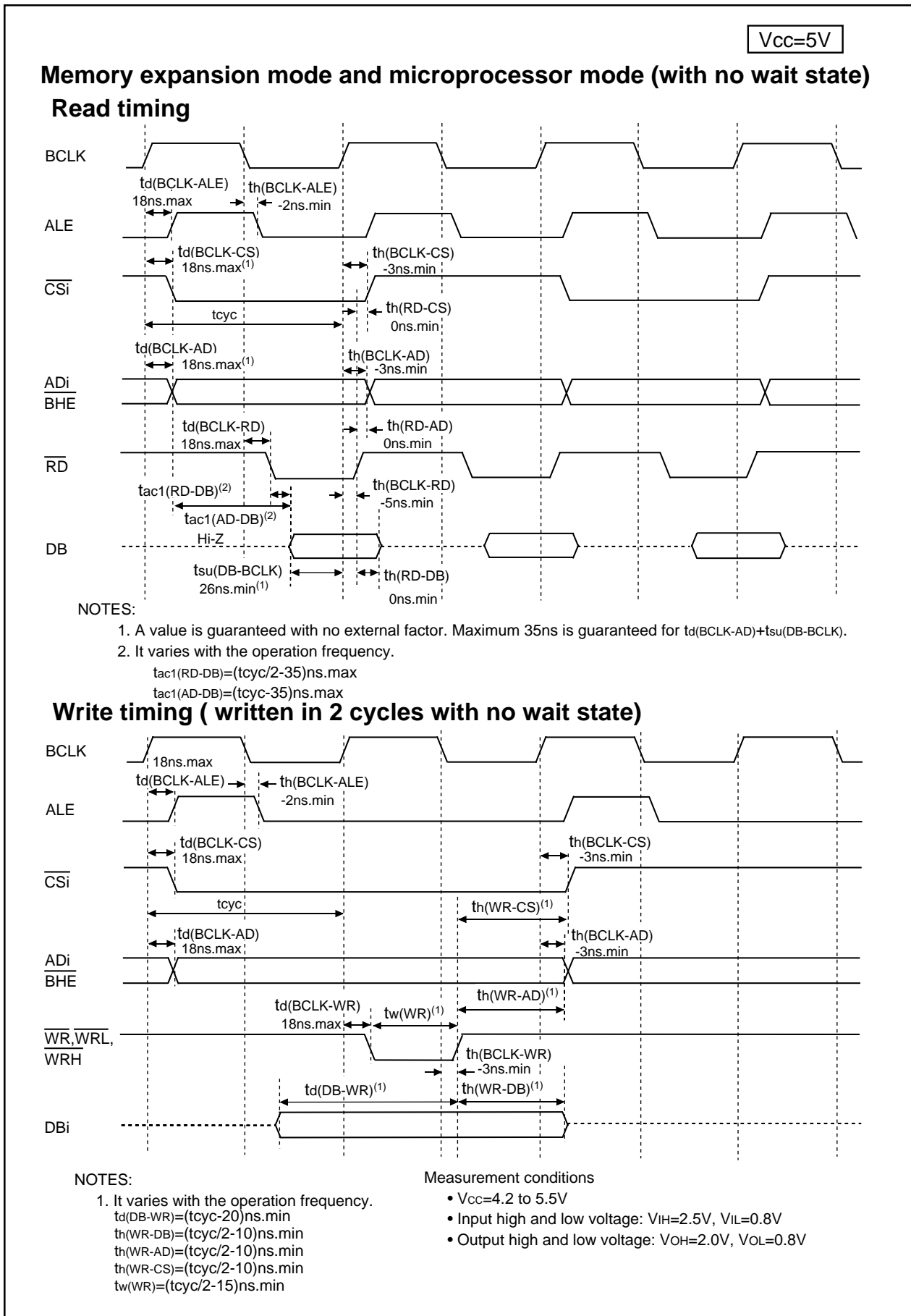


Figure 5.2 Vcc=5V Timing Diagram (1)

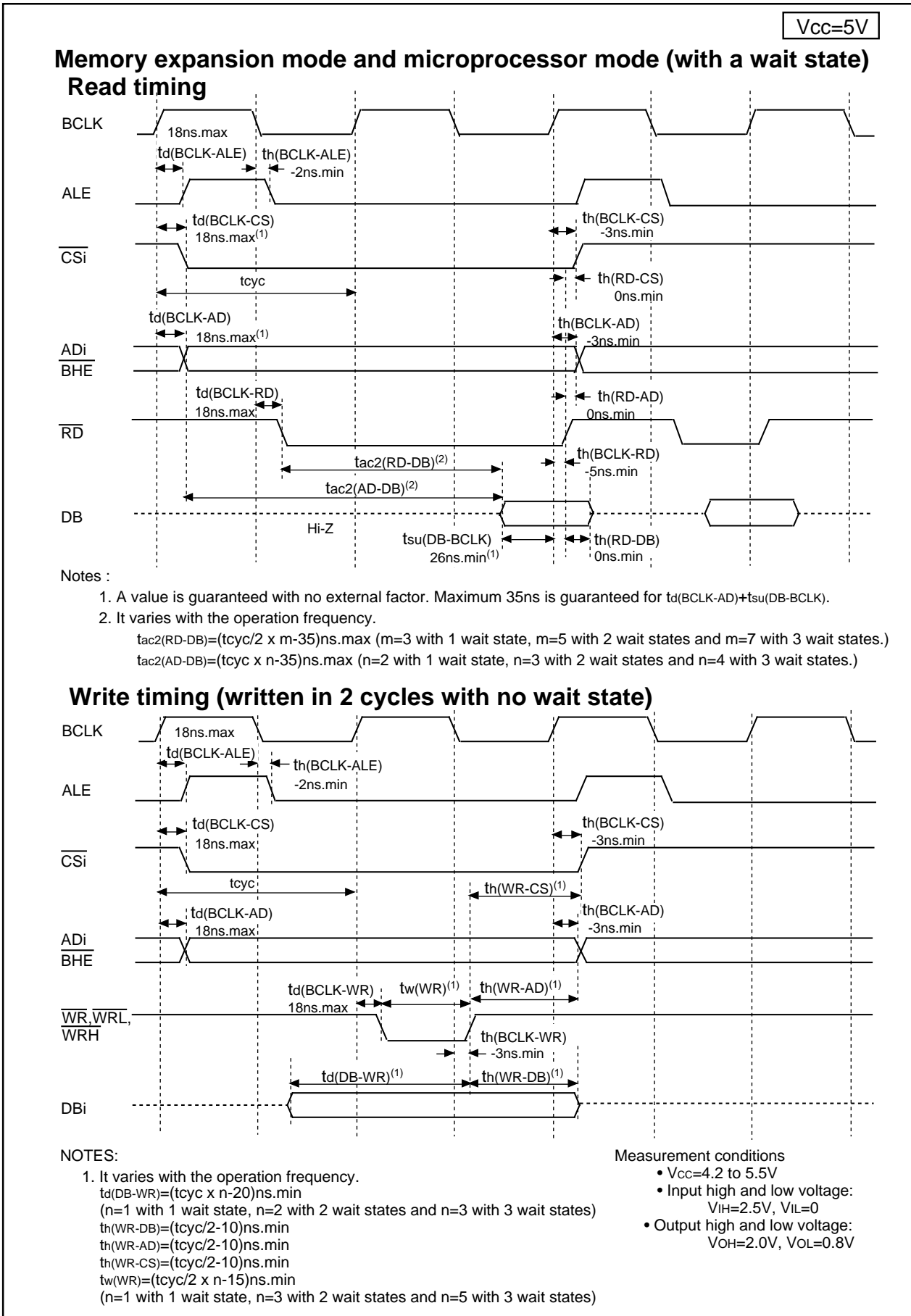


Figure 5.3 Vcc=5V Timing Diagram (2)

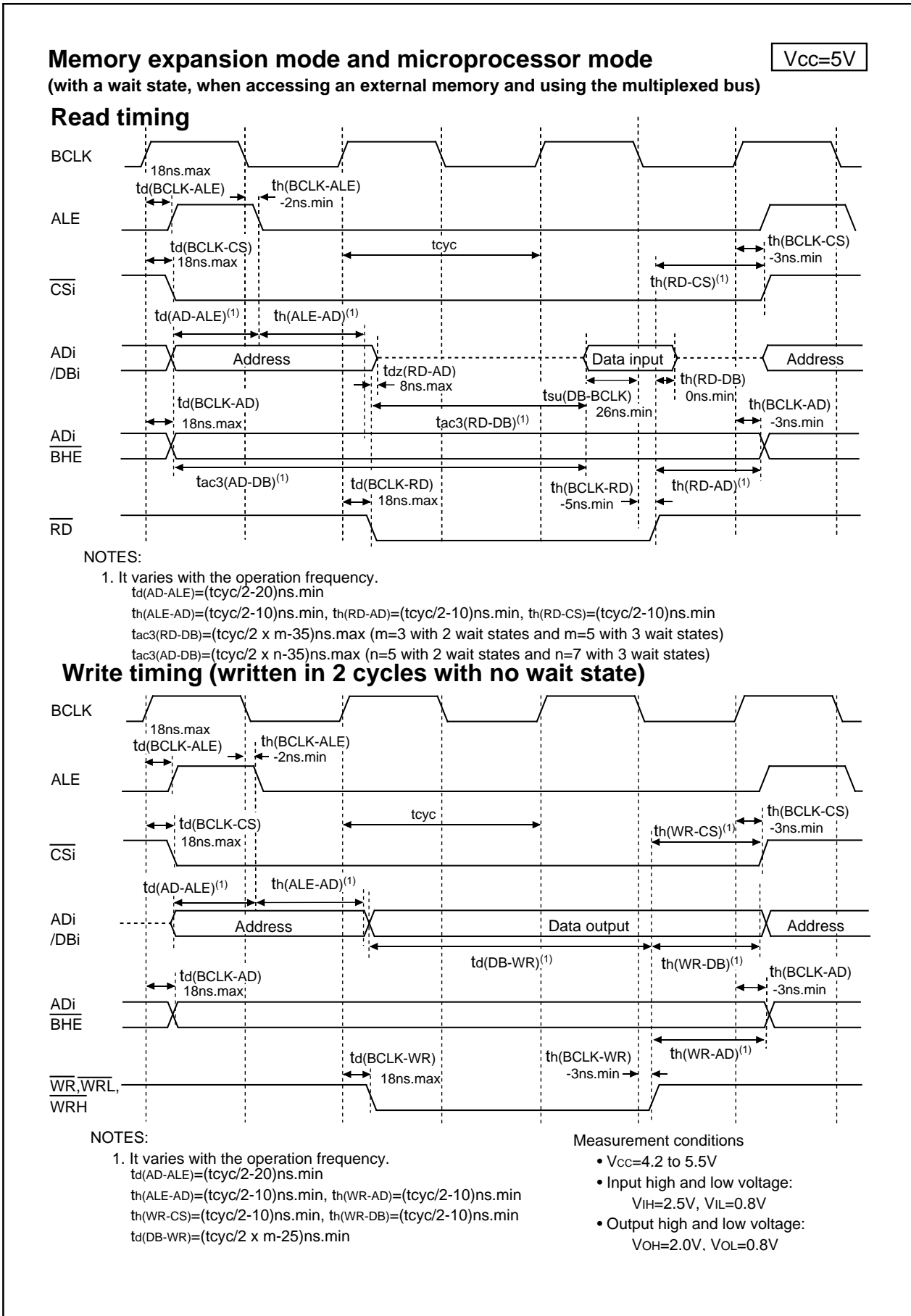


Figure 5.4 Vcc=5V Timing Diagram (3)

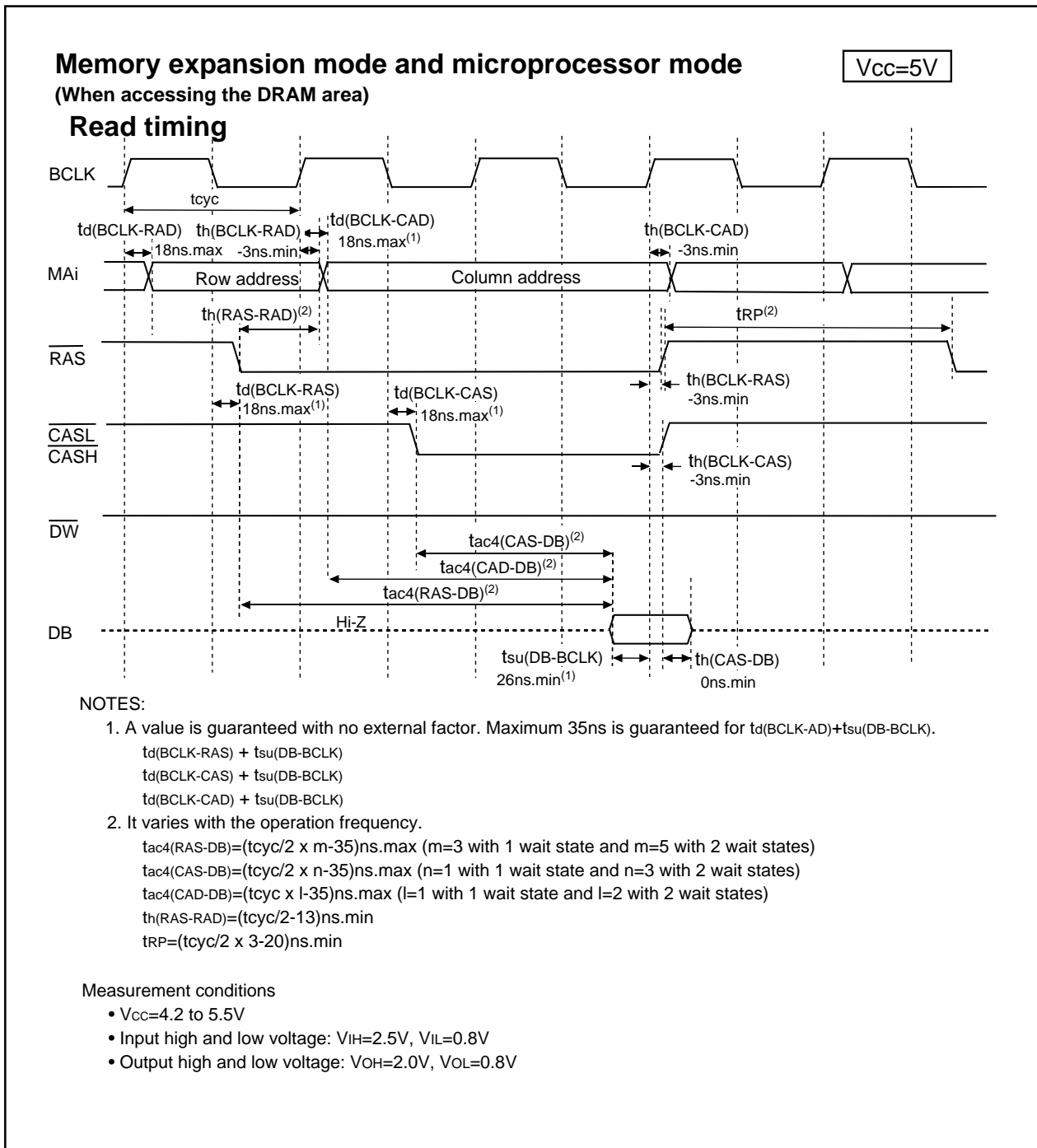


Figure 5.5 VCC=5V Timing Diagram (4)

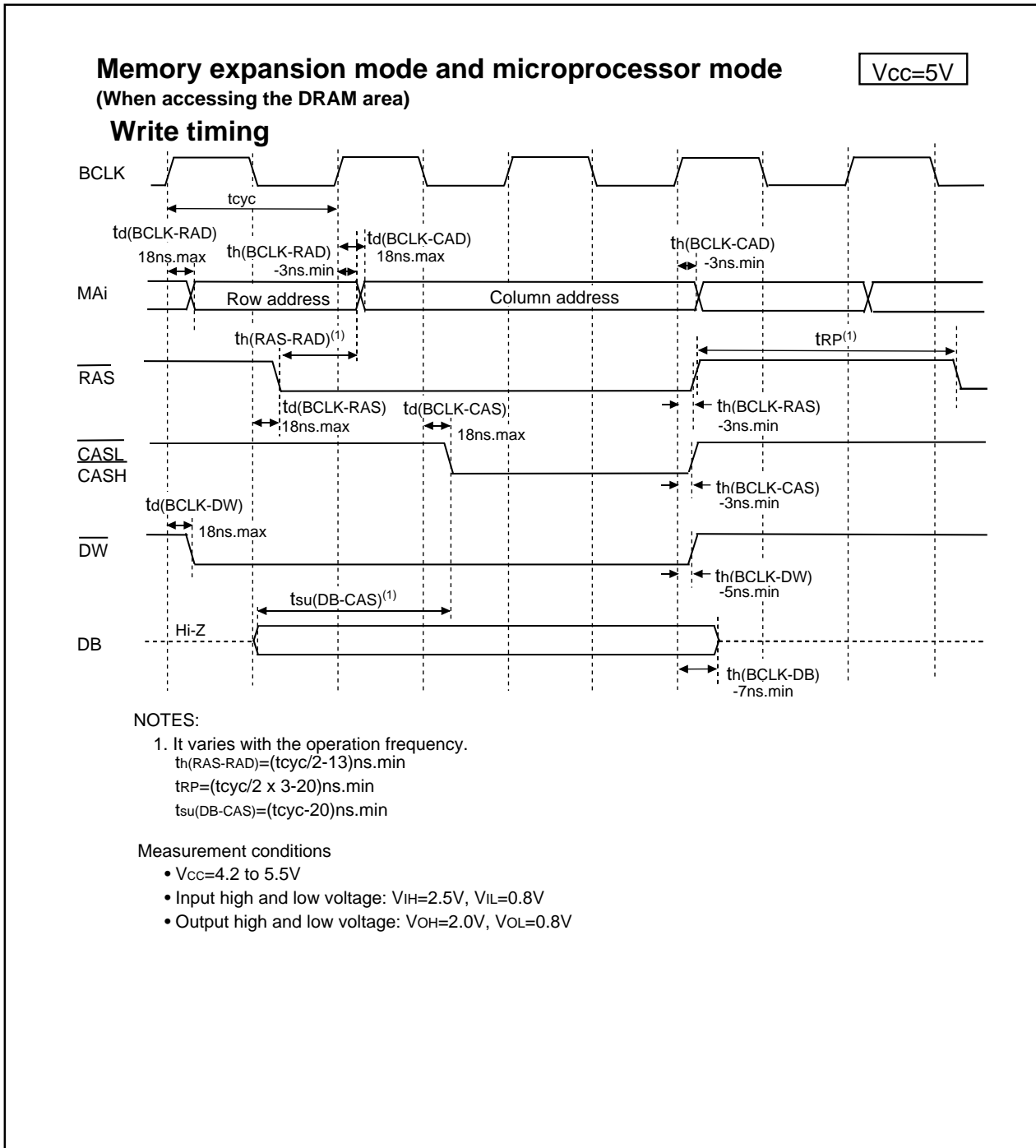


Figure 5.6 Vcc=5V Timing Diagram (5)

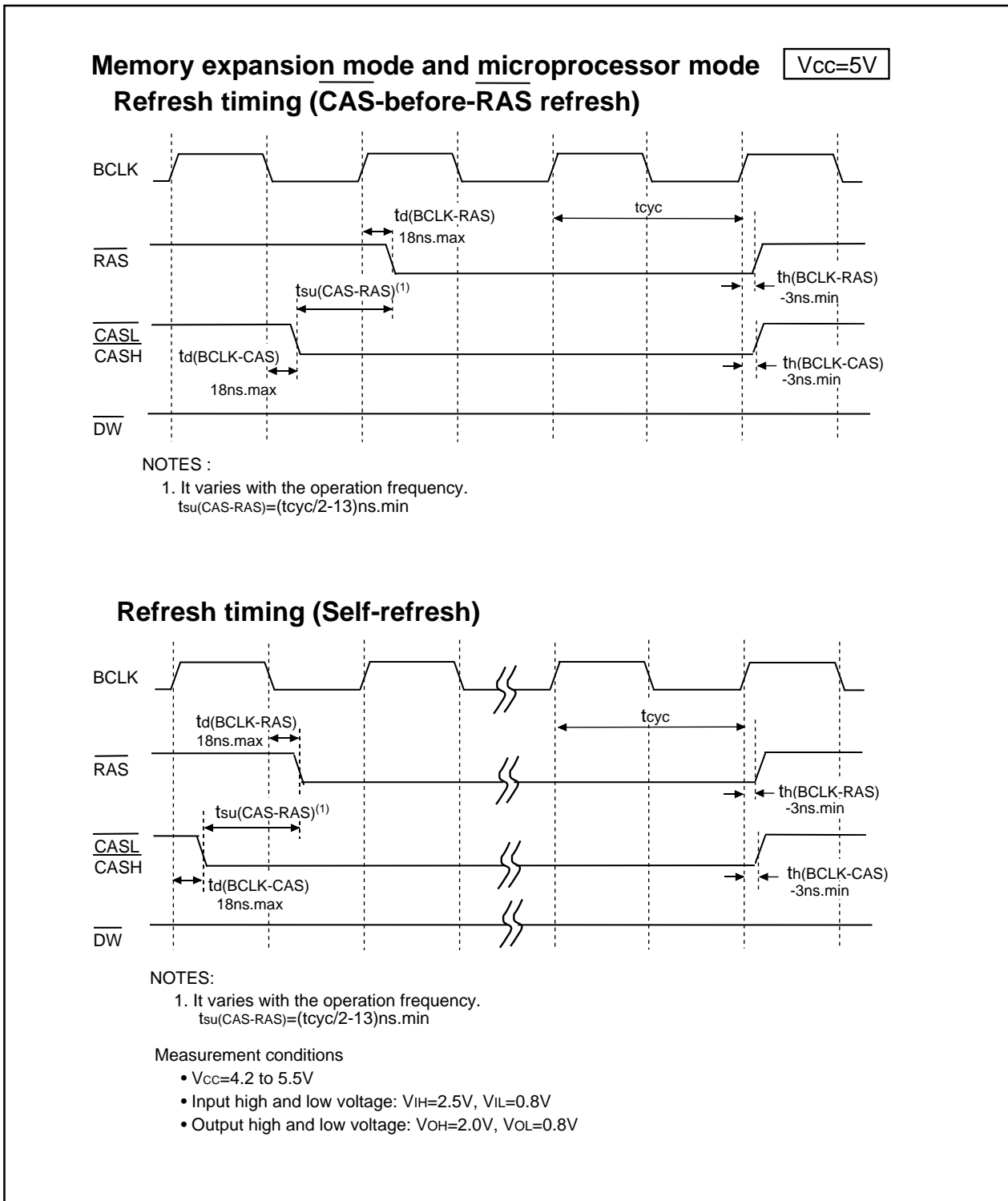


Figure 5.7 Vcc=5V Timing Diagram (6)

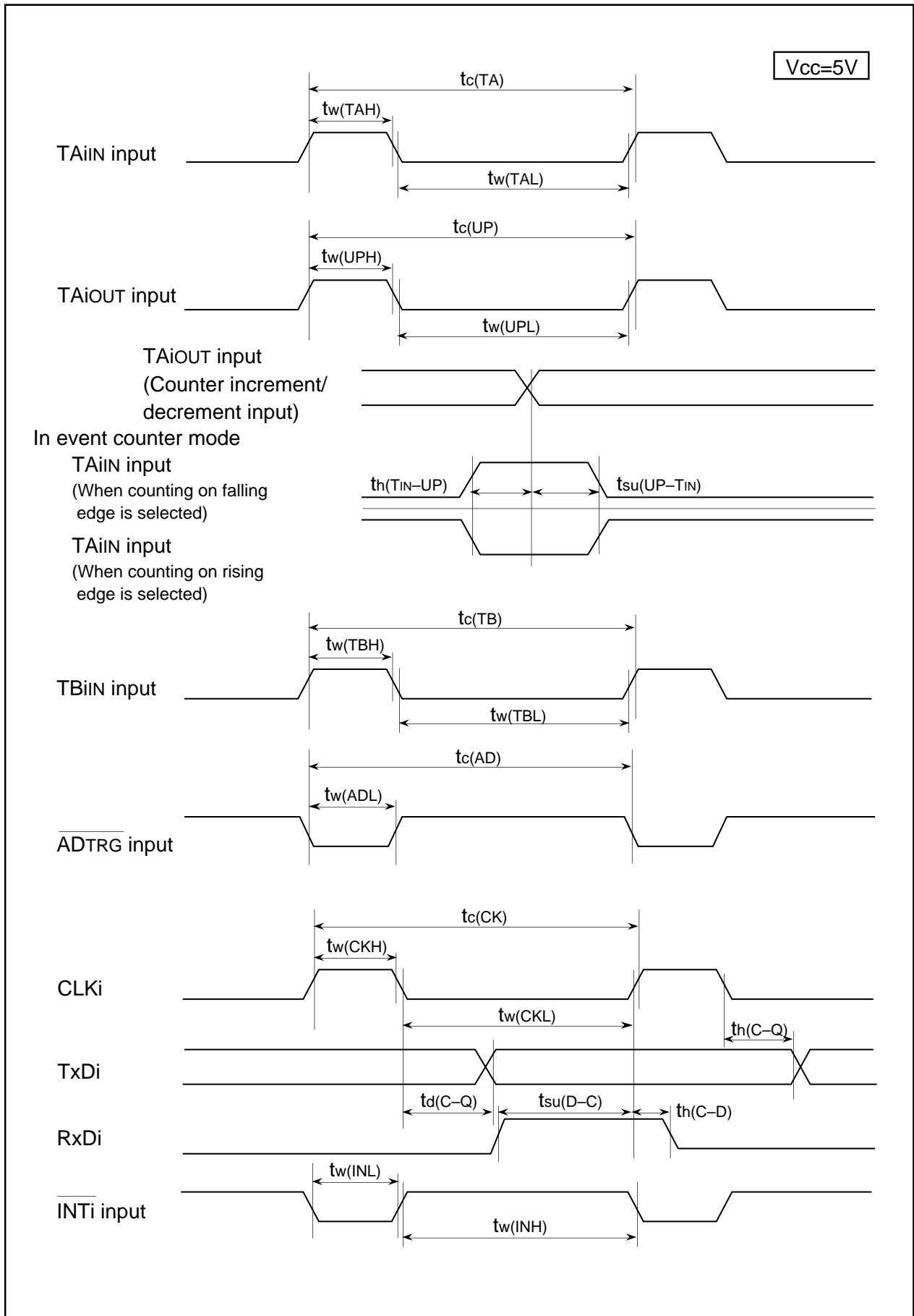


Figure 5.8 Vcc=5V Timing Diagram (7)

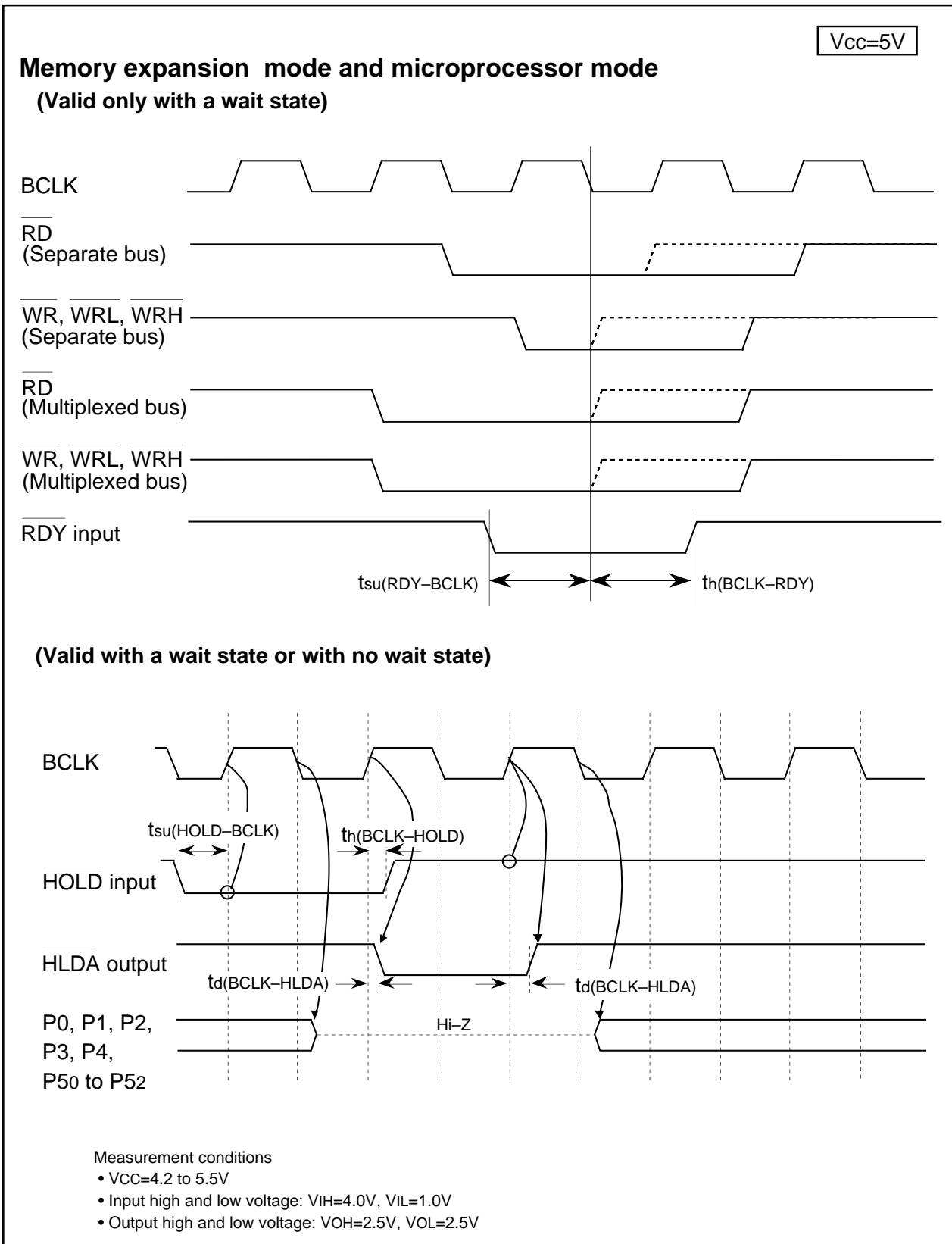


Figure 5.9 Vcc=5V Timing Diagram (8)

VCC = 3.3V**Table 5.23 Electrical Characteristics (VCC=3.0 to 3.6V, VSS=0V at Topr = -20 to 85°C, unless otherwise specified)**

Symbol	Parameter		Condition	Standard			Unit
				Min	Typ	Max	
VOH	Output high ("H") voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OH} =-1mA	2.7			V
		X _{OUT}	I _{OH} =-0.1mA	2.7			V
		X _{OUT}	No load applied		3.3		V
VOL	Output low ("L") voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	I _{OL} =1mA			0.5	V
		X _{OUT}	I _{OL} =0.1mA			0.5	V
		X _{OUT}	No load applied		0		V
VT+ - VT-	Hysteresis	HOLD, RDY, TA0IN-TA4IN, TB0IN-TB5IN, INT0-INT5, ADTRG, CTS0-CTS4, CLK0-CLK4, TA0OUT-TA4OUT, NMI, KI0-KI3, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		RESET		0.2		1.8	V
I _{IH}	Input high ("H") current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	V _I =V _{CC}			4.0	μA
I _{IL}	Input low ("L") current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾ , X _{IN} , RESET, CNV _{SS} , BYTE	V _I =0V			-4.0	μA
R _{PULLUP}	Pull-up resistance	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, P110-P114, P120-P127, P130-P137, P140-P146, P150-P157 ⁽¹⁾	V _I =0V	66	120	500	kΩ
R _{fXIN}	Feedback resistance	X _{IN}			3.0		MΩ
R _{fXCIN}	Feedback resistance	X _{CIN}			20.0		MΩ
V _{RAM}	RAM standby voltage	Through VDC		2.5			V
		Not through VDC		2.0			V
I _{CC}	Power supply current	Measurement condition: In single-chip mode, output pins are left open and other pins are connected to V _{SS} .	f(X _{IN})=20 MHz, square wave, no division		17	38	mA
			f(X _{CIN})=32 kHz, with a wait state, not through VDC, Topr=25° C		5.0		μA
			f(X _{CIN})=32 kHz, with a wait state, through VDC, Topr=25° C		340		μA
			Topr=25° C when the clock stops		0.4	20	μA

NOTES:

- P11 to P15 are provided in the 144-pin package only.

VCC = 3.3V**Table 5.24 A/D Conversion Characteristics (VCC = AVCC = VREF = 3.0 to 3.6V, VSS = AVSS = 0V
at Topr = -20 to 85°C unless otherwise specified)**

Symbol	Parameter		Measurement condition	Standard			Unit
				Min	Typ	Max	
-	Resolution		VREF=VCC			10	Bits
INL	Integral nonlinearity error	No S&H function (8-bit)	VCC=VREF=3.3V			±2	LSB
DNL	Differential nonlinearity error	No S&H function (8-bit)				±1	LSB
-	Offset error	No S&H function (8-bit)				±2	LSB
-	Gain error	No S&H function (8-bit)				±2	LSB
RLADDER	Resistor ladder		VREF=VCC	8		40	kΩ
tCONV	8-bit conversion time			4.9			μs
VREF	Reference voltage			3.0		VCC	V
VIA	Analog input voltage			0		VREF	V

S&H: Sample and hold

NOTES:

1. Divide $f(X_{IN})$, if exceeding 10 MHz, to keep ϕ_{AD} frequency less than or equal to 10 MHz.

**Table 5.25 D/A Conversion Characteristics (VCC = VREF = 3.0 to 3.6V, VSS = AVSS = 0V
at Topr = -20 to 85°C unless otherwise specified)**

Symbol	Parameter	Measurement condition	Standard			Unit
			Min	Typ	Max	
-	Resolution				8	Bits
-	Absolute accuracy				1.0	%
tsu	Setup time				3	μs
Ro	Output resistance		4	10	20	kΩ
IvREF	Reference power supply input current	(Note 1)			1.0	mA

NOTES:

1. Measurement condition is that one of two D/A converters is used and the DAi register (i=0, 1) for the unused D/A converter to "0016". The resistor ladder in the A/D converter is excluded. IvREF flows even if the ADiCON1 register is set to "0" (no VREF connection).

VCC = 3.3V

Timing Requirements (VCC = 3.0 to 3.6V, VSS = 0V at Topr = -20 to 85°C unless otherwise specified)

Table 5.26 External Clock Input

Symbol	Parameter	Standard		Unit
		Min	Max	
tc	External clock input cycle time	50		ns
tw(H)	External clock input high ("H") pulse width	22		ns
tw(L)	External clock input low ("L") pulse width	22		ns
tr	External clock rising-edge time		5	ns
tf	External clock falling-edge time		5	ns

Table 5.27 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min	Max	
tac1(RD-DB)	Data input access time (RD standard, with no wait state)		(Note 1)	ns
tac1(AD-DB)	Data input access time (AD standard, CS standard, with no wait state)		(Note 1)	ns
tac2(RD-DB)	Data input access time (RD standard, with a wait state)		(Note 1)	ns
tac2(AD-DB)	Data input access time (AD standard, CS standard, with a wait state)		(Note 1)	ns
tac3(RD-DB)	Data input access time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
tac3(AD-DB)	Data input access time (AD standard, CS standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
tac4(RAS-DB)	Data input access time (RAS standard, when accessing a DRAM space)		(Note 1)	ns
tac4(CAS-DB)	Data input access time (CAS standard, when accessing a DRAM space)		(Note 1)	ns
tac4(CAD-DB)	Data input access time (CAD standard, when accessing a DRAM space)		(Note 1)	ns
tsu(DB-BCLK)	Data input setup time	30		ns
tsu(RDY-BCLK)	RDY input setup time	40		ns
tsu(HOLD-BCLK)	HOLD input setup time	60		ns
th(RD-DB)	Data input hold time	0		ns
th(CAS-DB)	Data input hold time	0		ns
th(BCLK-RDY)	RDY input hold time	0		ns
th(BCLK-HOLD)	HOLD input hold time	0		ns
td(BCLK-HLDA)	HLDA output delay time		25	ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency. Insert a wait state or use lower f(BCLK) as an operation frequency if a calculated value is negative.

$$tac1(RD - DB) = \frac{10^9}{f(BCLK) \times 2} - 35 \quad [ns]$$

$$tac1(AD - DB) = \frac{10^9}{f(BCLK)} - 35 \quad [ns]$$

$$tac2(RD - DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns] \quad (m=3 \text{ with 1 wait state, } m=5 \text{ with 2 wait states and } m=7 \text{ with 3 wait states})$$

$$tac2(AD - DB) = \frac{10^9 \times n}{f(BCLK)} - 35 \quad [ns] \quad (n=2 \text{ with 1 wait state, } n=3 \text{ with 2 wait states and } n=4 \text{ with 3 wait states})$$

$$tac3(RD - DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns] \quad (m=3 \text{ with 2 wait states and } m=5 \text{ with 3 wait states})$$

$$tac3(AD - DB) = \frac{10^9 \times n}{f(BCLK) \times 2} - 35 \quad [ns] \quad (n=5 \text{ with 2 wait states and } n=7 \text{ with 3 wait states})$$

$$tac4(RAS - DB) = \frac{10^9 \times m}{f(BCLK) \times 2} - 35 \quad [ns] \quad (m=3 \text{ with 1 wait state and } m=5 \text{ with 2 wait states})$$

$$tac4(CAS - DB) = \frac{10^9 \times n}{f(BCLK) \times 2} - 35 \quad [ns] \quad (n=1 \text{ with 1 wait state and } n=3 \text{ when 2 wait states})$$

$$tac4(CAD - DB) = \frac{10^9 \times l}{f(BCLK)} - 35 \quad [ns] \quad (l=1 \text{ with 1 wait state and } l=2 \text{ with 2 wait states})$$

VCC = 3.3V

Timing Requirements

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = -20 to 85°C unless otherwise specified)

Table 5.28 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TAin input cycle time	100		ns
tw(TAH)	TAin input high ("H") pulse width	40		ns
tw(TAL)	TAin input low ("L") pulse width	40		ns

Table 5.29 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TAin input cycle time	400		ns
tw(TAH)	TAin input high ("H") pulse width	200		ns
tw(TAL)	TAin input low ("L") pulse width	200		ns

Table 5.30 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TA)	TAin input cycle time	200		ns
tw(TAH)	TAin input high ("H") pulse width	100		ns
tw(TAL)	TAin input low ("L") pulse width	100		ns

Table 5.31 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tw(TAH)	TAin input high ("H") pulse width	100		ns
tw(TAL)	TAin input low ("L") pulse width	100		ns

Table 5.32 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(UP)	TAiOUT input cycle time	2000		ns
tw(UPH)	TAiOUT input high ("H") pulse width	1000		ns
tw(UPL)	TAiOUT input low ("L") pulse width	1000		ns
tsu(UP-TIN)	TAiOUT input setup time	400		ns
th(TIN-UP)	TAiOUT input hold time	400		ns

VCC = 3.3V

Timing Requirements

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = -20 to 85°C unless otherwise specified)

Table 5.33 Timer B input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TB)	TBin input cycle time (counted on one edge)	100		ns
tw(TBH)	TBin input high ("H") pulse width (counted on one edge)	40		ns
tw(TBL)	TBin input low ("L") pulse width (counted on one edge)	40		ns
tc(TB)	TBin input cycle time (counted on both edges)	200		ns
tw(TBH)	TBin input high ("H") pulse width (counted on both edges)	80		ns
tw(TBL)	TBin input low ("L") pulse width (counted on both edges)	80		ns

Table 5.34 Timer B input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TB)	TBin input cycle time	400		ns
tw(TBH)	TBin input high ("H") pulse width	200		ns
tw(TBL)	TBin input low ("L") pulse width	200		ns

Table 5.35 Timer B input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(TB)	TBin input cycle time	400		ns
tw(TBH)	TBin input high ("H") pulse width	200		ns
tw(TBL)	TBin input low ("L") pulse width	200		ns

Table 5.36 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(AD)	ADTRG input high ("H") pulse width (trigger available at minimum)	1000		ns
tw(ADL)	ADTRG input low ("L") pulse width	125		ns

Table 5.37 Serial I/O

Symbol	Parameter	Standard		Unit
		Min	Max	
tc(CLK)	CLKi input cycle time	200		ns
tw(CLKH)	CLKi input high ("H") pulse width	100		ns
tw(CLKL)	CLKi input low ("L") pulse width	100		ns
td(C-Q)	TxDi output delay time		80	ns
th(C-Q)	TxDi hold time	0		ns
tsu(D-C)	RxDi input hold time	30		ns
th(C-Q)	RxDi input hold time	90		ns

Table 5.38 External Interrupt INTi input

Symbol	Parameter	Standard		Unit
		Min	Max	
tw(INH)	INTi input high ("H") pulse width	250		ns
tw(INL)	INTi input low ("L") pulse width	250		ns

VCC = 3.3V

Switching Characteristics

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = -20 to 85°C, unless otherwise specified)

Table 5.39 Memory Expansion Mode and Microprocessor Mode (with No Wait State)

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address output delay time	See Figure 5.1		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		0		ns
th(RD-AD)	Address output hold time (RD standard)		0		ns
th(WR-AD)	Address output hold time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		0		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)		0		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE signal output delay time			18	ns
th(BCLK-ALE)	ALE signal output hold time		-2		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-RD)	RD signal output hold time		-3		ns
td(BCLK-WR)	WR signal output delay time			18	ns
td(BCLK-WR)	WR signal output hold time		0		ns
td(DB-WR)	Data output delay time (WR standard)		(Note 1)		ns
th(WR-DB)	Data output hold time (WR standard)		(Note 1)		ns
tw(WR)	Write pulse width		(Note 1)		ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$td(DB - WR) = \frac{10^9}{f(BCLK)} - 20 \quad [ns]$$

$$th(WR - DB) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$tw(WR) = \frac{10^9}{f(BCLK) \times 2} - 15 \quad [ns]$$

V_{CC} = 3.3V**Switching Characteristics**(V_{CC} = 3.0 to 3.6V, V_{SS} = 0V at T_{opr} = -20 to 85°C unless otherwise specified)**Table 5.40 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory)**

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
t _{d(BCLK-AD)}	Address output delay time	See Figure 5.1		18	ns
t _{h(BCLK-AD)}	Address output hold time (BCLK standard)		0		ns
t _{h(RD-AD)}	Address output hold time (RD standard)		0		ns
t _{h(WR-AD)}	Address output hold time (WR standard)		(Note 1)		ns
t _{d(BCLK-CS)}	Chip-select signal output delay time			18	ns
t _{h(BCLK-CS)}	Chip-select signal output hold time (BCLK standard)		0		ns
t _{h(RD-CS)}	Chip-select signal output hold time (RD standard)		0		ns
t _{h(WR-CS)}	Chip-select signal output hold time (WR standard)		(Note 1)		ns
t _{d(BCLK-ALE)}	ALE signal output delay time			18	ns
t _{h(BCLK-ALE)}	ALE signal output hold time		-2		ns
t _{d(BCLK-RD)}	RD signal output delay time			18	ns
t _{h(BCLK-RD)}	RD signal output hold time		-3		ns
t _{d(BCLK-WR)}	WR signal output delay time			18	ns
t _{d(BCLK-WR)}	WR signal output hold time		0		ns
t _{d(DB-WR)}	Data output delay time (WR standard)		(Note 1)		ns
t _{h(WR-DB)}	Data output hold time (WR standard)		(Note 1)		ns
t _{w(WR)}	Write pulse width		(Note 1)		ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$t_{d(DB-WR)} = \frac{10^9 \times n}{f_{(BCLK)}} - 20 \quad [\text{ns}] \quad (n=1 \text{ with 1 wait state, } n=2 \text{ with 2 wait states} \\ \text{and } n=3 \text{ with 3 wait states})$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [\text{ns}]$$

$$t_{w(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [\text{ns}] \quad (n=1 \text{ with 1 wait state, } n=3 \text{ with 2 wait states} \\ \text{and } n=5 \text{ with 3 wait states})$$

VCC = 3.3V

Switching Characteristics

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = -20 to 85°C unless otherwise specified)

**Table 5.41 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory and Selecting a Space with the Multiplexed Bus)**

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
td(BCLK-AD)	Address output delay time	See Figure 5.1		18	ns
th(BCLK-AD)	Address output hold time (BCLK standard)		0		ns
th(RD-AD)	Address output hold time (RD standard)		(Note 1)		ns
th(WR-AD)	Address output hold time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-select signal output delay time			18	ns
th(BCLK-CS)	Chip-select signal output hold time (BCLK standard)		0		ns
th(RD-CS)	Chip-select signal output hold time (RD standard)		(Note 1)		ns
th(WR-CS)	Chip-select signal output hold time (WR standard)		(Note 1)		ns
td(BCLK-RD)	RD signal output delay time			18	ns
th(BCLK-AD)	RD signal output hold time		-3		ns
td(BCLK-WR)	WR signal output delay time			18	ns
td(BCLK-WR)	WR signal output hold time		0		ns
td(DB-WR)	Data output delay time (WR standard)		(Note 1)		ns
th(WR-DB)	Data output hold time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE signal output delay time (BCLK standard)			18	ns
th(BCLK-ALE)	ALE signal output hold time (BCLK standard)		-2		ns
td(AD-ALE)	ALE signal output delay time (address standard)		(Note 1)		ns
th(ALE-AD)	ALE signal output hold time (address standard)		(Note 1)		ns
tdZ(RD-AD)	Address output high-impedance time			8	ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$th(RD - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(RD - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$td(DB - WR) = \frac{10^9 \times m}{f(BCLK) \times 2} - 25 \quad [ns] \quad (m=3 \text{ with } 2 \text{ wait states and } m=5 \text{ with } 3 \text{ wait states})$$

$$th(WR - DB) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$td(AD - ALE) = \frac{10^9}{f(BCLK) \times 2} - 20 \quad [ns]$$

$$th(ALE - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

VCC = 3.3V

Switching Characteristics

(VCC = 3.0 to 3.6V, VSS = 0V at Topr = -20 to 85°C unless otherwise specified)

**Table 5.42 Memory Expansion Mode and Microprocessor Mode
(With a Wait State, Accessing an External Memory and Selecting the DRAM Area)**

Symbol	Parameter	Measurement condition	Standard		Unit
			Min	Max	
t _d (BCLK-AD)	Row address output delay time	See Figure 5.1		18	ns
t _h (BCLK-AD)	Row address output hold time (BCLK standard)		0		ns
t _h (BCLK-CAD)	Column address output delay time			18	ns
t _d (BCLK-CAD)	Column address output hold time (BCLK standard)		0		ns
t _h (RAS-RAD)	Row address output hold time after RAS output		(Note 1)		ns
t _d (BCLK-RAS)	RAS output delay time (BCLK standard)			18	ns
t _h (BCLK-RAS)	RAS output hold time (BCLK standard)		0		ns
t _{RP}	RAS high ("H") hold time		(Note 1)		ns
t _d (BCLK-CAS)	CAS output delay time (BCLK standard)			18	ns
t _h (BCLK-CAS)	CAS output hold time (BCLK standard)		0		ns
t _d (BCLK-DW)	DW output delay time (BCLK standard)			18	ns
t _h (BCLK-DW)	DW output hold time (BCLK standard)		-3		ns
t _{su} (DB-CAS)	CAS output setup time after DB output		(Note 1)		ns
t _h (BCLK-DB)	DB signal output hold time (BCLK standard)		-7		ns
t _{su} (CAS-RAS)	CAS output setup time before RAS output (refresh)		(Note 1)		ns

NOTES:

1. A value can be obtained from the following expressions according to the BCLK frequency.

$$t_{h(RAS-RAD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [\text{ns}]$$

$$t_{RP} = \frac{10^9 \times 3}{f_{(BCLK)} \times 2} - 20 \quad [\text{ns}]$$

$$t_{su(DB-CAS)} = \frac{10^9}{f_{(BCLK)}} - 20 \quad [\text{ns}]$$

$$t_{su(CAS-RAS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 13 \quad [\text{ns}]$$

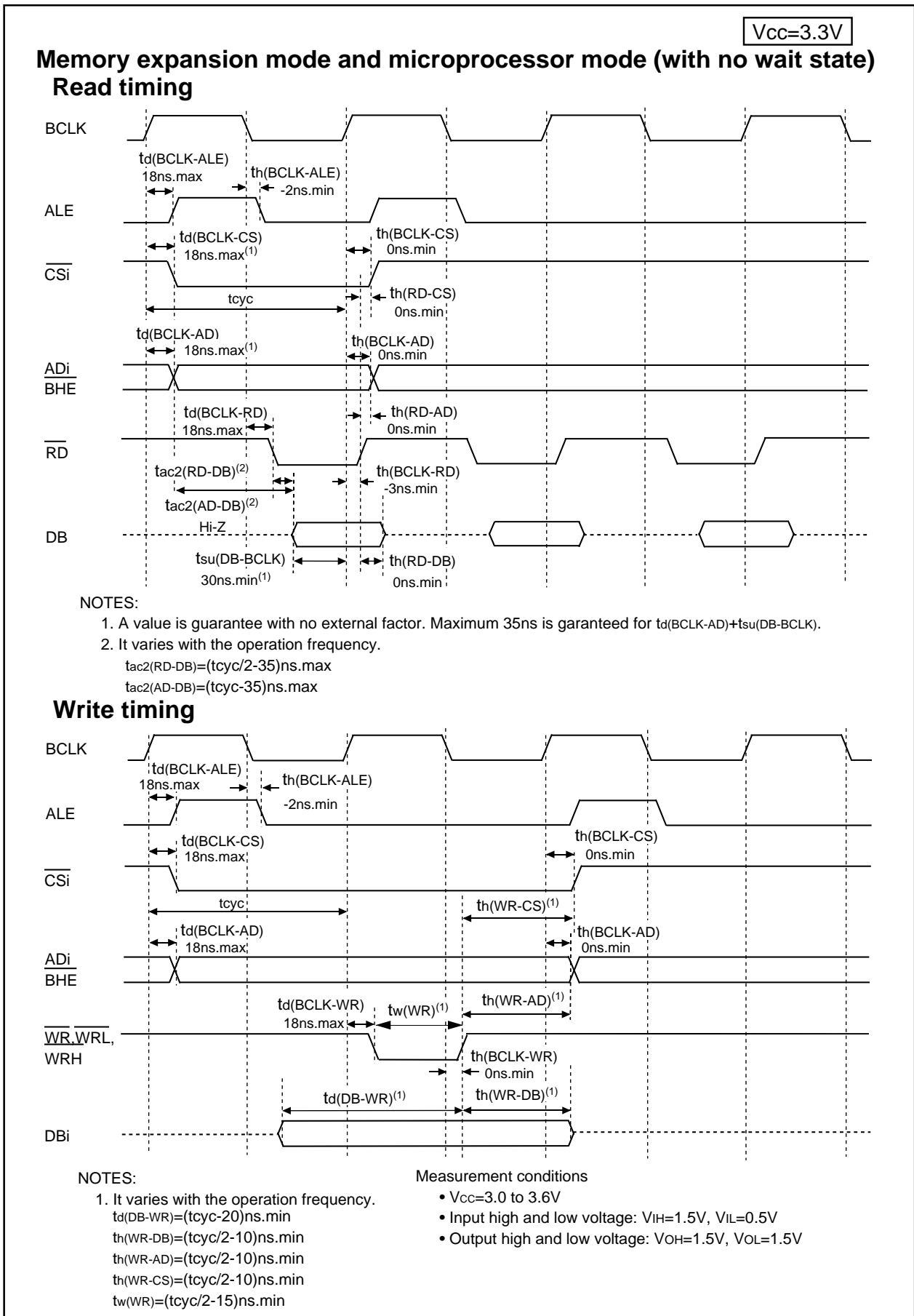


Figure 5.10 Vcc=3.3V Timing Diagram (1)

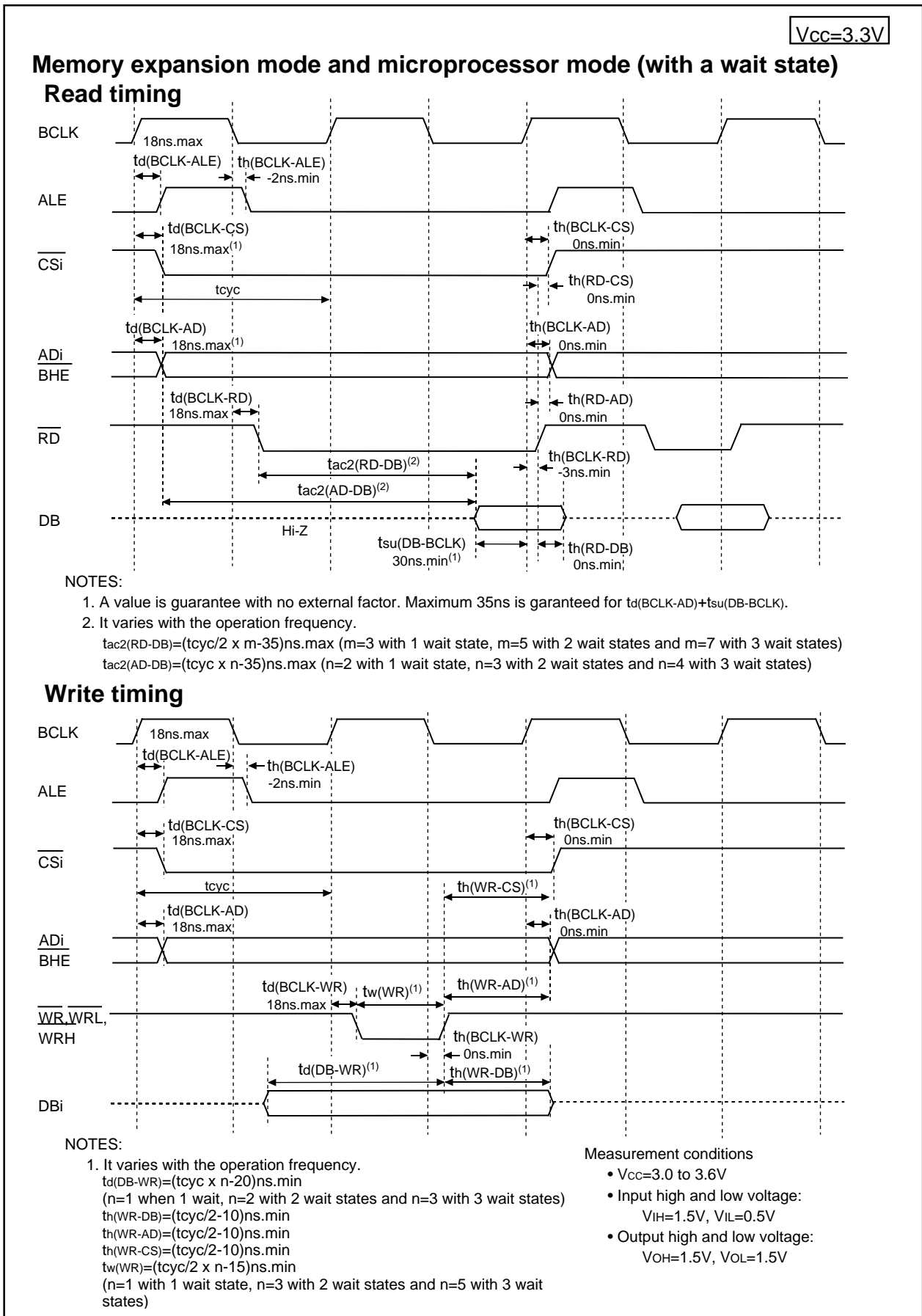


Figure 5.11 V_{CC}=3.3V Timing Diagram (2)

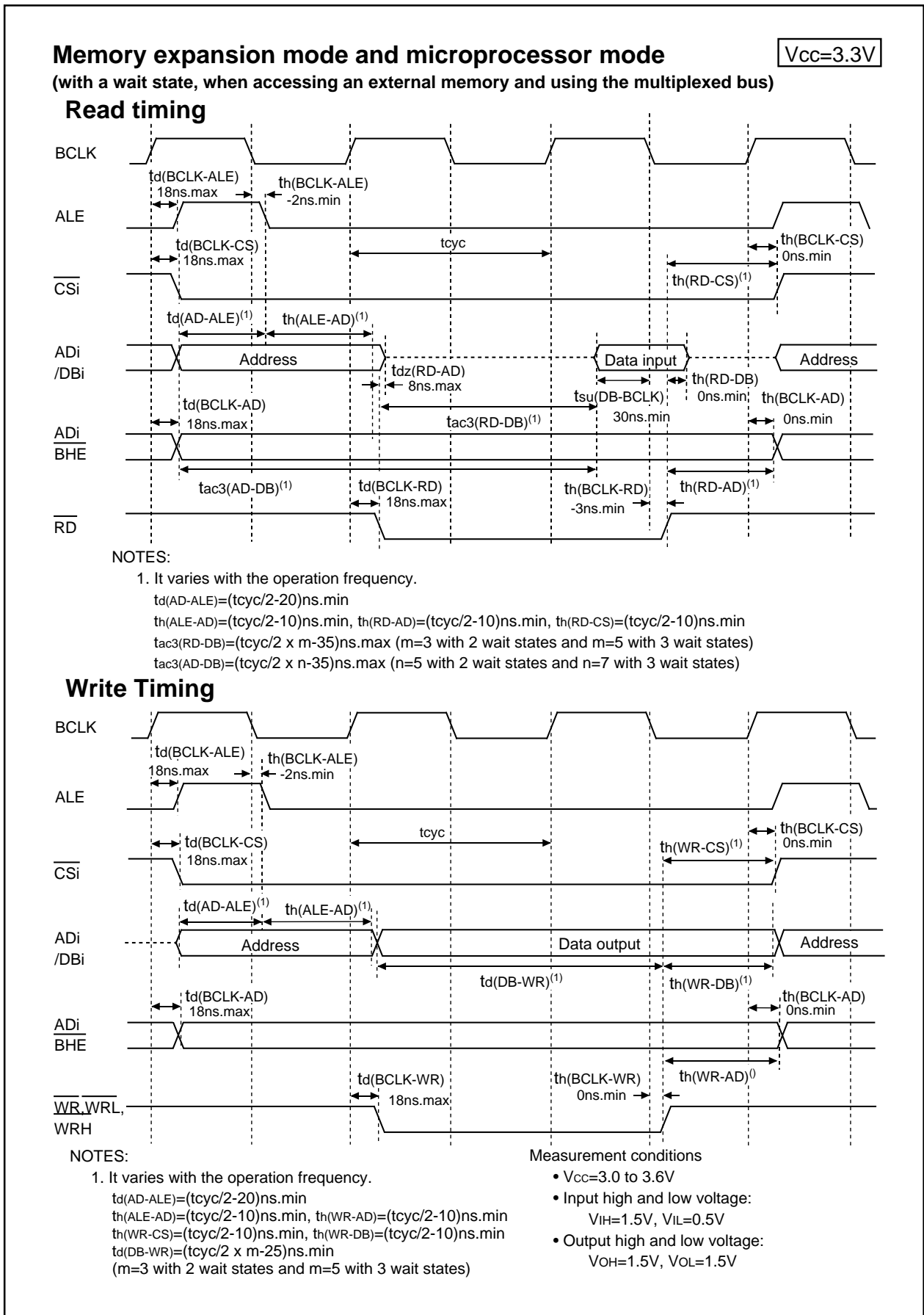


Figure 5.12 Vcc=3.3V Timing Diagram (3)

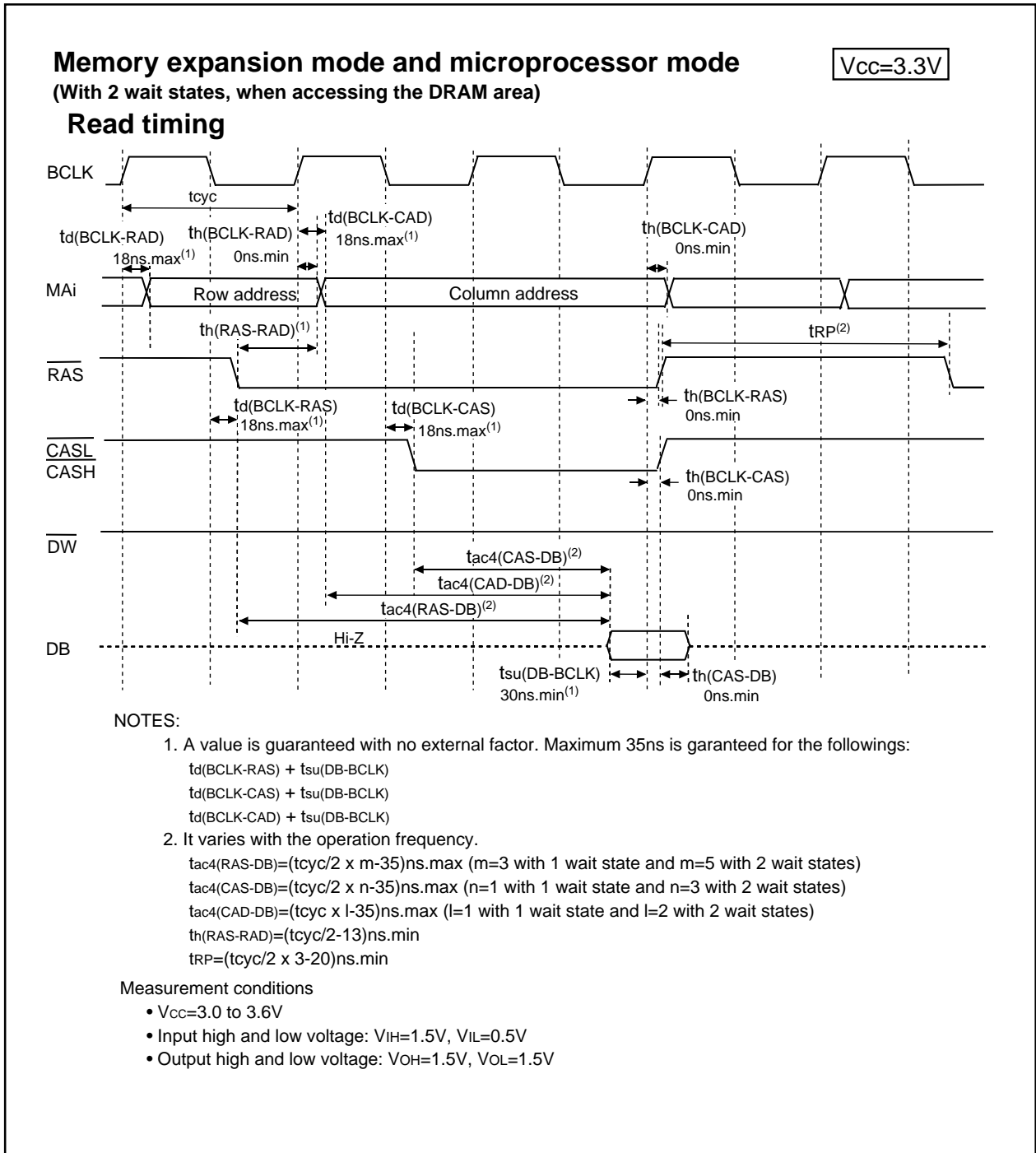


Figure 5.13 V_{CC}=3.3V Timing Diagram (4)

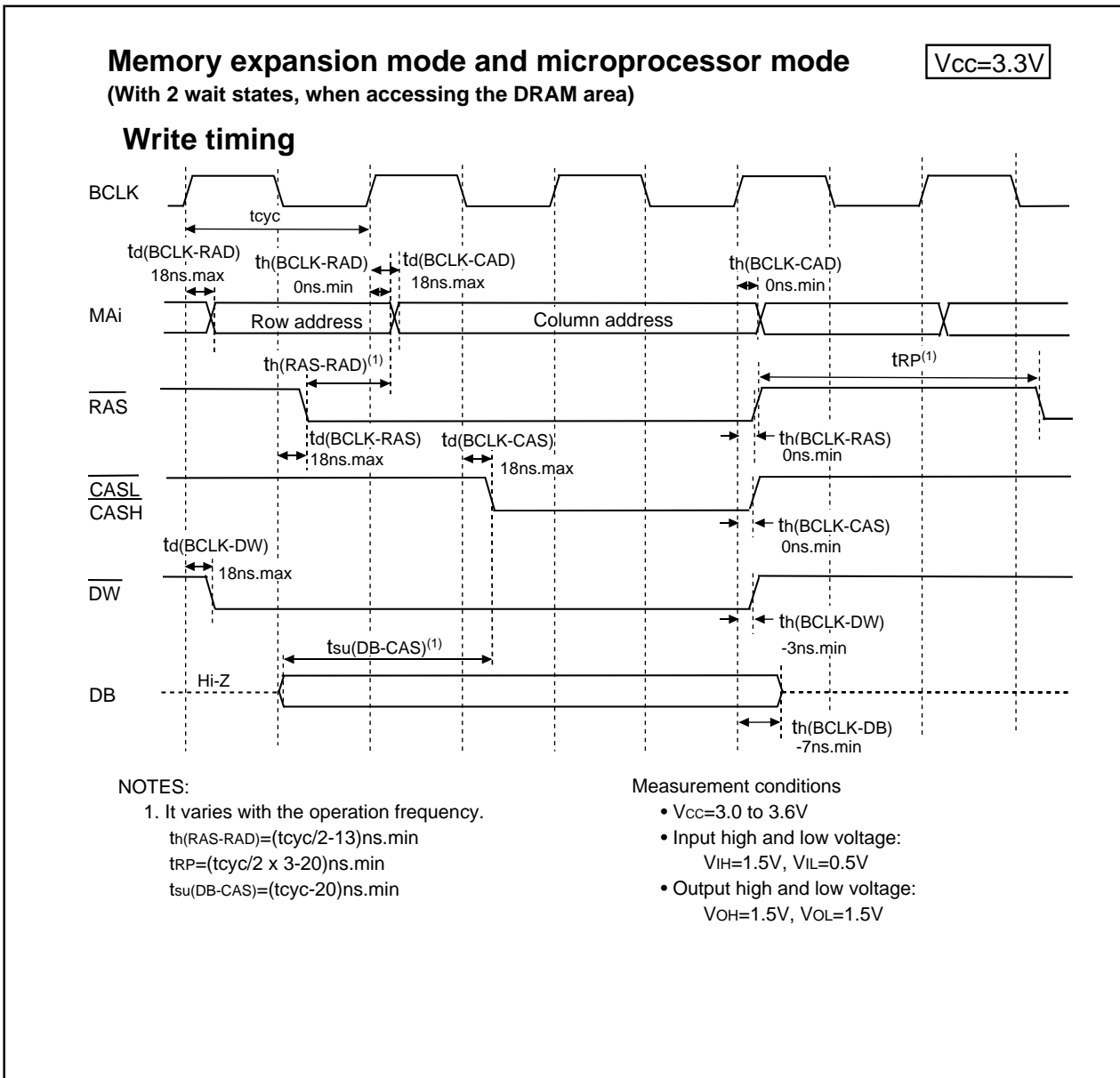


Figure 5.14 V_{CC}=3.3V Timing Diagram (5)

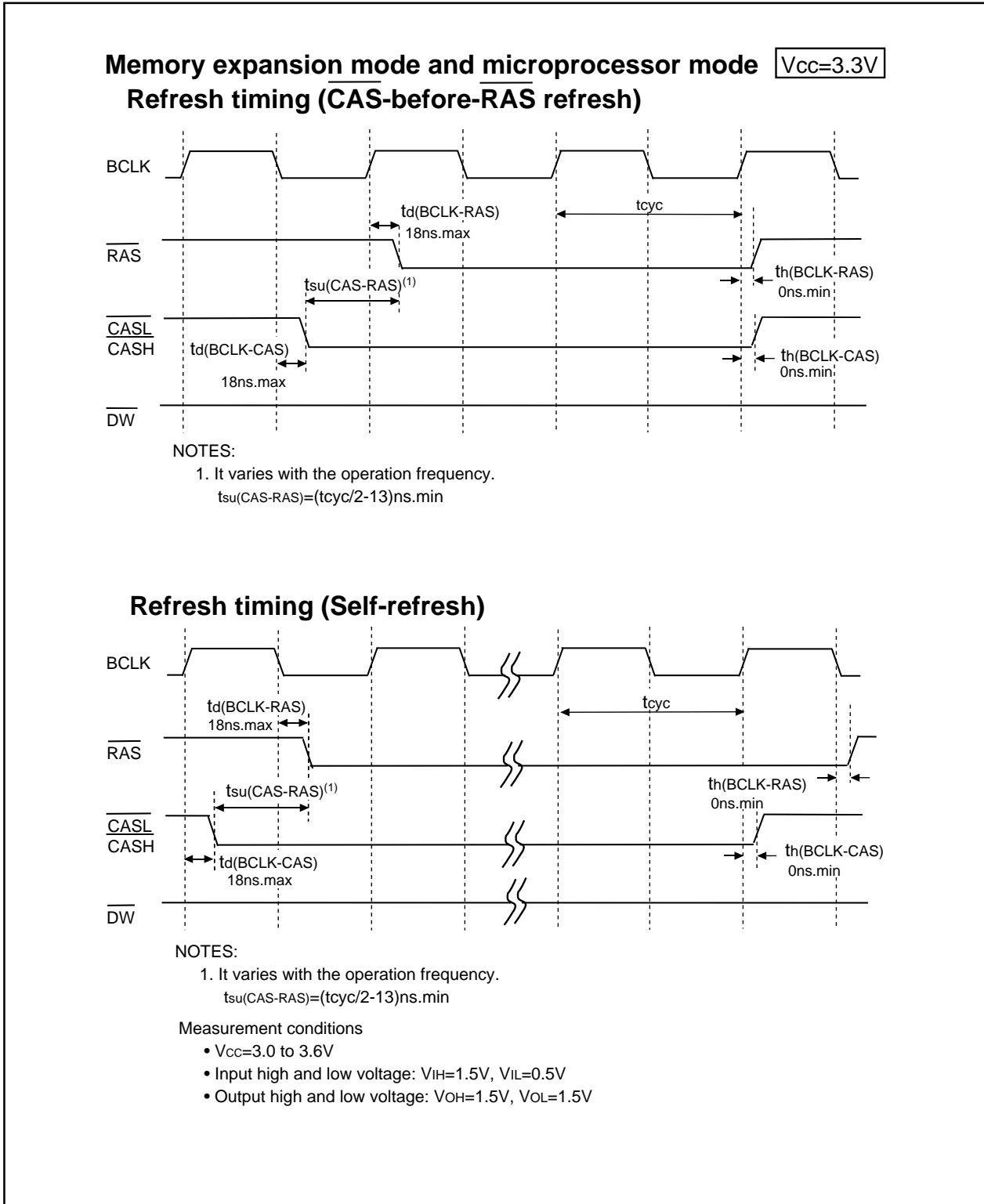


Figure 5.15 V_{CC}=3.3V Timing Diagram (6)

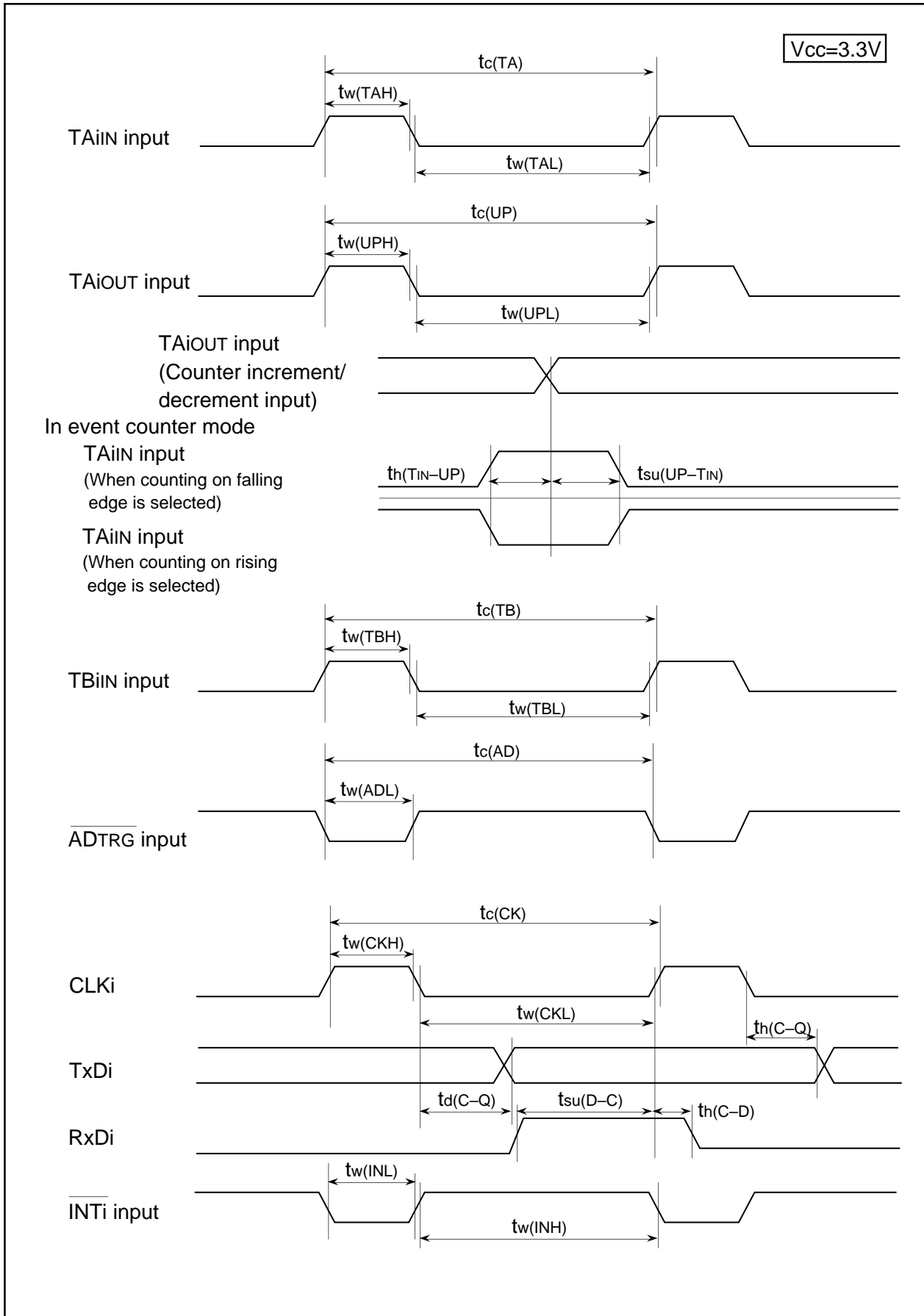


Figure 5.16 V_{CC}=3.3V Timing Diagram (7)

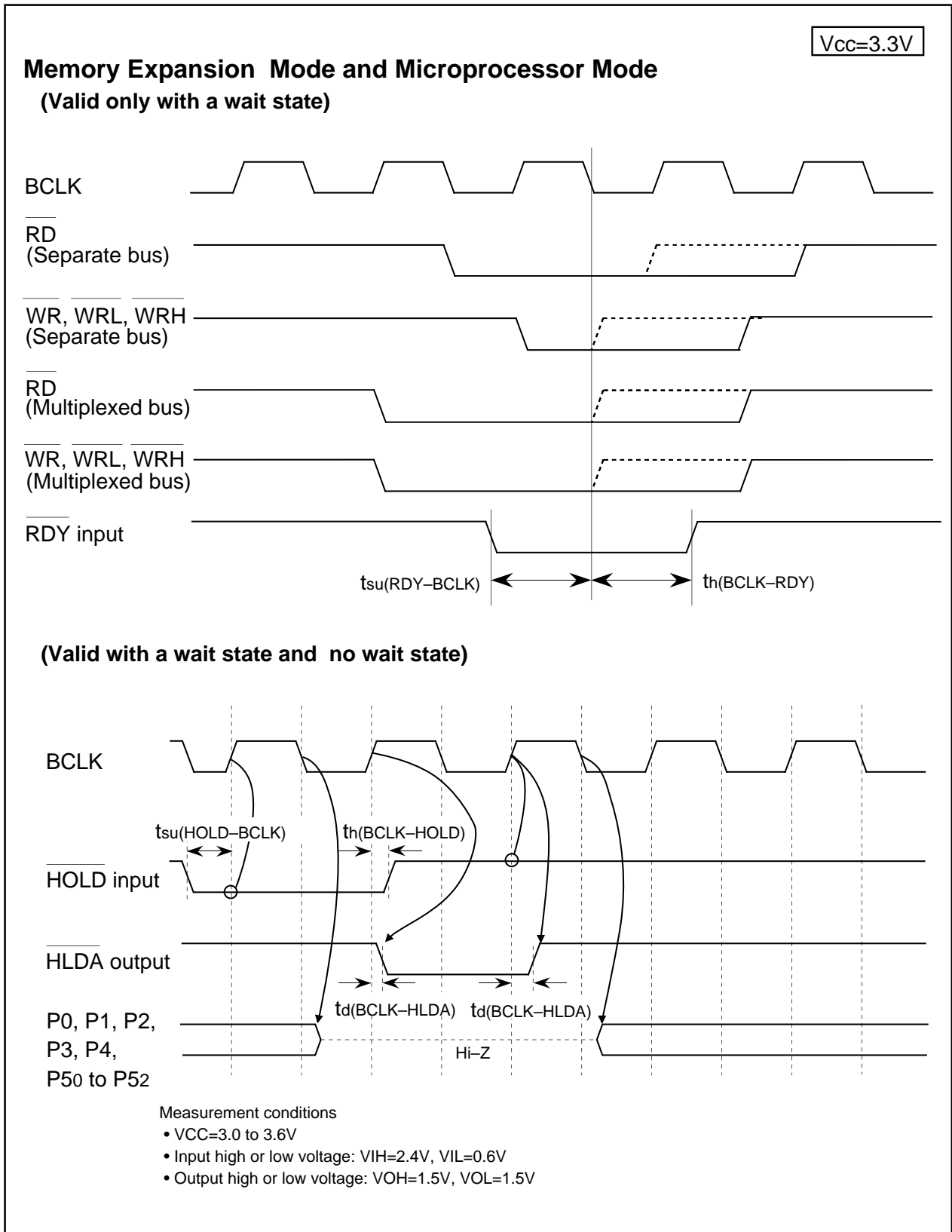


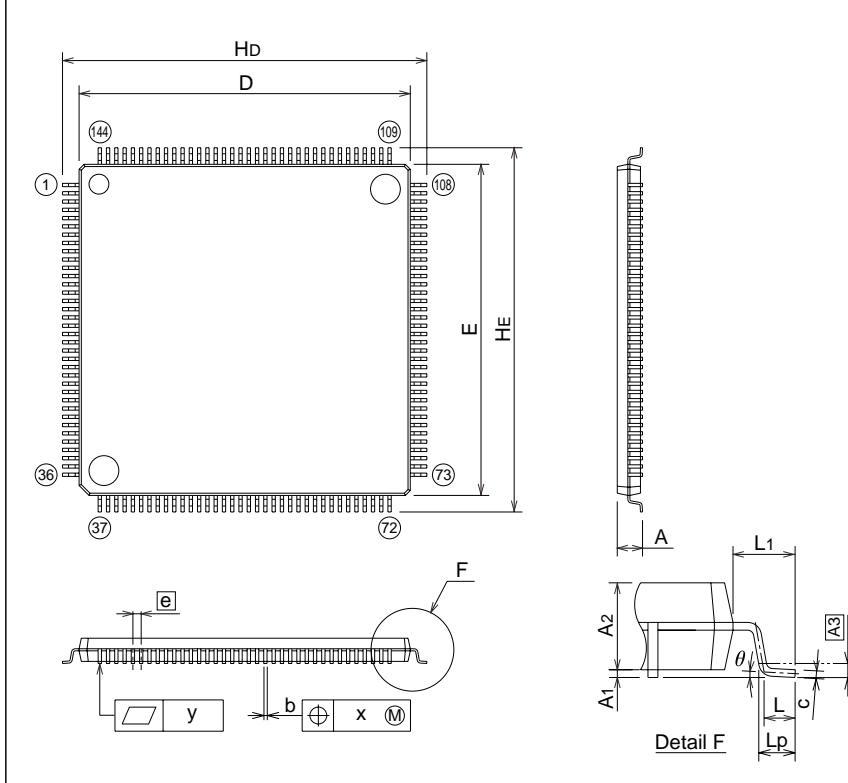
Figure 5.17 V_{CC}=3.3V Timing Diagram (8)

Package Dimensions

144P6Q-A Recommended

Plastic 144pin 20X20mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP144-P-2020-0.50	-	1.23	Cu Alloy

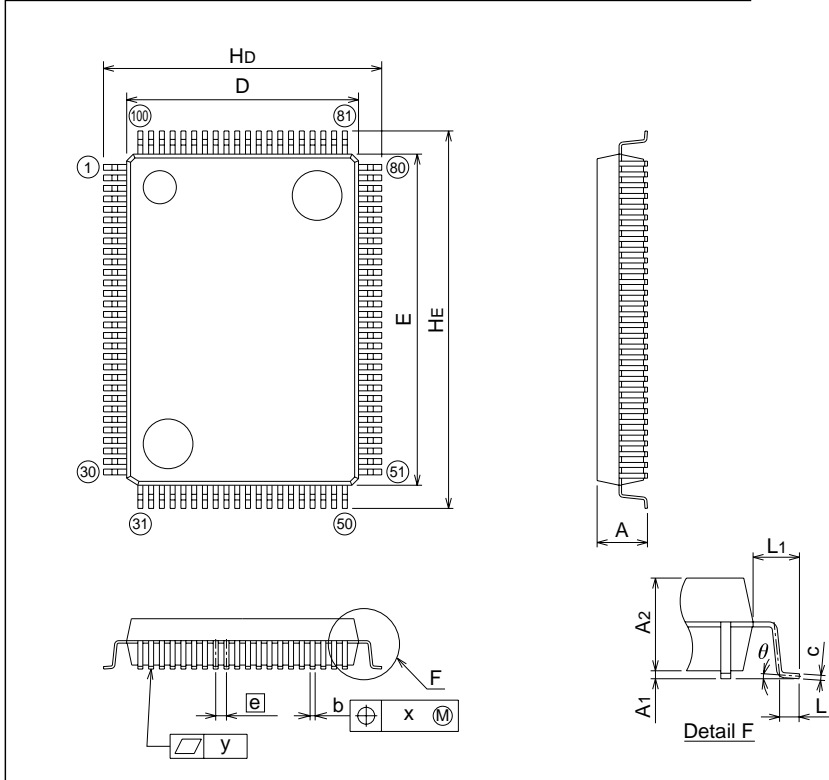


Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	1.7
A1	0.05	0.125	0.2
A2	-	1.4	-
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	19.9	20.0	20.1
E	19.9	20.0	20.1
e	-	0.5	-
Hd	21.8	22.0	22.2
HE	21.8	22.0	22.2
L	0.35	0.5	0.65
L1	-	1.0	-
Lp	0.45	0.6	0.75
A3	-	0.25	-
x	-	-	0.08
y	-	-	0.1
θ	0°	-	8°
b2	-	0.225	-
l2	0.95	-	-
MD	-	20.4	-
ME	-	20.4	-

100P6S-A Recommended

Plastic 100pin 14X20mm body QFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
QFP100-P-1420-0.65	-	1.58	Alloy 42

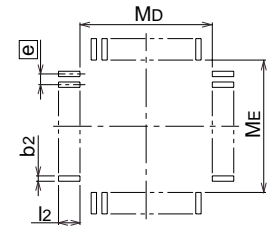
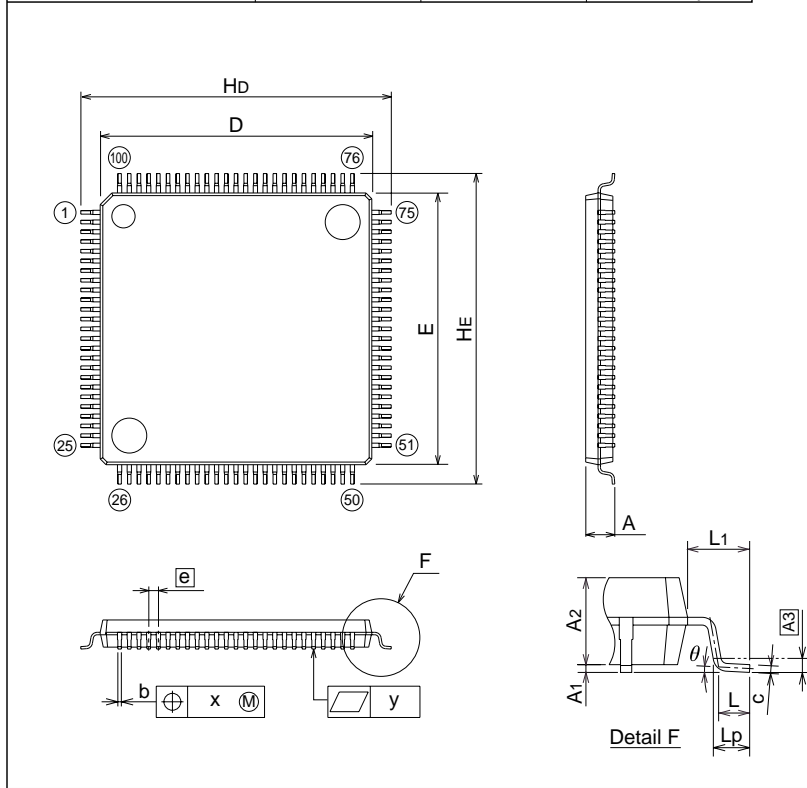


Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	3.05
A1	0	0.1	0.2
A2	-	2.8	-
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	13.8	14.0	14.2
E	19.8	20.0	20.2
e	-	0.65	-
Hd	16.5	16.8	17.1
HE	22.5	22.8	23.1
L	0.4	0.6	0.8
L1	-	1.4	-
x	-	-	0.13
y	-	-	0.1
θ	0°	-	10°
b2	-	0.35	-
l2	1.3	-	-
MD	-	14.6	-
ME	-	20.6	-

100P6Q-A Recommended

Plastic 100pin 14X14mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP100-P-1414-0.50	-	0.63	Cu Alloy



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	1.7
A1	0	0.1	0.2
A2	-	1.4	-
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	13.9	14.0	14.1
E	13.9	14.0	14.1
e	-	0.5	-
Hd	15.8	16.0	16.2
HE	15.8	16.0	16.2
L	0.3	0.5	0.7
L1	-	1.0	-
Lp	0.45	0.6	0.75
A3	-	0.25	-
x	-	-	0.08
y	-	-	0.1
θ	0°	-	10°
b2	-	0.225	-
l2	0.9	-	-
MD	-	14.4	-
ME	-	14.4	-

REVISION HISTORY

M32C/82 Group Short Sheet/Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	15/07/2003	-	New Document
1.10	30/09/2003	2 3 to 4 11,15 17,18 18 20 SFR 28 42	Overview - "1.2 Difference between the M32C/82 Group and the M32C/83 Group" has been added. - "DRAMC" and "Oscillator stop detect function" have been added to Tables 1.1 and 1.2 - VREF pin has been changed from analog input pin to control pin. - SDA0 to SDA4 pins have been changed from output pins to I/O pins. - Description of intelligent I/O has been modified. - BEIN and BEOUT pins have been modified to IEIN and IEOUT pins in port P13. SFR - Value after RLVL register reset has been modified. Electrical Characteristics - Maximum value of sub clock oscillation frequency has been added in Table 5.2.
1.20	Jun. 01, 2004	All pages	Words standardized: On-chip oscillator, A/D converter and D/A converter

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.

The information described here may contain technical inaccuracies or typographical errors.

Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.

Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).

4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
 5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
 6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
 7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
 8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.
-



RENESAS SALES OFFICES

<http://www.renesas.com>

Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH

Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.

7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.

FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.

26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.

1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001