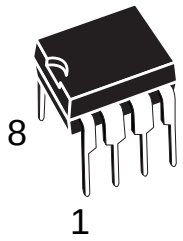
M34C02

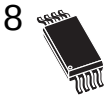
2 Kbit Serial I²C Bus EEPROM For DIMM Serial Presence Detect

- Two Wire I^2C Serial Interface Supports 400 kHz Protocol
- Single Supply Voltage:
  - 2.5V to 5.5V for M34C02-W
  - 2.2V to 5.5V for M34C02-L
- Software Data Protection for lower 128 bytes
- BYTE and PAGE WRITE (up to 16 bytes)
- RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Protection
- 1 Million Erase/Write Cycles (minimum)
- 40 Year Data Retention (minimum)



PSDIP8 (BN)
0.25 mm frame

SO8 (MN)
150 mil width



TSSOP8 (DW)
169 mil width

DESCRIPTION

The M34C02 is a 2 Kbit serial EEPROM memory able to lock permanently the data in its first half (from location 00h to 7Fh). This facility has been designed specifically for use in DRAM DIMMs (dual interline memory modules) with Serial Presence Detect. All the information concerning the DRAM module configuration (such as its access speed, its size, its organization) can be kept write protected in the first half of the memory.

This bottom half of the memory area can be write-protected using a specially designed software write protection mechanism. By sending the device a specific sequence, the first 128 bytes of

Table 1. Signal Names

E0, E1, E2	Chip Enable Inputs
SDA	Serial Data/Address Input/ Output
SCL	Serial Clock
$\overline{WC}$	Write Control
V_{CC}	Supply Voltage
V_{SS}	Ground

Figure 1. Logic Diagram

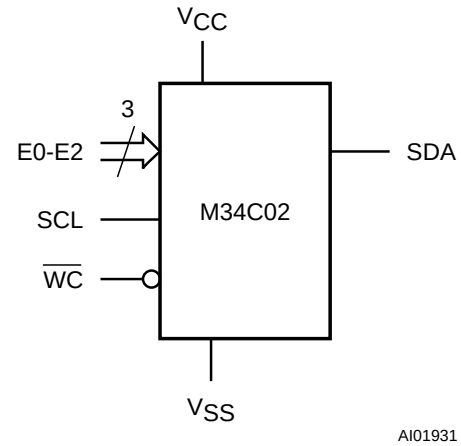


Figure 2A. DIP Connections

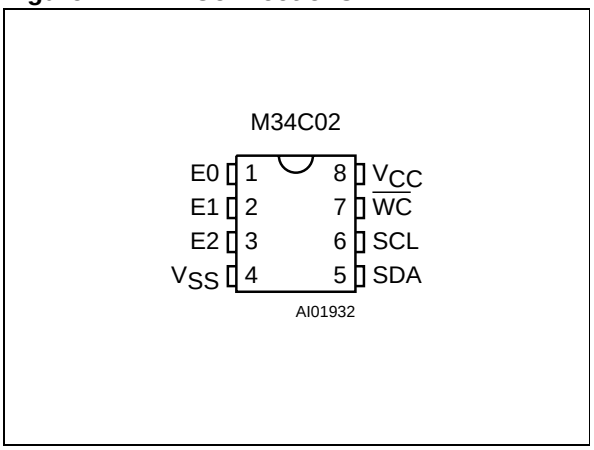
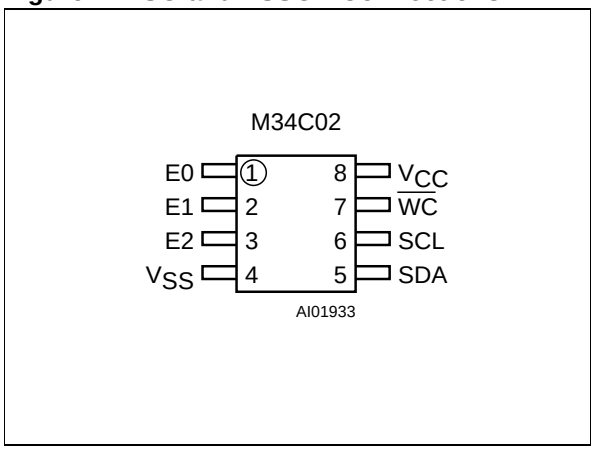


Figure 2B. SO and TSSOP Connections



the memory become permanently write protected. Care must be taken when using this sequence as its effect cannot be reversed. In addition, the device allows the entire memory area to be write protected, using the $\overline{WC}$ input (for example by tieing this input to V_{CC}).

The M34C02 is a 2 Kbit electrically erasable programmable memory (EEPROM), organized as 256x8 bits, fabricated with STMicroelectronics' High Endurance, Advanced, CMOS technology. This guarantees an endurance typically well above one million Erase/Write cycles, with a data retention of 40 years. These memory devices operate with a power supply down to 2.2 V for the M34C02-L.

The M34C02 is available in Plastic Dual In-line, Plastic Small Outline and Thin Shrink Small Outline packages.

These memory devices are compatible with the I^2C memory standard. This is a two wire serial interface that uses a bi-directional data bus and serial clock. The memory carries a built-in 4-bit Device Type Identifier code (1010) in accordance with the I^2C bus definition to access the memory area and a second Device Type Identifier Code (0110) to access the Protection Register. These codes are used together with three chip enable inputs (E2, E1, E0) so that up to eight 2 Kbit devices may be attached to the I²C bus and selected individually.

The memory behaves as a slave device in the I^2C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a START condition, generated by the bus master. The START condition is followed by a Device Select Code and $\overline{RW}$ bit (as described in Table 3), terminated by an acknowledge bit.

When writing data to the memory, the memory inserts an acknowledge bit during the 9^{th} bit time, following the bus master's 8-bit transmission.

Table 2. Absolute Maximum Ratings [1]

Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		-40 to 85	°C
T_{STG}	Storage Temperature		-65 to 150	°C
T_{LEAD}	Lead Temperature during Soldering	PSDIP8: 10 sec SO8: 40 sec TSSOP8: 40 sec	260 215 215	°C
V_{IO}	Input or Output range		-0.6 to 6.5	V
V_{CC}	Supply Voltage		-0.3 to 6.5	V
V_{ESD}	Electrostatic Discharge Voltage (Human Body model) [2]		4000	V

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents.
2. MIL-STD-883C, 3015.7 (100 pF, 1500 Ω)

When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way. Data transfers are terminated by a STOP condition after an Ack for WRITE, and after a NoAck for READ.

Power On Reset: V_{CC} Lock-Out Write Protect

In order to prevent data corruption and inadvertent write operations during power up, a Power On Reset (POR) circuit is included. The internal reset is held active until the V_{CC} voltage has reached the POR threshold value, and all operations are disabled – the device will not respond to any command. In the same way, when V_{CC} drops from the operating voltage, below the POR threshold value, all operations are disabled and the device will not respond to any command. A stable and valid V_{CC} must be applied before applying any logic signal.

SIGNAL DESCRIPTION

Serial Clock (SCL)

The SCL input pin is used to strobe all data in and out of the memory. In applications where this line is used by slaves to synchronize the bus to a slower clock, the master must have an open drain output, and a pull-up resistor must be connected from the SCL line to V_{CC}. (Figure 3 indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the master has a push-pull (rather than open drain) output.

Serial Data (SDA)

The SDA pin is bi-directional, and is used to transfer data in or out of the memory. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from the SDA bus to V_{CC}. (Figure 3 indicates how the value of the pull-up resistor can be calculated).

Chip Enable (E2, E1, E0)

These chip enable inputs are used to set the value that is to be looked for on the three least significant bits (b3, b2, b1) of the 7-bit device select code. These inputs may be driven dynamically or tied to V_{CC} or V_{SS} to establish the device select code.

Write Control ($\overline{WC}$)

A hardware Write Control ($\overline{WC}$, pin 7) is provided for protecting the contents of the whole memory from erroneous erase/write cycles. The Write Control signal is used to enable ($\overline{WC}$=V_{IL}) or disable ($\overline{WC}$=V_{IH}) write instructions to the entire memory area or to the Protection Register.

When $\overline{WC}$ is tied to V_{SS} or left unconnected, the write protection of the first half of the memory is determined by the status of the Protection Register.

DEVICE OPERATION

The memory device supports the I^2C protocol. This is summarized in Figure 4. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the master, and the other as the slave. A data transfer can only be initiated by the master, which will also provide the serial clock for synchronization. The memory device is always a slave device in all communication.

Figure 3. Maximum R_L Value versus Bus Capacitance (C_{BUS}) for an I^2C Bus

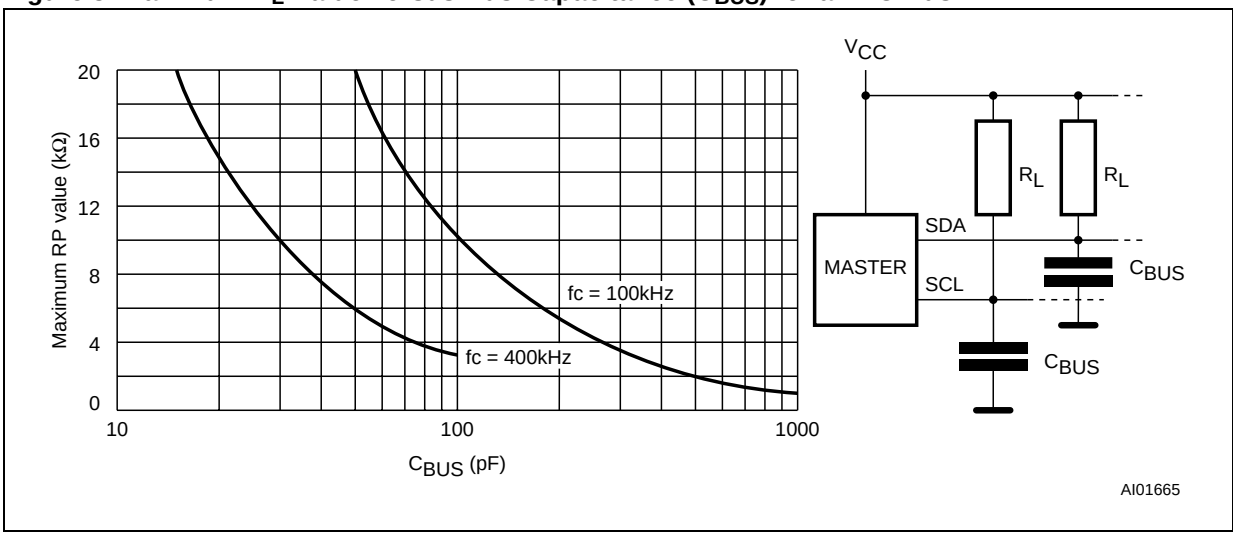
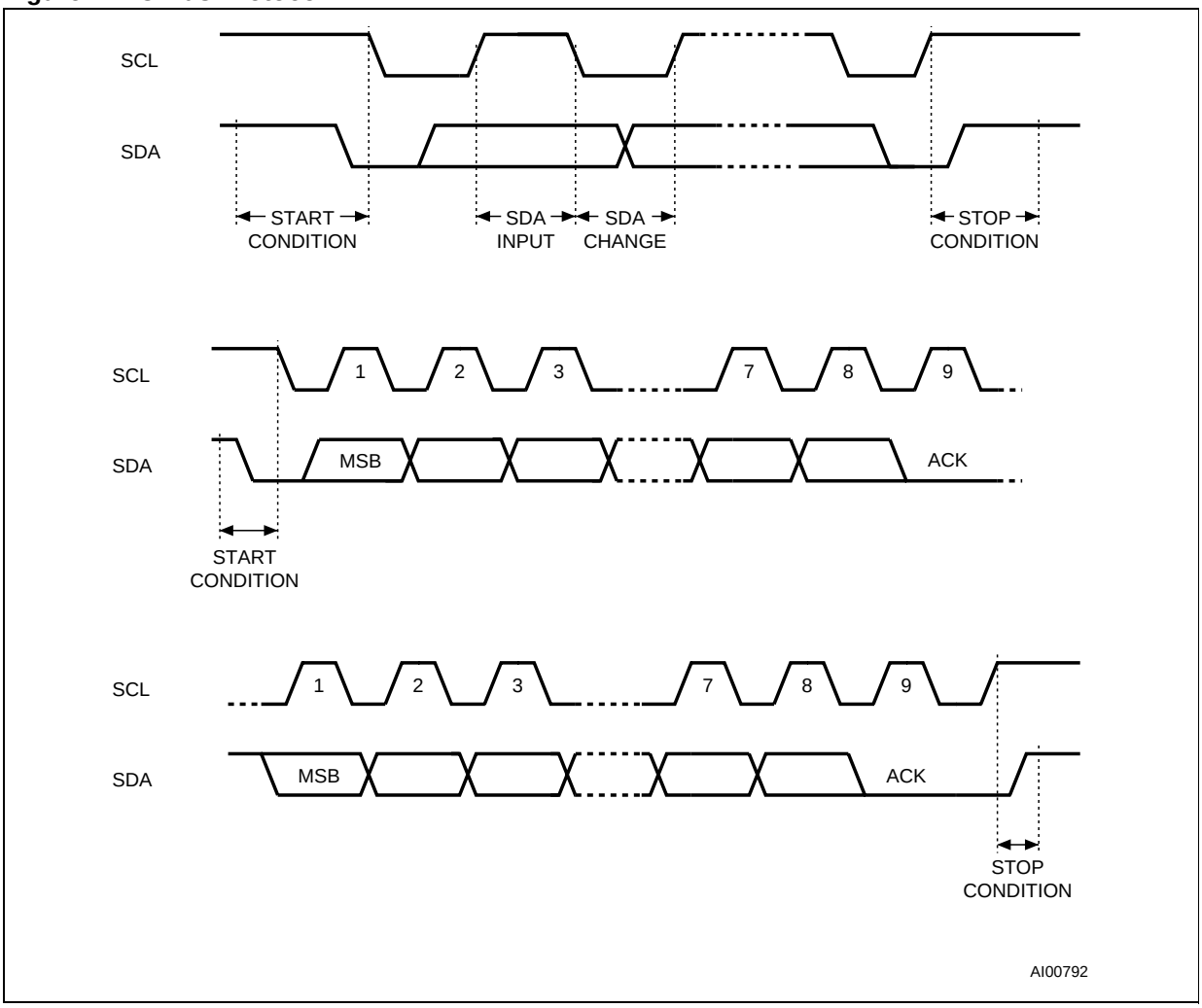


Figure 4. I²C Bus Protocol



Start Condition

START is identified by a high to low transition of the SDA line while the clock, SCL, is stable in the high state. A START condition must precede any data transfer command. The memory device continuously monitors (except during a programming cycle) the SDA and SCL lines for a START condition, and will not respond unless one is given.

Stop Condition

STOP is identified by a low to high transition of the SDA line while the clock SCL is stable in the high state. A STOP condition terminates communication between the memory device and the bus master. A STOP condition at the end of a Read command, provided that it is followed by a NoAck, forces the memory device into its standby state. A STOP condition at the end of a Write

Table 3. Device Select Code [1]

	Device Type Identifier				Chip Enable			$R\overline{W}$
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays)	1	0	1	0	E2	E1	E0	$R\overline{W}$
Protection Register Select Code	0	1	1	0	E2	E1	E0	$R\overline{W}$

Note: 1. The most significant bit (b7) is sent first.

Table 4. Operating Modes

Mode	R$\overline{W}$ bit	$\overline{WC}$ [1]	Bytes	Initial Sequence
Current Address Read	1	X	1	START, Device Select, R$\overline{W}$ = '1'
Random Address Read	0	X	1	START, Device Select, R$\overline{W}$ = '0', Address
	1	X		reSTART, Device Select, R$\overline{W}$ = '1'
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	START, Device Select, R$\overline{W}$ = '0'
Page Write	0	V_{IL}	≤ 16	START, Device Select, R$\overline{W}$ = '0'

Note: 1. X = V_{IH} or V_{IL}.

command triggers the internal EEPROM write cycle.

Acknowledge Bit (ACK)

An acknowledge signal is used to indicate a successful byte transfer. The bus transmitter, whether it be master or slave, releases the SDA bus after sending eight bits of data. During the 9th clock pulse period, the receiver pulls the SDA bus low to acknowledge the receipt of the eight data bits.

Data Input

During data input, the memory device samples the SDA bus signal on the rising edge of the clock, SCL. For correct device operation, the SDA signal must be stable during the clock low-to-high transition, and the data must change *only* when the SCL line is low.

Memory Addressing

To start communication between the bus master and the slave memory, the master must initiate a START condition. Following this, the master sends the 8-bit byte, shown in Table 3, on the SDA bus line (most significant bit first). This consists of the 7-bit Device Select Code, and the 1-bit Read/Write Designator (R$\overline{W}$). The Device Select Code is further subdivided into: a 4-bit Device Type Identifier, and a 3-bit Chip Enable "Address" (E2, E1, E0).

To address the memory array, the 4-bit Device Type Identifier is 1010b. To address the Protection Register, it is 0110b.

If all three chip enable inputs are connected, up to eight memory devices can be connected on a single I^2C bus. Each one is given a unique 3-bit code on its Chip Enable inputs. When the Device Select Code is received on the SDA bus, the memory only responds if the Chip Select Code is the same as the pattern applied to its Chip Enable pins.

The 8th bit is the read or write bit (R$\overline{W}$). This bit is set to '1' for read and '0' for write operations. If a match occurs on the Device Select Code, the corresponding memory gives an acknowledgment on the SDA bus during the 9th bit time. If the memory does not match the Device Select code, it will deselect itself from the bus, and go into stand-by mode.

Write Operations

Following a START condition the master sends a Device Select Code with the R$\overline{W}$ bit set to '0', as shown in Table 4. The memory acknowledges this, and waits for an address byte. The memory responds to the address byte with an acknowledge bit, and then waits for the data byte.

Writing to the memory may be inhibited if the $\overline{WC}$ input pin is taken high.

Byte Write

In the Byte Write mode, after the Device Select Code and the address byte, the master sends one data byte. If the addressed location is in a write protected area, the memory replies with a NoAck, and the location is not modified. If, instead, the addressed location is not in a write protected area, the memory replies with an Ack. The master terminates the transfer by generating a STOP condition.

Page Write

The Page Write mode allows up to 16 bytes to be written in a single write cycle, provided that they are all located in the same 'row' in the memory: that is the most significant memory address bits (b7-b4) are the same. If more bytes are sent than will fit up to the end of the row, a condition known as 'roll-over' occurs. Data starts to become overwritten (in a way not formally specified in this data sheet).

The master sends from one up to 16 bytes of data, each of which is acknowledged by the memory if the $\overline{WC}$ pin is low. If the $\overline{WC}$ pin is high, the contents of the addressed memory location are not modified. After each byte is transferred, the internal byte address counter (the 4 least

Figure 5. How to Set the Write Protection

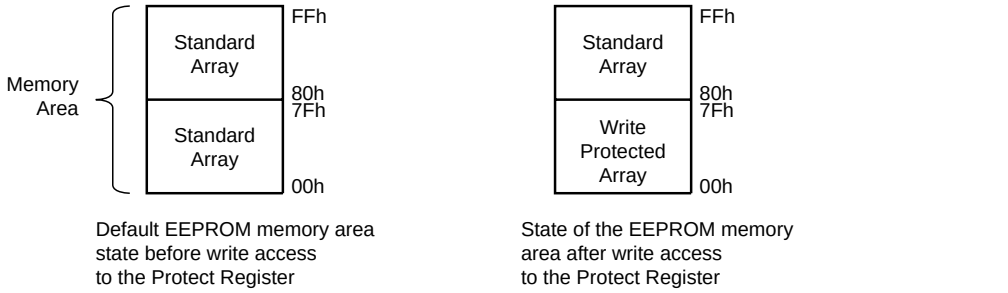
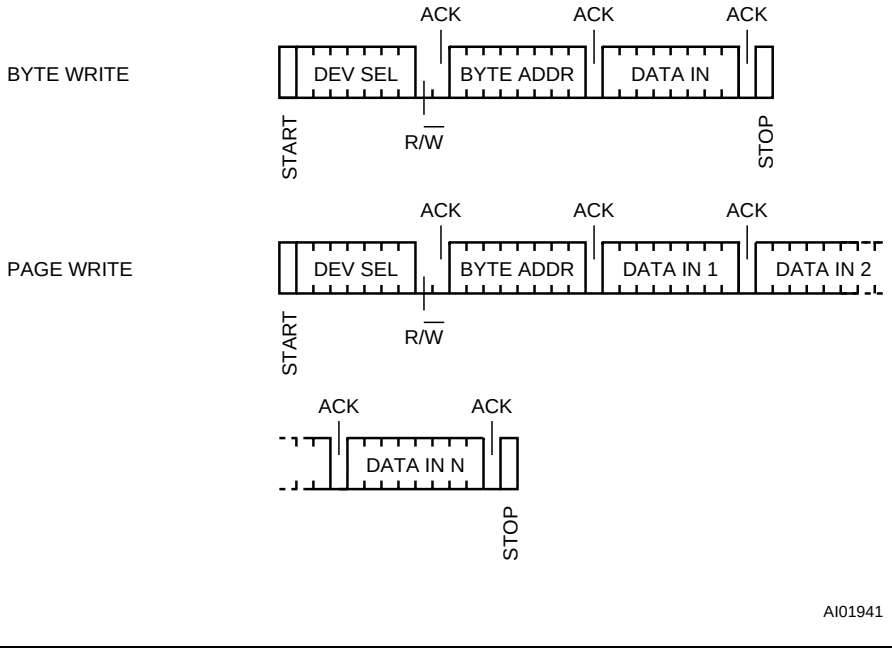


Figure 6. Write Mode Sequences in the Non Write-Protected Area



significant bits only) is incremented. The transfer is terminated by the master generating a STOP condition.

When the master generates a STOP condition immediately after the Ack bit (in the "10th bit" time slot), either at the end of a byte write or a page write, the internal memory write cycle is triggered. A STOP condition at any other time does not trigger the internal write cycle.

During the internal write cycle, the SDA input is disabled internally, and the device does not respond to any requests.

Minimizing System Delays by Polling On ACK

During the internal write cycle, the memory disconnects itself from the bus, and copies the data from its internal latches to the memory cells. The maximum write time (t_W) is shown in Table 9, but the typical time is shorter. To make use of this, an Ack polling sequence can be used by the master.

Figure 7. Write Cycle Polling Flowchart using ACK

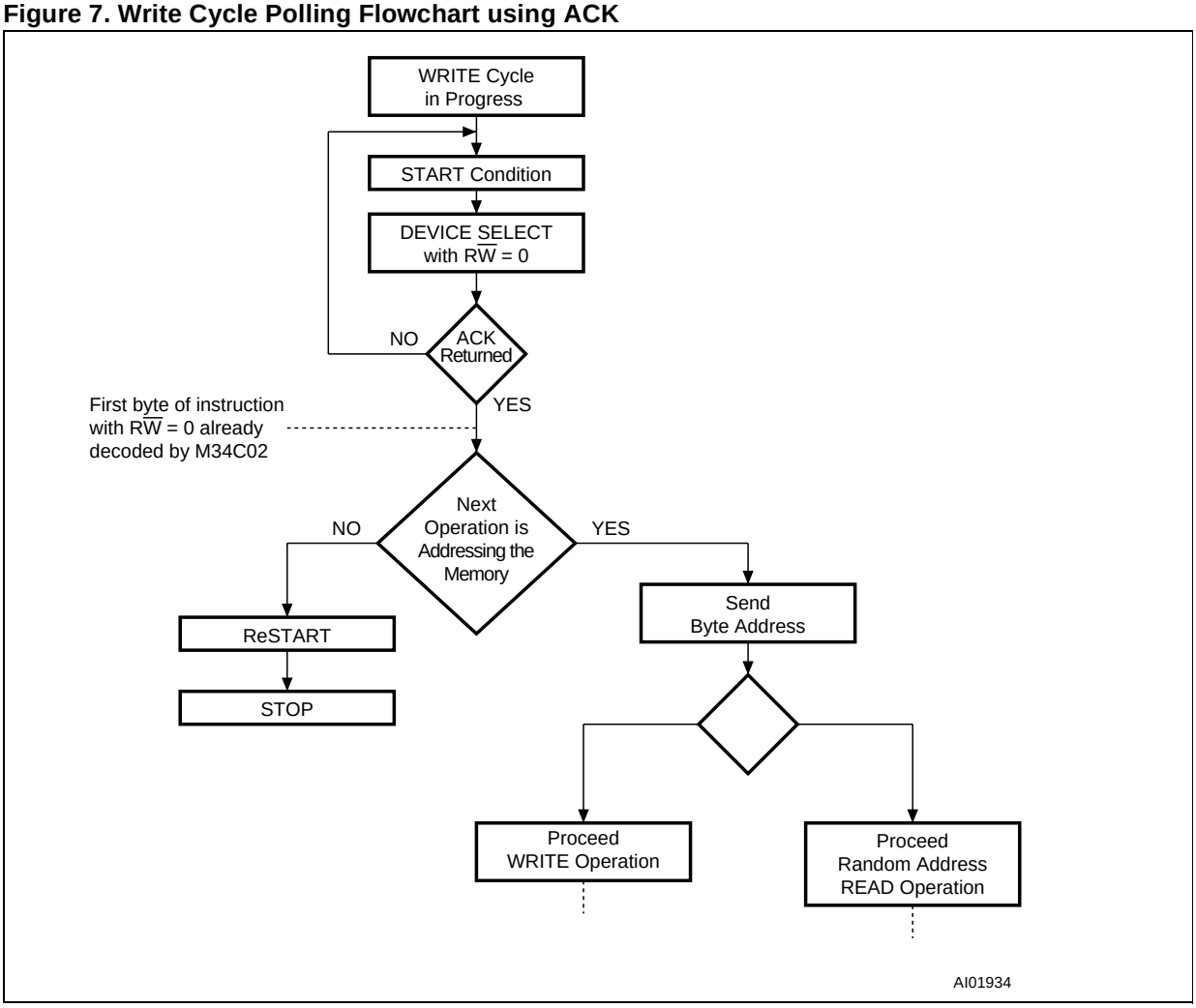
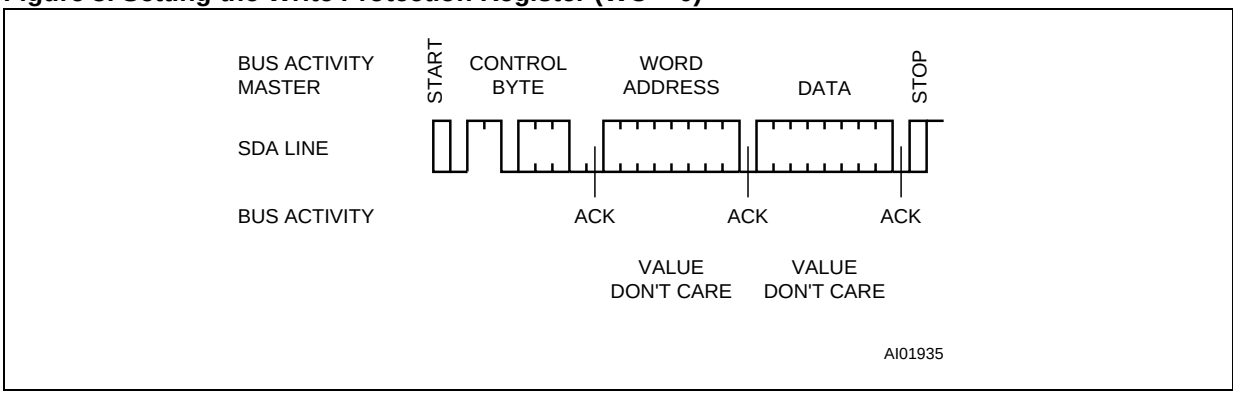


Figure 8. Setting the Write Protection Register ($\overline{WC}$ = 0)



The sequence, as shown in Figure 7, is:

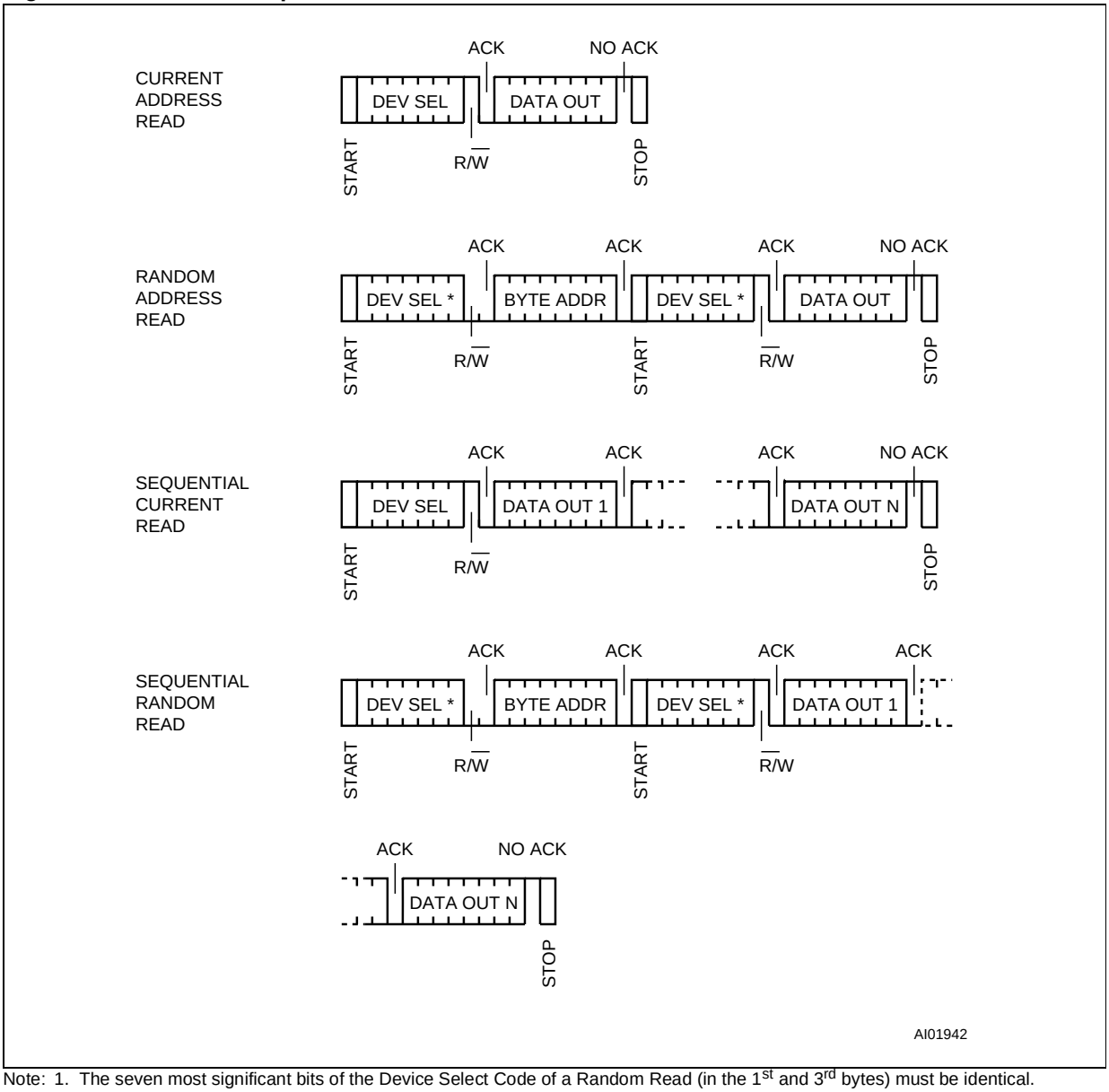
– Initial condition: a Write is in progress.
– Step 1: the master issues a START condition followed by a Device Select Code (the first byte of the new instruction).
– Step 2: if the memory is busy with the internal write cycle, no Ack will be returned and the master goes back to Step 1. If the memory has terminated the internal write cycle, it responds with an Ack, indicating that the memory is ready to receive the second part of the next instruction (the first byte of this instruction having been sent during Step 1).

Setting the Protection, Using the Protection Register

The M34C02 has a software write-protection function, using the Protecton Register, that allows the bottom half of the memory area (addresses 00h to 7Fh) to be permanently write protected. The write protection feature is activated by writing once to the Protection Register (with the $\overline{WC}$ input held at V_{SS}).

The Protection Register is accessed with the device select code set to 0110b (as shown in Table 3), and the E2-E1-E0 bits set according to the states being applied to the E2-E1-E0 pins. As

Figure 9. Read Mode Sequences



Note: 1. The seven most significant bits of the Device Select Code of a Random Read (in the 1st and 3rd bytes) must be identical.

for any other write command, the $\overline{WC}$ input needs to be held at V_{SS}. Address and data bytes must be sent with this command, but their values are all ignored, and are treated as Don't Care. Once the Protection Register has been written, the write protection of the first 128 bytes of the memory is enabled, and it is not possible to unprotect these 128 bytes, even if the device is powered off and on, and regardless the state of the $\overline{WC}$ input.

When the Protection Register has been written, the M34C02 no longer responds to the device type identifier 0110b in either read or write mode.

Read Operations

Read operations are performed independently of the state of the $\overline{WC}$ pin.

Random Address Read

A dummy write is performed to load the address into the address counter, as shown in Figure 9. Then, *without* sending a STOP condition, the master sends another START condition, and repeats the Device Select Code, with the $\overline{RW}$ bit set to '1'. The memory acknowledges this, and outputs the contents of the addressed byte. The master must *not* acknowledge the byte output, and terminates the transfer with a STOP condition.

Current Address Read

The device has an internal address counter which is incremented each time a byte is read. For the Current Address Read mode, following a START condition, the master sends a Device Select Code with the $\overline{RW}$ bit set to '1'. The memory acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The master terminates the transfer with a STOP condition, as shown in Figure 9, *without* acknowledging the byte output.

Table 5. 168 Pin DRAM DIMM Connections

DIMM Position	E2 (pin 167)	E1 (pin 166)	E0 (pin 165)
0	V_{SS}	V_{SS}	V_{SS}
1	V_{SS}	V_{SS}	V_{CC}
2	V_{SS}	V_{CC}	V_{SS}
3	V_{SS}	V_{CC}	V_{CC}
4	V_{CC}	V_{SS}	V_{SS}
5	V_{CC}	V_{SS}	V_{CC}
6	V_{CC}	V_{CC}	V_{SS}
7	V_{CC}	V_{CC}	V_{CC}

Sequential Read

This mode can be initiated with either a Current Address Read or a Random Address Read. The master *does* acknowledge the data byte output in this case, and the memory continues to output the next byte in sequence. To terminate the stream of bytes, the master must *not* acknowledge the last byte output, and *must* generate a STOP condition.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over' and the memory continues to output data from address 00h (at the start of the memory block).

Acknowledge in Read Mode

In all read modes, the memory waits, after each byte read, for an acknowledgment during the 9^{th} bit time. If the master does not pull the SDA line low during this time, the memory terminates the data transfer and switches to its standby state.

USE WITHIN A DRAM DIMM

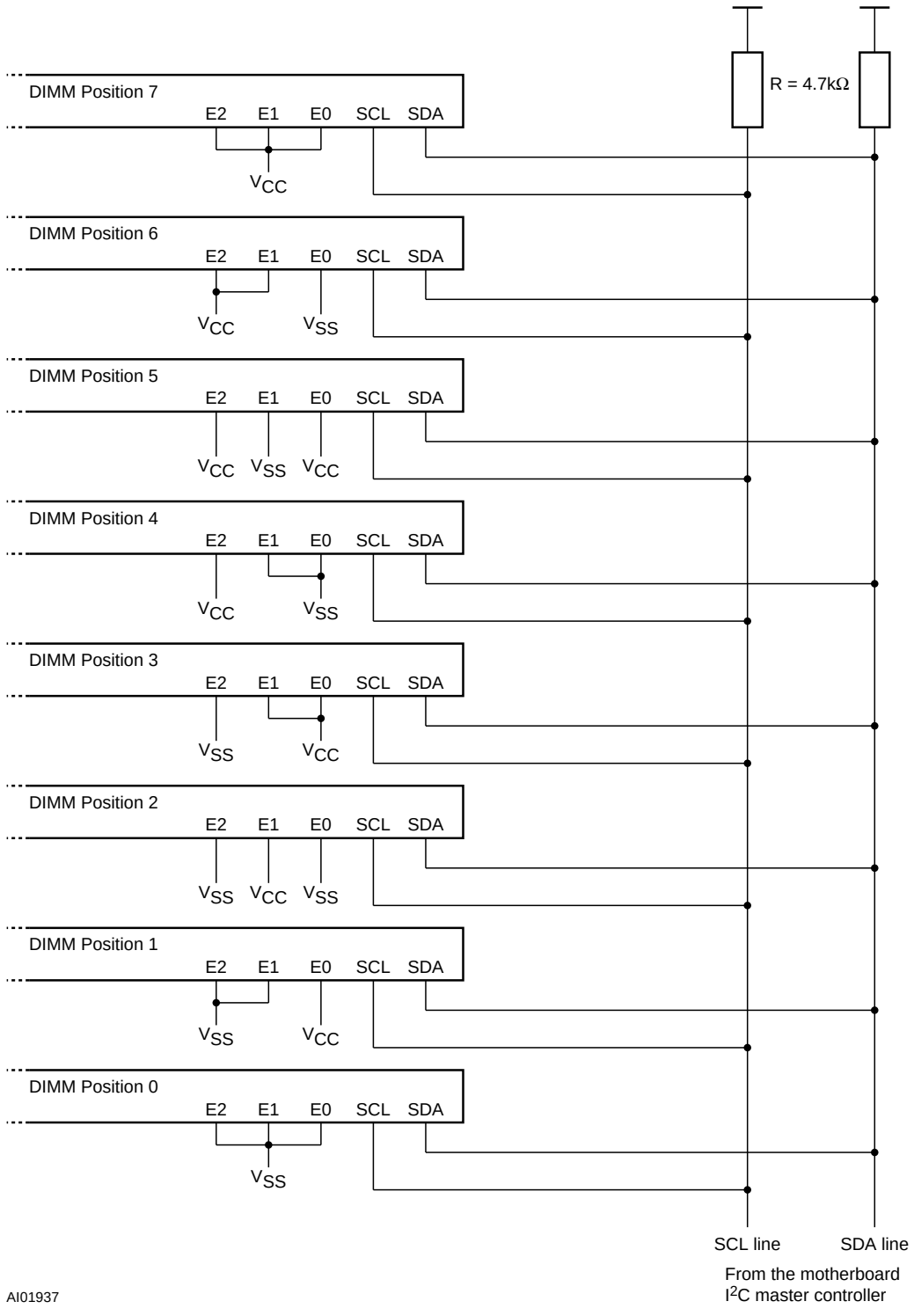
In the application, the M34C02 is soldered directly in the printed circuit module. The 3 Chip Enable inputs (pins 1, 2 and 3) are connected to pins 165, 166 and 167, respectively, of the 168-pin DRAM DIMM module. They are wired at V_{CC} or V_{SS} through the DIMM socket (see Table 5). The SCL and SDA lines (pins 6 and 5) are connected respectively to pins 83 and 82 of the memory module. The pull-up resistors needed for normal behavior of the I^2C bus are connected on the I^2C bus of the mother-board (as shown in Figure 10).

The Write Control input of the M34C02 ($\overline{WC}$ on pin 7) can be left unconnected. However, connecting it to V_{SS} is recommended, to maintain full read and write access to the top half of the memory.

Programming the M34C02

When the M34C02 is delivered, full read and write access is given to the whole memory array. It is recommended that the first step is to use the test equipment to write the module information (such as its access speed, its size, its organization) to the first half of the memory, starting from the first memory location. When the data has been validated, the test equipment can send a Write command to the Protection Register, using the device select code '01100000b' followed by an address and data byte (made up of Don't Care values) as shown in Figure 8. The first 128 bytes of the memory area are then write-protected, and the M34C02 will no longer respond to the specific device select code '0110000xb'. It is not possible to reverse this sequence.

Figure 10. Serial Presence Detect Block Diagram



Note: 1. E0, E1 and E2 are wired at each DIMM socket in a binary sequence for a maximum of 8 devices.
2. Common clock and common data are shared across all the devices.
3. Pull-up resistors are required on all SDA and SCL bus lines (typically 4.7 kΩ) because these lines are open drain when used as outputs.

Table 6. DC Characteristics
(T_A = –40 to 85 °C; V_{CC} = 2.5 to 5.5 V, 2.2 to 5.5 V)

Symbol	Parameter		Test Condition	Min.	Max.	Unit
I_{LI}	Input Leakage Current	SCL, SDA	0 V ≤ V_{IN} ≤ V_{CC}		± 2	µA
I_{LO}	Output Leakage Current		0 V ≤ V_{OUT} ≤ V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply Current	-W or -L series	V_{CC} =5V, f_c=400kHz (rise/fall time < 30ns)		2	mA
		-W series	V_{CC} =2.5V, f_c=400kHz (rise/fall time < 30ns)		1	mA
		-L series	V_{CC} =2.2V, f_c=400kHz (rise/fall time < 30ns)		1	mA
I_{CC1}	Supply Current (Stand-by)	-W or -L series	V_{IN} = V_{SS} or V_{CC} , V_{CC} = 5 V		1	µA
		-W series	V_{IN} = V_{SS} or V_{CC} , V_{CC} = 2.5 V		0.5	µA
		-L series	V_{IN} = V_{SS} or V_{CC} , V_{CC} = 2.2 V		0.5	µA
V_{IL}	Input Low Voltage	SCL, SDA		– 0.3	0.3V_{CC}	V
		E0, E1, E2		– 0.3	0.3V_{CC}	V
		$\overline{WC}$		– 0.3	0.5	V
V_{IH}	Input High Voltage	SCL, SDA		0.7V_{CC}	V_{CC}+1	V
		E0, E1, E2		0.7V_{CC}	V_{CC}+1	V
		$\overline{WC}$		0.7V_{CC}	V_{CC}+1	V
V_{OL}	Output Low Voltage	-W or -L series	I_{OL} = 3 mA, V_{CC} = 5 V		0.4	V
		-W series	I_{OL} = 2.1 mA, V_{CC} = 2.5 V		0.4	V
		-L series	I_{OL} = 2.1 mA, V_{CC} = 2.2 V		0.4	V

Table 7. AC Measurement Conditions

Input Rise and Fall Times	≤ 50 ns
Input Pulse Voltages	0.2V_{CC} to 0.8V_{CC}
Input and Output Timing Reference Voltages	0.3V_{CC} to 0.7V_{CC}

Figure 11. AC Testing Input Output Waveforms

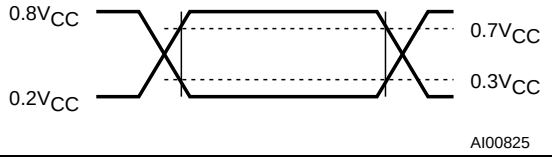


Table 8. Input Parameters [1](T_A = 25 °C, f = 400 kHz)

Symbol	Parameter	Test Condition	Min.	Max.	Unit
C_{IN}	Input Capacitance (SDA)			8	pF
C_{IN}	Input Capacitance (other pins)			6	pF
Z_{WCL}	$\overline{WC}$ Input Impedance	V_{IN} < 0.5 V	5	20	kΩ
Z_{WCH}	$\overline{WC}$ Input Impedance	V_{IN} > 0.7V_{CC}	500		kΩ
t_{NS}	Low Pass Filter Input Time Constant (SCL and SDA)		100	500	ns

Note: 1. Sampled only, not 100% tested.

Table 9. AC Characteristics

Symbol	Alt.	Parameter	M34C02-W		M34C02-L		Unit
			V_{CC}=2.5 to 5.5V T_A = –40 to 85°C		V_{CC}=2.2 to 5.5V T_A = –40 to 85°C		
			Min	Max	Min	Max	
t_{CH1CH2}	t_R	Clock Rise Time		300		300	ns
t_{CL1CL2}	t_F	Clock Fall Time		300		300	ns
t_{DH1DH2} [2]	t_R	SDA Rise Time	20	300	20	300	ns
t_{DL1DL2} [2]	t_F	SDA Fall Time	20	300	20	300	ns
t_{CHDX} [1]	$t_{SU:STA}$	Clock High to Input Transition	600		600		ns
t_{CHCL}	t_{HIGH}	Clock Pulse Width High	600		600		ns
t_{DLCL}	$t_{HD:STA}$	Input Low to Clock Low (START)	600		600		ns
t_{CLDX}	$t_{HD:DAT}$	Clock Low to Input Transition	0		0		µs
t_{CLCH}	t_{LOW}	Clock Pulse Width Low	1.3		1.3		µs
t_{DXCX}	$t_{SU:DAT}$	Input Transition to Clock Transition	100		100		ns
t_{CHDH}	$t_{SU:STO}$	Clock High to Input High (STOP)	600		600		ns
t_{DHDL}	t_{BUF}	Input High to Input Low (Bus Free)	1.3		1.3		µs
t_{CLQV} [3]	t_{AA}	Clock Low to Data Out Valid	200	900	200	900	ns
t_{CLQX}	t_{DH}	Data Out Hold Time After Clock Low	200		200		ns
f_C	f_{SCL}	Clock Frequency		400		400	kHz
t_W	t_{WR}	Write Time		10		10	ms

Note: 1. For a reSTART condition, or following a write cycle.
2. Sampled only, not 100% tested.
3. To avoid spurious START and STOP conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.

Figure 12. AC Waveforms

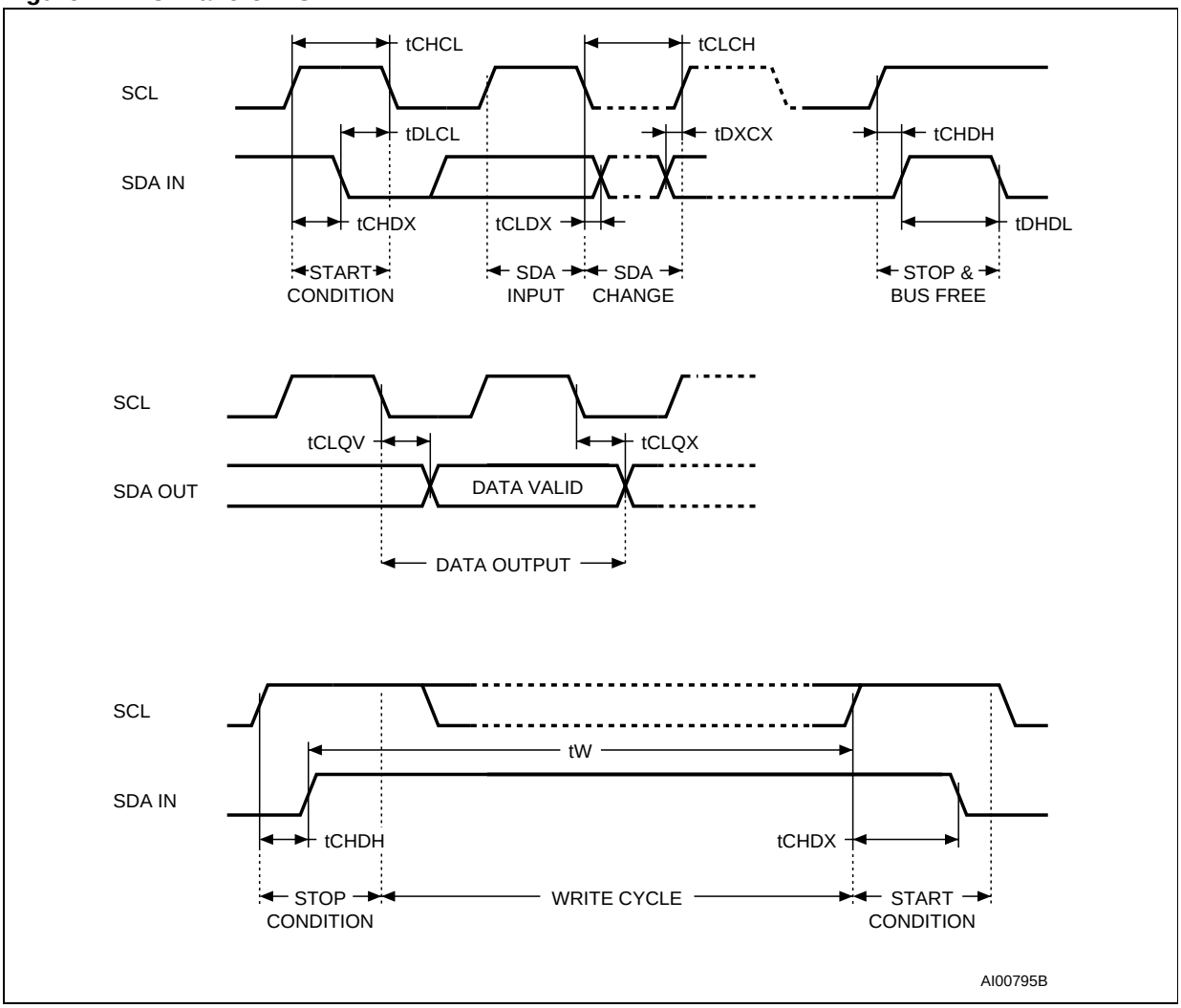


Table 10. Ordering Information Scheme

Example: M34C02 – W MN 6 T

Operating Voltage	
W	2.5 V to 5.5 V
L	2.2 V to 5.5 V

Package	
BN[1]	PSDIP8 (0.25 mm frame)
MN	SO8 (150 mil width)
DW	TSSOP8 (169 mil width)

Option	
T	Tape and Reel Packing

Temperature Range	
6	–40 °C to 85 °C

Note: 1. Package-type available only on request.

ORDERING INFORMATION

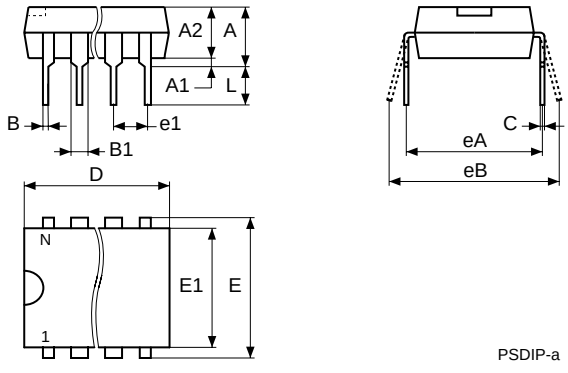
Devices are shipped from the factory with the memory content set at all ‘1’s (FFh), and the Protection Register set at all ‘0’s (00h).

The notation used for the device number is as shown in Table 10. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST Sales Office.

Table 11. PSDIP8 - 8 pin Plastic Skinny DIP, 0.25mm lead frame

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		3.90	5.90		0.154	0.232
A1		0.49	–		0.019	–
A2		3.30	5.30		0.130	0.209
B		0.36	0.56		0.014	0.022
B1		1.15	1.65		0.045	0.065
C		0.20	0.36		0.008	0.014
D		9.20	9.90		0.362	0.390
E	7.62	–	–	0.300	–	–
E1		6.00	6.70		0.236	0.264
e1	2.54	–	–	0.100	–	–
eA		7.80	–		0.307	–
eB			10.00			0.394
L		3.00	3.80		0.118	0.150
N	8			8		

Figure 13. PSDIP8 (BN)

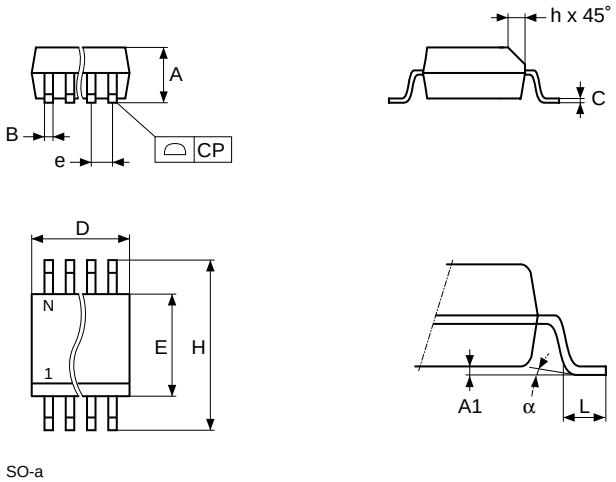


Note: 1. Drawing is not to scale.

Table 12. SO8 - 8 lead Plastic Small Outline, 150 mils body width

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A		1.35	1.75		0.053	0.069
A1		0.10	0.25		0.004	0.010
B		0.33	0.51		0.013	0.020
C		0.19	0.25		0.007	0.010
D		4.80	5.00		0.189	0.197
E		3.80	4.00		0.150	0.157
e	1.27	–	–	0.050	–	–
H		5.80	6.20		0.228	0.244
h		0.25	0.50		0.010	0.020
L		0.40	0.90		0.016	0.035
α		0°	8°		0°	8°
N	8			8		
CP			0.10			0.004

Figure 14. SO8 narrow (MN)



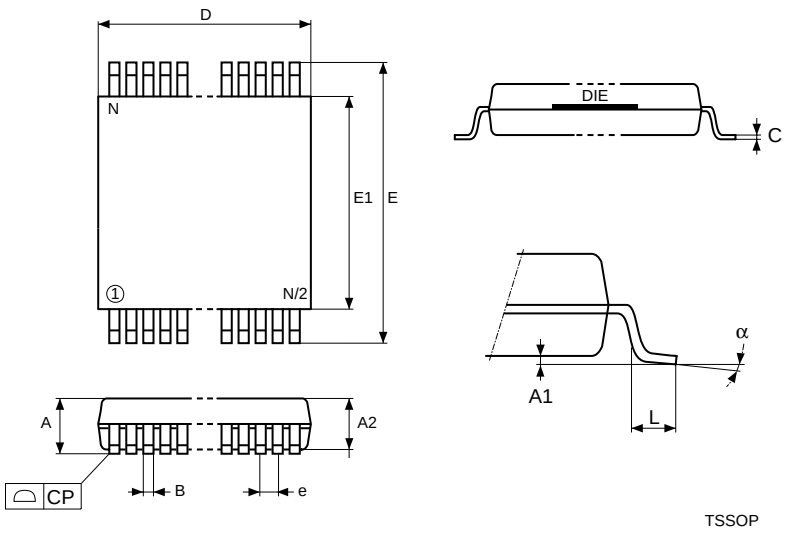
SO-a

Note: 1. Drawing is not to scale.

Table 13. TSSOP8 - 8 lead Thin Shrink Small Outline

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.10			0.043
A1		0.05	0.15		0.002	0.006
A2		0.85	0.95		0.033	0.037
B		0.19	0.30		0.007	0.012
C		0.09	0.20		0.004	0.008
D		2.90	3.10		0.114	0.122
E		6.25	6.50		0.246	0.256
E1		4.30	4.50		0.169	0.177
e	0.65	–	–	0.026	–	–
L		0.50	0.70		0.020	0.028
α		0°	8°		0°	8°
N	8			8		
CP			0.08			0.003

Figure 15. TSSOP8 (DW)



Note: 1. Drawing is not to scale.

Table 14. Revision History

Date	Description of Revision
27-Dec-1999	Adjustments to the formatting. 0 to 70°C temperature range removed from DC and AC tables. No change to description of device, or parameters