numonyx

M36P0R8070E0

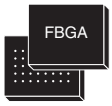
256 Mbit (x16, multiple bank, multilevel, burst) Flash memory 128 Mbit (burst) PSRAM, 1.8 V supply, multichip package

Features

- Multichip package
  - 1 die of 256 Mbit (16 Mb x 16, multiple bank, multilevel, burst) Flash memory
  - 1 die of 128 Mbit (8 Mb x16) PSRAM
- Supply voltage
  - $V_{DDF} = V_{CCP} = V_{DDQ} = 1.7$ to 1.95 V
  - $V_{PPF} = 9$ V for fast program (12 V tolerant)
- Electronic signature
  - Manufacturer code: 20h
  - Device code: 8818
- Package
  - ECOPACK®

Flash memory

- Synchronous/asynchronous read
  - Synchronous burst read mode: 108 MHz, 66 MHz
  - Asynchronous page read mode
  - Random access: 93 ns
- Programming time
  - 4 µs typical Word program time using Buffer Enhanced Factory Program command
- Memory organization
  - Multiple bank memory array: 32 Mbit banks
  - Four EFA (extended flash array) blocks of 64 Kbits
- Dual operations
  - Program/erase in one bank while read in others
  - No delay between read and write operations
- Security
  - 64bit unique device number
  - 2112 bit user programmable OTP Cells
- 100 000 program/erase cycles per block



TFBGA107 (ZAC)

- Block locking
  - All blocks locked at power-up
  - Any combination of blocks can be locked with zero latency
  - $\overline{WP}_F$ for block lock-down
  - Absolute write protection with $V_{PPF} = V_{SS}$
- CFI (common Flash interface)

PSRAM

- Access time: 70 ns
- Asynchronous page read
  - Page size: 4, 8 or 16 words
  - Subsequent read within page: 20 ns
- Synchronous burst read/write
- Low power consumption
  - Active current: < 25 mA
  - Standby current: 200 µA
  - Deep power-down current: 10 µA
- Low power features
  - PASR (partial array self refresh)
  - DPD (deep power-down) mode

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1 Description

The M36P0R8070E0 combines two memories in a multichip package:

- 256-Mbit multiple bank Flash memory (the M58PR256J)
- 128-Mbit PSRAM (the M69KB128AA).

This datasheet should be read in conjunction with the M58PR256J and M69KB128AA datasheets, which are available from your local Numonyx distributor.

Recommended operating conditions do not allow more than one memory to be active at the same time.

The memory is offered in a stacked TFBGA107 package, and it is supplied with all the bits erased (set to '1').

Figure 1. Logic diagram

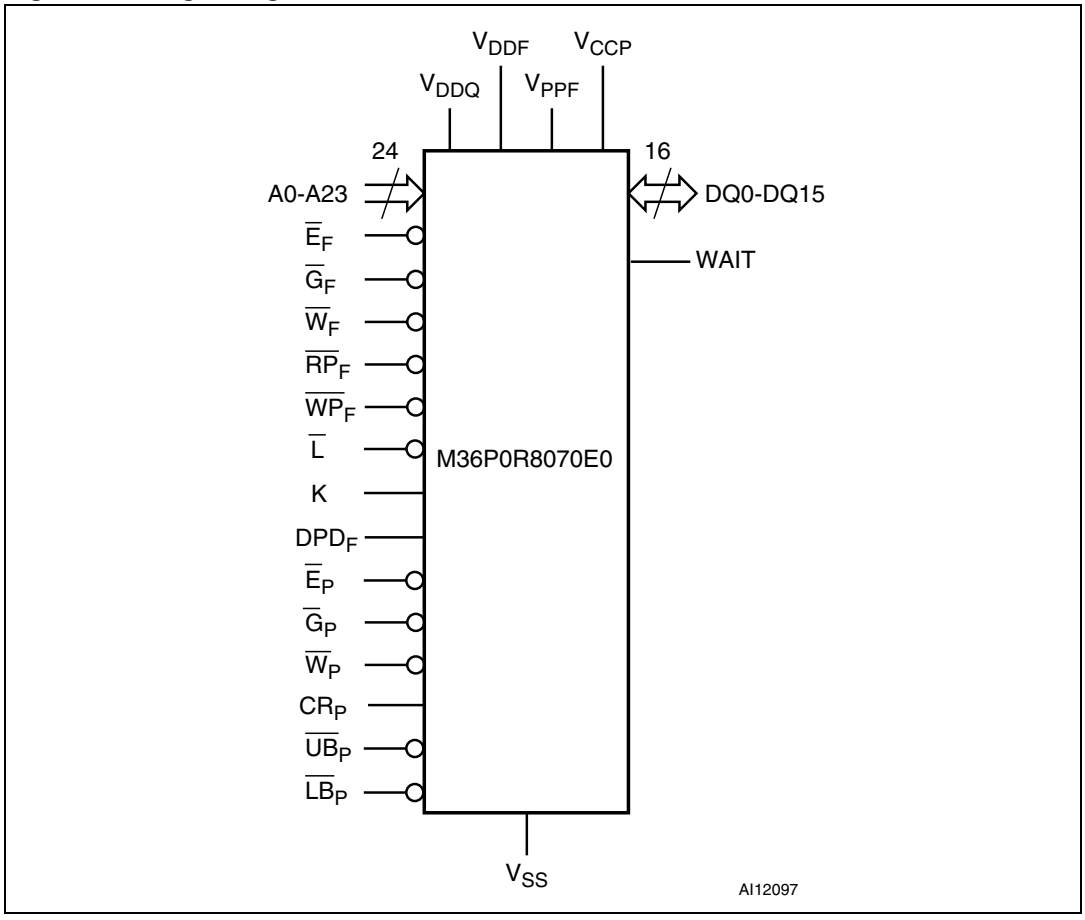
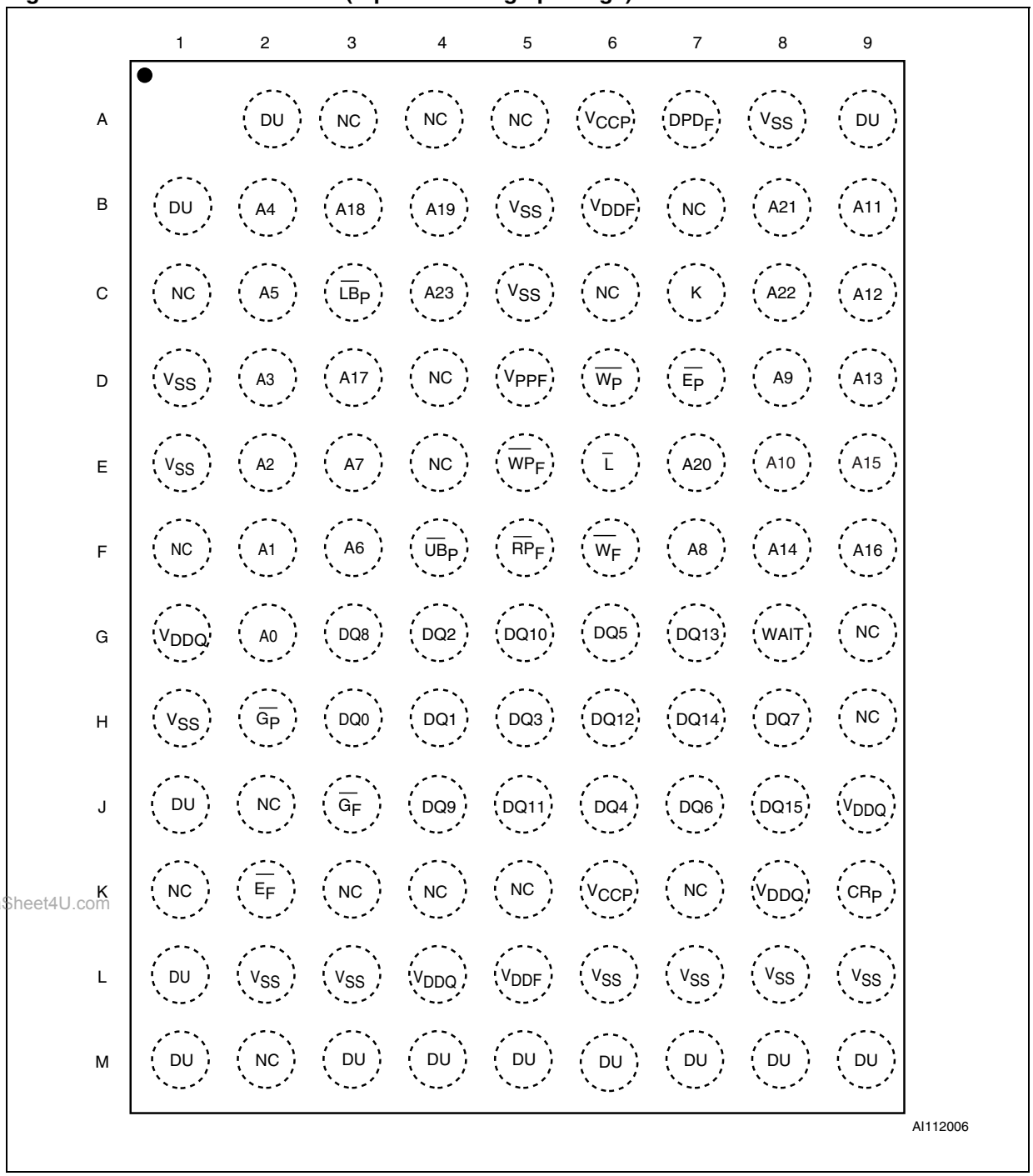


Table 1. Signal names

Name	Function
A0-A23(1)	Address inputs
DQ0-DQ15	Common data input/output
V_{DDQ}	Common Flash and PSRAM power supply for I/O buffers
V_{PPF}	Flash memory optional supply voltage for fast program and erase
V_{DDF}	Flash memory power supply
V_{CCP}	PSRAM power supply
V_{SS}	Ground
$\overline{L}$	Latch Enable input
K	Burst Clock
WAIT	Wait output
NC	Not connected internally
DU	Do not use as internally connected
Flash memory	
$\overline{E}_F$	Chip Enable input
$\overline{G}_F$	Output Enable input
$\overline{W}_F$	Write Enable input
$\overline{RP}_F$	Reset input
$\overline{WP}_F$	Write Protect input
DPD_F	Deep power-down
PSRAM	
$\overline{E}_P$	Chip Enable input
$\overline{G}_P$	Output Enable input
$\overline{W}_P$	Write Enable input
CR_P	Configuration Register Enable input
$\overline{UB}_P$	Upper Byte Enable input
$\overline{LB}_P$	Lower Byte Enable input

1. A23 is an address input for the Flash memory component only.

Figure 2. TFBGA connections (top view through package)



2 Signal descriptions

See *Figure 1: Logic diagram* and *Table 1: Signal names* for a brief overview of the signals connected to this device.

2.1 Address inputs (A0-A23)

Addresses A0-A22 are common inputs for the Flash memory and PSRAM components. Address A23 is an input for the Flash memory component only. The address inputs select the cells in the Flash memory array to access during bus read operations. During bus write operations they control the commands sent to the command interface of the Flash memory's Program/Erase Controller.

In the PSRAM the address inputs select the cells in the memory array to access during bus read and write operations.

2.2 Data input/output (DQ0-DQ15)

The data I/O output the data stored at the selected address during a bus read operation or input a command or the data to be programmed during a bus write operation.

For the PSRAM component, the Upper Byte Data Inputs/Outputs (DQ8-DQ15) carry the data to or from the upper part of the selected address when Upper Byte Enable ($\overline{UB}_P$) is driven Low. The Lower Byte Data Inputs/Outputs (DQ0-DQ7) carry the data to or from the lower part of the selected address when Lower Byte Enable ($\overline{LB}_P$) is driven Low. When both $\overline{UB}_P$ and $\overline{LB}_P$ are disabled, the data inputs/ outputs are high impedance.

2.3 Latch Enable ($\overline{L}$)

The Latch Enable pin is common to the Flash memory and PSRAM components.

For more details about the Latch Enable signal, please refer to the datasheets of the respective memory components: M69KB128AA for the PSRAM and M58PR256J for the Flash memory.

2.4 Clock (K)

The Clock input pin is common to the Flash memory and PSRAM components.

For more details about the Clock signal, please refer to the datasheets of the respective memory components: M69KB128AA for the PSRAM and M58PR256J for the Flash memory.

2.5 Wait (WAIT)

WAIT is an output pin common to the Flash memory and PSRAM components. However, the WAIT signal does not behave in the same way for the PSRAM and the Flash memory.

For details on this signal, please refer to the M69KB128AA datasheet for the PSRAM and to the M58PR256J datasheet for the Flash memory.

2.6 Flash Chip Enable input ($\overline{E}_F$)

The Chip Enable input activates the control logic, input buffers, decoders, and sense amplifiers of the Flash memory. When Chip Enable is Low, V_{IL}, and Reset is High, V_{IH}, the device is in active mode. When Chip Enable is at V_{IH} the Flash memory are deselected, the outputs are high impedance and the power consumption is reduced to the standby level.

It is not allowed to have $\overline{E}_F$ at V_{IL} and $\overline{E}_P$ at V_{IL} at the same time. Only one memory component can be enabled at a time.

2.7 Flash Output Enable inputs ($\overline{G}_F$)

The Output Enable input controls the data outputs during Flash memory bus read operations.

2.8 Flash Write Enable ($\overline{W}_F$)

The Write Enable input controls the bus write operation of the Flash memory command interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable, whichever occurs first.

2.9 Flash Write Protect ($\overline{WP}_F$)

Write Protect is an input that provides additional hardware protection for each block. When Write Protect is Low, V_{IL}, lock-down is enabled and the protection status of the locked-down blocks cannot be changed. When Write Protect is at High, V_{IH}, lock-down is disabled and the locked-down blocks can be locked or unlocked. (See the lock status table in the M58PR256J datasheet).

2.10 Flash Reset ($\overline{RP}_F$)

The Reset input provides a hardware reset of the Flash memories. When Reset is at V_{IL}, the memory is in reset mode: the outputs are high impedance and the current consumption is reduced to the Reset supply current I_{DD2}. After Reset, all blocks are in the locked state and the Configuration Register is reset. When Reset is at V_{IH}, the device is in normal operation. Upon exiting reset mode the device enters asynchronous read mode, but a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs.

The Reset pin can be interfaced with 3 V logic without any additional circuitry, and can be tied to V_{RPH} .

2.11 Flash Deep Power-Down (DPD_F)

The deep power-down input put sthe device in deep power-down mode.

When the device is in standby mode and the Enhanced Configuration Register bit ECR15 is set, asserting the deep power-down input causes the memory to enter deep power-down mode.

When the device is in the deep power-down mode, the memory cannot be modified and the data is protected.

The polarity of the DPD_F pin is determined by ECR14. The deep power-down input is active Low by default.

2.12 PSRAM Chip Enable input ($\overline{E}_P$)

The Chip Enable input activates the PSRAM when driven Low (asserted). When de-asserted (V_{IH}), the device is disabled, and goes automatically in low-power standby mode or deep power-down mode, according to the RCR (Refresh Configuration Register) setting.

2.13 PSRAM Write Enable ($\overline{W}_P$)

Write Enable, $\overline{W}_P$, controls the bus write operation of the PSRAM. When asserted (V_{IL}), the device is in write mode and write operations can be performed either to the configuration registers or to the memory array.

2.14 PSRAM Output Enable ($\overline{G}_P$)

When held Low, V_{IL}, the Output Enable, $\overline{G}_P$, enables the bus read operations of the PSRAM.

2.15 PSRAM Upper Byte Enable ($\overline{UB}_P$)

The Upper Byte Enable, $\overline{UB}_P$, gates the data on the Upper Byte Data Inputs/Outputs (DQ8-DQ15) to or from the upper part of the selected address during a write or read operation.

2.16 PSRAM Lower Byte Enable ($\overline{LB}_P$)

The Lower Byte Enable, $\overline{LB}_P$, gates the data on the Lower Byte Data Inputs/Outputs (DQ0-DQ7) to or from the lower part of the selected address during a write or read operation.

If both $\overline{LB}_P$ and $\overline{UB}_P$ are disabled (High), the device disables the data bus from receiving or transmitting data. Although the device seems to be deselected, it remains in an active mode as long as $\overline{E}_P$ remains Low.

2.17 PSRAM Configuration Register Enable (CR_P)

When this signal is driven High, V_{IH}, bus read or write operations access either the value of the RCR or the BCR (Bus Configuration Register) according to the value of A19.

2.18 V_{DDF} supply voltage

V_{DDF} provides the power supply to the internal core of the Flash memory. It is the main power supply for all Flash memory operations (read, program and erase).

2.19 V_{CCP} supply voltage

The V_{CCP} supply voltage is the core supply voltage.

2.20 V_{DDQ} supply voltage

V_{DDQ} provides the power supply for the Flash memory and PSRAM I/O pins. This allows all outputs to be powered independently of the Flash memory and PSRAM core power supplies, V_{DDF} and V_{CCP}.

2.21 V_{PPF} program supply voltage

V_{PPF} is both a control input and a power supply pin for the Flash memory. The two functions are selected by the voltage range applied to the pin.

If V_{PPF} is kept in a low voltage range (0V to V_{DDQ}) V_{PPF} is seen as a control input. In this case a voltage lower than V_{PPLK} gives absolute protection against program or erase, while $V_{PPF} > V_{PP1}$ enables these functions. V_{PPF} is only sampled at the beginning of a program or erase; a change in its value after the operation has started does not have any effect and program or erase operations continue.

If V_{PPF} is in the range of V_{PPH} it acts as a power supply pin. In this condition V_{PPF} must be stable until the program/erase algorithm is completed.

2.22 V_{SS} ground

V_{SS} is the common ground reference for all voltage measurements in the Flash memory (core and I/O Buffers) and PSRAM chips. It must be connected to the system ground.

Note: Each Flash memory device in a system should have its supply voltage (V_{DDF}) and the program supply voltage V_{PPF} decoupled with a 0.1 µF ceramic capacitor close to the pin (high-frequency, inherently-low inductance capacitors should be as close as possible to the package). See Figure 5: AC measurement load circuit. The PCB track widths should be sufficient to carry the required V_{PPF} program and erase currents.

3 Functional description

The PSRAM and Flash memory components have separate power supplies but share the same grounds. They are distinguished by two Chip Enable inputs: $\overline{E}_F$ for the Flash memory and $\overline{E}_P$ for the PSRAM.

Recommended operating conditions do not allow more than one device to be active at a time. The most common example is a simultaneous read operations on the Flash memory and the PSRAM which results in a data bus contention. Therefore, it is recommended to put the other device in the high impedance state when reading the selected device.

Figure 3. Functional block diagram

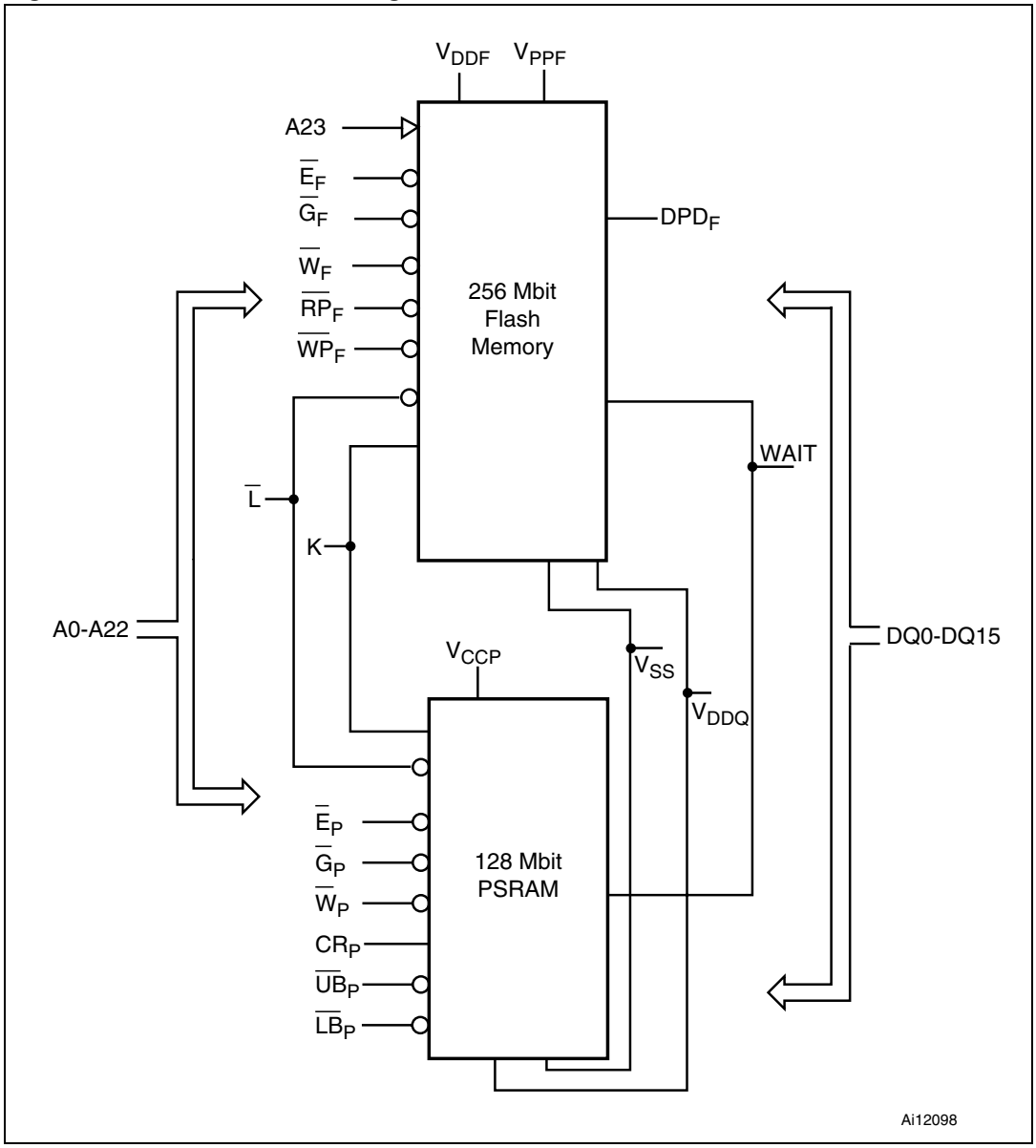


Table 2. Main operating modes(1)

	Operation	$\overline{E}_F$	$\overline{G}_F$	$\overline{W}_F$	$\overline{RP}_F$	DPD_F(2)	WAIT(3)	$\overline{L}$	$\overline{E}_P$	CR_P	$\overline{G}_P$	$\overline{W}_P$	$\overline{LB}_P$	$\overline{UB}_P$	A18-A19(4)	A0-A17 A20-A22	DQ15-DQ0
Flash memory	Bus Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	de-asserted(5)		V_{IL}(6)	PSRAM must be disabled. Only one Flash memory can be enabled at a time.								Flash data out
	Bus Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	de-asserted(5)		V_{IL}(6)									Flash data in
	Address Latch	V_{IL}	X	V_{IH}	V_{IH}	de-asserted(5)		V_{IL}									Flash data out or Hi-Z (7)
	Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	de-asserted(5)	Hi-Z	X	Any PSRAM mode is allowed. Flash memories must be disabled.								Hi-Z
	Standby	V_{IH}	X	X	V_{IH}	de-asserted(5)	Hi-Z	X									Hi-Z
	Reset	X	X	X	V_{IL}	de-asserted(5)	Hi-Z	X									Hi-Z
	Deep Power-Down	V_{IH}	X	X	V_{IH}	asserted(8)	Hi-Z	X									Hi-Z
PSRAM	Read	Flash memories must be disabled					Low-Z	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	Valid		PSRAM data out
	Write						Low-Z	V_{IL}	V_{IL}	V_{IL}	X	V_{IL}	V_{IL}	V_{IL}	Valid		PSRAM data in
	Read Configuration Register						Low-Z	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	00(RCR) 10(BCR) X1(DIDR)	X	BCR/RCR/DIDR contents
	Program Configuration Register(9)						Low-Z	V_{IL}	V_{IL}	V_{IH}	X	V_{IH}	X	X	00(RCR) 10(BCR)	BCR/RCR data	Hi-Z
	Standby	Any Flash memory mode is allowed. Only one Flash memory can be enabled at a time					Hi-Z	X	V_{IH}	V_{IL}	X	X	X	X			Hi-Z
	Deep Power-Down(10)						Hi-Z	X	V_{IH}	X	X	X	X	X			Hi-Z

1. X = Don't Care.
2. The DPD_F signal polarity depends on the value of the ECR14 bit.
3. WAIT signal polarity is configured using the Set Configuration Register command. See the M58PR256J datasheet for details.
4. A18 and A19 are used to select the BCR (Bus Configuration Register), RCR (Refresh Configuration Register) or DIDR (Device ID Register).
5. If ECR15 is set to '0', the Flash memory device cannot enter the Deep Power-Down mode, even if DPD_F is asserted.
6. $\overline{L}$ can be tied to V_{IH} if the valid address has been previously latched.
7. Depends on $\overline{G}_F$.
8. ECR15 has to be set to '1' for the Flash memory device to enter Deep Power-Down.
9. BCR and RCR only.
10. Bit 4 of the Refresh Configuration Register must be set to '0', bit 4 (BCR4) of the Bus Configuration Register must be set to '0', and $\overline{E}$ has to be maintained High, V_{IH}, during Deep Power-Down mode.

4 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the Numonyx SURE program and other relevant quality documents.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient operating temperature	–30	85	°C
T_{BIAS}	Temperature under bias	–30	85	°C
T_{STG}	Storage temperature	–55	125	°C
V_{IO}	Input or output voltage	–0.2	2.45	V
V_{DDF}	Flash memory supply voltage	–1	3	V
V_{CCP}	PSRAM supply voltage	–0.2	2.45	V
V_{DDQ}	Input/output supply voltage	–0.2	2.45	V
V_{PPF}	Flash memory program voltage	–1	12.6	V
I_O	Output short circuit current		100	mA
t_{VPPH}	Time for V_{PPF} at V_{PPH}		100	hours

5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables in this section are derived from tests performed under the measurement conditions summarized in *Table 4., Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 4. Operating and AC measurement conditions

Parameter	Flash memory		PSRAM		Unit
	Min	Max	Min	Max	
V_{DDF} supply voltage	1.7	1.95	–	–	V
V_{CCP} supply voltage	–	–	1.7	1.95	V
V_{DDQ} supply voltage	1.7	1.95	1.7	1.95	V
V_{PPF} supply voltage (factory environment)	8.5	9.5	–	–	V
V_{PPF} supply voltage (application environment)	–0.4	V_{DDQ} +0.4	–	–	V
Load capacitance (C_L)	30		30		pF
Output circuit resistors (R_1, R_2)	16.7		16.7		kΩ
Input rise and fall times		3		1(1), (2)	ns
Input pulse voltages	0 to V_{DDQ}		0 to V_{DDQ}		V
Input and output timing ref. voltages	$V_{DDQ}/2$		$V_{DDQ}/2$		V

1. Referenced to V_{SS}.
2. $V_{CCP} = V_{DDQ}$.

Figure 4. AC measurement I/O waveform

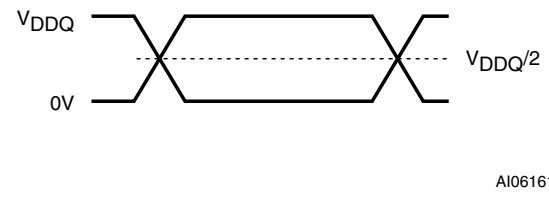
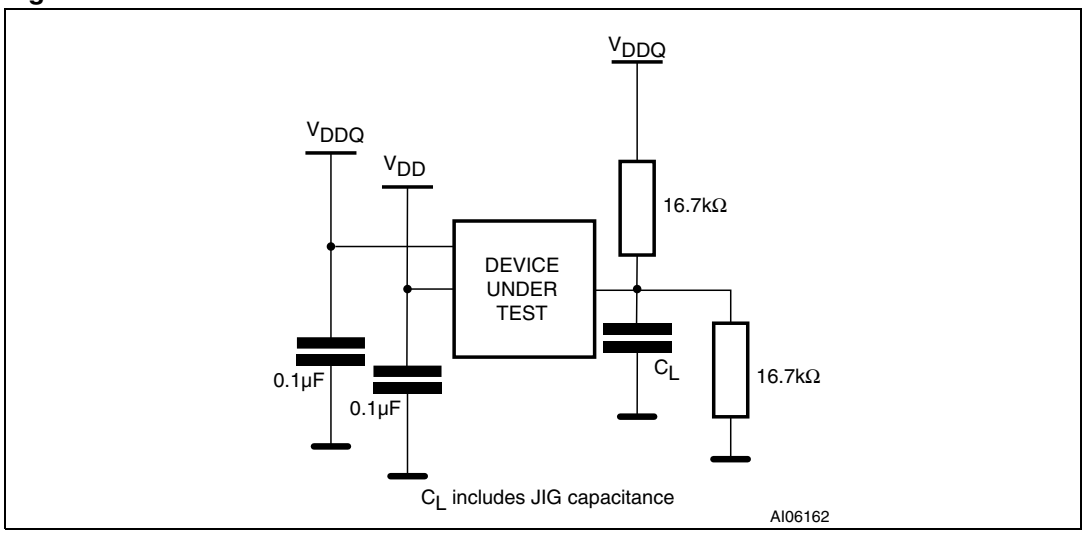


Figure 5. AC measurement load circuit



1. V_{DD} means $V_{DDF} = V_{CCP}$.

Table 5. Capacitance(1)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V	–	12	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V	–	15	pF

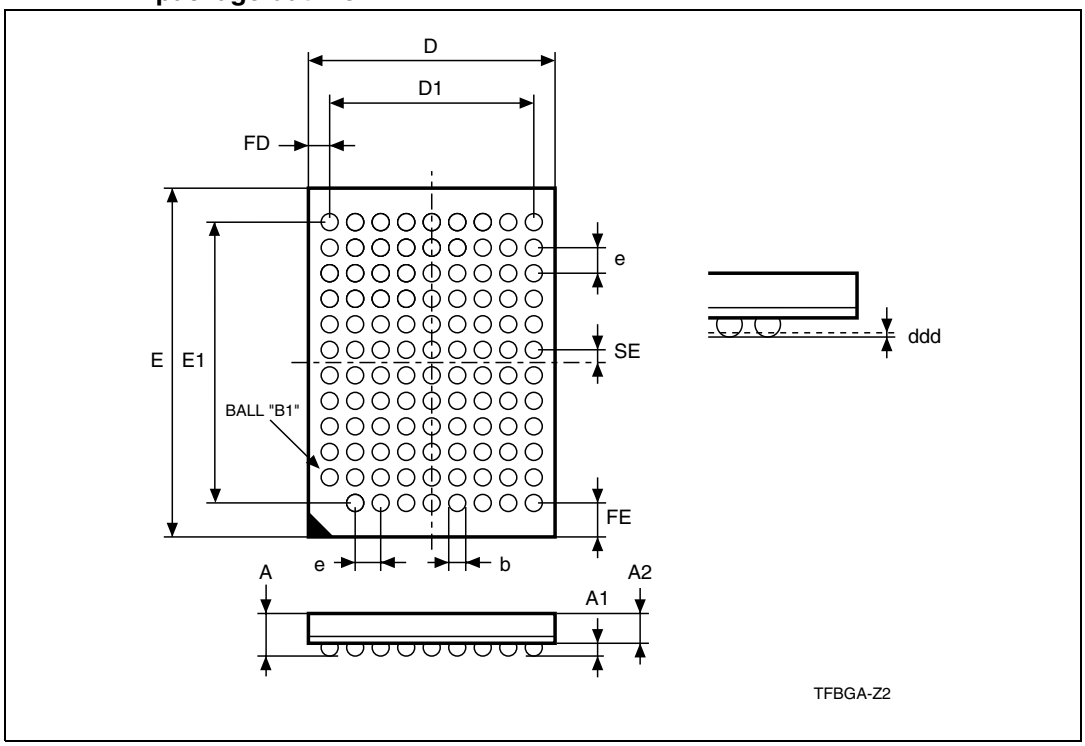
1. Sampled only, not 100% tested.

6 Package mechanical

To meet environmental requirements, Numonyx offers these devices in ECOPACK® packages, which have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label.

Figure 6. TFBGA107 8 x 11 mm 9 x 12 active ball array, 0.8 mm pitch, package outline



1. Drawing is not to scale.

Table 6. Stacked TFBGA107 8 x 11 mm 9 x 12 active ball array, 0.8 mm pitch, package data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.20			0.008	
A2	0.85			0.033		
b	0.35	0.30	0.40	0.014	0.012	0.016
D	8.00	7.90	8.10	0.315	0.311	0.319
D1	6.40			0.252		
ddd			0.10			0.004
E	11.00	10.90	11.10	0.433	0.429	0.437
E1	8.80			0.346		
e	0.80			0.031		
FD	0.80			0.031		
FE	1.10			0.043		
SE	0.40			0.016		

7 Part numbering

Table 7. Ordering information scheme

Example: M36 P 0 R 8 0 7 0 E 0 ZAC E

Device type

M36 = multichip package (Flash + PSRAM)

Flash 1 architecture

P = Multilevel, multiple bank, large buffer

Flash 2 architecture

0 = no die

Operating voltage

R = V_{DDF} = V_{CCP} = V_{DDQ} = 1.7 to 1.95 V

Flash 1 density

8 = 256 Mbits

Flash 2 density

0 = no die

RAM 1 density

7 = 128 Mbits

RAM 0 density

0 = no Die

Parameter blocks location

E = even block flash memory configuration

Product version

0 = 90 nm Flash technology, 93 ns speed; 0.11 µm PSRAM technology, 70 ns speed

Package

ZAC = stacked TFBGA107 C stacked footprint.

Option

E = ECOPACK package, standard packing

F = ECOPACK package, tape and reel packing

Note: Devices are shipped from the factory with the memory content bits erased to '1'. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact the Numonyx sales office nearest to you.

8 Revision history

Table 8. Document revision history

Date	Revision	Changes
2-Oct-2007	1	Initial release.
10-Dec-2007	2	Applied Numonyx branding.

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