



M36P0R9070E0

512 Mbit (x16, Multiple Bank, Multi-Level, Burst) Flash Memory
128 Mbit (Burst) PSRAM, 1.8V Supply, Multi-Chip Package

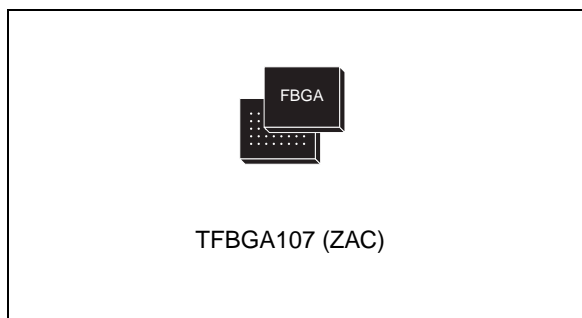
PRELIMINARY DATA

Features summary

- Multi-chip package
 - 1 die of 512 Mbit (32Mb x 16, Multiple Bank, Multi-Level, Burst) Flash Memory
 - 1 die of 128Mbit (8Mb x16) PSRAM
- Supply voltage
 - $V_{DDF} = V_{CCP} = V_{DDQ} = 1.7$ to 1.95V
 - $V_{PPF} = 9V$ for fast program (12V tolerant)
- Electronic signature
 - Manufacturer Code: 20h
 - Device Code: 8819
- Package
 - ECOPACK®

Flash memory

- Synchronous / asynchronous read
 - Synchronous Burst Read mode: 108MHz, 66MHz
 - Asynchronous Page Read mode
 - Random Access: 93ns
- Programming time
 - 4 μ s typical Word program time using Buffer Enhanced Factory Program command
- Memory organization
 - Multiple Bank Memory Array: 64 Mbit Banks
 - Four Extended Flash Array (EFA) Blocks of 64 Kbits
- Dual operations
 - program/erase in one Bank while read in others
 - No delay between read and write operations



- Security
 - 2112-bit user programmable OTP Cells
 - 64-bit unique device number
- 100,000 program/erase cycles per block
- Block locking
 - All Blocks locked at power-up
 - Any combination of Blocks can be locked with zero latency
 - \overline{WP}_F for Block Lock-Down
 - Absolute Write Protection with $V_{PPF} = V_{SS}$
- Common Flash Interface (CFI)

PSRAM

- Access time: 70ns
- Asynchronous Page Read
 - Page Size: 4, 8 or 16 Words
 - Subsequent read within page: 20ns
- Low power features
 - Partial Array Self Refresh (PASR)
 - Deep Power-Down mode (DPD)
- Synchronous Burst Read/Write

November 2005

Rev. 1
1/26

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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1 Summary description

The M36P0R9070E0 combines two memory devices in one Multi-Chip Package:

- 512-Mbit Multiple Bank Flash memory (the M58PR512J).
- 128 Mbit PSRAM (the M69KB128AA).

This datasheet should be read in conjunction with the M58PR512J and M69KB128AA datasheets, which are available from www.st.com.

Recommended operating conditions do not allow more than one memory to be active at the same time.

The memory is offered in a Stacked TFBGA107 package. It is supplied with all the bits erased (set to '1').

Table 1. Logic Diagram

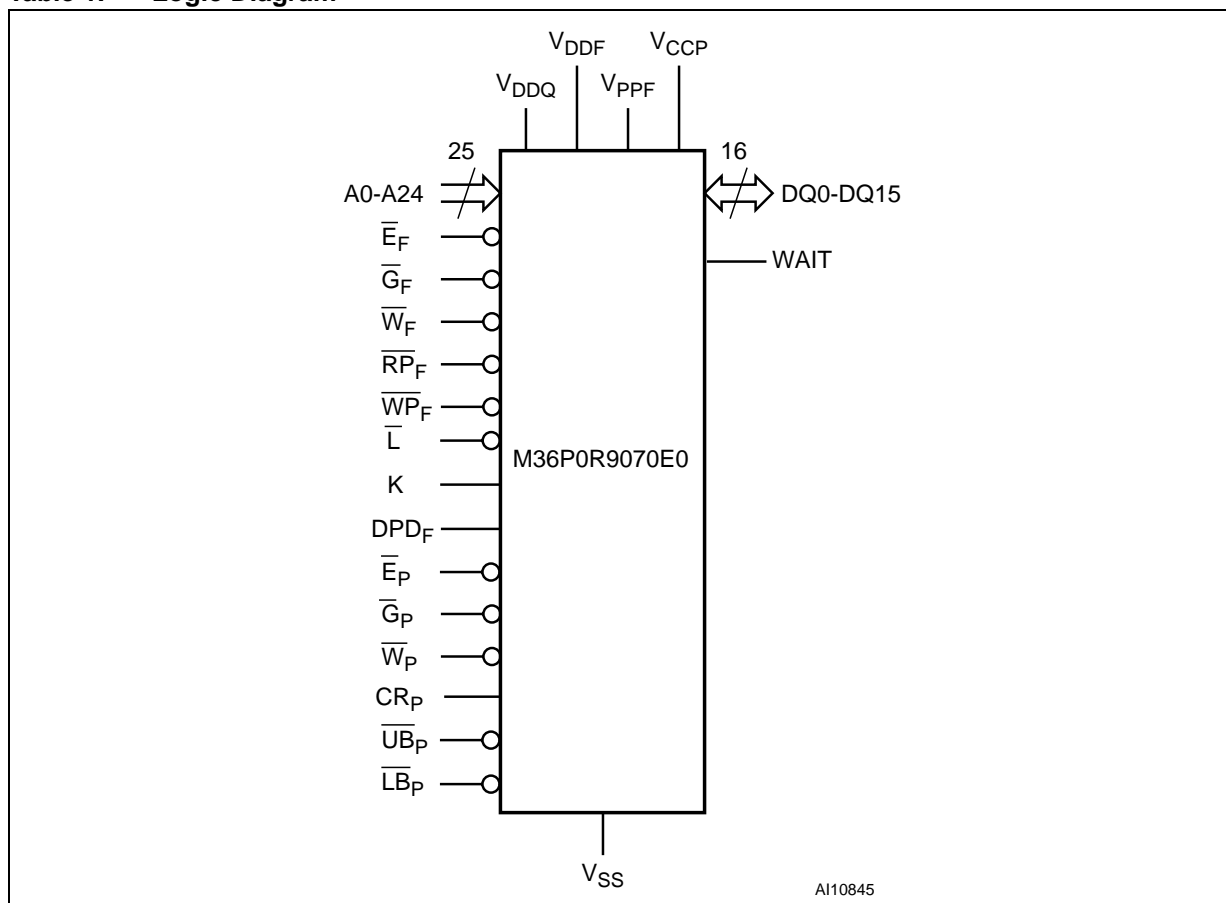
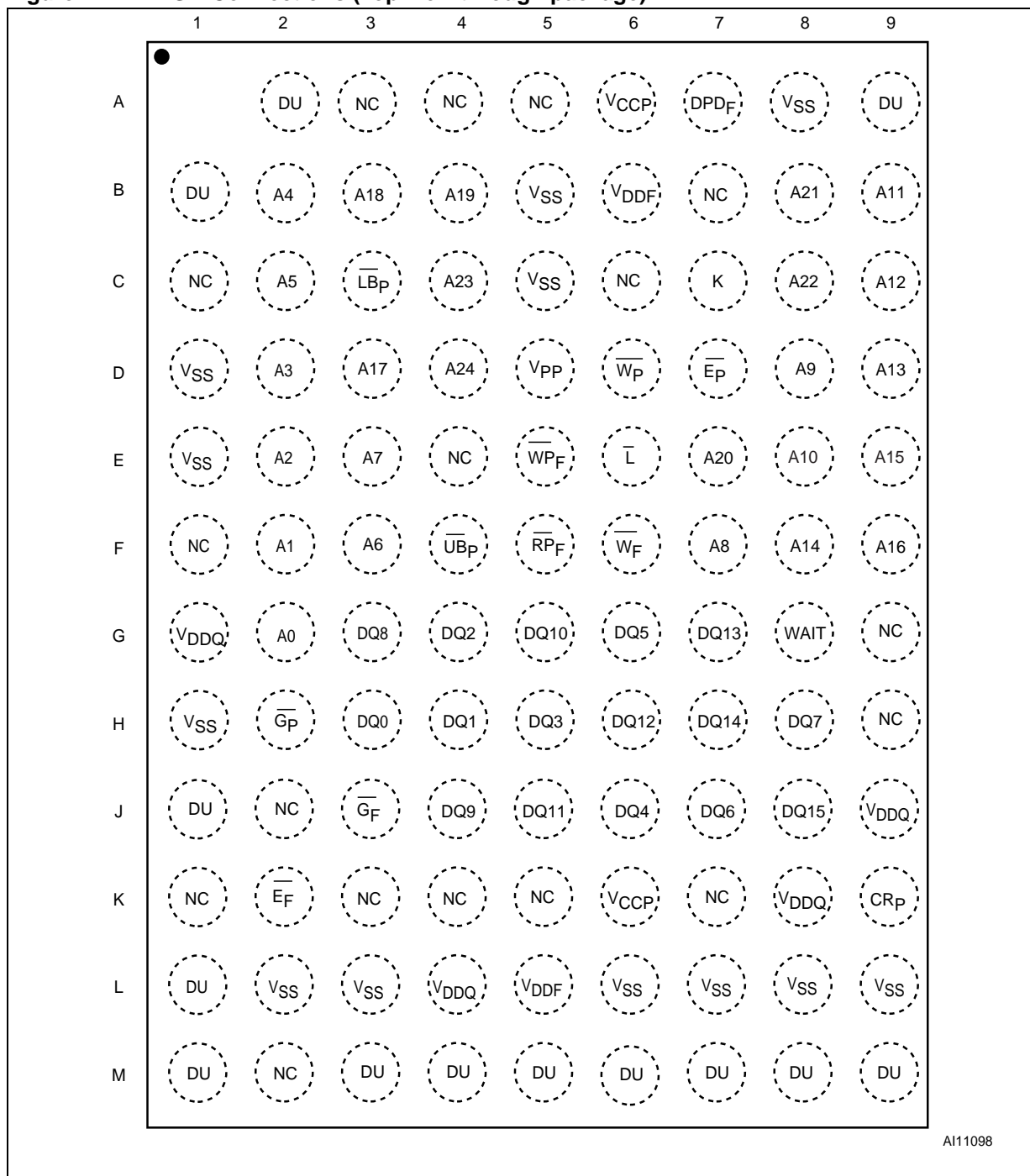


Table 2. Signal Names

| | |
|---|---|
| A0-A24 ⁽¹⁾ | Address Inputs |
| DQ0-DQ15 | Common Data Input/Output |
| V _{DDQ} | Common Flash and PSRAM Power Supply for I/O Buffers |
| V _{PPF} | Flash Memory Optional Supply Voltage for Fast Program & Erase |
| V _{DDF} | Flash Memory Power Supply |
| V _{CCP} | PSRAM Power Supply |
| V _{SS} | Ground |
| $\overline{\text{L}}$ | Latch Enable input |
| K | Burst Clock |
| WAIT | Wait Output |
| NC | Not Connected Internally |
| DU | Do Not Use as Internally Connected |
| Flash Memory | |
| $\overline{\text{E}}_{\text{F}}$ | Chip Enable input |
| $\overline{\text{G}}_{\text{F}}$ | Output Enable Input |
| $\overline{\text{W}}_{\text{F}}$ | Write Enable input |
| $\overline{\text{R}}_{\text{P}}_{\text{F}}$ | Reset input |
| $\overline{\text{W}}_{\text{P}}_{\text{F}}$ | Write Protect input |
| DPD _F | Deep Power-Down |
| PSRAM | |
| $\overline{\text{E}}_{\text{P}}$ | Chip Enable Input |
| $\overline{\text{G}}_{\text{P}}$ | Output Enable Input |
| $\overline{\text{W}}_{\text{P}}$ | Write Enable Input |
| CR _P | Configuration Register Enable Input |
| $\overline{\text{U}}_{\text{B}}_{\text{P}}$ | Upper Byte Enable Input |
| $\overline{\text{L}}_{\text{B}}_{\text{P}}$ | Lower Byte Enable Input |

Note: 1 A23-A24 are Address Inputs for the Flash memory component only.

Figure 1. TFBGA Connections (Top view through package)



2 Signal descriptions

See [Table 1., Logic Diagram](#) and [Table 2., Signal Names](#), for a brief overview of the signals connected to this device.

2.1 Address inputs (A0-A24)

Addresses A0-A22 are common inputs for the Flash memory and PSRAM components. Addresses A23 and A24 are inputs for Flash memory components only. The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine. The Flash memory is accessed through the Chip Enable signal (\overline{E}_F) and through the Write Enable signal (\overline{W}_F), while the PSRAM is accessed through the Chip Enable signal (\overline{E}_P) and the Write Enable signal (\overline{W}_P).

\overline{E}_F Low, and \overline{E}_P must not be Low at the same time.

2.2 Data input/output (DQ0-DQ15)

The Data I/O output the data stored at the selected address during a Bus Read operation or input a command or the data to be programmed during a Bus Write operation.

For the PSRAM component, the upper Byte Data Inputs/Outputs (DQ8-DQ15) carry the data to or from the upper part of the selected address when Upper Byte Enable (\overline{UB}_P) is driven Low. The lower Byte Data Inputs/Outputs (DQ0-DQ7) carry the data to or from the lower part of the selected address when Lower Byte Enable (\overline{LB}_P) is driven Low. When both \overline{UB}_P and \overline{LB}_P are disabled, the Data Inputs/ Outputs are high impedance.

2.3 Latch Enable (\overline{L})

The Latch Enable pin is common to the Flash memory and PSRAM components.

For details of how the Latch Enable signal behaves, please refer to the datasheets of the respective memory components: M69KB128AA for the PSRAM and M58PR512J for the Flash memory.

2.4 Clock (K)

The Clock input pin is common to the Flash memory and PSRAM components.

For details of how the Clock signal behaves, please refer to the datasheets of the respective memory components: M69KB128AA for the PSRAM and M58PR512J for the Flash memory.

2.5 Wait (WAIT)

WAIT is an output pin common to the Flash memory and PSRAM components. However the WAIT signal does not behave in the same way for the PSRAM and the Flash memory.

For details of how it behaves, please refer to the M69KB128AA datasheet for the PSRAM and to the M58PR512J datasheet for the Flash memory.

2.6 Flash Chip Enable input (\overline{E}_F)

The Flash Chip Enable input activates the control logic, input buffers, decoders and sense amplifiers of the Flash memory component selected. When Chip Enable is Low, V_{IL} , and Reset is High, V_{IH} , the device is in active mode. When Chip Enable is at V_{IH} the corresponding Flash memory are deselected, the outputs are high impedance and the power consumption is reduced to the standby level.

It is not allowed to have \overline{E}_F at V_{IL} and \overline{E}_P at V_{IL} at the same time. Only one memory component can be enabled at a time.

2.7 Flash Output Enable inputs (\overline{G}_F)

The Output Enable pins control the data outputs during Flash memory Bus Read operations.

2.8 Flash Write Enable (\overline{W}_F)

The Write Enable controls the Bus Write operation of the Flash memory Command Interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable whichever occurs first.

2.9 Flash Write Protect (\overline{WP}_F)

Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is Low, V_{IL} , Lock-Down is enabled and the protection status of the Locked-Down blocks cannot be changed. When Write Protect is at High, V_{IH} , Lock-Down is disabled and the Locked-Down blocks can be locked or unlocked. (See the Lock Status Table in the M58PR512J datasheet).

2.10 Flash Reset (\overline{RP}_F)

The Reset input provides a hardware reset of the Flash memories. When Reset is at V_{IL} , the memory is in Reset mode: the outputs are high impedance and the current consumption is reduced to the Reset Supply Current I_{DD2} . Refer to [Table 7., Flash Memory DC Characteristics - Currents](#), for the value of I_{DD2} . After Reset all blocks are in the Locked state and the Configuration Register is reset. When Reset is at V_{IH} , the device is in normal operation. Exiting Reset mode the device enters Asynchronous Read mode, but a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs.

The Reset pin can be interfaced with 3V logic without any additional circuitry. It can be tied to V_{RPH} (refer to [Table 8., Flash Memory DC Characteristics - Voltages](#)).

2.11 PSRAM Chip Enable input (\overline{E}_P)

The Chip Enable input activates the PSRAM when driven Low (asserted). When deasserted (V_{IH}), the device is disabled, and goes automatically in low-power Standby mode or Deep Power-down mode.

2.12 PSRAM Write Enable (\overline{W}_P)

Write Enable, \overline{W}_P controls the Bus Write operation of the PSRAM. When asserted (V_{IL}), the device is in Write mode and Write operations can be performed either to the configuration registers or to the memory array.

2.13 PSRAM Output Enable (\overline{G}_P)

Output Enable, \overline{G}_P provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus.

2.14 PSRAM Upper Byte Enable (\overline{UB}_P)

The Upper Byte Enable, \overline{UB}_P gates the data on the Upper Byte Data Inputs/Outputs (DQ8-DQ15) to or from the upper part of the selected address during a Write or Read operation.

2.15 PSRAM Lower Byte Enable (\overline{LB}_P)

The Lower Byte Enable, \overline{LB}_P gates the data on the Lower Byte Data Inputs/Outputs (DQ0-DQ7) to or from the lower part of the selected address during a Write or Read operation.

If both \overline{LB}_P and \overline{UB}_P are disabled (High) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as \overline{E}_P remains Low.

2.16 PSRAM Configuration Register Enable (CR_P)

When this signal is driven High, V_{IH} , Write operations load either the value of the Refresh Configuration Register (RCR) or the Bus configuration register (BCR).

2.17 Deep Power-Down input (DPD_F)

The Deep Power-Down input is used to place the device in a Deep Power-Down mode. When the device is in Deep Power-Down mode, the memory cannot be modified and data is protected.

For further details on how the Deep Power-Down input signal works, please refer to the M58PR512J datasheet.

2.18 V_{DDF} Supply Voltages

V_{DDF} provides the power supply to the internal cores of the Flash memory. It is the main power supply for all Flash memory operations (Read, Program and Erase).

2.19 V_{CCP} Supply Voltage

V_{CCP} provides the power supply to the internal core of the PSRAM device. It is the main power supply for all PSRAM operations.

2.20 V_{DDQ} Supply Voltage

V_{DDQ} provides the power supply for the Flash memory and PSRAM I/O pins. This allows all Outputs to be powered independently of the Flash memory and SRAM core power supplies, V_{DDF} and V_{CCP}.

2.21 V_{PPF} Program Supply Voltage

V_{PPF} is both a control input and a power supply pin for the Flash memory. The two functions are selected by the voltage range applied to the pin.

If V_{PPF} is kept in a low voltage range (0V to V_{DDQ}) V_{PPF} is seen as a control input. In this case a voltage lower than V_{PPLK} gives an absolute protection against Program or Erase, while V_{PPF} > V_{PP1} enables these functions (see Tables 7 and 8, Flash Memory DC Characteristics for the relevant values). V_{PPF} is only sampled at the beginning of a Program or Erase; a change in its value after the operation has started does not have any effect and Program or Erase operations continue.

If V_{PPF} is in the range of V_{PPH} it acts as a power supply pin. In this condition V_{PPF} must be stable until the Program/Erase algorithm is completed.

2.22 V_{SS} Ground

V_{SS} is the common ground reference for all voltage measurements in the Flash (core and I/O Buffers) and PSRAM chips. It must be connected to the system ground.

Note: Each Flash memory device in a system should have their supply voltage (V_{DDF}) and the program supply voltage V_{PPF} decoupled with a 0.1 μ F ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See [Figure 4., AC Measurement Load Circuit](#). The PCB track widths should be sufficient to carry the required V_{PPF} program and erase currents.

3 Functional description

The PSRAM and Flash memory components have separate power supplies but share the same grounds. They are distinguished by two Chip Enable inputs: \overline{E}_F for Flash and \overline{E}_P for the PSRAM.

Recommended operating conditions do not allow more than one device to be active at a time. The most common example is a simultaneous read operations on the Flash memory and the PSRAM which would result in a data bus contention. Therefore it is recommended to put the other devices in the high impedance state when reading the selected device.

Figure 2. Functional Block Diagram

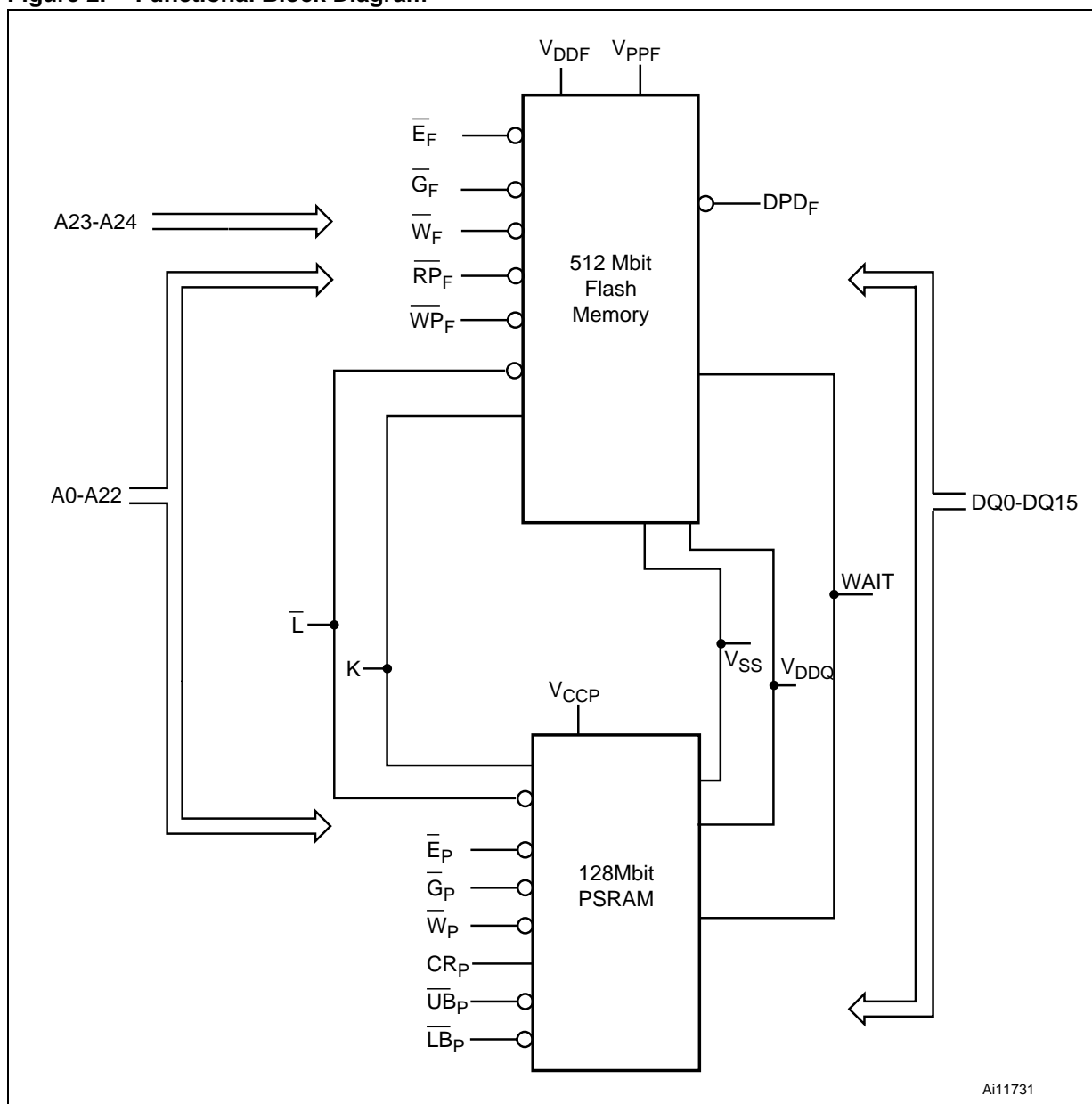


Table 3. Main Operating Modes

| Operation | \bar{E}_F | \bar{G}_F | \bar{W}_F | \bar{L}_F | \bar{R}_P | $WAIT_F^{(4)}$ | \bar{E}_P | CR_P | \bar{G}_P | \bar{W}_P | \bar{L}_P, \bar{U}_P | DQ15-DQ0 |
|-----------------------------------|--|-------------|-------------|----------------|-------------|----------------|--|----------|-------------|-------------|------------------------|---------------------------------------|
| Flash Read | V_{IL} | V_{IL} | V_{IH} | $V_{IL}^{(2)}$ | V_{IH} | | PSRAM must be disabled. Only one Flash memory can be enabled at a time. | | | | | Flash Data Out |
| Flash Write | V_{IL} | V_{IH} | V_{IL} | $V_{IL}^{(2)}$ | V_{IH} | | | | | | | Flash Data In |
| Flash Address Latch | V_{IL} | X | V_{IH} | V_{IL} | V_{IH} | | | | | | | Flash Data Out or Hi-Z ⁽³⁾ |
| Flash Output Disable | V_{IL} | V_{IH} | V_{IH} | X | V_{IH} | | Any PSRAM mode is allowed. Flash memories must be disabled. | | | | | Hi-Z |
| Flash Standby | V_{IH} | X | X | X | V_{IH} | Hi-Z | | | | | | Hi-Z |
| Flash Reset | X | X | X | X | V_{IL} | Hi-Z | | | | | | Hi-Z |
| Flash Deep Power-Down | V_{IH} | X | X | X | V_{IH} | Hi-Z | | | | | | Hi-Z |
| PSRAM Read | Flash memories must be disabled | | | | | | V_{IL} | V_{IL} | V_{IL} | V_{IH} | V_{IL} | PSRAM data out |
| PSRAM Write | | | | | | | V_{IL} | V_{IL} | X | V_{IL} | V_{IL} | PSRAM data in |
| PSRAM Read Configuration Register | | | | | | | V_{IL} | V_{IH} | V_{IL} | V_{IH} | V_{IL} | PSRAM data out |
| PSRAM Standby | Any Flash memory mode is allowed. Only one Flash memory can be enabled at a time | | | | | | V_{IH} | V_{IL} | X | X | X | Hi-Z |
| PSRAM Deep Power-Down | | | | | | | V_{IH} | X | X | X | X | Hi-Z |

Note: 1 X = Don't care

2 \bar{L}_F can be tied to V_{IH} if the valid address has been previously latched

3 Depends on \bar{G}_F

4 $WAIT_F$ signal polarity is configured using the Set Configuration Register command. See the M58PR512J datasheet for details.

4 Maximum rating

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 4. Absolute Maximum Ratings

| Symbol | Parameter | Value | | Unit |
|------------|--------------------------------|-------|------|-------|
| | | Min | Max | |
| T_A | Ambient Operating Temperature | -30 | 85 | °C |
| T_{BIAS} | Temperature Under Bias | -30 | 85 | °C |
| T_{STG} | Storage Temperature | -65 | 125 | °C |
| V_{IO} | Input or Output Voltage | -0.2 | 2.45 | V |
| V_{DD} | Supply Voltage | -0.2 | 2.45 | V |
| V_{DDQ} | Input/Output Supply Voltage | -0.2 | 2.45 | V |
| V_{PP} | Program Voltage | -1.0 | 12.6 | V |
| I_O | Output Short Circuit Current | | 100 | mA |
| t_{VPPH} | Time for V_{PP} at V_{PPH} | | 100 | hours |

5 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in [Table 5., Operating and AC Measurement Conditions](#). Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 5. Operating and AC Measurement Conditions

| Parameter | Flash Memory | | PSRAM | | Unit |
|---|-----------------------|-----------------------|-----------------------|------|------|
| | Min | Max | Min | Max | |
| V _{CCP} Supply Voltage | 1.7 | 1.95 | 1.7 | 1.95 | V |
| V _{DDF} Supply Voltage | 1.7 | 1.95 | 1.7 | 1.95 | V |
| V _{DDQ} Supply Voltage | 1.7 | 1.95 | 1.7 | 1.95 | V |
| V _{PPF} Supply Voltage (Factory environment) | 8.5 | 9.5 | – | – | V |
| V _{PPF} Supply Voltage (Application environment) | –0.4 | V _{DDQ} +0.4 | – | – | V |
| Ambient Operating Temperature | –30 | 85 | –30 | 85 | °C |
| Load Capacitance (C _L) | 30 | | 30 | | pF |
| Impedance Output (Z ₀) | 50 | | | | Ω |
| Output Circuit Protection Resistance (R) | 50 | | | | Ω |
| Input Rise and Fall Times | | 3 | | | ns |
| Input Pulse Voltages | 0 to V _{DDQ} | | 0 to V _{DDQ} | | V |
| Input and Output Timing Ref. Voltages | V _{DDQ} /2 | | V _{DDQ} /2 | | V |

Figure 3. AC Measurement I/O Waveform

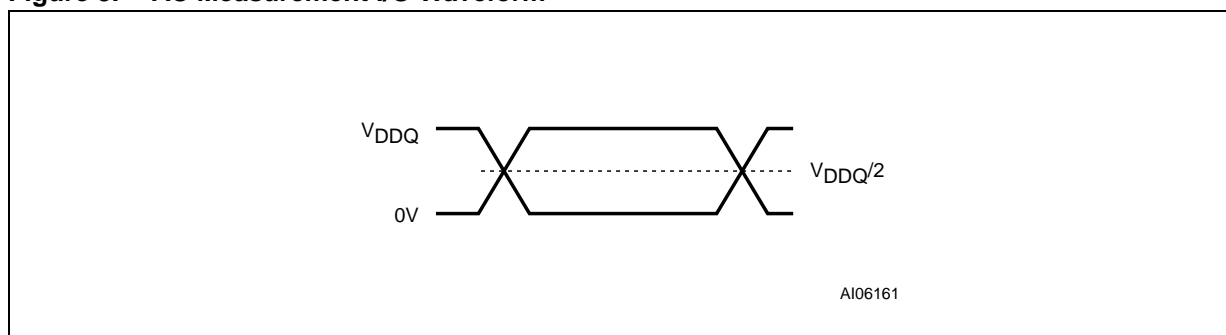
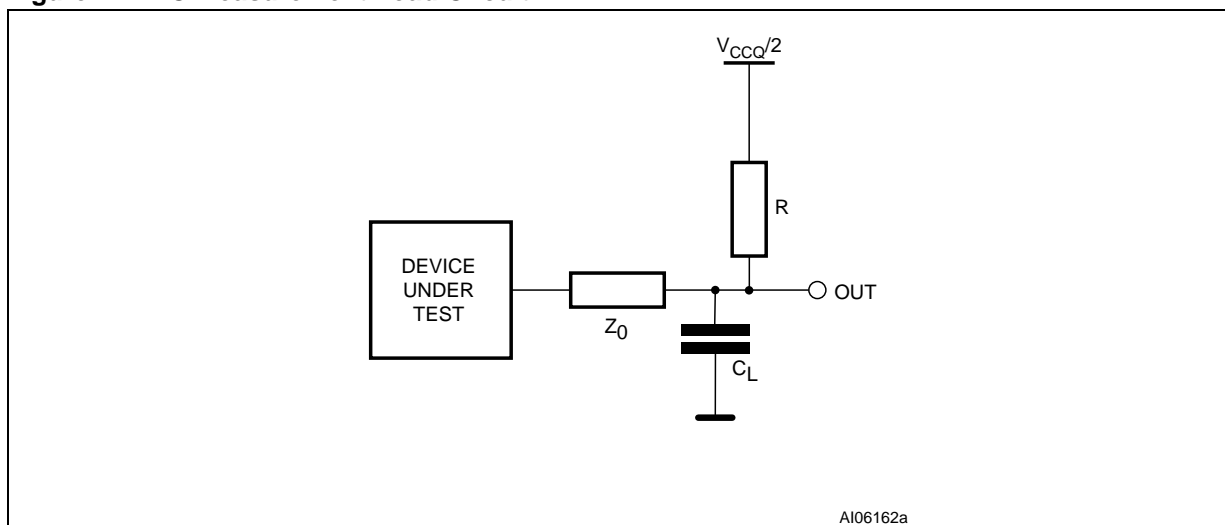


Figure 4. AC Measurement Load Circuit**Table 6. Capacitance**

| Symbol | Parameter | Test Condition | Min | Max | Unit |
|-----------|--------------------|----------------|-----|-----|------|
| C_{IN} | Input Capacitance | $V_{IN} = 0V$ | | 14 | pF |
| C_{OUT} | Output Capacitance | $V_{OUT} = 0V$ | | 14 | pF |

1. Sampled only, not 100% tested.

Table 7. Flash Memory DC Characteristics - Currents

| Symbol | Parameter | Test Condition | | Typ | Max | Unit |
|--------------------|--|--|----------|------|---------|---------|
| I_{LI} | Input Leakage Current | $0V \leq V_{IN} \leq V_{DDQ}$ | | | ± 1 | μA |
| I_{LO} | Output Leakage Current | $0V \leq V_{OUT} \leq V_{DDQ}$ | | | ± 1 | μA |
| I_{DD1} | Supply Current Asynchronous Read (f=5MHz) | $\bar{E}_F = V_{IL}, \bar{G}_F = V_{IH}$ | | 25 | 30 | mA |
| | Supply Current Page Read (f=13MHz) | | | 11 | 15 | mA |
| | Supply Current Synchronous Read (f=66MHz) | 8 Word | | 22 | 32 | mA |
| | | 16 Word | | 19 | 26 | mA |
| | | Continuous | | 25 | 34 | mA |
| | Supply Current Synchronous Read (f = 108MHz) | 8 Word | | 26 | 36 | mA |
| 16 Word | | 23 | 30 | mA | | |
| Continuous | | 30 | 42 | mA | | |
| I_{DD2} | Supply Current (Reset) | $R\bar{P}_F = V_{SS} \pm 0.2V$ | 512 Mbit | 50 | 120 | μA |
| I_{DD3} | Supply Current (Standby) | $\bar{E}_F = V_{DDF} \pm 0.2V$ | | 50 | 120 | μA |
| I_{DD4} | Supply Current (Automatic Standby) | $\bar{E}_F = V_{IL}, \bar{G}_F = V_{IH}$ | 512 Mbit | 50 | 120 | μA |
| $I_{DD5}^{(1)}$ | Supply Current (Deep Power Down) | | | 2 | 30 | μA |
| $I_{DD6}^{(2)}$ | Supply Current (Program) | $V_{PPF} = V_{PPH}$ | | 35 | 50 | mA |
| | | $V_{PPF} = V_{DDF}$ | | 35 | 50 | mA |
| | Supply Current (Erase) | $V_{PPF} = V_{PPH}$ | | 35 | 50 | mA |
| | | $V_{PPF} = V_{DDF}$ | | 35 | 50 | mA |
| | Supply Current (Blank Check) | $V_{PPF} = V_{PPH}$ | | 35 | 50 | mA |
| | | $V_{PPF} = V_{DDF}$ | | 35 | 50 | mA |
| $I_{DD7}^{(2)(3)}$ | Supply Current (Dual Operations) | Program/Erase in one Bank, Asynchronous Read in another Bank | | 60 | 80 | mA |
| | | Program/Erase in one Bank, Synchronous Read (Continuous f=66MHz) in another Bank | | 65 | 92 | mA |
| $I_{DD8}^{(2)}$ | Supply Current Program/ Erase Suspended (Standby) | $\bar{E}_F = V_{DDF} \pm 0.2V$ | 512 Mbit | 50 | 120 | μA |
| $I_{PP1}^{(2)}$ | V_{PPF} Supply Current (Program) | $V_{PPF} = V_{PPH}$ | | 8 | 22 | mA |
| | | $V_{PPF} = V_{DDF}$ | | 0.05 | 0.1 | μA |
| | V_{PPF} Supply Current (Erase) | $V_{PPF} = V_{PPH}$ | | 8 | 22 | mA |
| | | $V_{PPF} = V_{DDF}$ | | 0.05 | 0.1 | μA |
| I_{PP2} | V_{PPF} Supply Current (Read) | $V_{PPF} \leq V_{DDF}$ | | 2 | 15 | μA |
| $I_{PP3}^{(2)}$ | V_{PPF} Supply Current (Standby, Program/Erase Suspend) | $V_{PPF} \leq V_{DDF}$ | | 0.2 | 5 | μA |
| I_{PP4} | V_{PPF} Supply Current (Blank Check) | $V_{PPF} = V_{PPH}$ | | 0.05 | 0.1 | mA |
| | | $V_{PPF} = V_{PP1}$ | | 0.05 | 0.1 | mA |

1. The DPD current is measured 40 μs after entering the Deep Power Down mode.
2. Sampled only, not 100% tested.
3. V_{DDF} Dual Operation current is the sum of read and program or erase currents.

Table 8. Flash Memory DC Characteristics - Voltages

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|------------|---|----------------------|-----------------|-----|-----------------|------|
| V_{IL} | Input Low Voltage | | 0 | | 0.4 | V |
| V_{IH} | Input High Voltage | | $V_{DDQ} - 0.4$ | | $V_{DDQ} + 0.4$ | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 100\mu A$ | | | 0.1 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -100\mu A$ | $V_{DDQ} - 0.1$ | | | V |
| V_{PP1} | V_{PPF} Program Voltage-Logic | Program, Erase | 1.1 | 1.8 | 3.3 | V |
| V_{PPH} | V_{PPF} Program Voltage Factory | Program, Erase | 8.5 | 9.0 | 9.5 | V |
| V_{PPLK} | Program or Erase Lockout | | | | 0.4 | V |
| V_{LKO} | V_{DDF} Lock Voltage | | 1 | | | V |
| V_{RPH} | \overline{RP}_F pin Extended High Voltage | | | | 3.3 | V |
| V_{LKOQ} | V_{DDQ} Lock Voltage | | 0.9 | | | V |

Table 9. PSRAM DC Characteristics

| Symbol | Parameter | Refreshed Array | Test Conditions | Min. | Typ. | Max. | Unit |
|------------------|--|-----------------|--|-----------------|------|-----------------|---------------|
| $V_{OH}^{(3)}$ | Output High Voltage | | $I_{OH} = -0.2\text{mA}$ | $0.8V_{DDQ}$ | | | V |
| $V_{OL}^{(3)}$ | Output Low Voltage | | $I_{OL} = 0.2\text{mA}$ | | | $0.2V_{DDQ}$ | V |
| $V_{IH}^{(1)}$ | Input High Voltage | | | $V_{DDQ} - 0.4$ | | $V_{DDQ} + 0.2$ | V |
| $V_{IL}^{(2)}$ | Input Low Voltage | | | -0.2 | | 0.4 | V |
| I_{LI} | Input Leakage Current | | $V_{IN} = 0 \text{ to } V_{DDQ}$ | | | 1 | μA |
| I_{LO} | Output Leakage Current | | $\bar{G}_P = V_{IH} \text{ or } \bar{E}_P = V_{IH}$ | | | 1 | μA |
| $I_{CC1}^{(4)}$ | Asynchronous Read/Write Random at t_{RC} min | | $V_{IN} = 0\text{V or } V_{DDQ}$, $I_{OUT} = 0\text{mA}, \bar{E}_P = V_{IL}$ | 70ns | | 25 | mA |
| | | | | 85ns | | 22 | mA |
| $I_{CC2}^{(4)}$ | Asynchronous Page Read | | $V_{IN} = 0\text{V or } V_{DDQ}$, $I_{OUT} = 0\text{mA}, \bar{E}_P = V_{IL}$ | 70ns | | 15 | mA |
| | | | | 85ns | | 12 | mA |
| $I_{CC3}^{(4)}$ | Burst, Initial Read/Write Access | | $V_{IN} = 0\text{V or } V_{DDQ}$, $I_{OUT} = 0\text{mA}, \bar{E}_P = V_{IL}$ | 104MHz | | 35 | mA |
| | | | | 80MHz | | 30 | mA |
| | | | | 66MHz | | 25 | mA |
| $I_{CC4R}^{(4)}$ | Continuous Burst Read | | $V_{IN} = 0\text{V or } V_{DDQ}$, $I_{OUT} = 0\text{mA}, \bar{E}_P = V_{IL}$ | 104MHz | | 30 | mA |
| | | | | 80MHz | | 25 | mA |
| | | | | 66MHz | | 20 | mA |
| $I_{CC4W}^{(4)}$ | Continuous Burst Write | | $V_{IN} = 0\text{V or } V_{DDQ}$, $I_{OUT} = 0\text{mA}, \bar{E}_P = V_{IL}$ | 104MHz | | 35 | mA |
| | | | | 80MHz | | 30 | mA |
| | | | | 66MHz | | 25 | mA |
| $I_{PASR}^{(4)}$ | Partial Array Refresh Standby Current | Full Array | $V_{IN} = 0\text{V or } V_{DDQ}$, $\bar{E}_P = V_{DDQ}$ | | | 200 | μA |
| | | 1/2 Array | | | | 170 | μA |
| | | 1/4 Array | | | | 155 | μA |
| | | 1/8 Array | | | | 150 | μA |
| | | None | | | | 140 | μA |
| $I_{SB}^{(5)}$ | Standby Current | | $V_{IN} = 0\text{V or } V_{DDQ}$, $\bar{E}_P = V_{DDQ}$ | | | 200 | μA |
| I_{CCPD} | Deep-Power Down Current | | $V_{IN} = 0\text{V or } V_{DDQ}$, $V_{CCP}, V_{DDQ} = 1.95\text{V}; T_A = +85^\circ\text{C}$ | | 3 | 10 | μA |

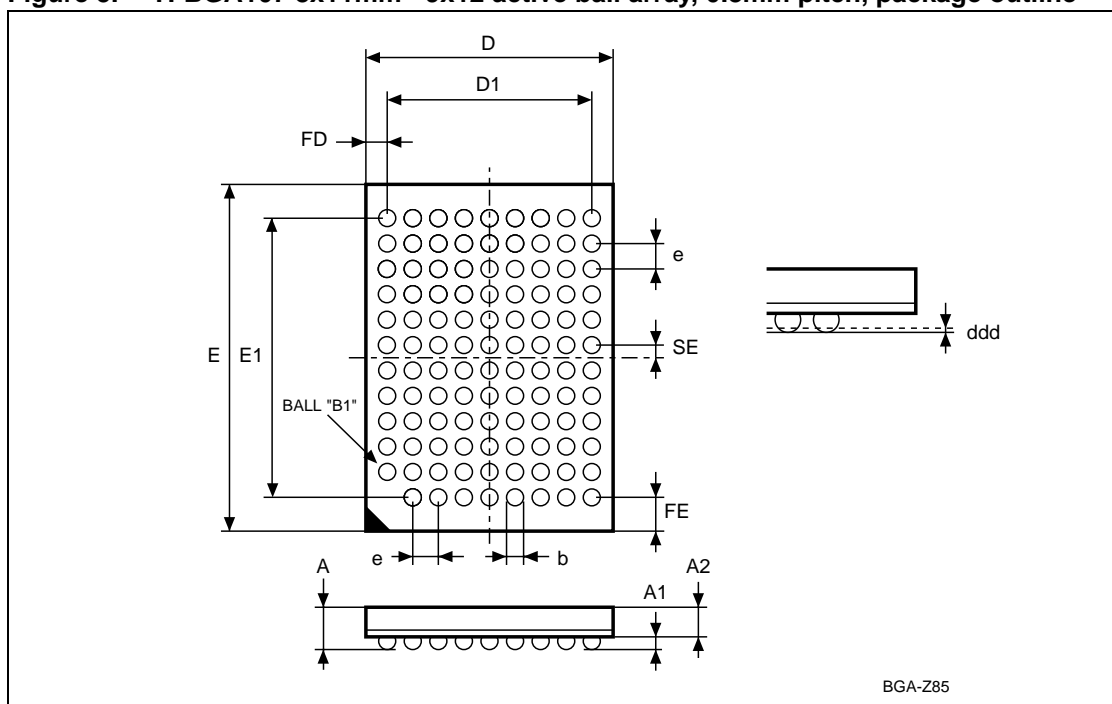
- Input signals may overshoot to $V_{DDQ} + 1.0\text{V}$ for periods of less than 2ns during transitions.
- Output signals may undershoot to $V_{SS} - 1.0\text{V}$ for periods of less than 2ns during transitions.
- BCR5-BCR4 = 01 (default settings).
- This parameter is specified with all outputs disabled to avoid external loading effects. The user must add the current required to drive output capacitance expected for the actual system.
- I_{SB} maximum value is measured at $+85^\circ\text{C}$ with PAR set to Full Array. In order to achieve low standby current, all inputs must be driven either to V_{DDQ} or V_{SSQ} . I_{SB} might be slightly higher for up to 500ms after Power-up, or when entering Standby mode.

6 Package mechanical

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second-level interconnect. The category of Second-Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97.

The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 5. TFBGA107 8x11mm - 9x12 active ball array, 0.8mm pitch, package outline



1. Drawing is not to scale.

Table 10. Stacked TFBGA107 8x11mm - 9x12 active ball array, 0.8mm pitch, package data

| Symbol | millimeters | | | inches | | |
|--------|-------------|-------|-------|--------|-------|-------|
| | Typ | Min | Max | Typ | Min | Max |
| A | | | 1.20 | | | 0.047 |
| A1 | | 0.20 | | | 0.008 | |
| A2 | 0.85 | | | 0.033 | | |
| b | 0.35 | 0.30 | 0.40 | 0.014 | 0.012 | 0.016 |
| D | 8.00 | 7.90 | 8.10 | 0.315 | 0.311 | 0.319 |
| D1 | 6.40 | | | 0.252 | | |
| ddd | | | 0.10 | | | 0.004 |
| E | 11.00 | 10.90 | 11.10 | 0.433 | 0.429 | 0.437 |
| E1 | 8.80 | | | 0.346 | | |
| e | 0.80 | | | 0.031 | | |
| FD | 0.80 | | | 0.031 | | |
| FE | 1.10 | | | 0.043 | | |
| SE | 0.40 | | | 0.016 | | |

7 Part numbering

Table 11. Ordering Information Scheme

| | M36 | P | 0 | R | 9 | 0 | 7 | 0 | E | 0 | ZAC | E |
|--|-----|---|---|---|---|---|---|---|---|---|-----|---|
| Example: | | | | | | | | | | | | |
| Device Type | | | | | | | | | | | | |
| M36 = Multi-Chip Package (Multiple Flash + PSRAM) | | | | | | | | | | | | |
| Flash 1 Architecture | | | | | | | | | | | | |
| P = Multi-Level, Multiple Bank, Large Buffer | | | | | | | | | | | | |
| Flash 2 Architecture | | | | | | | | | | | | |
| 0 = No Die | | | | | | | | | | | | |
| Operating Voltage | | | | | | | | | | | | |
| $R = V_{DDF} = V_{CCP} = V_{DDQ} = 1.7 \text{ to } 1.95\text{V}$ | | | | | | | | | | | | |
| Flash 1 Density | | | | | | | | | | | | |
| 9 = 512 Mbits | | | | | | | | | | | | |
| Flash 2 Density | | | | | | | | | | | | |
| 0 = No Die | | | | | | | | | | | | |
| RAM 1 Density | | | | | | | | | | | | |
| 7 = 128 Mbits | | | | | | | | | | | | |
| RAM 0 Density | | | | | | | | | | | | |
| 0 = No Die | | | | | | | | | | | | |
| Parameter Blocks Location | | | | | | | | | | | | |
| E = Even Block Flash Memory Configuration | | | | | | | | | | | | |
| Product Version | | | | | | | | | | | | |
| 0 = 90nm Flash technology, 93ns speed; PSRAM | | | | | | | | | | | | |
| Package | | | | | | | | | | | | |
| ZAC= stacked TFBGA107 C stacked footprint. | | | | | | | | | | | | |
| Option | | | | | | | | | | | | |
| Blank = Standard Packing | | | | | | | | | | | | |
| E = ECOPACK® Package, Standard packing | | | | | | | | | | | | |
| F = ECOPACK® Package, Tape & Reel packing | | | | | | | | | | | | |

Note: Devices are shipped from the factory with the memory content bits erased to '1'. For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

8 Revision history

Table 12. Document revision history

| Date | Revision | Changes |
|-------------|----------|------------------|
| 28-Nov-2005 | 1 | Initial release. |

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