M36W0R5020T0
M36W0R5020B0

32 Mbit (2Mb x16, Multiple Bank, Burst) Flash Memory and 4 Mbit SRAM, 1.8V Supply Multi-Chip Package

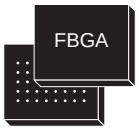
FEATURES SUMMARY

- MULTI-CHIP PACKAGE
  - 1 die of 32 Mbit (2Mb x 16) Flash Memory
  - 1 die of 4 Mbit (256Kb x16) SRAM
- SUPPLY VOLTAGE
  - V_{DDF} = V_{DDQ} = V_{DDS} = 1.7 to 1.95V
- LOW POWER CONSUMPTION
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Device Code (Top Flash Configuration): 8814h
  - Device Code (Bottom Flash Configuration): 8815h
- PACKAGE
  - Compliant with Lead-Free Soldering Processes
  - Lead-Free Versions

FLASH MEMORY

- PROGRAMMING TIME
  - 8µs by Word typical for Fast Factory Program
  - Double/Quadruple Word Program option
  - Enhanced Factory Program options
- MEMORY BLOCKS
  - Multiple Bank Memory Array: 4 Mbit Banks
  - Parameter Blocks (Top or Bottom location)
- SYNCHRONOUS / ASYNCHRONOUS READ
  - Synchronous Burst Read mode: 66MHz
  - Asynchronous/ Synchronous Page Read mode
  - Random Access: 70ns
- DUAL OPERATIONS
  - Program Erase in one Bank while Read in others
  - No delay between Read and Write operations

Figure 1. Package



Stacked TFBGA88
(ZAQ)

- BLOCK LOCKING
  - All blocks locked at Power-up
  - Any combination of blocks can be locked
  - $\overline{WP}_F$ for Block Lock-Down
- SECURITY
  - 128-bit user programmable OTP cells
  - 64-bit unique device number
- COMMON FLASH INTERFACE (CFI)
- 100,000 PROGRAM/ERASE CYCLES per BLOCK

SRAM

- ACCESS TIME: 70ns
- LOW V_{DDS} DATA RETENTION: 1.0V
- POWER DOWN FEATURES USING TWO CHIP ENABLE INPUTS

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SUMMARY DESCRIPTION

The M36W0R5020T0 and M36W0R5020B0 combine two memory devices in a Multi-Chip Package:

- a 32-Mbit, Multiple Bank Flash memory, the M58WR032FT/B
- and a 4-Mbit SRAM.

Recommended operating conditions do not allow more than one memory to be active at the same time.

The memory is offered in a Stacked TFBGA88 (8 x 10mm, 8x10 ball array, 0.8mm pitch) package.

In addition to the standard version, the package is also available in Lead-free version, in compliance with JEDEC Std J-STD-020B, the ST ECOPACK 7191395 Specification, and the RoHS (Restriction of Hazardous Substances) directive. All packages are compliant with Lead-free soldering processes.

The memory supplied with all the bits erased (set to '1').

Figure 2. Logic Diagram

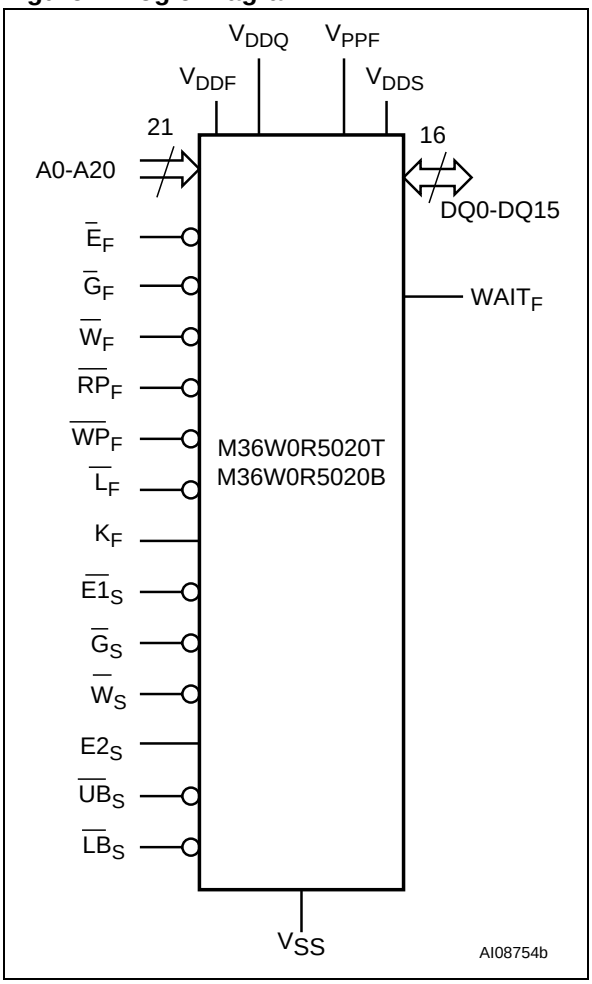
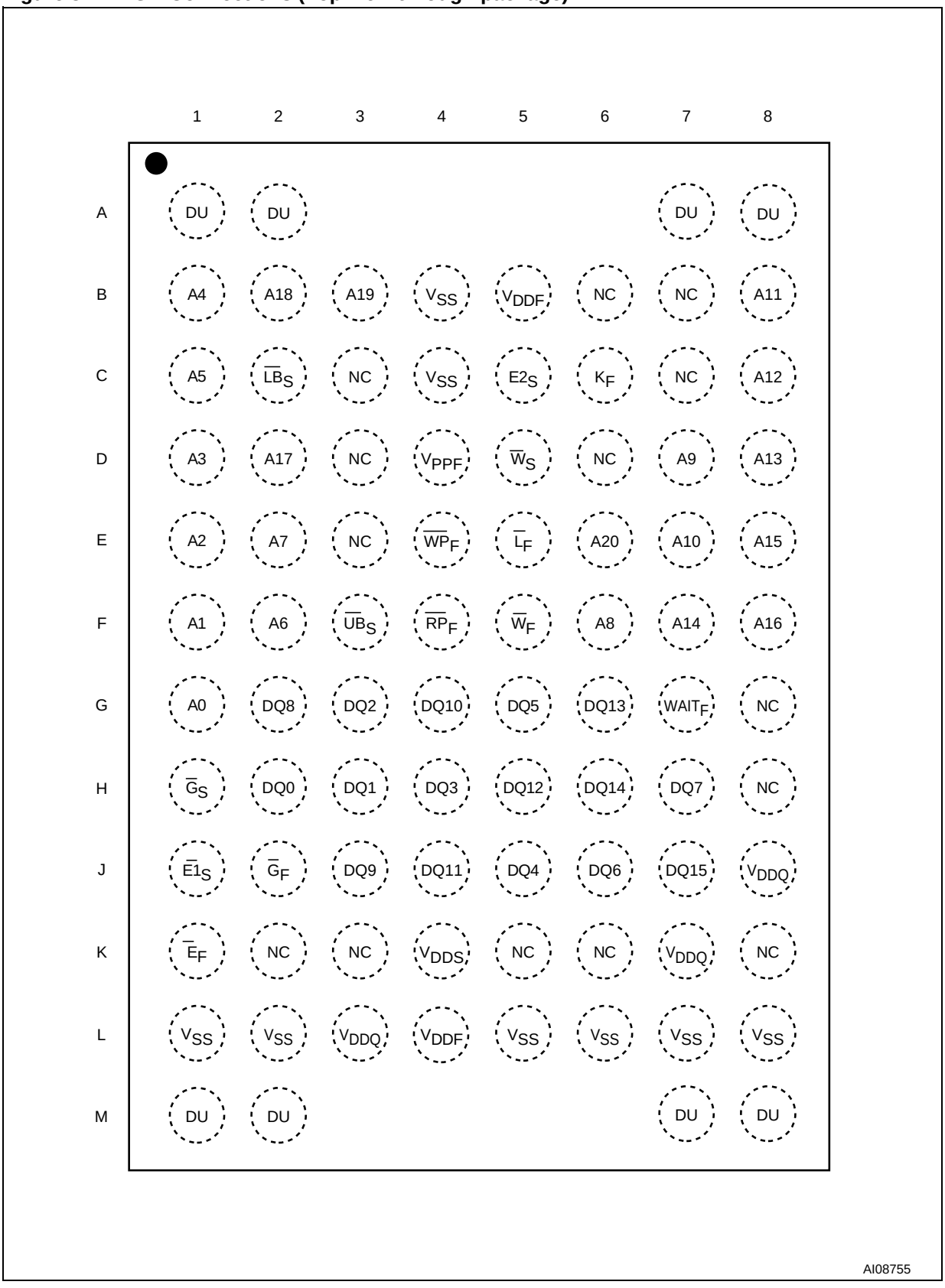


Table 1. Signal Names

A0-A20 (1)	Address Inputs
DQ0-DQ15	Common Data Input/Output
V_{DDF}	Flash Memory Power Supply
V_{DDQ}	Common Flash and SRAM Power Supply for I/O Buffers
V_{PPF}	Common Flash Optional Supply Voltage for Fast Program and Erase
V_{SS}	Ground
V_{DDS}	SRAM Power Supply
NC	Not Connected Internally
DU	Do Not Use as Internally Connected
Flash Memory	
$\overline{L}_F$	Latch Enable input
$\overline{E}_F$	Chip Enable input
$\overline{G}_F$	Output Enable input
$\overline{W}_F$	Write Enable input
$\overline{RP}_F$	Reset input
$\overline{WP}_F$	Write Protect input
K_F	Burst Clock
$WAIT_F$	Wait Data in Burst Mode
SRAM	
$\overline{E1}_S$, $E2_S$	Chip Enable input
$\overline{G}_S$	Output Enable input
$\overline{W}_S$	Write Enable input
$\overline{UB}_S$	Upper Byte Enable input
$\overline{LB}_S$	Lower Byte Enable input

Note: 1. A20-A18 are address inputs for the Flash memory component only.

Figure 3. TFBGA Connections (Top view through package)



SIGNAL DESCRIPTIONS

See Figure 2., Logic Diagram and Table 1., Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A0-A20). Addresses A0-A17 are common inputs for the Flash memory and SRAM components. The other lines (A18-A20) are inputs for the Flash memory component only.

The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine. The Flash memory is accessed through the Chip Enable signal ($\overline{E}_F$) and through the Write Enable (W_F) signal, while the SRAM is accessed through two Chip Enable signals ($E1_S$ and $E2_S$) and the Write Enable signal (W_S).

Data Input/Output (DQ0-DQ15). The Data I/O output the data stored at the selected address during a Bus Read operation or input a command or the data to be programmed during a Write Bus operation.

Flash Chip Enable ($\overline{E}_F$). The Chip Enable input activates the Flash memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is Low, V_{IL}, and Reset is High, V_{IH}, the device is in active mode. When Chip Enable is at V_{IH} the Flash memory is deselected, the outputs are high impedance and the power consumption is reduced to the standby level.

It is not allowed to set $\overline{E}_F$ at V_{IL}, $\overline{E1}_S$ at V_{IL} and $E2_S$ at V_{IH} at the same time.

Flash Output Enable ($\overline{G}_F$). The Output Enable pin controls data outputs during Flash memory Bus Read operations.

Flash Write Enable ($\overline{W}_F$). The Write Enable input controls the Bus Write operation of the Flash memory's Command Interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable whichever occurs first.

Flash Write Protect ($\overline{WP}_F$). Write Protect is an input that gives an additional hardware protection for each block. When Write Protect is Low, V_{IL}, Lock-Down is enabled and the protection status of the Locked-Down blocks cannot be changed. When Write Protect is at High, V_{IH}, Lock-Down is disabled and the Locked-Down blocks can be locked or unlocked. (Refer to Lock Status Table in M58WR032FT/B datasheet).

Flash Reset ($\overline{RP}_F$). The Reset input provides a hardware reset of the memory. When Reset is at V_{IL}, the memory is in Reset mode: the outputs are high impedance and the current consumption is reduced to the Reset Supply Current I_{DD2}. Refer to Table 6., Flash Memory DC Characteristics - Currents, for the value of I_{DD2}. After Reset all blocks are in the Locked state and the Configuration Register is reset. When Reset is at V_{IH}, the device is in normal operation. Exiting Reset mode the device enters Asynchronous Read mode, but a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs.

The Reset pin can be interfaced with 3V logic without any additional circuitry. It can be tied to V_{RPH} (refer to Table 7., Flash Memory DC Characteristics - Voltages).

Flash Latch Enable ($\overline{L}_F$). Latch Enable latches the address bits on its rising edge. The address latch is transparent when Latch Enable is Low, V_{IL}, and it is inhibited when Latch Enable is High, V_{IH}. Latch Enable can be kept Low (also at board level) when the Latch Enable function is not required or supported.

Flash Clock (K_F). The Clock input synchronizes the Flash memory to the microcontroller during synchronous read operations; the address is latched on a Clock edge (rising or falling, according to the configuration settings) when Latch Enable is at V_{IL}. Clock is don't care during Asynchronous Read and in write operations.

Flash Wait ($WAIT_F$). WAIT is a Flash memory output signal used during Synchronous Read to indicate whether the data on the output bus are valid. This output is high impedance when the Flash memory Chip Enable is at V_{IH} or Reset is at V_{IL}. It can be configured to be active during the wait cycle or one clock cycle in advance. The $WAIT_F$ signal is not gated by Output Enable.

SRAM Chip Enable inputs ($E1_S$, $E2_S$). The Chip Enable inputs activate the SRAM memory control logic, input buffers and decoders. $E1_S$ at V_{IH} with $E2_S$ at V_{IH} deselects the memory, reducing the power consumption to the standby level, whereas $E2_S$ at V_{IL} deselects the memory and reduces the power consumption to the Power-down level, regardless of the level of $E1_S$. $E1_S$ and $E2_S$ can also be used to control writing to the SRAM memory array, while W_S remains at V_{IL}. It is not allowed to set $\overline{E}_F$ at V_{IL}, $E1_S$ at V_{IL} and $E2_S$ at V_{IH} at the same time.

SRAM Write Enable ($\overline{W}_S$). The Write Enable input controls writing to the SRAM memory array. W_S is active low.

SRAM Output Enable ($\overline{G}_S$). The Output Enable gates the outputs through the data buffers during a Read operation of the SRAM memory. G_S is active low.

SRAM Upper Byte Enable ($\overline{UB}_S$). The Upper Byte Enable input enables the upper byte for SRAM (DQ8-DQ15). UB_S is active low.

SRAM Lower Byte Enable ($\overline{LB_S}$). The Lower Byte Enable input enables the lower byte for SRAM (DQ0-DQ7). $\overline{LB_S}$ is active low.

V_{DDF} Supply Voltage. V_{DDF} provides the power supply to the internal core of the Flash memory component. It is the main power supply for all Flash memory operations (Read, Program and Erase).

V_{DDS} Supply Voltage. V_{DDS} provides the power supply to the internal core of the SRAM device. It is the main power supply for all SRAM operations.

V_{DDQ} Supply Voltage. V_{DDQ} provides the power supply for the Flash memory and SRAM I/O pins. This allows all Outputs to be powered independently of the Flash memory and SRAM core power supplies: V_{DDF} and V_{DDS}, respectively.

V_{PPF} Program Supply Voltage. V_{PPF} is a Flash memory power supply pin. The Supply Voltage V_{DDF} and the Program Supply Voltage V_{PP} can be applied in any order. The pin can also be used as a control input for the Flash memory.

The two functions are selected by the voltage range applied to the pin. If V_{PPF} is kept in a low voltage range (0V to V_{DDQ}) V_{PPF} is seen as a control input. In this case a voltage lower than V_{PPLK} gives an absolute protection against program or erase, while $V_{PPF} > V_{PP1}$ enables these functions (see Tables 6 and 7, DC Characteristics for the relevant values). V_{PPF} is only sampled at the beginning of a program or erase; a change in its value after the operation has started does not have any effect and program or erase operations continue.

If V_{PPF} is in the range of V_{PPH} it acts as a power supply pin. In this condition V_{PPF} must be stable until the Program/Erase algorithm is completed.

V_{SS} Ground. V_{SS} is the common ground reference for all voltage measurements in the Flash memory (core and I/O Buffers) and SRAM components.

Note: Each Flash memory device in a system should have its supply voltage (V_{DDF}) and the program supply voltage V_{PPF} decoupled with a 0.1µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See Figure 7., AC Measurement Load Circuit. The PCB track widths should be sufficient to carry the required V_{PPF} program and erase currents.

FUNCTIONAL DESCRIPTION

The Flash memory and SRAM components have separate power supplies but share the same grounds. They are distinguished by three Chip Enable inputs: E_F for the Flash memory and $E1_S$ and $E2_S$ for the SRAM.

Recommended operating conditions do not allow more than one device to be active at a time. The most common example is simultaneous read operations on the Flash memory and SRAM components which would result in a data bus contention. Therefore it is recommended to put the other devices in the high impedance state when reading the selected device.

Figure 4. Functional Block Diagram

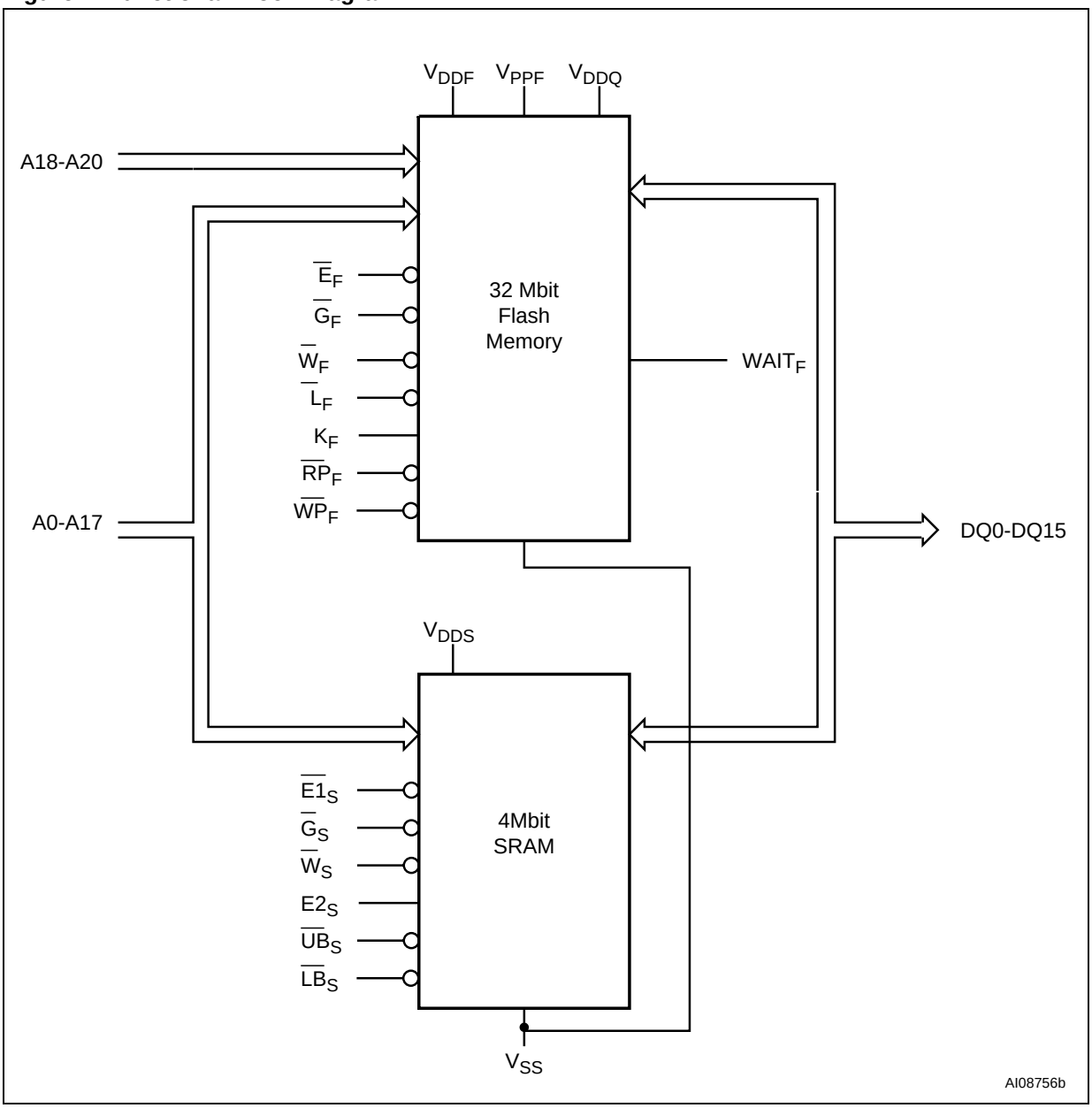


Table 2. Main Operating modes

Operation	$\overline{E}_F$	$\overline{G}_F$	$\overline{W}_F$	$\overline{L}_F$	$\overline{RP}_F$	$WAIT_F$(4)	$\overline{E1}_S$	$\overline{E2}_S$	$\overline{G}_S$	$\overline{W}_S$	$\overline{UB}_S$	$\overline{LB}_S$	DQ15-DQ0
Flash Read	V_{IL}	V_{IL}	V_{IH}	V_{IL}(2)	V_{IH}		SRAM must be disabled						Flash Data Out
Flash Write	V_{IL}	V_{IH}	V_{IL}	V_{IL}(2)	V_{IH}								Flash Data In
Flash Address Latch	V_{IL}	X	V_{IH}	V_{IL}	V_{IH}								Flash Data Out or Hi-Z (3)
Flash Output Disable	V_{IL}	V_{IH}	V_{IH}	X	V_{IH}		Any SRAM mode is allowed						Flash Hi-Z
Flash Standby	V_{IH}	X	X	X	V_{IH}	Hi-Z							Flash Hi-Z
Flash Reset	X	X	X	X	V_{IL}	Hi-Z							Flash Hi-Z
SRAM Read	Flash Memory must be disabled						V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	SRAM data out
SRAM Write							V_{IL}	V_{IH}	X	V_{IL}	V_{IL}	V_{IL}	SRAM data in
Output Disable	Any Flash mode is allowed.						V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	SRAM Hi-Z
SRAM Standby							V_{IH}	X	X	X	X	X	SRAM Hi-Z
							X	V_{IL}	X	X	X	X	SRAM Hi-Z

Note: 1. X = Don't care.
2. L_F can be tied to V_{IH} if the valid address has been previously latched.
3. Depends on $\overline{G}_F$.
4. WAIT signal polarity is configured using the Set Configuration Register command. Refer to M58WR032FT/B datasheet for details.

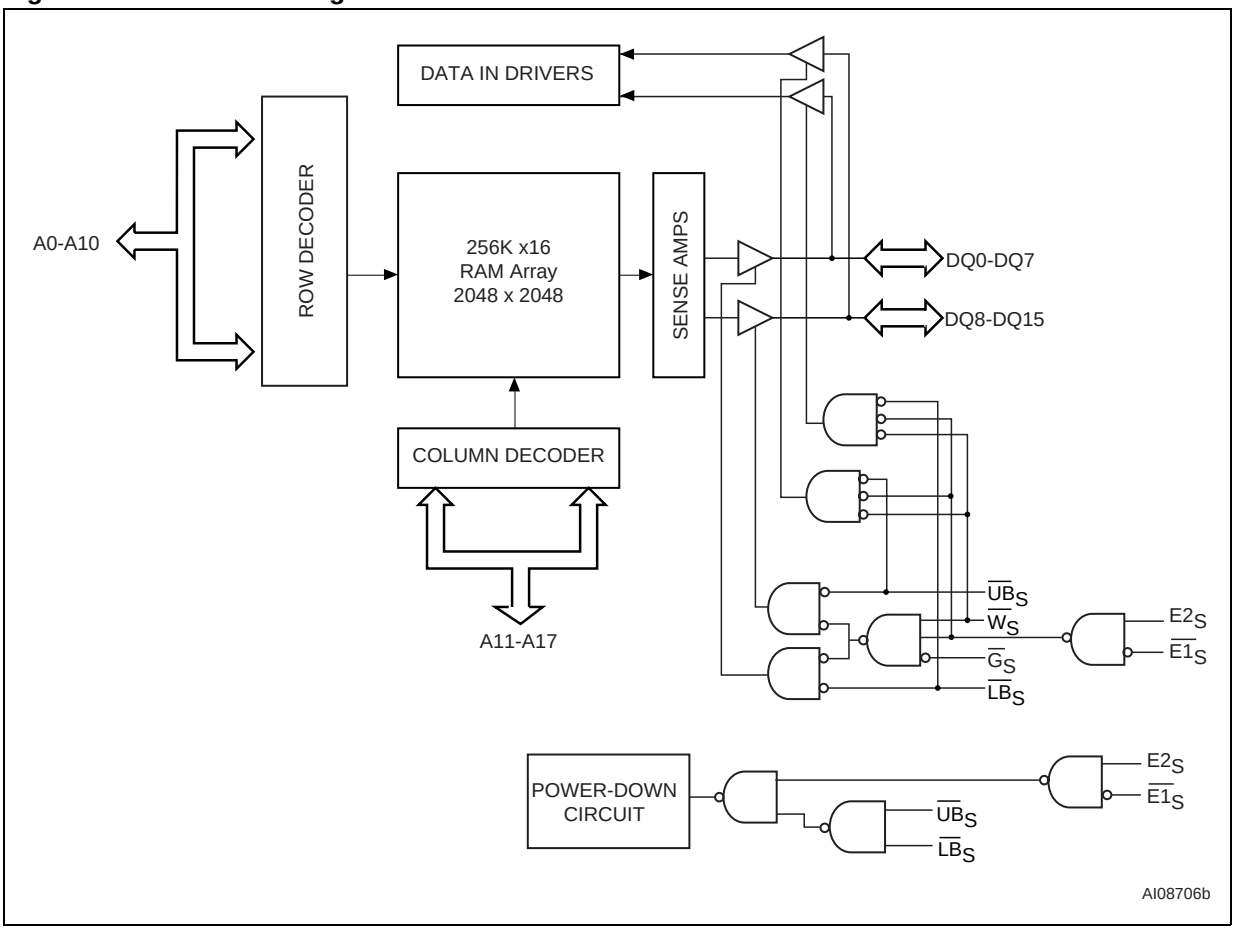
FLASH MEMORY COMPONENT

The M36W0R5020T0 and M36W0R5020B0 contain a 32 Mbit Flash memory. For detailed information on how to use it, see the M58WR032FT/B datasheet which is available from your local STMicroelectronics distributor.

SRAM COMPONENT

The M36W0R5020T0 and M36W0R5020B0 contain a 4 Mbit SRAM. See Figure 5., SRAM Block Diagram in conjunction with the SRAM OPERATIONS section, Table 2., Main Operating modes and the SRAM AC Waveforms and Characteristics for details.

Figure 5. SRAM Block Diagram



SRAM OPERATIONS

There are five standard operations that control the device. These are Read, Write, Standby/Power-down, Data Retention and Output Disable.

Read. Read operations are used to output the contents of the SRAM Array.

The device is in Byte Read mode whenever Write Enable, W_S, is at V_{IH}, Output Enable, G_S, is at V_{IL}, Chip Enable, $E1_S$, is at V_{IL}, Chip Enable, $E2_S$, is at V_{IH}, and UB_S or LB_S is at V_{IL}.

The device is in Word Read mode whenever Write Enable, W_S, is at V_{IH}, Output Enable, G_S, is at V_{IL}, Byte Enable inputs UB_S and LB_S are both at V_{IL} and the two Chip Enable inputs, $E1_S$, and $E2_S$ are Don't Care.

The Read and Standby AC Waveforms are shown in Figures 9 and 10, respectively and the parameters are given in Table 9., SRAM Read AC Characteristics.

Write. Write operations are used to write data to the SRAM. The device is in Write mode whenever W_S, $E1_S$ and UB_S and/or LB_S are at V_{IL}, and $E2_S$ is at V_{IH}. All these signals must be asserted to initiate a Write cycle. The data is latched on the falling edge of $E1_S$, the rising edge of $E2_S$, the falling edge of W_S, or the falling edge of UB_S and/or LB_S, whichever occurs last. The Write cycle will terminate on the rising edge of $E1_S$, the rising edge of W_S, the rising edge of UB_S and/or LB_S, or the falling edge of $E2_S$, whichever occurs first. The timings are referenced to the signal that terminates the Write cycle.

The outputs are disabled during Write cycles (whenever $E1_S$, at V_{IL}, $E2_S$ at V_{IH}, and W_S at V_{IL}).

The Write AC Waveforms are shown in Figures 11, 12, 13 and 14, while Table 10. gives the Write AC Characteristics.

Standby/Power-Down. The device automatically enters the Standby/Power-Down mode when DQ0-DQ15 are not toggling, reducing the power consumption to the Standby level, I_{SB}.

The device is also in Standby/Power-Down mode whenever $E1_S$ is at V_{IH}, $E2_S$ is at V_{IL} or both UB_S and LB_S are at V_{IH}. The outputs then become high impedance.

The Standby AC Waveforms are shown in Figure 10. See Table 9., SRAM Read AC Characteristics, for timings.

Data Retention. The data retention mode is entered t_{CDR} after de-asserting $E1_S$, $E2_S$ or UB_S and LB_S. The data retention performance as V_{DD} goes down to V_{DR} is described in Table 11., Figures 15 and 16, SRAM Low V_{DDS} Data Retention AC Waveforms, $E1_S$ or UB_S / LB_S Controlled and SRAM Low V_{DDS} Data Retention AC Waveforms, $E2_S$ Controlled, respectively.

Output Disable. The device is in the Output Disable mode whenever G_S, is at V_{IH}. In this mode, DQ0-DQ15 are high impedance.

MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient Operating Temperature	–40	85	°C
T_{BIAS}	Temperature Under Bias	–40	125	°C
T_{STG}	Storage Temperature	–65	155	°C
T_{LEAD}	Lead Temperature During Soldering		(1)	°C
V_{IO}	Input or Output Voltage	–0.5	V_{DDQ}+0.6	V
V_{DDF}	Flash Memory Core Supply Voltage	–0.2	2.45	V
V_{DDQ}	Input/Output Supply Voltage	–0.2	2.45	V
V_{DDS}	SRAM Supply Voltage	–0.2	2.4	V
V_{PPF}	Flash Memory Program Voltage	–0.2	14	V
I_O	Output Short Circuit Current		100	mA
t_{VPPFH}	Time for V_{PPF} at V_{PPFH}		100	hours

Note: 1. Compliant with the JEDEC Std J-STD-020B (for small body, Sn-Pb or Pb assembly), the ST ECOPACK ® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.

DC AND AC PARAMETERS

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 4., Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 4. Operating and AC Measurement Conditions

Parameter	Flash Memory		SRAM		Unit
	Min	Max	Min	Max	
V_{DDF} Supply Voltage	1.7	1.95	–	–	V
V_{DDS} Supply Voltage	–	–	1.7	1.95	V
V_{DDQ} Supply Voltage	1.7	1.95	–	–	V
V_{PPF} Supply Voltage (Factory environment)	11.4	12.6	–	–	V
V_{PPF} Supply Voltage (Application environment)	–0.4	V_{DDQ} +0.4	–	–	V
Ambient Operating Temperature	–40	85	–40	85	°C
Load Capacitance (C_L)	30		30		pF
Output Circuit Resistors (R_1, R_2)	16.7		16.7		kΩ
Input Rise and Fall Times		5		1	ns
Input Pulse Voltages	0 to V_{DDQ}		0 to V_{DDS}		V
Input and Output Timing Ref. Voltages	$V_{DDQ}/2$		$V_{DDS}/2$		V

Figure 6. AC Measurement I/O Waveform

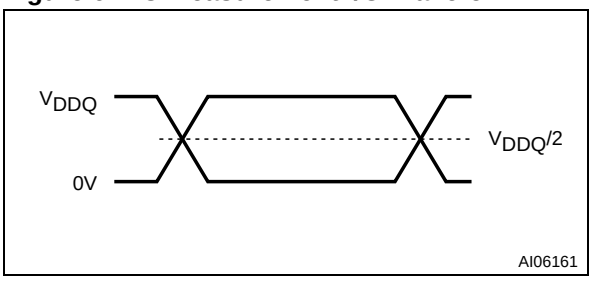


Figure 7. AC Measurement Load Circuit

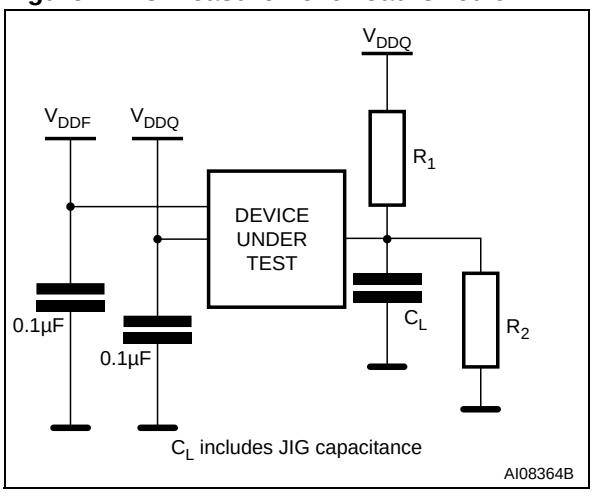


Table 5. Device Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		15	pF

Note: Sampled only, not 100% tested.

Table 6. Flash Memory DC Characteristics - Currents

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{DDQ}$			±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{DDQ}$			±1	µA
I_{DD1}	Supply Current Asynchronous Read (f=6MHz)	$\overline{E}_F = V_{IL}$, $\overline{G}_F = V_{IH}$		3	6	mA
	Supply Current Synchronous Read (f=54MHz)	4 Word		7	16	mA
		8 Word		10	18	mA
		16 Word		12	22	mA
		Continuous		13	25	mA
	Supply Current Synchronous Read (f=66MHz)	4 Word		8	17	mA
		8 Word		11	20	mA
		16 Word		14	25	mA
		Continuous		16	30	mA
I_{DD2}	Supply Current (Reset)	$\overline{RP}_F = V_{SS} \pm 0.2V$		10	50	µA
I_{DD3}	Supply Current (Standby)	$\overline{E}_F = V_{DDF} \pm 0.2V$		10	50	µA
I_{DD4}	Supply Current (Automatic Standby)	$\overline{E}_F = V_{IL}$, $\overline{G}_F = V_{IH}$		10	50	µA
I_{DD5} (1)	Supply Current (Program)	$V_{PPF} = V_{PPH}$		8	15	mA
		$V_{PPF} = V_{DDF}$		10	20	mA
	Supply Current (Erase)	$V_{PPF} = V_{PPH}$		8	15	mA
		$V_{PPF} = V_{DDF}$		10	20	mA
I_{DD6} (1,2)	Supply Current (Dual Operations)	Program/Erase in one Bank, Asynchronous Read in another Bank		13	26	mA
		Program/Erase in one Bank, Synchronous Read in another Bank		23	45	mA
I_{DD7}(1)	Supply Current Program/ Erase Suspended (Standby)	$\overline{E}_F = V_{DDF} \pm 0.2V$		10	50	µA
I_{PP1}(1)	V_{PPF} Supply Current (Program)	$V_{PPF} = V_{PPH}$		2	5	mA
		$V_{PPF} = V_{DDF}$		0.2	5	µA
	V_{PPF} Supply Current (Erase)	$V_{PPF} = V_{PPH}$		2	5	mA
		$V_{PPF} = V_{DDF}$		0.2	5	µA
I_{PP2}	V_{PPF} Supply Current (Read)	$V_{PPF} \le V_{DDF}$		0.2	5	µA
I_{PP3}(1)	V_{PPF} Supply Current (Standby)	$V_{PPF} \le V_{DDF}$		0.2	5	µA

Note: 1. Sampled only, not 100% tested.
2. V_{DDF} Dual Operation current is the sum of read and program or erase currents.

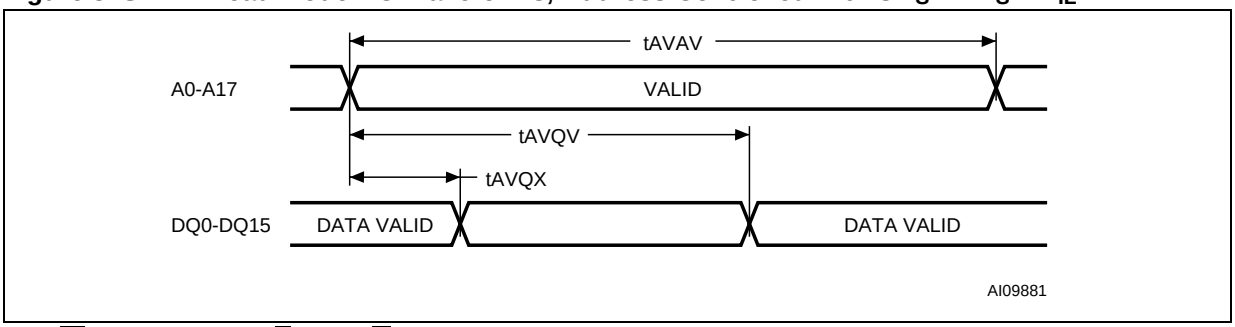
Table 7. Flash Memory DC Characteristics - Voltages

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage		–0.5		0.4	V
V_{IH}	Input High Voltage		V_{DDQ} –0.4		V_{DDQ} + 0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100µA			0.1	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	V_{DDQ} –0.1			V
V_{PP1}	V_{PPF} Program Voltage-Logic	Program, Erase	1.1	1.8	3.3	V
V_{PPH}	V_{PPF} Program Voltage Factory	Program, Erase	11.4	12	12.6	V
V_{PPLK}	Program or Erase Lockout				0.4	V
V_{LKO}	V_{DDF} Lock Voltage		1			V
V_{RPH}	$\overline{RP}_F$ pin Extended High Voltage				3.3	V

Table 8. SRAM DC Characteristics

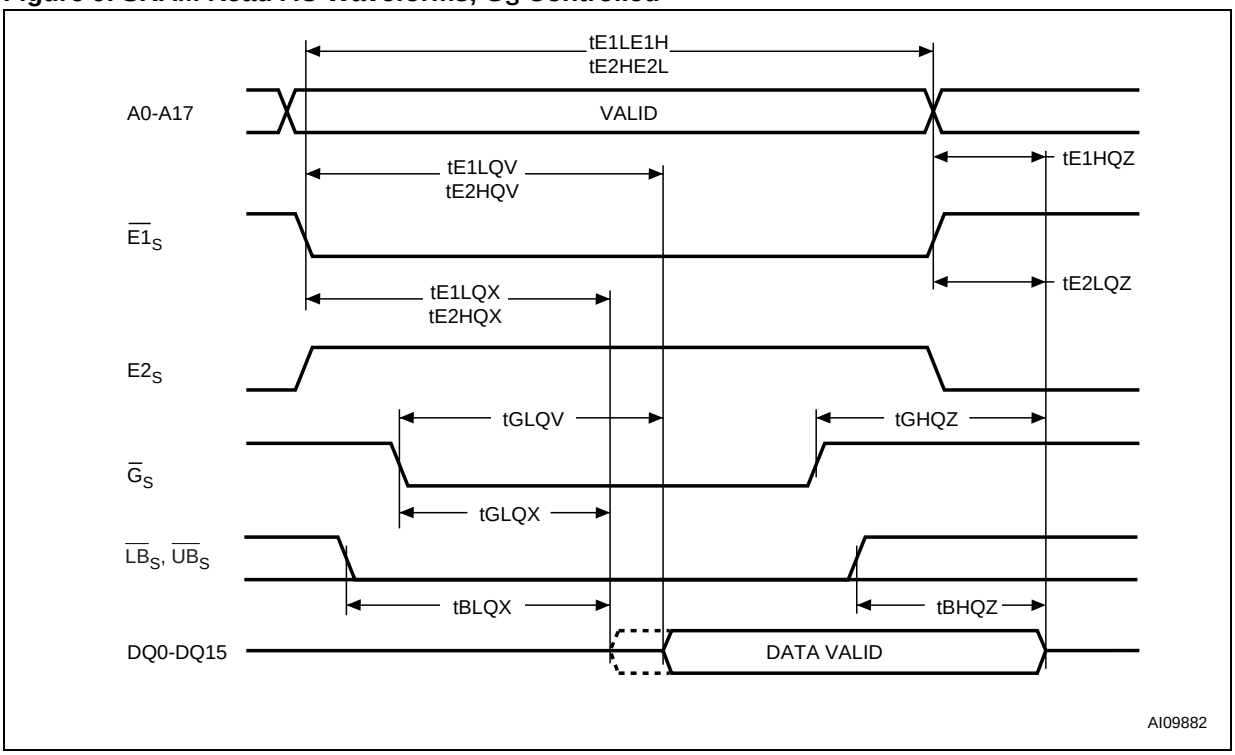
Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{DD}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{DDS}$, Output disabled		±1	µA
I_{DDS}	V_{DD} Standby Current	$\overline{E1}_S \ge V_{DDS} - 0.2V$ or $E2_S \le 0.2V$ $V_{IN} \ge V_{DDS} - 0.2V$ or $V_{IN} \le 0.2V$ f = f_{max} (Address and Data inputs only) f = 0 ($\overline{G}_S$, $\overline{W}_S$, $\overline{UB}_S$ and $\overline{LB}_S$)		10	µA
		$\overline{E1}_S \ge V_{DDS} - 0.2V$ or $E2_S \le 0.2V$ $V_{IN} \ge V_{DDS} - 0.2V$ or $V_{IN} \le 0.2V$ f = 0, V_{DD}(max)		10	µA
I_{DD}	Supply Current	f = f_{max} = $1/t_{AVAV}$, CMOS levels V_{DDS} = V_{DDS}(max)		6	mA
		I_{OUT} = 0 mA, f = 1MHz, CMOS levels		3	mA
V_{IL}	Input Low Voltage		–0.2	0.4	V
V_{IH}	Input High Voltage		1.4	V_{DDS}+0.2	V
V_{OL}	Output Low Voltage	I_{OL} = 0.1mA, V_{DSD} = 1.65V		0.2	V
V_{OH}	Output High Voltage	I_{OH} = –0.1mA, V_{DDS} = 1.65V	1.4		V

Figure 8. SRAM Read Mode AC Waveforms, Address Controlled with $\overline{UB}_S$ = $\overline{LB}_S$ = V_{IL}



Note: $\overline{E1}_S$ = Low, $E2_S$ = High, $\overline{G}_S$ = Low, $\overline{W}_S$ = High.

Figure 9. SRAM Read AC Waveforms, $\overline{G}_S$ Controlled



Note: 1. $\overline{UB}_S$, $\overline{LB}_S$ means both $\overline{UB}_S$ and $\overline{LB}_S$.
2. Write Enable ($\overline{W}_S$) = High. Address Valid prior to or at the same time as $\overline{E1}_S$ and $\overline{UB}_S$, $\overline{LB}_S$ go Low and $E2_S$ goes High.

Figure 10. SRAM Standby AC Waveforms

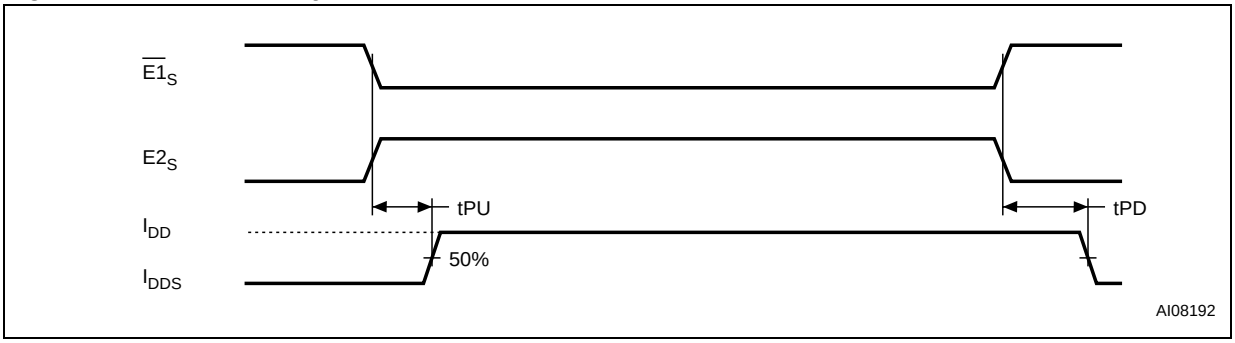
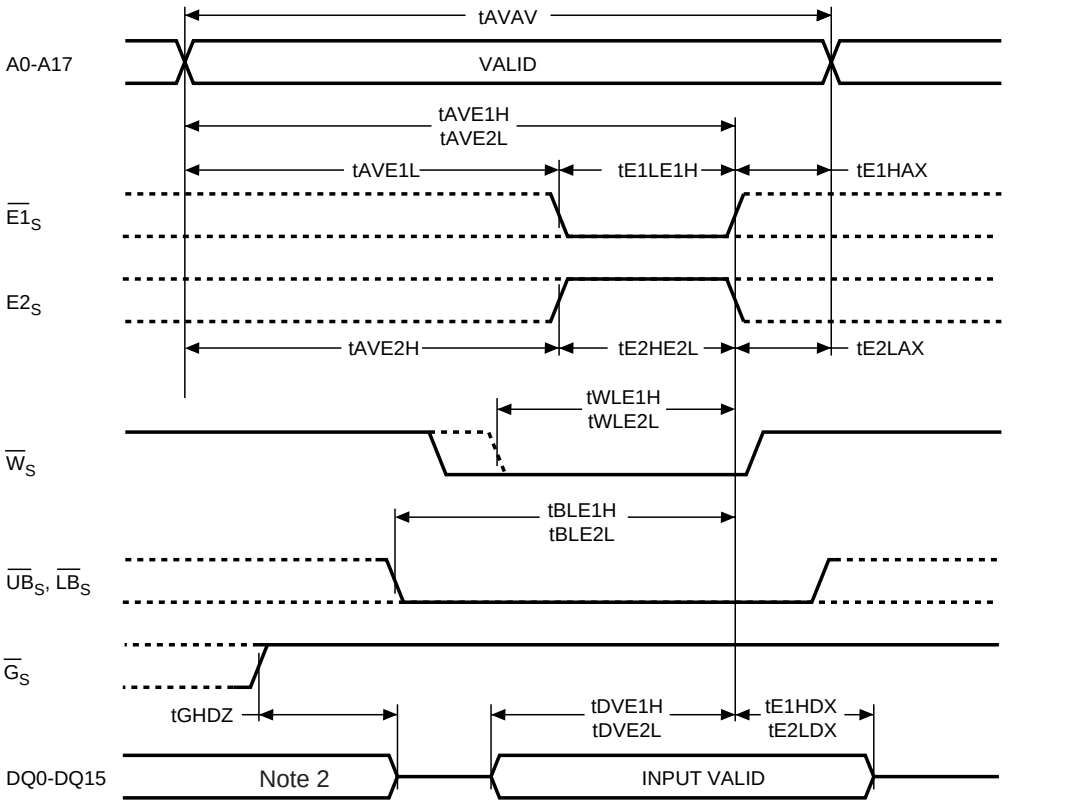


Table 9. SRAM Read AC Characteristics

Symbol	Alt	Parameter	M36W0R5020T0, M36W0R5020B0		Unit
			Min	Max	
t_{AVAV} t_{E1LE1H} t_{E2HE2L}	t_{RC}	Read Cycle Time	70		ns
t_{AVQV}	t_{AA}	Address Valid to Output Valid		70	ns
t_{AVQX}	t_{OHA}	Address Transition to Output Transition	10		ns
t_{BHQZ}(2)	t_{HZBE}	Byte Enable High to Data Hi-Z		25	ns
t_{BLQV}	t_{DBE}	Byte Enable Low to Data Valid		70	ns
t_{BLQX}(2)	t_{LZBE}	Byte Enable Low to Data Transition	5		ns
t_{E1HQZ} t_{E2LQZ}	t_{HZCE}	Chip Enable 1 High or Chip Enable 2 Low to Data Hi-Z		25	ns
t_{E1LQV} t_{E2HQV}	t_{ACE}	Chip Enable 1 Low or Chip Enable 2 High to Data Valid		70	ns
t_{E1LQX} t_{E2HQX}	t_{LZCE}	Chip Enable 1 Low or Chip Enable 2 High to Data Transition	10		ns
t_{GHQZ}	t_{HZOE}	Output Enable High to Data Hi-Z		25	ns
t_{GLQV}	t_{DOE}	Output Enable Low to Data Valid		35	ns
t_{GLQX}	t_{LZOE}	Output Enable Low to Data Transition	5		ns
t_{PD}(1)		Chip Enable 1 High or Chip Enable 2 Low to Power Down		70	ns
t_{PU}(1)		Chip Enable 1 Low or Chip Enable 2 High to Power Up	0		ns

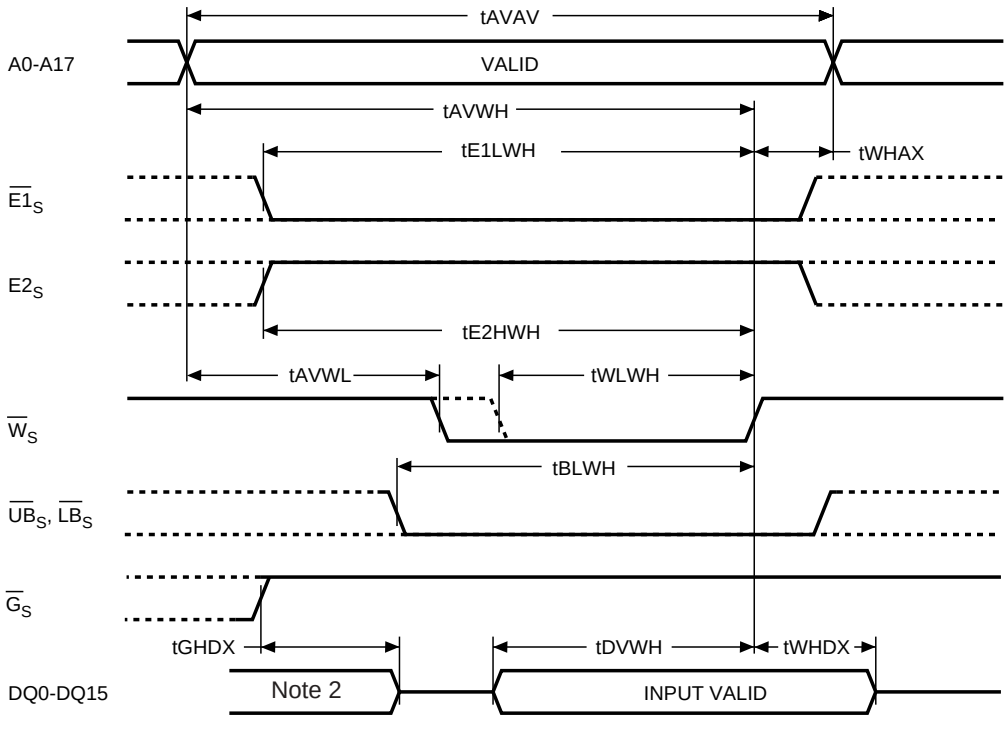
Note: 1. Sampled only. Not 100% tested.
2. Whatever the temperature and voltage, t_{E1HDZ} and t_{E2LDZ} are less than t_{E1LDX} and t_{E2HDX}; t_{BHDZ} is less than t_{BLDX} and, t_{GHDZ} is less than t_{GHDX}.

Figure 11. SRAM Write AC Waveforms, $\overline{E1}_S$ or $E2_S$ Controlled



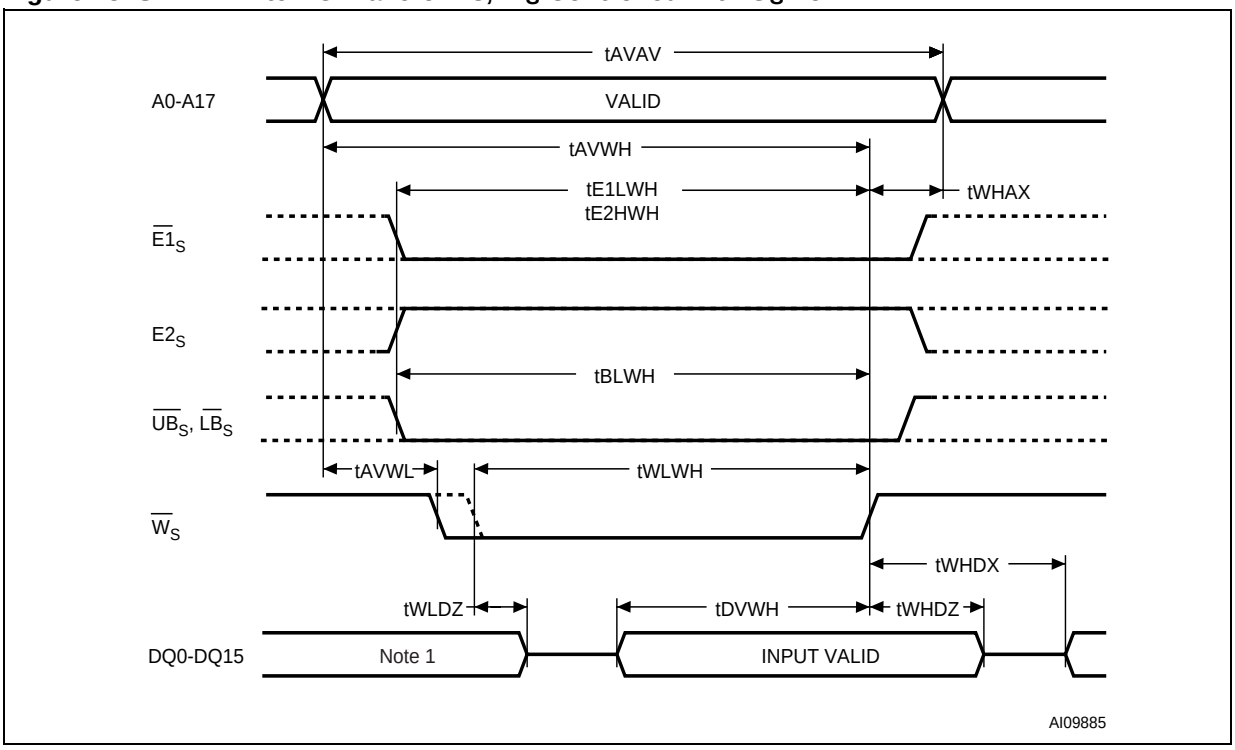
Note: 1. $\overline{W}_S$, $\overline{E1}_S$, $E2_S$ and $\overline{UB}_S$,$\overline{LB}_S$ must be asserted to initiate a write cycle.
2. The I/O pins are in output mode and input signals should not be applied.
3. If $\overline{E1}_S$, $E2_S$ and $\overline{W}_S$ are deasserted at the same time, DQ0-DQ15 remain high impedance.
4. $\overline{UB}_S$, $\overline{LB}_S$ means both $\overline{UB}_S$ and $\overline{LB}_S$.

Figure 12. SRAM Write AC Waveforms, $\overline{W}_S$ Controlled, $\overline{G}_S$ High during Write



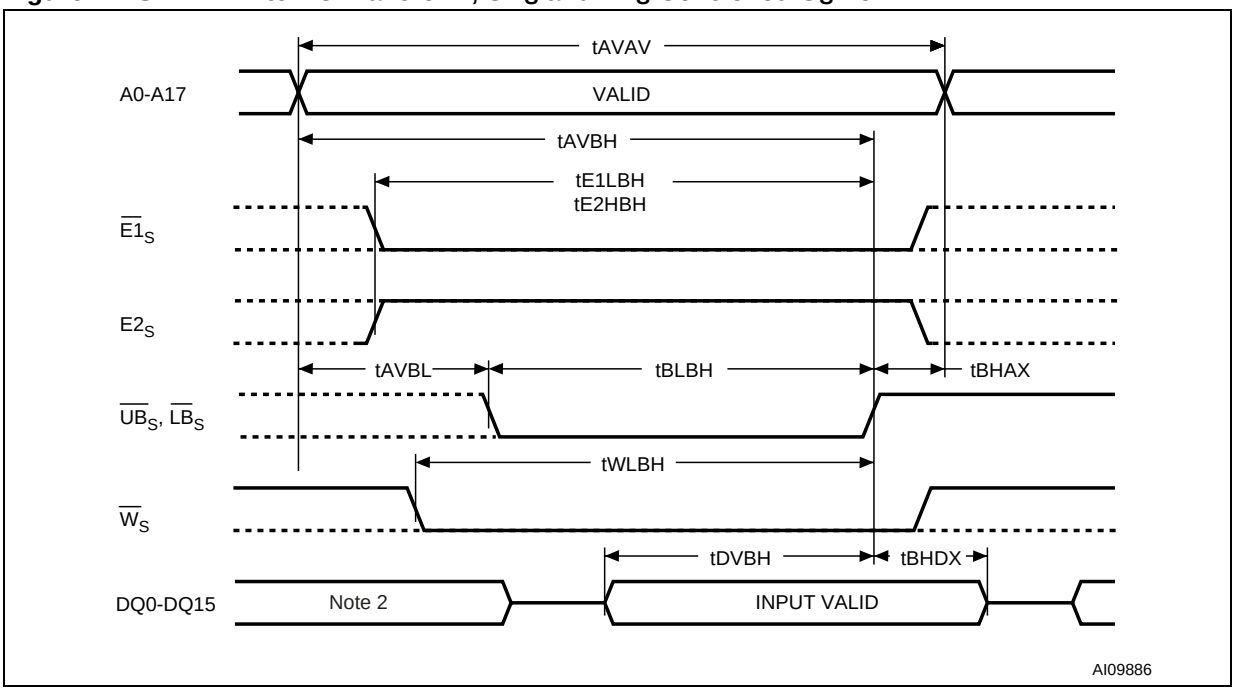
Note: 1. $\overline{W}_S$, $\overline{E1}_S$, $E2_S$ and $\overline{UB}_S$,$\overline{LB}_S$ must be asserted to initiate a write cycle.
2. The I/O pins are in output mode and input signals should not be applied.
3. If $\overline{E1}_S$, $E2_S$ and $\overline{W}_S$ are deasserted at the same time, DQ0-DQ15 remain high impedance.
4. $\overline{UB}_S$, $\overline{LB}_S$ means both $\overline{UB}_S$ and $\overline{LB}_S$.

Figure 13. SRAM Write AC Waveforms, $\overline{W}_S$ Controlled with $\overline{G}_S$ Low



Note: 1. During this period, the I/O pins are in output mode and input signals should not be applied.
2. If $\overline{E1}_S$, $E2_S$ and $\overline{W}_S$ are deasserted at the same time, DQ0-DQ15 remain high impedance.
3. $\overline{UB}_S$, $\overline{LB}_S$ means both $\overline{UB}_S$ and $\overline{LB}_S$.

Figure 14. SRAM Write AC Waveform, $\overline{UB}_S$ and $\overline{LB}_S$ Controlled $\overline{G}_S$ Low



Note: 1. If $\overline{E1}_S$, $E2_S$ and $\overline{W}_S$ are deasserted at the same time, DQ0-DQ15 remain high impedance.
2. The I/O pins are in output mode and input signals should not be applied.
3. $\overline{UB}_S$, $\overline{LB}_S$ means both $\overline{UB}_S$ and $\overline{LB}_S$.

Table 10. SRAM Write AC Characteristics

Symbol	Alt	Parameter	M36W0R5020T0, M36W0R5020B0		Unit
			Min	Max	
t_{AVAV}	t_{WC}	Write Cycle Time	70		ns
t_{AVE1L}, t_{AVE2H}, t_{AVWL} t_{AVBL}	t_{SA}	Address Valid to Beginning of Write	0		ns
t_{AVWH} t_{AVE1H} t_{AVE2L} t_{AVBH}	t_{AW}	Address Valid to Write Enable High	60		ns
t_{BLWH} t_{BLE1H} t_{BLE2L} t_{BLBH}	t_{BW}	$\overline{UB}_S$, $\overline{LB}_S$ Valid to End of Write	60		ns
t_{DVE1H}, t_{DVE2L}, t_{DVWH} t_{DVBH}	t_{SD}	Input Valid to End of Write	30		ns
t_{E1HAX}, t_{E2LAX}, t_{WHAX} t_{BHAX}	t_{HA}	End of Write to Address Change	0		ns
t_{E1HDX}, t_{E2LDX}, t_{WHDX} t_{BHDX}	t_{HD}	Data Transition to End of Write	0		ns
t_{E1LE1H}, t_{E2HE2L}, t_{E1LWH} t_{E2HWH} t_{E1LBH}, t_{E2HBH}	t_{SCE}	Chip Enable 1 Low or Chip Enable 2 High to End of Write	60		ns
t_{GHDZ}	t_{HZOE}	Output Enable High to Output Hi-Z		25	ns
t_{WHDZ}(1)	t_{LZWE}	Write Enable High to Input Transition	10		ns
t_{WLDZ}(1)	t_{HZWE}	Write Enable Low to Output Hi-Z		25	ns
t_{WLWH} t_{WLE1H} t_{WLE2L} t_{WLBH}	t_{PWE}	Write Enable Pulse Width	50		ns

Note: 1. Whatever the temperature and voltage, t_{WLDZ} is less than t_{WHDX}.

Figure 15. SRAM Low V_{DDS} Data Retention AC Waveforms, $\overline{E1}_S$ or $\overline{UB}_S$ / $\overline{LB}_S$ Controlled

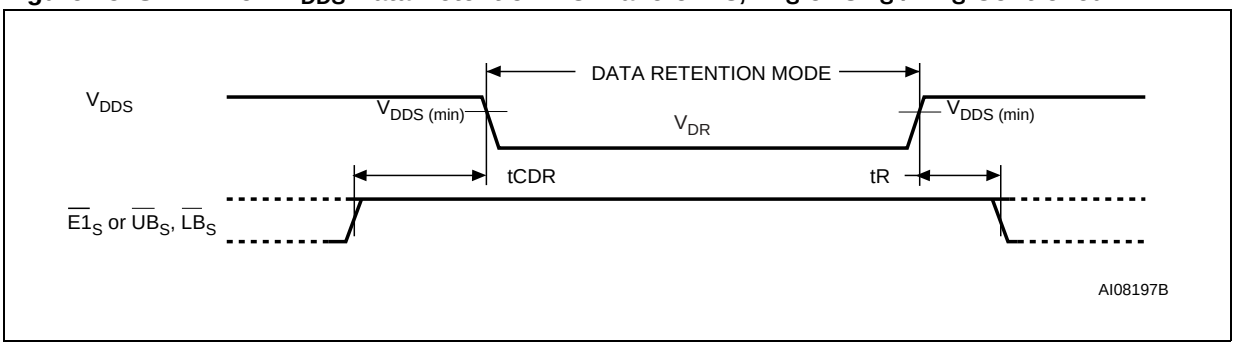


Figure 16. SRAM Low V_{DDS} Data Retention AC Waveforms, $E2_S$ Controlled

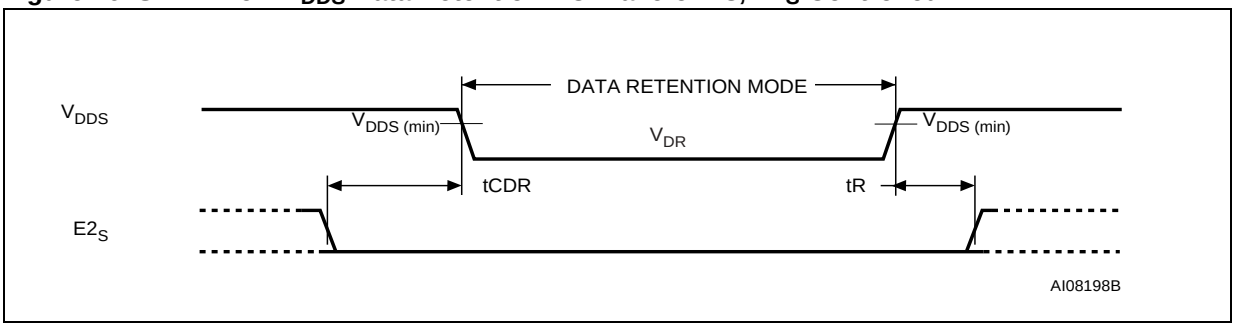


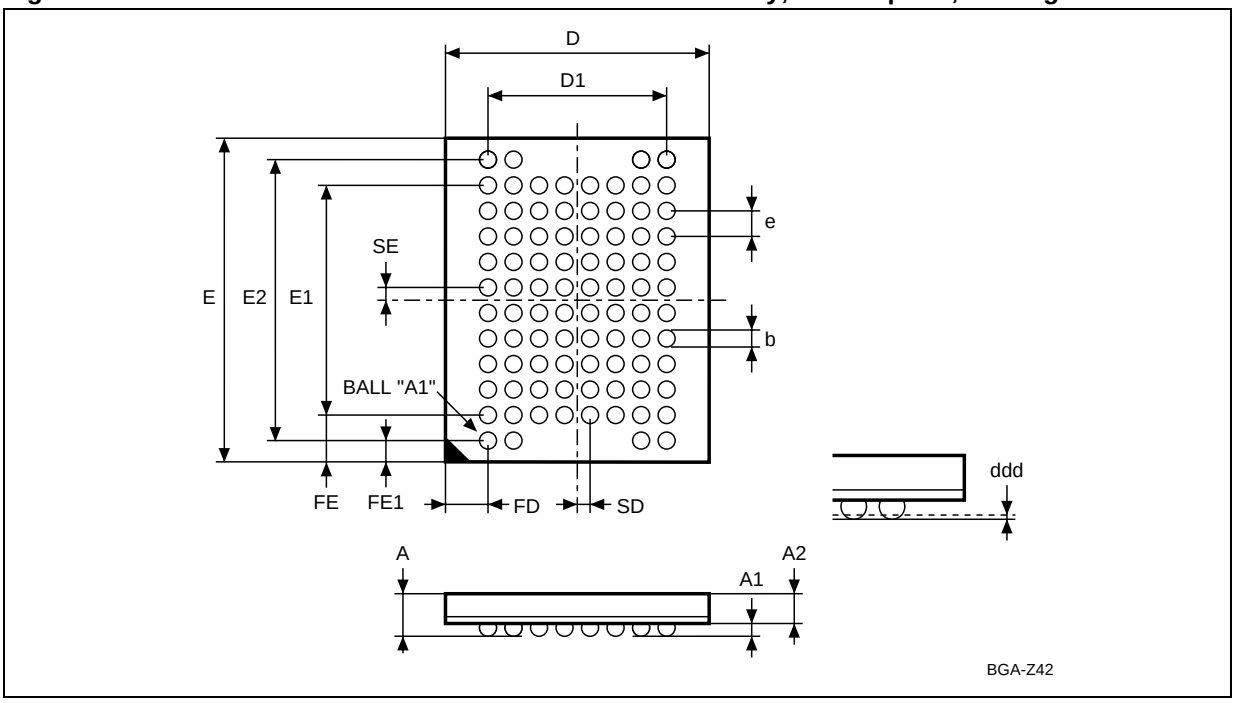
Table 11. SRAM Low V_{DDS} Data Retention Characteristic

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{DDDR}	Supply Current (Data Retention)	V_{DDS} = 1.0V, $\overline{E1}_S \geq V_{DDS} - 0.2V$ or $E2_S \leq 0.2V$, $V_{IN} \geq V_{DDS} - 0.2V$ or $V_{IN} \leq 0.2V$		8	µA
V_{DR}	Supply Voltage (Data Retention)		1.0	1.95	V
t_{CDR}	Chip Disable to Power Down		0		ns
t_R	Operation Recovery Time		70		ns

Note: 1. Sampled only. Not 100% tested.

PACKAGE MECHANICAL

Figure 17. Stacked TFBGA88 8x10mm - 8x10 active ball array, 0.8mm pitch, Package Outline



Note: Drawing is not to scale.

Table 12. Stacked TFBGA88 8x10mm - 8x10 active ball array, 0.8mm pitch, Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.200			0.0079	
A2	0.850			0.0335		
b	0.350	0.300	0.400	0.0138	0.0118	0.0157
D	8.000	7.900	8.100	0.3150	0.3110	0.3189
D1	5.600			0.2205		
ddd			0.100			0.0039
E	10.000	9.900	10.100	0.3937	0.3898	0.3976
E1	7.200			0.2835		
E2	8.800			0.3465		
e	0.800	–	–	0.0315	–	–
FD	1.200			0.0472		
FE	1.400			0.0551		
FE1	0.600			0.0236		
SD	0.400			0.0157		
SE	0.400			0.0157		

PART NUMBERING

Table 13. Ordering Information Scheme

Example: M36W0R5020T0ZAQT

Device Type
M36 = Multi-Chip Package (Flash + RAM)

Flash 1 Architecture
W = Multiple Bank, Burst mode

Flash 2 Architecture
0 = none present

Operating Voltage
R = V_{DDF} = V_{DDQ} =V_{DDP} = 1.7 to 1.95V

Flash 1 Density
5 = 32 Mbit

Flash 2 Density
0 = none present

RAM 1 Density
2 = 4 Mbit

RAM 0 Density
0 = none present

Parameter Blocks Location
T = Top Boot Block Flash
B = Bottom Boot Block Flash

Product Version
0 = 0.13µm Flash technology, 70ns; 0.15µm RAM, 70ns speed

Package
ZAQ = Stacked TFBGA88 8 x 10mm - 8x10 active ball array, 0.8mm pitch

Option
Blank = Standard Packing
T = Tape & Reel Packing
E = Lead-free and RoHS Package, Standard Packing
F = Lead-free and RoHS Package, Tape & Reel Packing

Devices are shipped from the factory with the memory content bits erased to ’1’. For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the ST-Microelectronics Sales Office nearest to you.

REVISION HISTORY

Table 14. Document Revision History

Date	Version	Revision Details
27-Aug-2003	1.0	First Issue
06-May-2004	2.0	M36W0R5030T0 and M36W0R5030B0 part numbers and 8 Mbit SRAM option removed. 0.15µm Flash memory technology replaced by the 0.13µm technology. Package specifications updated. E and F Lead-free Package options added to Table 13., Ordering Information Scheme.
17-Dec-2004	3.0	Document status promoted to full Datasheet. Flash memory and PSRAM data updated. TFBGA88 package fully compliant with the ST ECOPACK specification.