

MITSUBISHI MICROCOMPUTERS

M37705M2AXXXSP

M37705S1ASP

M37705M2-XXXSP and M37705S1SP are respectively unified into M37705M2AXXXSP and M37705S1ASP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37705M2AXXXSP and M37705S1ASP are single-chip microcomputers designed with high-performance CMOS silicon gate technology. These are housed in a 64-pin shrink plastic molded DIP. These single-chip microcomputers have a large 16M bytes address space, three instruction queue buffers, and two data buffers for high-speed instruction execution. The CPU is a 16-bit parallel processor that can also be switched to perform 8-bit parallel processing. These microcomputers are suitable for office, business and industrial equipment controller that require high-speed processing of large data.

Also, the incorporated motor control circuit makes these microcomputers suitable for control of equipment that requires motor control.

The differences between M37705M2AXXXSP and M37705S1ASP are the ROM size as shown below. Therefore, the following descriptions will be for the M37705M2AXXXSP unless otherwise noted.

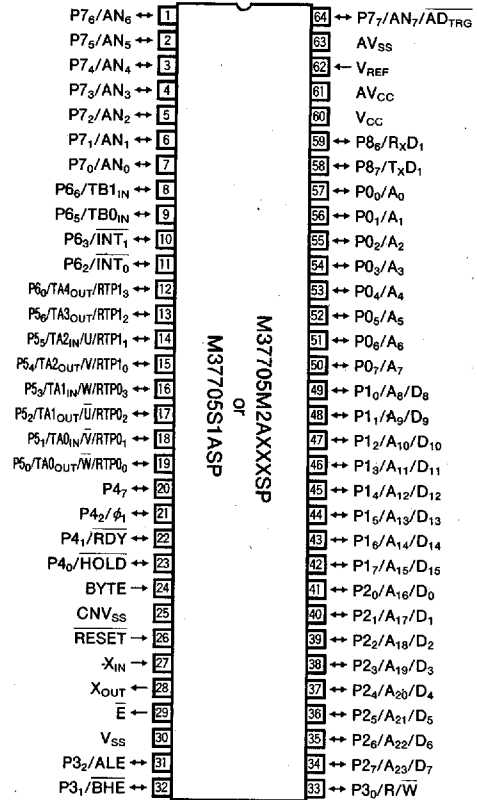
Type name	ROM size	External clock input frequency
M37705M2AXXXSP	16K bytes	16MHz
M37705S1ASP	External	16MHz

The M37705M2AXXXSP cuts down the pins of M37704M2AXXXFP. Refer to the BASIC FUNCTION BLOCKS for the functional differences.

DISTINCTIVE FEATURES

- Number of basic instructions 103
- Memory size ROM 16K bytes
- RAM 512 bytes
- Instruction execution time
- The fastest instruction at 16 MHz frequency 250ns
- Single power supply $5V \pm 10\%$
- Low power dissipation (at 16 MHz frequency) 60mW (Typ.)
- Interrupts 16 types 7 levels
- Multiple function 16-bit timer 5+3
(Three-phase motor drive waveform or pulse motor drive waveform can be output.)
- UART 1
- 8-bit A-D converter 8-channel inputs
- 12-bit watchdog timer
- Programmable input/output (ports P0, P1, P2, P3, P4, P5, P6, P7, P8) 53

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

APPLICATION

Motor control devices such as inverter type air conditioners and general purpose inverters

Control devices for office equipment such as copiers, printers, typewriters, facsimiles, word processors, and personal computers

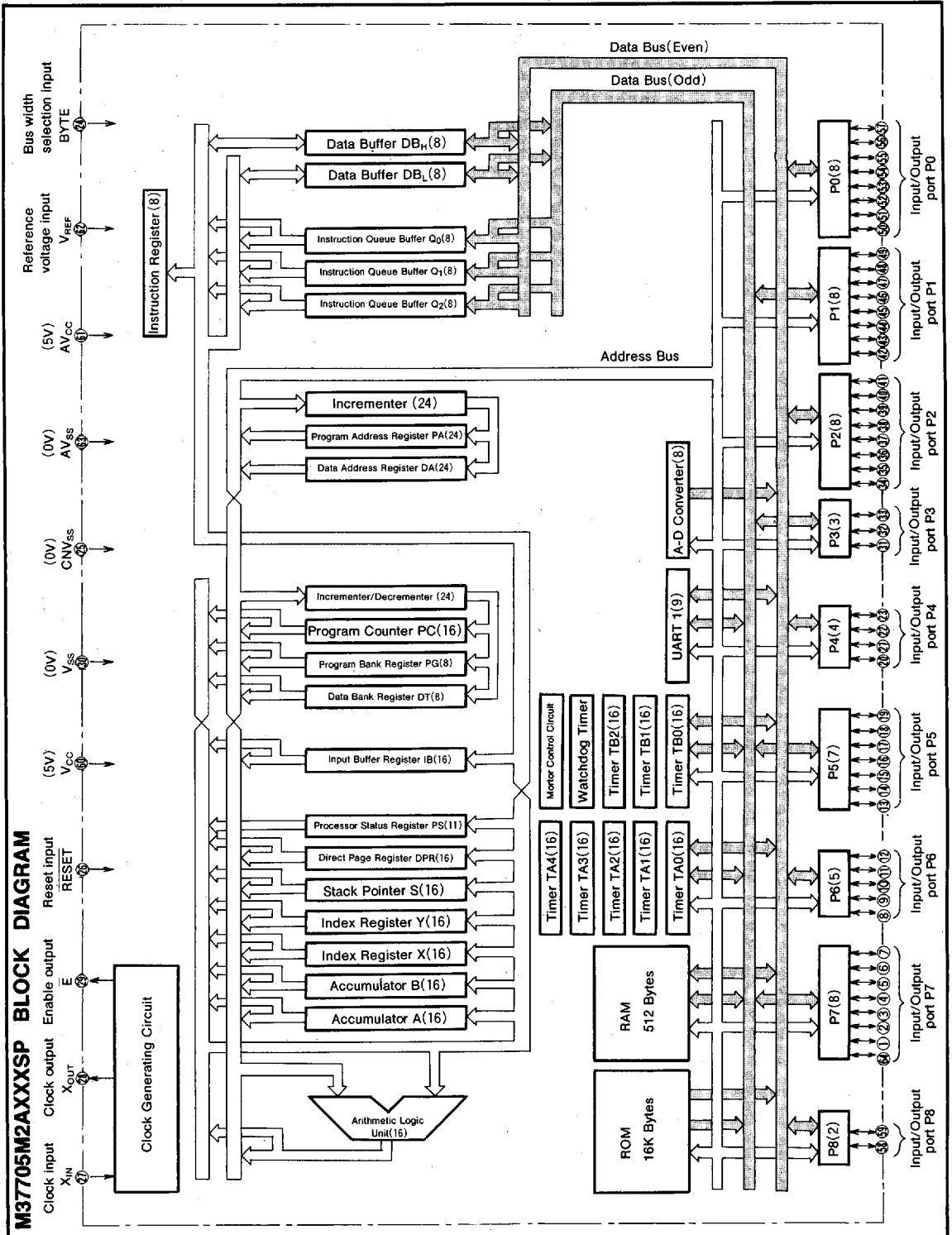
NOTE

Refer to "Chapter 5 PRECAUTIONS" when using this microcomputer.

The M37705M2AXXXSP and M37705S1ASP satisfy the timing requirements and the switching characteristics of the former M37705M2-XXXSP and M37705S1SP

M37705M2AXXSP
M37705S1ASP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER



6249828 0026551 803



M37705M2AXXXSP
M37705S1ASP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

FUNCTIONS OF M37705M2AXXXSP

Parameter		Functions
Number of basic instructions		103
Instruction execution time	M37705M2AXXXSP, M37705S1ASP	250ns (the fastest instruction at external clock 16MHz frequency)
Memory size	ROM	16K bytes
	RAM	512 bytes
Input/Output ports	P0, P1, P2, P7	8-bitX 4
	P5	7-bitX 1
	P6	5-bitX 1
	P4	4-bitX 1
	P3	3-bitX 1
	P8	2-bitX 1
Multi-function timers	TA0, TA1, TA2, TA3, TA4	16-bitX 5 (3 input/output and 2 output functions)
	TB0, TB1, TB2	16-bitX 3 (2 input functions)
Serial I/O		UART X1
A-D converter		8-bitX 1 (8 channels)
Watchdog timer		12-bitX 1
Dead-time timer		8-bitX 3
Interrupts		2 external types, 14 internal types (Each interrupt can be set the priority levels to 0~7.)
Clock generating circuit		Built-in(externally connected to a ceramic resonator or quartz crystal resonator)
Supply voltage		5 V±10%
Power dissipation		60mW(at external clock 16MHz frequency)
Input/Output characteristic	Input/Output voltage	5 V
	Output current	5 mA
Memory expansion		Maximum 16M bytes
Operating temperature range		-20~85°C
Device structure		CMOS high-performance silicon gate process
Package		64-pin shrink plastic molded DIP

MITSUBISHI MICROCOMPUTERS
M37705M2AXXSP
M37705S1ASP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

PIN DESCRIPTION

Pin	Name	Input/Output	Functions
V _{CC} , V _{SS}	Power supply		Supply 5 V±10% to V _{CC} and 0 V to V _{SS} .
CNV _{SS}	CNV _{SS} input	Input	This pin controls the processor mode. Connect to V _{SS} for single-chip mode, and to V _{CC} for external ROM types.
RESET	Reset input	Input	To enter the reset state, this pin must be kept at a "L" condition which should be maintained for the required time.
X _{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit. Connect a ceramic or quartz crystal resonator between X _{IN} and X _{OUT} . When an external clock is used, the clock source should be connected to the X _{IN} pin and the X _{OUT} pin should be left open.
X _{OUT}	Clock output	Output	
\bar{E}	Enable output	Output	Data or instruction read and data write are performed when output from this pin is "L".
BYTE	Bus width selection input	Input	In memory expansion mode or microprocessor mode, this pin determines whether the external data bus is 8-bit width or 16-bit width. The width is 16 bits when "L" signal inputs and 8 bits when "H" signal inputs.
AV _{CC} , AV _{SS}	Analog supply input		Power supply for the A-D converter. Connect AV _{CC} to V _{CC} and AV _{SS} to V _{SS} externally.
V _{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D converter.
P0 ₀ ~P0 ₇	I/O port P0	I/O	In single-chip mode, port P0 becomes an 8-bit I/O port. An I/O directional register is available so that each pin can be programmed for input or output. These ports are in input mode when reset. Address(A ₇ ~A ₀) is output in memory expansion mode or microprocessor mode.
P1 ₀ ~P1 ₇	I/O port P1	I/O	In single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to "L" in memory expansion mode or microprocessor mode and external data bus is 16-bit width, high-order data (D ₁₅ ~D ₈) is input or output when \bar{E} output is "L" and an address (A ₁₅ ~A ₈) is output when \bar{E} output is "H". If the BYTE pin is "H" that is an external data bus is 8-bit width, only address(A ₁₅ ~A ₈) is output.
P2 ₀ ~P2 ₇	I/O port P2	I/O	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode low-order data(D ₇ ~D ₀) is input or output when \bar{E} output is "L" and an address(A ₂₃ ~A ₁₆) is output when \bar{E} output is "H".
P3 ₀ ~P3 ₂	I/O port P3	I/O	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, R/W, BHE, and ALE signals are output.
P4 ₀ ~P4 ₂ , P4 ₇	I/O port P4	I/O	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, P4 ₀ and P4 ₁ become \overline{HOLD} and \overline{RDY} input pin respectively. Functions of other pins are the same as in single-chip mode. In single-chip mode or memory expansion mode, port P4 ₂ can be programmed for ϕ_1 output pin divided the clock to X _{IN} pin by 2. In microprocessor mode, P4 ₂ always has the function as ϕ_1 output pin.
P5 ₀ ~P5 ₆	I/O port P5	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as I/O pins for timer A0, timer A1, timer A2 and output pin for timer A3. These pins also have the function as motor control output pin.
P6 ₀ , P6 ₂ , P6 ₃ , P6 ₅ , P6 ₆	I/O port P6	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as output pins for timer A4, and input pins for external interrupt input $\overline{INT_0}$ and $\overline{INT_1}$ pins, and for timer B0 and timer B1. P6 ₀ also has the function as motor control output pin and P6 ₂ has the function as motor control pin.
P7 ₀ ~P7 ₇	I/O port P7	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as analog input AN ₀ ~AN ₇ input pins. P7 ₇ also has an A-D conversion trigger input function.
P8 ₆ , P8 ₇	I/O port P8	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as RxD and TxD pins for UART 1.

6249828 0026553 686

MITSUBISHI MICROCOMPUTERS
M37705M2AXXSP
M37705S1ASP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

M37705M2AXXSP

ELECTRICAL CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=16MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
V_{OH}	High-level output voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0$, $P3_1$, $P4_0 \sim P4_2$, $P4_7$, $P5_0 \sim P5_6$, $P6_0$, $P6_2$, $P6_3$, $P6_5$, $P6_6$, $P7_0 \sim P7_7$, $P8_6$, $P8_7$	$I_{OH} = -10mA$	3			V	
V_{OH}	High-level output voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0$, $P3_1$	$I_{OH} = -400\mu A$	4.7			V	
V_{OH}	High-level output voltage $P3_2$	$I_{OH} = -10mA$	3.1			V	
		$I_{OH} = -400\mu A$	4.8				
V_{OH}	High-level output voltage \bar{E}	$I_{OH} = -10mA$	3.4			V	
		$I_{OH} = -400\mu A$	4.8				
V_{OL}	Low-level output voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0$, $P3_1$, $P4_0 \sim P4_2$, $P4_7$, $P5_6$, $P6_0$, $P6_2$, $P6_3$, $P6_5$, $P6_6$, $P7_0 \sim P7_7$, $P8_6$, $P8_7$	$I_{OL} = 10mA$			2	V	
		$I_{OL} = 20mA$			2		
V_{OL}	Low-level output voltage $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0$, $P3_1$	$I_{OL} = 2mA$			0.45	V	
V_{OL}	Low-level output voltage $P3_2$	$I_{OL} = 10mA$			1.9	V	
		$I_{OL} = 2mA$			0.43		
V_{OL}	Low-level output voltage \bar{E}	$I_{OL} = 10mA$			1.6	V	
		$I_{OL} = 2mA$			0.4		
$V_{T+} - V_{T-}$	Hysteresis $HOLD$, RDY , $TA0_{IN} \sim TA2_{IN}$, $TB0_{IN}$, $TB1_{IN}$, INT_0 , INT_1 , AD_{TRG}		0.4		1	V	
$V_{T+} - V_{T-}$	Hysteresis $RESET$		0.2		0.5	V	
$V_{T+} - V_{T-}$	Hysteresis X_{IN}		0.1		0.3	V	
I_{IH}	High-level input current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0 \sim P3_2$, $P4_0 \sim P4_2$, $P4_7$, $P5_0 \sim P5_6$, $P6_0$, $P6_2$, $P6_3$, $P6_5$, $P6_6$, $P7_0 \sim P7_7$, $P8_6$, $P8_7$, X_{IN} , $RESET$, CNV_{SS} , $BYTE$	$V_I = 5V$			5	μA	
I_{IL}	Low-level input current $P0_0 \sim P0_7$, $P1_0 \sim P1_7$, $P2_0 \sim P2_7$, $P3_0 \sim P3_2$, $P4_0 \sim P4_2$, $P4_7$, $P5_0 \sim P5_6$, $P6_0$, $P6_2$, $P6_3$, $P6_5$, $P6_6$, $P7_0 \sim P7_7$, $P8_6$, $P8_7$, X_{IN} , $RESET$, CNV_{SS} , $BYTE$	$V_I = 0V$			-5	μA	
V_{RAM}	RAM hold voltage	When clock is stopped.	2			V	
I_{CC}	Power supply current	In single-chip mode output only pin is open and other pins are V_{SS} during reset.	$f(X_{IN})=16MHz$, square waveform		12	24	mA
			$T_a=25^\circ C$ when clock is stopped.			1	
			$T_a=85^\circ C$ when clock is stopped.			20	μA

A-D CONVERTER CHARACTERISTICS ($V_{CC}=5V$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=16MHz$, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	$V_{REF} = V_{CC}$			8	Bits
—	Absolute accuracy	$V_{REF} = V_{CC}$			± 2	LSB
R_{LADDER}	Ladder resistance	$V_{REF} = V_{CC}$	2		10	$k\Omega$
t_{CONV}	Conversion time		14.25			μs
V_{REF}	Reference voltage		2		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

6249828 0026555 459

M37705M2AXXSP
M37705S1ASP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.3~7	V
AV _{CC}	Analog supply voltage		-0.3~7	V
V _I	Input voltage RESET, CNV _{SS} , BYTE		-0.3~12	V
V _I	Input voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₂ , P4 ₀ ~P4 ₂ , P4 ₇ , P5 ₀ ~P5 ₅ , P6 ₀ , P6 ₂ , P6 ₃ , P6 ₅ , P6 ₆ , P7 ₀ ~P7 ₇ , P8 ₆ , P8 ₇ , V _{REF} , X _{IN}		-0.3~V _{CC} +0.3	V
V _O	Output voltage P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₂ , P4 ₀ ~P4 ₂ , P4 ₇ , P5 ₀ ~P5 ₅ , P6 ₀ , P6 ₂ , P6 ₃ , P6 ₅ , P6 ₆ , P7 ₀ ~P7 ₇ , P8 ₆ , P8 ₇ , X _{OUT} , E		-0.3~V _{CC} +0.3	V
P _d	Power dissipation	T _a =25°C	1000	mW
T _{opr}	Operating temperature		-20~85	°C
T _{stg}	Storage temperature		-40~150	°C

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=-10~70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V _{CC}	Supply voltage	4.5	5.0	5.5	V
AV _{CC}	Analog supply voltage		V _{CC}		V
V _{SS}	Supply voltage		0		V
AV _{SS}	Analog supply voltage		0		V
V _{IH}	High-level input voltage P0 ₀ ~P0 ₇ , P3 ₀ ~P3 ₂ , P4 ₀ ~P4 ₂ , P4 ₇ , P5 ₀ ~P5 ₅ , P6 ₀ , P6 ₂ , P6 ₃ , P6 ₅ , P6 ₆ , P7 ₀ ~P7 ₇ , P8 ₆ , P8 ₇ , X _{IN} , RESET, CNV _{SS} , BYTE	0.8V _{CC}		V _{CC}	V
V _{IH}	High-level input voltage P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ (in single-chip mode)	0.8V _{CC}		V _{CC}	V
V _{IH}	High-level input voltage P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ (in memory expansion mode and microprocessor mode)	0.5V _{CC}		V _{CC}	V
V _{IL}	Low-level input voltage P0 ₀ ~P0 ₇ , P3 ₀ ~P3 ₂ , P4 ₀ ~P4 ₂ , P4 ₇ , P5 ₀ ~P5 ₅ , P6 ₀ , P6 ₂ , P6 ₃ , P6 ₅ , P6 ₆ , P7 ₀ ~P7 ₇ , P8 ₆ , P8 ₇ , X _{IN} , RESET, CNV _{SS} , BYTE	0		0.2V _{CC}	V
V _{IL}	Low-level input voltage P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ (in single-chip mode)	0		0.2V _{CC}	V
V _{IL}	Low-level input voltage P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ (in memory expansion mode and microprocessor mode)	0		0.16V _{CC}	V
I _{OH(peak)}	High-level peak output current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₂ , P4 ₀ ~P4 ₂ , P4 ₇ , P5 ₀ ~P5 ₅ , P6 ₀ , P6 ₂ , P6 ₃ , P6 ₅ , P6 ₆ , P7 ₀ ~P7 ₇ , P8 ₆ , P8 ₇			-10	mA
I _{OH(avg)}	High-level average output current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₂ , P4 ₀ ~P4 ₂ , P4 ₇ , P5 ₀ ~P5 ₅ , P6 ₀ , P6 ₂ , P6 ₃ , P6 ₅ , P6 ₆ , P7 ₀ ~P7 ₇ , P8 ₆ , P8 ₇			-5	mA
I _{OL(peak)}	Low-level peak output current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₂ , P4 ₀ ~P4 ₂ , P4 ₇ , P5 ₆ , P6 ₀ , P6 ₂ , P6 ₃ , P6 ₅ , P6 ₆ , P7 ₀ ~P7 ₇ , P8 ₆ , P8 ₇			10	mA
I _{OL(peak)}	Low-level peak output current P5 ₀ ~P5 ₅			20	mA
I _{OL(avg)}	Low-level average output current P0 ₀ ~P0 ₇ , P1 ₀ ~P1 ₇ , P2 ₀ ~P2 ₇ , P3 ₀ ~P3 ₂ , P4 ₀ ~P4 ₂ , P4 ₇ , P5 ₆ , P6 ₀ , P6 ₂ , P6 ₃ , P6 ₅ , P6 ₆ , P7 ₀ ~P7 ₇ , P8 ₆ , P8 ₇			5	mA
I _{OL(avg)}	Low-level average output current P5 ₀ ~P5 ₅			15	mA
f(X _{IN})	External clock frequency input			16	MHZ

Note 1. Average output current is the average value of a 100ms interval.

- The sum of I_{OL(peak)} for ports P0, P1, P2, P3, and P8 must be 80mA or less, the sum of I_{OH(peak)} for ports P0, P1, P2, P3, and P8 must be 80mA or less, the sum of I_{OL(peak)} for ports P4, P5, P6, and P7 must be 110mA or less, and the sum of I_{OH(peak)} for ports P4, P5, P6, and P7 must be 80mA or less.

MITSUBISHI MICROCOMPUTERS
M37705M2AXXSP
M37705S1ASP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

TIMING REQUIREMENTS ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=25^\circ C$, $f(X_{IN})=16MHz$, unless otherwise noted)

External clock input

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_C	External clock input cycle time		62			ns
$t_{W(H)}$	External clock input high-level pulse width		25			ns
$t_{W(L)}$	External clock input low-level pulse width		25			ns
t_r	External clock rise time				10	ns
t_f	External clock fall time				10	ns

Single-chip mode

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{SU(P0D-E)}$	Port P0 input setup time		100			ns
$t_{SU(P1D-E)}$	Port P1 input setup time		100			ns
$t_{SU(P2D-E)}$	Port P2 input setup time		100			ns
$t_{SU(P3D-E)}$	Port P3 input setup time		100			ns
$t_{SU(P4D-E)}$	Port P4 input setup time		100			ns
$t_{SU(P5D-E)}$	Port P5 input setup time		100			ns
$t_{SU(P6D-E)}$	Port P6 input setup time		100			ns
$t_{SU(P7D-E)}$	Port P7 input setup time		100			ns
$t_{SU(P8D-E)}$	Port P8 input setup time		100			ns
$t_{H(E-P0D)}$	Port P0 input hold time		0			ns
$t_{H(E-P1D)}$	Port P1 input hold time		0			ns
$t_{H(E-P2D)}$	Port P2 input hold time		0			ns
$t_{H(E-P3D)}$	Port P3 input hold time		0			ns
$t_{H(E-P4D)}$	Port P4 input hold time		0			ns
$t_{H(E-P5D)}$	Port P5 input hold time		0			ns
$t_{H(E-P6D)}$	Port P6 input hold time		0			ns
$t_{H(E-P7D)}$	Port P7 input hold time		0			ns
$t_{H(E-P8D)}$	Port P8 input hold time		0			ns

Memory expansion mode and microprocessor mode

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{SU(P1D-E)}$	Port P1 input setup time		45			ns
$t_{SU(P2D-E)}$	Port P2 input setup time		45			ns
$t_{SU(RDY-A)}$	RDY input setup time		60			ns
$t_{H(E-P1D)}$	Port P1 input hold time		0			ns
$t_{H(E-P2D)}$	Port P2 input hold time		0			ns
$t_{H(A-RDY)}$	RDY input hold time		0			ns

6249828 0026557 221

Timer A input (Count input in event counter mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(TA)}$	TA_{iN} input cycle time		125			ns
$t_{W(TAH)}$	TA_{iN} input high-level pulse width		62			ns
$t_{W(TAL)}$	TA_{iN} input low-level pulse width		62			ns

Timer A input (Gating input in timer mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(TA)}$	TA_{iN} input cycle time		500			ns
$t_{W(TAH)}$	TA_{iN} input high-level pulse width		250			ns
$t_{W(TAL)}$	TA_{iN} input low-level pulse width		250			ns

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(TA)}$	TA_{iN} input cycle time		250			ns
$t_{W(TAH)}$	TA_{iN} input high-level pulse width		125			ns
$t_{W(TAL)}$	TA_{iN} input low-level pulse width		125			ns

Timer A input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{W(TAH)}$	TA_{iN} input high-level pulse width		125			ns
$t_{W(TAL)}$	TA_{iN} input low-level pulse width		125			ns

Timer A input (Up-down input in event counter mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(UP)}$	TA_{iOUT} input cycle time		2500			ns
$t_{W(UPH)}$	TA_{iOUT} input high-level pulse width		1250			ns
$t_{W(UPL)}$	TA_{iOUT} input low-level pulse width		1250			ns
$t_{SU(UP-TN)}$	TA_{iOUT} input setup time		500			ns
$t_{H(TN-UP)}$	TA_{iOUT} input hold time		500			ns

Timer B input (Count input in event counter mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(TB)}$	TB _{IN} input cycle time (one edge count)		125			ns
$t_{W(TBH)}$	TB _{IN} input high-level pulse width (one edge count)		62			ns
$t_{W(TBL)}$	TB _{IN} input low-level pulse width (one edge count)		62			ns
$t_{C(TB)}$	TB _{IN} input cycle time (both edges count)		250			ns
$t_{W(TBH)}$	TB _{IN} input high-level pulse width (both edges count)		125			ns
$t_{W(TBL)}$	TB _{IN} input low-level pulse width (both edges count)		125			ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(TB)}$	TB _{IN} input cycle time		500			ns
$t_{W(TBH)}$	TB _{IN} input high-level pulse width		250			ns
$t_{W(TBL)}$	TB _{IN} input low-level pulse width		250			ns

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(TB)}$	TB _{IN} input cycle time		500			ns
$t_{W(TBH)}$	TB _{IN} input high-level pulse width		250			ns
$t_{W(TBL)}$	TB _{IN} input low-level pulse width		250			ns

A-D trigger input

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(AD)}$	AD _{TRG} input cycle time (minimum allowable trigger)		1000			ns
$t_{W(ADL)}$	AD _{TRG} input low-level pulse width		125			ns

Serial I/O

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(CLK)}$	CLK _I input cycle time		250			ns
$t_{W(CLKH)}$	CLK _I input high-level pulse width		125			ns
$t_{W(CLKL)}$	CLK _I input low-level pulse width		125			ns
$t_{d(C-Q)}$	TxD _I output delay time				90	ns
$t_{h(C-Q)}$	TxD _I hold time		0			ns
$t_{SU(D-C)}$	RxD _I input setup time		30			ns
$t_{h(C-D)}$	RxD _I input hold time		90			ns

External interrupt INT_i input

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{W(INH)}$	INT _i input high-level pulse width		250			ns
$t_{W(INL)}$	INT _i input low-level pulse width		250			ns

M37705M2AXXXSP
M37705S1ASP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

SWITCHING CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_A=25^\circ C$, $f(X_{IN})=16MHz$, unless otherwise noted)

Single-chip mode

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(E-P0Q)}$	Port P0 data output delay time	Fig. 1			100	ns
$t_{d(E-P1Q)}$	Port P1 data output delay time				100	ns
$t_{d(E-P2Q)}$	Port P2 data output delay time				100	ns
$t_{d(E-P3Q)}$	Port P3 data output delay time				100	ns
$t_{d(E-P4Q)}$	Port P4 data output delay time				100	ns
$t_{d(E-P5Q)}$	Port P5 data output delay time				100	ns
$t_{d(E-P6Q)}$	Port P6 data output delay time				100	ns
$t_{d(E-P7Q)}$	Port P7 data output delay time				100	ns
$t_{d(E-P8Q)}$	Port P8 data output delay time				100	ns

Memory expansion mode and microprocessor mode (when wait bit = "1")

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(P0A-E)}$	Port P0 address output delay time	Fig. 1	30			ns
$t_{d(E-P1Q)}$	Port P1 data output delay time (BYTE="L")				80	ns
$t_{PXZ(E-P1Z)}$	Port P1 floating start delay time (BYTE="L")				5	ns
$t_{d(P1A-E)}$	Port P1 address output delay time		30			ns
$t_{d(E-P2Q)}$	Port P2 data output delay time				80	ns
$t_{PXZ(E-P2Z)}$	Port P2 floating start delay time				5	ns
$t_{d(P2A-E)}$	Port P2 address output delay time		30			ns
$t_{d(ALE-E)}$	ALE output delay time		4			ns
$t_{W(ALE)}$	ALE pulse width		40			ns
$t_{d(BHE-E)}$	BHE output delay time		30			ns
$t_{d(R/W-E)}$	R/W output delay time		30			ns
$t_{d(E-\phi)}$	ϕ output delay time		0		20	ns
$t_{H(E-P0A)}$	Port P0 address hold time		25			ns
$t_{H(ALE-P1A)}$	Port P1 address hold time (BYTE="L")		9			ns
$t_{H(E-P1Q)}$	Port P1 data hold time (BYTE="L")		25			ns
$t_{P2X(E-P1Z)}$	Port P1 floating release delay time (BYTE="L")		25			ns
$t_{H(E-P1A)}$	Port P1 address hold time (BYTE="H")		25			ns
$t_{H(ALE-P2A)}$	Port P2 address hold time		9			ns
$t_{H(E-P2Q)}$	Port P2 data hold time		25			ns
$t_{P2X(E-P2Z)}$	Port P2 floating release delay time		25			ns
$t_{H(E-BHE)}$	BHE hold time		20			ns
$t_{H(E-R/W)}$	R/W hold time		20			ns
$t_{W(EL)}$	\bar{E} pulse width		95			ns

Memory expansion mode and microprocessor mode (when wait bit = "0", and external memory area is accessed)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{d(P0A-E)}$	Port P0 address output delay time	Fig. 1	155			ns
$t_{d(E-P1Q)}$	Port P1 data output delay time (BYTE="L")				80	ns
$t_{PXZ(E-P1Z)}$	Port P1 floating start delay time (BYTE="L")				5	ns
$t_{d(P1A-E)}$	Port P1 address output delay time		155			ns
$t_{d(E-P2Q)}$	Port P2 data output delay time				80	ns
$t_{PXZ(E-P2Z)}$	Port P2 floating start delay time				5	ns
$t_{d(P2A-E)}$	Port P2 address output delay time		155			ns
$t_{d(ALE-E)}$	ALE output delay time		4			ns
$t_{W(ALE)}$	ALE pulse width		165			ns
$t_{d(BHE-E)}$	BHE output delay time		155			ns
$t_{d(R/W-E)}$	R/W output delay time		155			ns
$t_{d(E-\phi_1)}$	ϕ_1 output delay time		0		20	ns
$t_{H(E-P0A)}$	Port P0 address hold time		25			ns
$t_{H(ALE-P1A)}$	Port P1 address hold time (BYTE="L")		9			ns
$t_{H(E-P1Q)}$	Port P1 data hold time (BYTE="L")		25			ns
$t_{PZX(E-P1Z)}$	Port P1 floating release delay time (BYTE="L")		25			ns
$t_{H(E-P1A)}$	Port P1 address hold time (BYTE="H")		25			ns
$t_{H(ALE-P2A)}$	Port P2 address hold time		9			ns
$t_{H(E-P2Q)}$	Port P2 data hold time		25			ns
$t_{PZX(E-P2Z)}$	Port P2 floating release delay time		25			ns
$t_{H(E-BHE)}$	BHE hold time		20			ns
$t_{H(E-R/W)}$	R/W hold time		20			ns
$t_{W(EL)}$	\bar{E} pulse width		220			ns

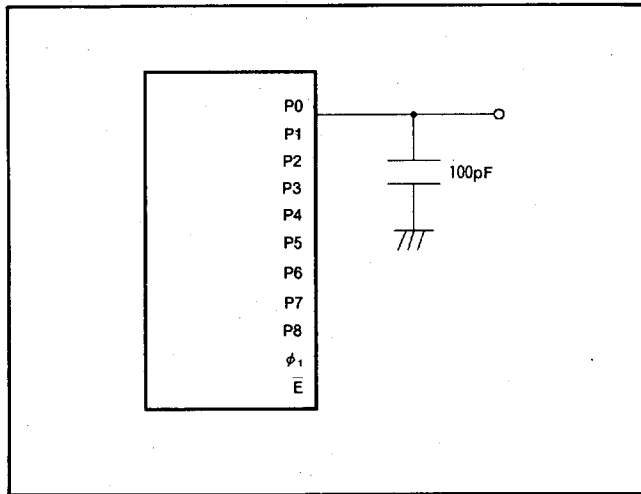
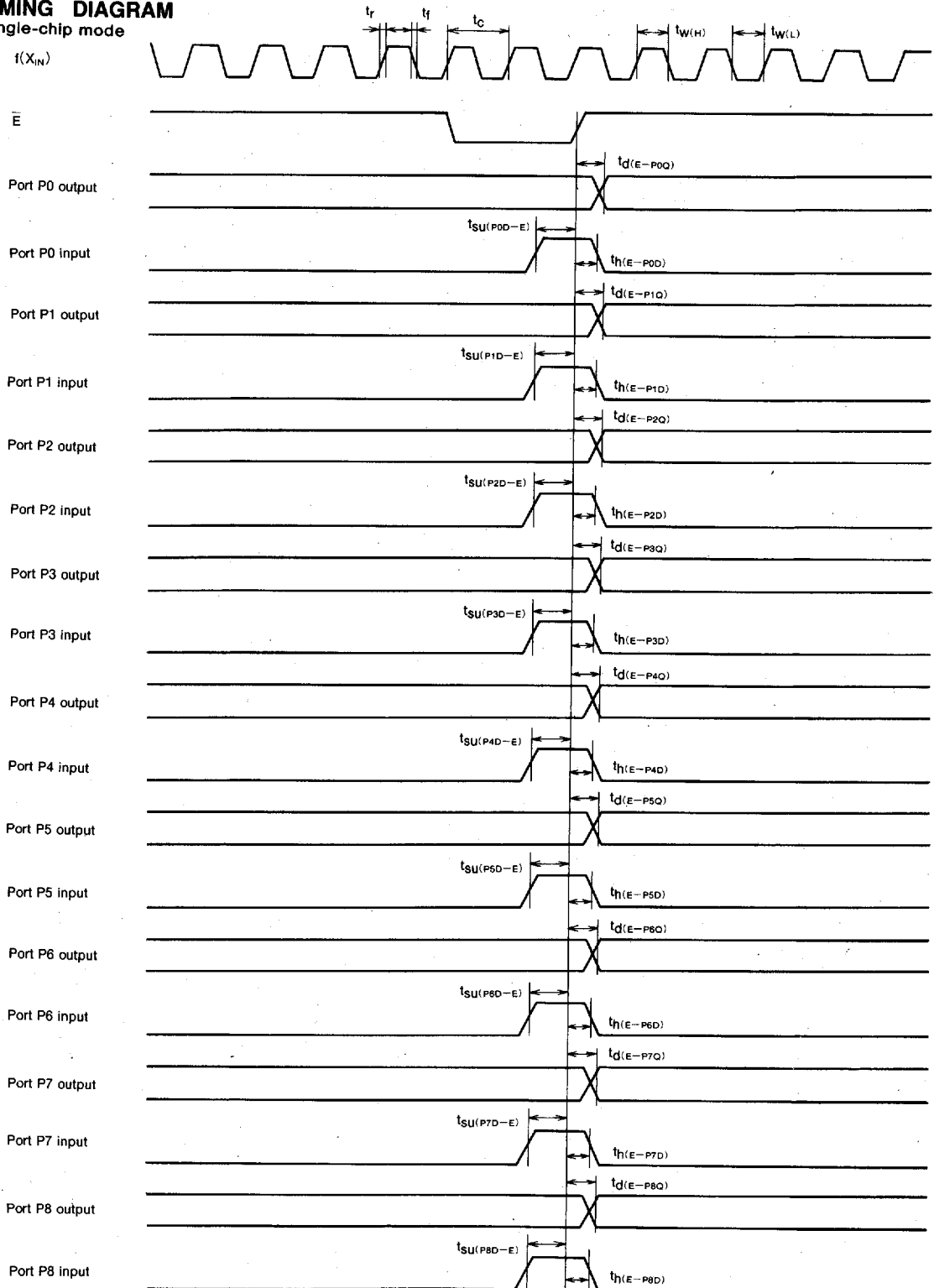


Fig. 1 Testing circuit for ports P0~P8, ϕ_1

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

TIMING DIAGRAM

Single-chip mode

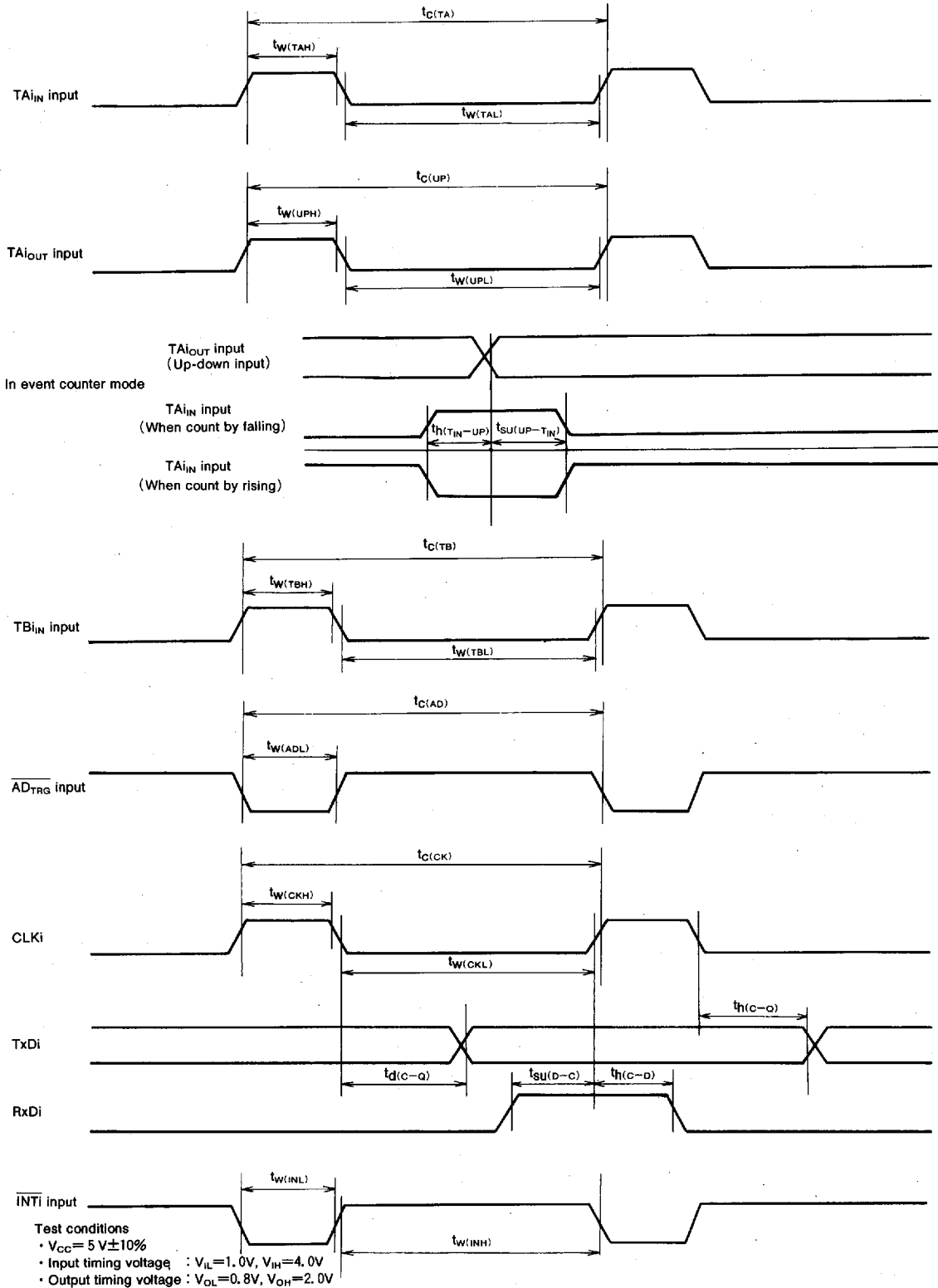


6249828 0026562 699



MITSUBISHI MICROCOMPUTERS
M37705M2AXXXSP
M37705S1ASP

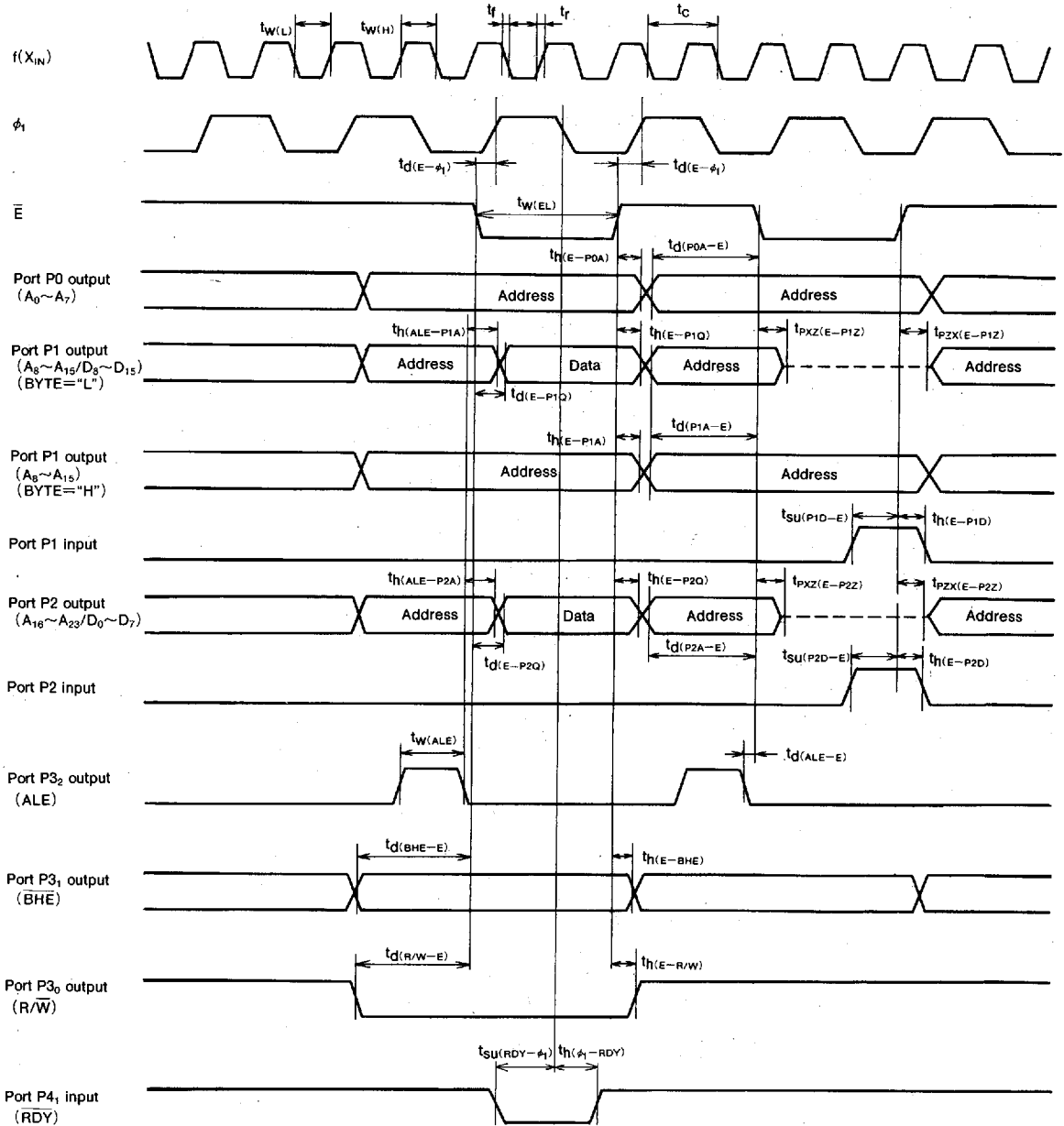
SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER



6249828 0026563 525

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

Memory expansion mode and microprocessor mode(When wait bit = "1")



Test conditions

- $V_{CC} = 5V \pm 10\%$
- Output timing voltage : $V_{OL} = 0.8V$, $V_{OH} = 2.0V$
- Port P1, P2 input : $V_{IL} = 0.8V$, $V_{IH} = 2.5V$
- Port P4₁ input : $V_{IL} = 1.0V$, $V_{IH} = 4.0V$

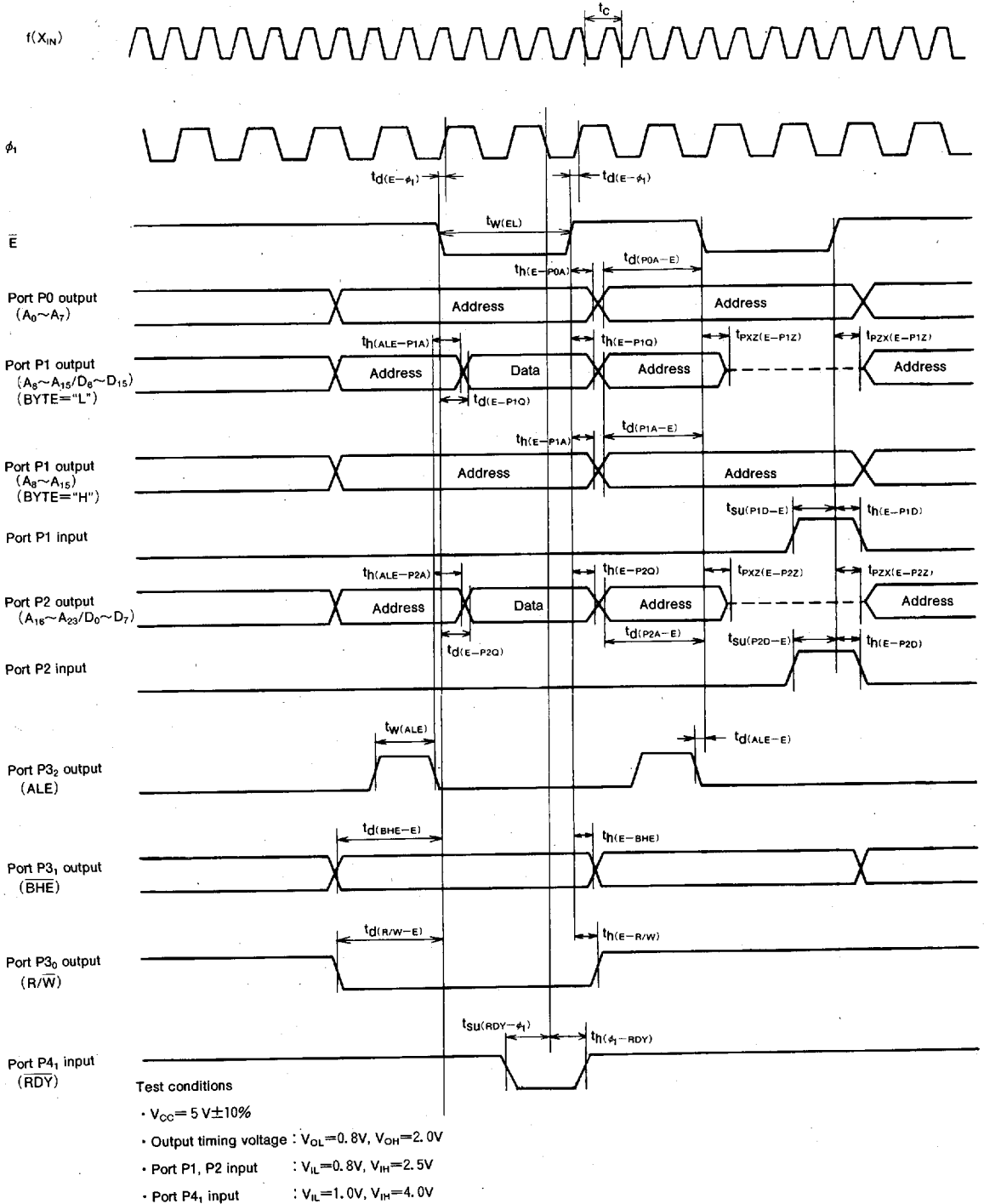
6249828 0026564 461



MITSUBISHI MICROCOMPUTERS
M37705M2AXXSP
M37705S1ASP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

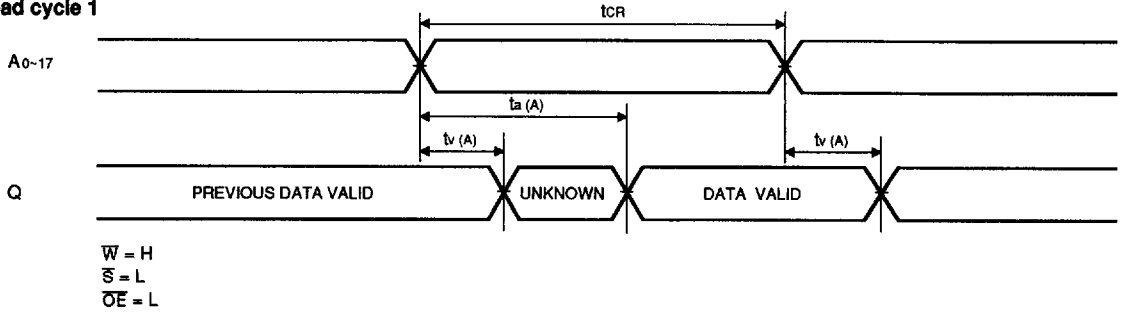
Memory expansion mode and microprocessor mode (When wait bit = "0", and external memory area is accessed)



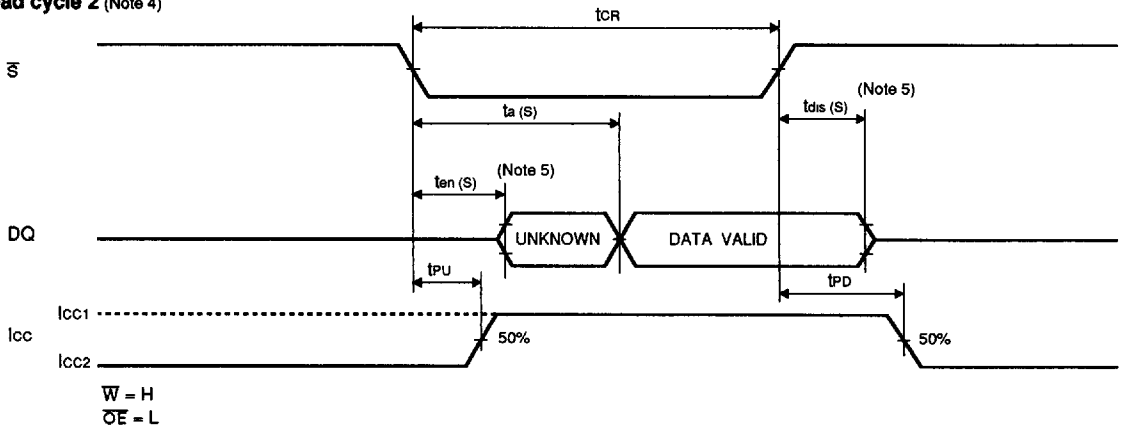
6249828 0026565 3T8

(4) TIMING DIAGRAMS

Read cycle 1



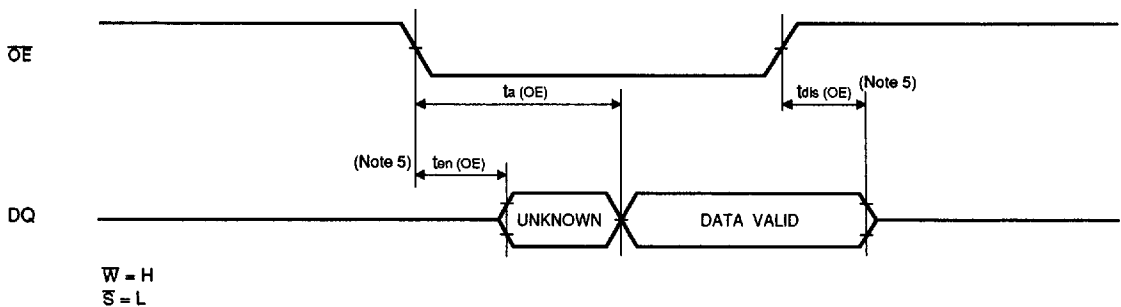
Read cycle 2 (Note 4)



Note 4 : Addresses valid prior to or coincident with \bar{S} transition low.

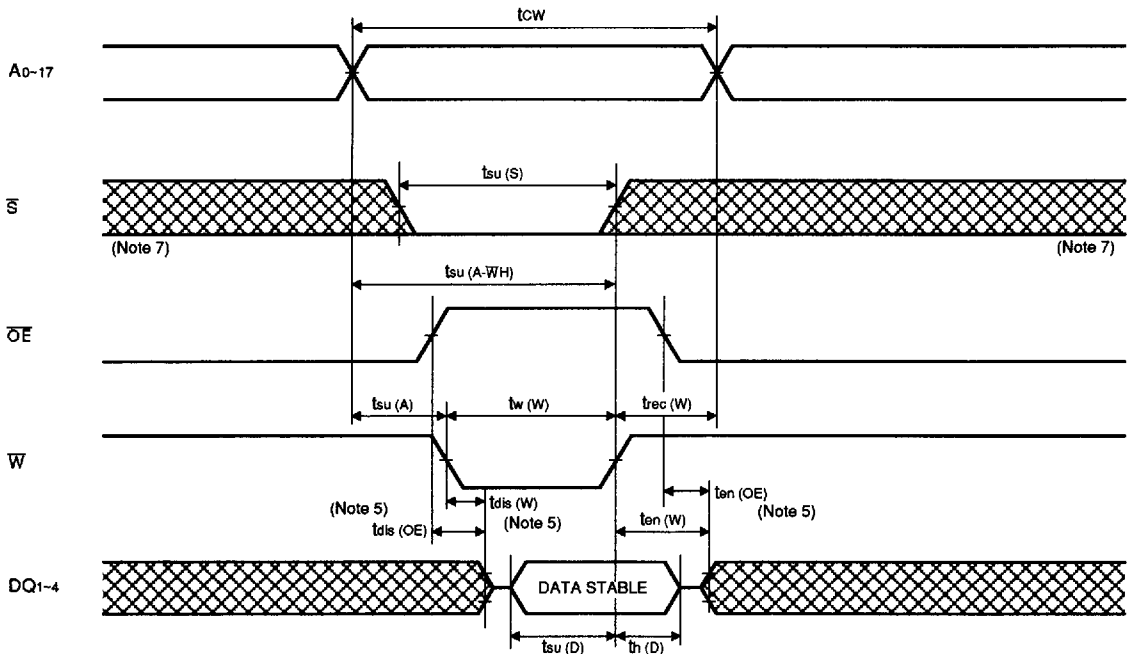
5 : Transition is measured $\pm 500mV$ from steady state voltage with specified loading in Figure 2.

Read cycle 3 (Note 6)

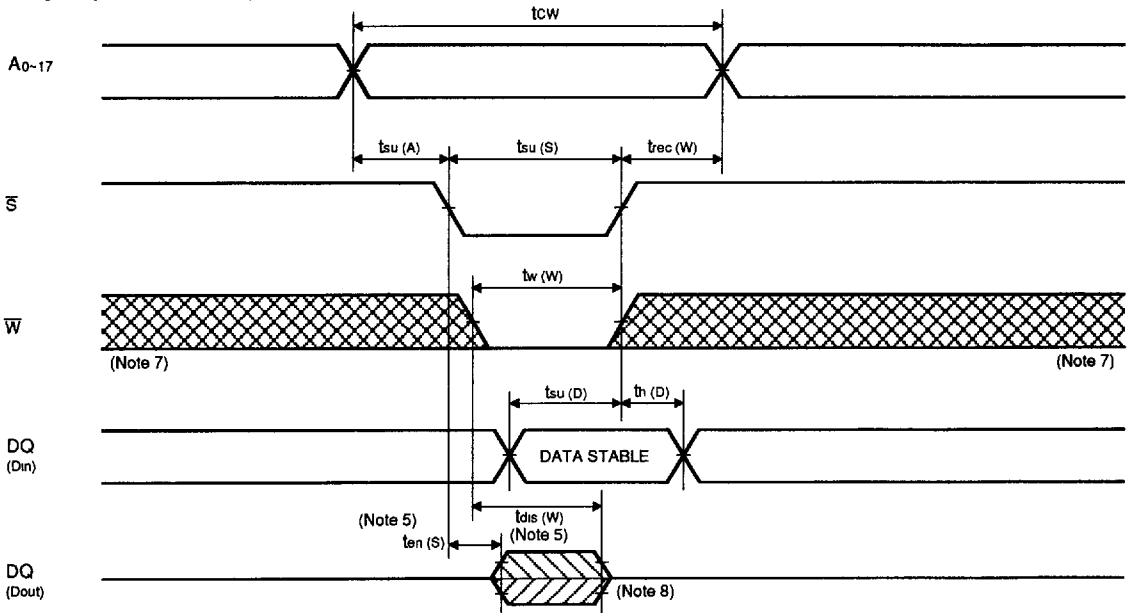


Note 6 : Addresses and \bar{S} valid prior to \bar{OE} transition low by $(t_a(A)-t_a(OE))$, $(t_a(S)-t_a(OE))$

Write cycle (\overline{W} control mode)



Write cycle (\overline{S} control mode)



Note 7 : Hatching indicates the state is don't care.

8 : When the falling edge of \overline{W} is simultaneous or prior to the falling edge of \overline{S} , the output is maintained in the high impedance.

9 : t_{ten} , t_{dis} are periodically sampled and are not 100% tested.

PRELIMINARY
 Note: Pin 19 is not a signal source. Input
 Some parameters are not supported.

MITSUBISHI LSIs

M5M5V1001CP,J-15,-20,-25

1048576-BIT (1048576-WORD BY 1-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5V1001CP,J are a family of 1048576-word by 1-bit static RAMs, fabricated with the high performance CMOS silicon gate process and designed for high-speed application.

The M5M5V1001CP,J are offered in a 28-pin plastic dual-in-line package (DIP), 28-pin plastic small outline J-lead package (SOJ).

These devices operate on a single 3.3V supply, and are directly TTL compatible. They include a power down feature as well.

FEATURES

Type name	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5V1001CP,J - 15	15ns	120mA	
M5M5V1001CP,J - 20	20ns	100mA	1mA
M5M5V1001CP,J - 25	25ns	90mA	

- Single +3.3V power supply
- Fully static operation : No clocks, No refresh
- Power down by \bar{S}
- Easy memory expansion by \bar{S}
- Three-state outputs : OR-tie capability
- Directly TTL compatible : All inputs and outputs
- TEST MODE is available

PACKAGE

M5M5V1001CP 28pin 400mil DIP
 M5M5V1001CJ 28pin 400mil SOJ

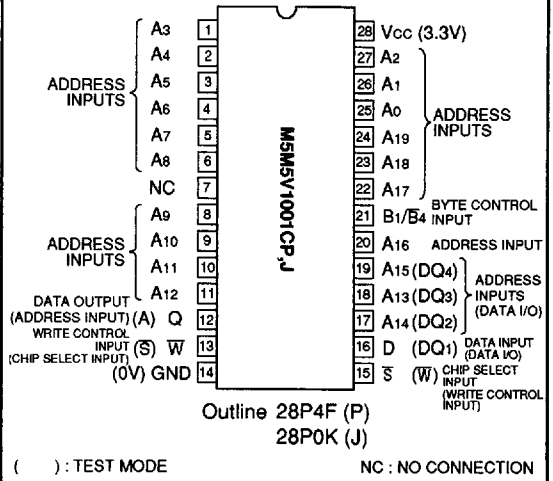
APPLICATION

High speed memory units

FUNCTION

The operation mode of the M5M5V1001C series is determined by

PIN CONFIGURATION (TOP VIEW)



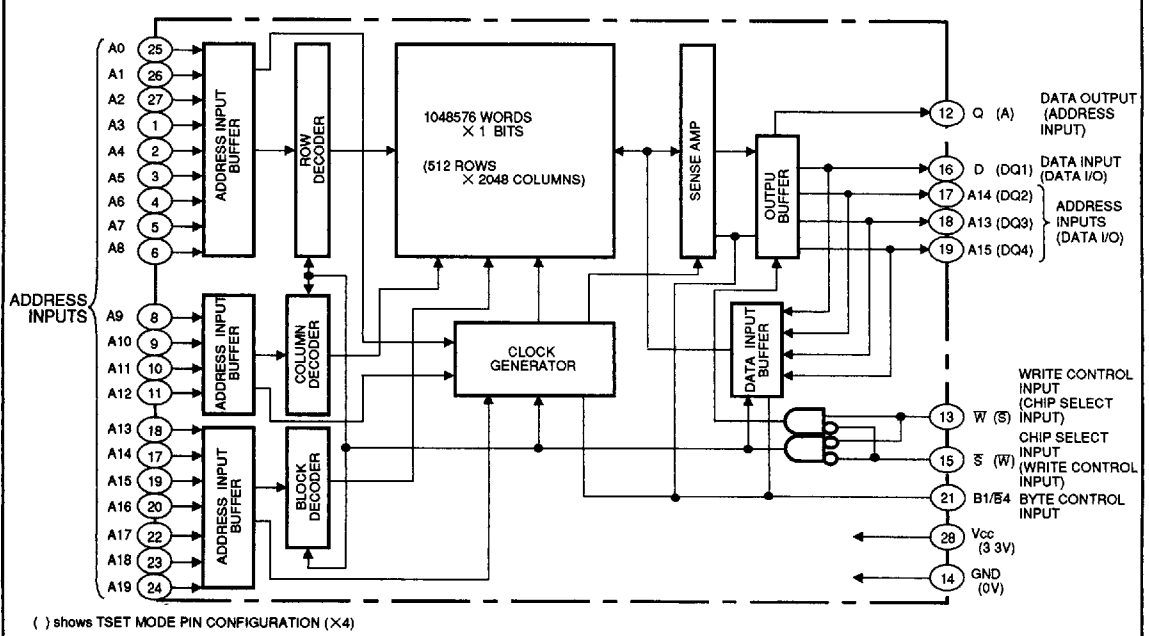
a combination of the device control inputs \bar{S} and \bar{W} . Each mode is summarized in the function table shown in next page.

The RAM works with an organization of 1048576-word by 1-bit, when $B1/\bar{B}4$ is high of floating. And an organization of 262144-word by 4-bit is also obtained for reducing the test time, when $B1/\bar{B}4$ is low.

A write cycle is executed whenever the low level \bar{W} overlaps with the low level \bar{S} . The address must be set-up before the write cycle and must be stable during the entire cycle.

The data is latched into a cell on the trailing edge of \bar{W} , \bar{S} whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. When \bar{S} is high, the chip is non-selectable state, disabling both reading and writing. In the

BLOCK DIAGRAM



MITSUBISHI LSIs
M5M5V1001CP,J-15,-20,-25

1048576-BIT (1048576-WORD BY 1-BIT) CMOS STATIC RAM

case, the output stage is in a high-impedance state.

A read cycle is executed by setting \bar{W} at a high level while \bar{S} are in an active state ($\bar{S} = L$)

When setting \bar{S} at a high level, the chip is in a non-selectable mode in which both reading and write are disabled.

In this mode, the output stage is in a high-impedance state, allowing OR -tie with other chips and memory expansion by \bar{S} .

Signal \bar{S} controls the power-down feature. When \bar{S} goes high, power dissipation is reduced extremely. The access time from \bar{S} is equivalent to the address access time.

FUNCTION TABLE

\bar{S}	\bar{W}	Mode	Q	D	I _{cc}
H	X	Non selection	High-impedance	High-impedance	Stand-by
L	L	Write	Din	High-impedance	Active
L	H	Read	High-impedance	Dout	Active

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage	With respect to GND	-2.0*~4.6	V
V _I	Input voltage		-2.0*~V _{cc} + 0.5	V
V _O	Output voltage		-2.0*~V _{cc}	V
P _d	Power dissipation	T _a = 25°C	1000	mW
T _{opr}	Operating temperature		0~70	°C
T _{stg (bias)}	Storage temperature (bias)		-10~85	°C
T _{stg}	Storage temperature		-65~150	°C

*-0.5V in case of DC (Pulse width ≤ 20ns)

DC ELECTRICAL CHARACTERISTICS (T_a = 0~70°C, V_{cc} = 3.3V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{IH}	High-level input voltage		2.2		V _{cc} +0.3V	V
V _{IL}	Low-level input voltage		-0.3*		0.8	V
V _{OH}	High-level output voltage	I _{OH} = -4mA	2.4			V
V _{OL}	Low-level output voltage	I _{OL} = 8mA			0.4	V
I _I	Input current	V _I = 0~V _{cc}			2	μA
I _{oz}	Output current in off-state	V _I (S) = V _{IH} V _{IO} = 0~V _{cc}			10	μA
I _{cc1}	Active supply current (TTL level)	V _I (S) = V _{IL} other inputs = V _{IH} or V _{IL} Output-open (duty 100%)	AC (15ns cycle)		120	mA
			AC (20ns cycle)		100	
			AC (25ns cycle)		90	
			DC	45	55	
I _{cc2}	Stand-by supply current (TTL level)	V _I (S) = V _{IH}	AC (15ns cycle)		45	mA
			AC (20/25ns cycle)		35	
			DC		20	
I _{cc3}	Stand-by current (MOS level)	V _I (S) ≥ V _{cc} - 0.2V other inputs V _I ≤ 0.2V or V _I ≥ V _{cc} - 0.2V		0.1	1	mA

*-3.0V in case of AC(Pulse width ≤ 20ns)

CAPACITANCE (T_a = 0~70°C, V_{cc} = 3.3V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _I	Input capacitance	V _I = GND, V _I = 25mVrms, f = 1MHz			6	pF
C _O	Output capacitance	V _O = GND, V _O = 25mVrms, f = 1MHz			6	pF

Note 1 : Direction for current flowing into an IC is positive (no mark).
 2 : Typical value is V_{cc} = 3.3V, T_a = 25°C.
 3 : C_I, C_O are periodically sampled and are not 100% tested.