M37102E8-XXXSP/FP
M37201E6-XXXSP

PROM VERSION of M37102M8-XXXSP/FP,M37201M6-XXXSP

DESCRIPTION

The M37102E8-XXXSP/FP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP or an 80-pin plastic molded QFP. The features of this chip are similar to those of the M37102M8-XXXSP/FP except that this chip has a 16384 bytes PROM built in. This single-chip microcomputer is useful for the high-tech channel selection system for TVs. In addition to its simple instruction sets, the PROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming. Since general purpose PROM writers can be used for the built-in PROM, this chip is suitable for small quantity production runs.

The differences between the M37102E8-XXXSP and the M37201E6-XXXSP are noted below. The following explanations apply to the M37102E8-XXXSP

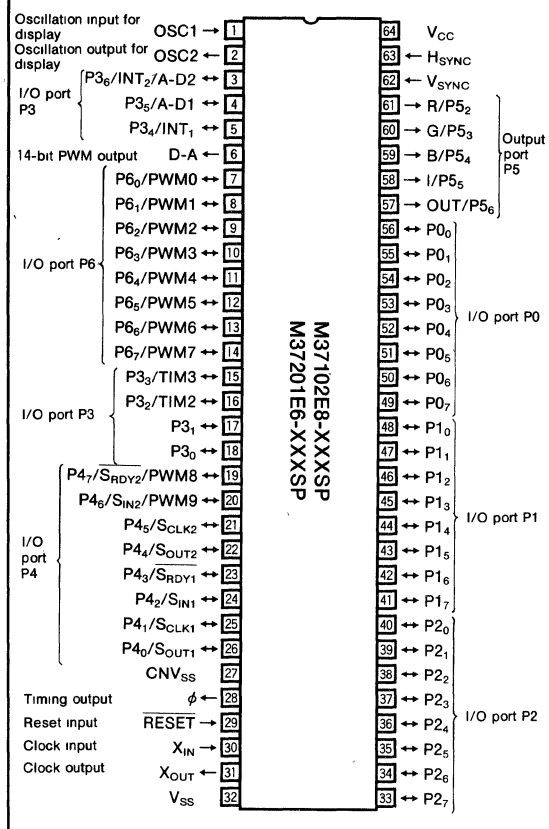
Specification variations for other chips are noted accordingly.

Type name	ROM size	RAM size
M37102E8-XXXSP	16384 bytes	320 bytes
M37201E6-XXXSP	24576 bytes	384 bytes

FEATURES

- Number of basic instructions 69
- Memory size PROM .. 16384 bytes (M37102E8-XXXSP/FP)
  24576 bytes (M37201E6-XXXSP)
  RAM .. 320 bytes (M37102E8-XXXSP/FP)
  384 bytes (M37201E6-XXXSP)
- Instruction execution time
  ..... 1μs (minimum instructions at 4MHz frequency)
- Single power supply ..... 5V$\pm$10%
- Power dissipation
  normal operation mode (at 4MHz frequency)
  ..... 110mW (V_{CC}=5.5V, CRT display)
- Subroutine nesting ..... 96 levels (Max.)
- Interrupt 13types, 13vectors
- 8-bit timer 4
- Programmable I/O ports
  (Ports P0, P1, P2, P3, P4, P6) 47
- Output port (Port P5) 5
- Serial I/O (8-bit) 2
- PWM function ..... 14-bit×1
  8-bit×10
- A-D converter (4-bit resolution) ..... 2 channels
- 72-character on screen display function
  Number of character ..... 24 characters×3 lines
  Kinds of character 126
- PROM (equivalent to the M5L27256)
  Program voltage 12.5V

PIN CONFIGURATION (TOP VIEW)

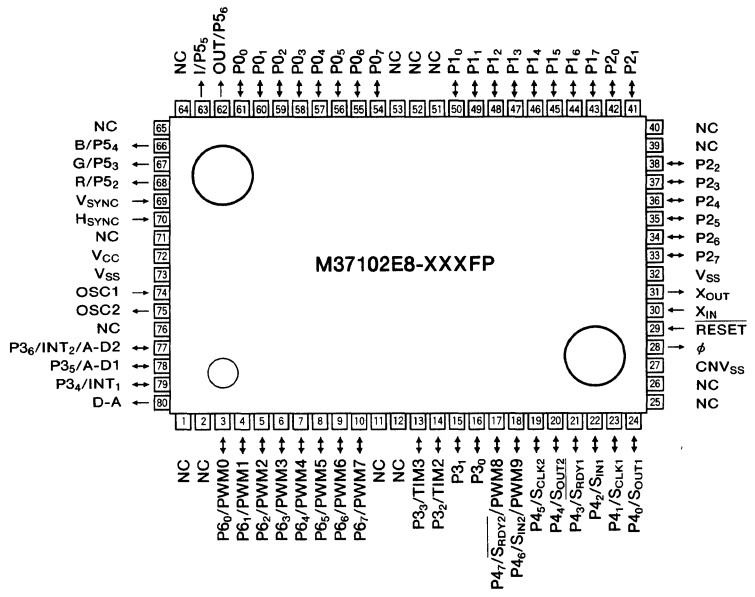


Outline 64P4B

APPLICATION

TV

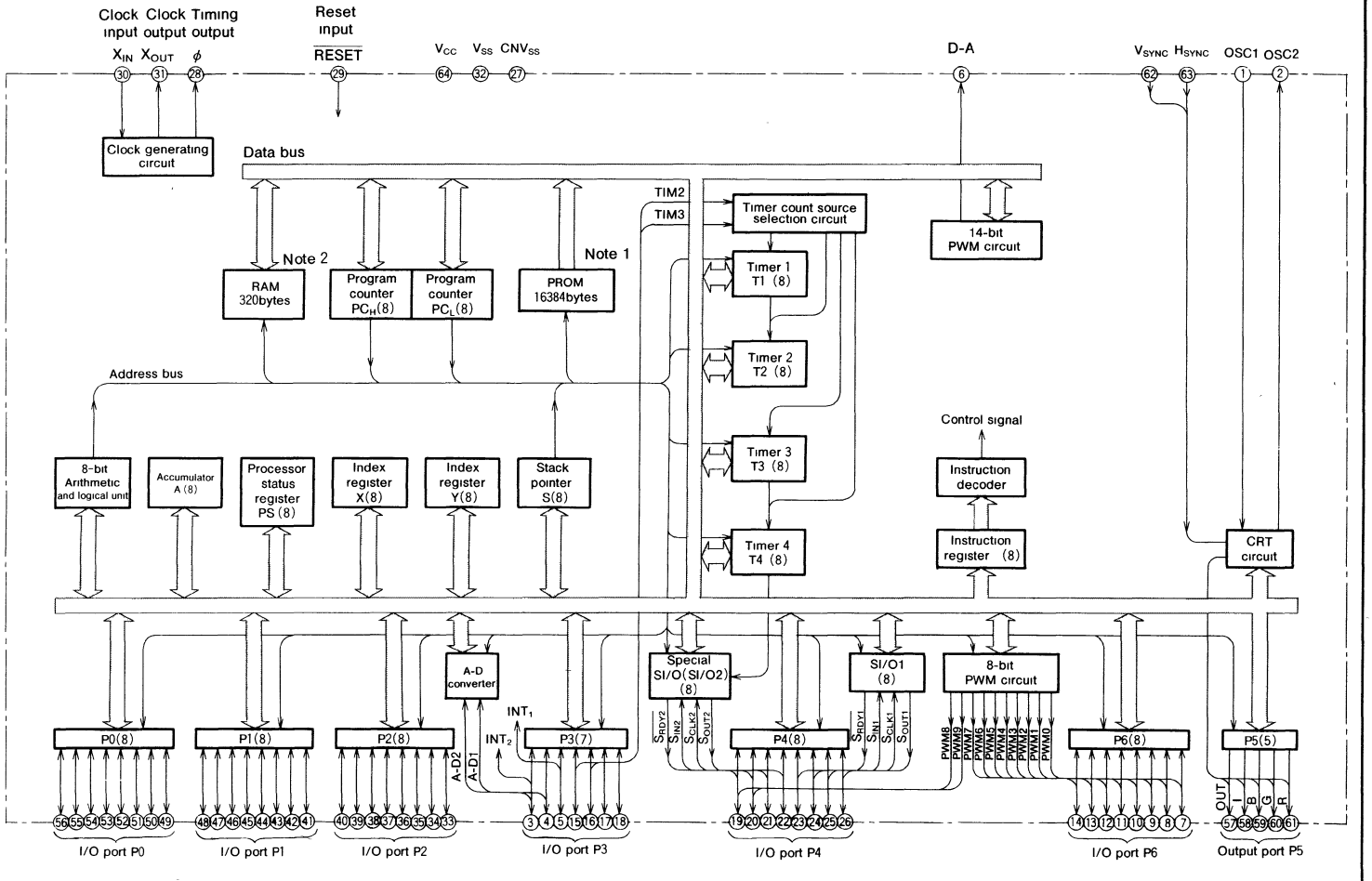
PIN CONFIGURATION (TOP VIEW)



Outline 80P6N

NC : No connection

M37102E8-XXXSP BLOCK DIAGRAM



Note 1 24576 bytes for M37201E6-XXXSP
2 · 384 bytes for M37201E6-XXXSP

FUNCTIONS OF M37102E8-XXXSP/FP, M37201E6-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			1 μs (minimum instructions, at 4MHz frequency)
Clock frequency			4MHz
Memory size	M37102E8-XXXSP/FP	ROM	16384 bytes
		RAM	320 bytes
	M37201E6-XXXSP	ROM	24576 bytes
		RAM	384 bytes
Input/Output ports	P0, P1, P2	I/O	8-bit×3
	$P3_0$, $P3_1$	I/O	2-bit×1
	$P3_2$-$P3_6$	I/O	5-bit×1 (can be used as timer input pins, INT_1, INT_2 input pins and A-D input pins)
	P4	I/O	8-bit×1 (can be used as serial I/O function pins and PWM output pins)
	P5	Output	5-bit×1 (can be used as R, G, B, I, OUT pins)
	P6	I/O	8-bit×1 (can be used as PWM output pins)
Serial I/O			8-bit×2 (Special serial I/O (8-bit)×1)
Timers			8-bit timer×4
Subroutine nesting			96levels (max.)
Interrupt			Two external interrupts, nine internal interrupts, one software interrupt
Clock generating circuit			Built-in circuit (externally connected ceramic or quartz crystal oscillator)
Supply voltage			5V±10%
Power dissipation	at CRT display ON		110mW (clock frequency X_{IN}=4MHz, V_{CC}=5.5V, Typ.)
	at CRT display OFF		55mW (clock frequency X_{IN}=4MHz, V_{CC}=5.5V, Typ.)
	at stop mode		1.65mW (Max.)
Input/Output characteristics	Input/Output voltage		5V (Port $P4_6$, $P4_7$, $P6_0$-$P6_7$)
	Output current		10mA (Port $P2_4$-$P2_7$)
Operating temperature range			−10 to 70°C
Device structure			CMOS silicon gate process
Package	M37102E8-XXXSP, M37201E6-XXXSP		64-pin shrink plastic molded DIP
	M37102E8-XXXFP		80-pin plastic molded QFP
CRT display function	Number of character		24 characters×3 lines
	Kinds of character		126 (12×16 dots)

PIN DESCRIPTION

Pin	Mode	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Single-chip	Power supply		Power supply inputs 5V±10% (typ) to V_{CC}, and 0V to V_{SS}
	EPROM			Power supply inputs 5V, or 6V (writing to built-in PROM) to V_{CC}, and 0V to V_{SS}
CNV_{SS}	Single-chip	CNV_{SS}	Input	This is connected to V_{SS}
	EPROM			V_{PP} inputs when writing to built-in PROM or verify check of built-in PROM contents
$\overline{RESET}$	Single-chip	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
	EPROM			Input "L" level
X_{IN}	Single-chip /EPROM	Clock input	Input	This chip has an internal clock generating circuit To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open
X_{OUT}		Clock output	Output	
ϕ	Single-chip	Timing output	Output	This is the timing output pin and has the reset out signal output function
	EPROM			This pin is setting to open
$P0_0$-$P0_7$	Single-chip	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output At reset, this port is set to input mode The output structure is CMOS output.
	EPROM	Address input	Input	Low-order 8-bit of address is input
$P1_0$-$P1_7$	Single-chip	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same function as port P0
	EPROM	Address input	Input	High-order 8-bit of address is input.
$P2_0$-$P2_7$	Single-chip	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same function as port P0
	EPROM	Data input/output		8-bit data is input or output.
$P3_0$-$P3_6$	Single-chip	I/O port P3	I/O	Port P3 is a 7-bit I/O port and has basically the same function as port P0, but the output structure of $P3_0$ and $P3_1$ is CMOS output and the output structure of $P3_2$-$P3_6$ is N-channel open drain $P3_2$ and $P3_3$ are in common with external clock input pins of timer 2 and Timer 3 $P3_4$ and $P3_6$ are in common with external interrupt input pins INT_1 and INT_2 $P3_5$ and $P3_6$ are in common with analog input pins of A-D converter (A-D1, A-D2)
	EPROM	Mode input	Input	$P3_0$ and $P3_1$ are the input pins as $\overline{OE}$ and $\overline{CE}$ $P3_2$ and $P3_3$ are connected to V_{CC} $P3_4$-$P3_6$ are connected to V_{SS}
$P4_0$-$P4_7$	Single-chip	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is N-channel open drain When serial I/O1 is used, $P4_0$, $P4_1$, $P4_2$, and $P4_3$ work as S_{OUT1}, S_{CLK1}, S_{IN1} and $\overline{S_{RDY1}}$ pins, respectively When serial I/O2 is used, $P4_4$ $P4_5$, $P4_6$, and $P4_7$ work as S_{OUT2}, S_{CLK2}, S_{IN2} and $\overline{S_{RDY2}}$ pins, respectively. Also $P4_6$, $P4_7$ are in common with PWM output pins of PWM8 and PWM 9
	EPROM	Input port P4	Input	$P4_0$-$P4_6$ are all connected to V_{SS}, and $P4_7$ is connected to V_{CC}
OSC1 OSC2	Single-chip	Clock I/O for CRT display	I/O	This is the I/O pins of the clock generating circuit for the CRT display function
	EPROM		Output	These pins are setting to open

PIN DESCRIPTION

Pin	Mode	Name	Input/ Output	Functions
H_{SYNC}	Single-chip	Horizontal synchronous signal	Input	This is the horizontal synchronizing signal input for CRT display.
	EPROM			This is connected to V_{SS}
V_{SYNC}	Single-chip	Vertical synchronous signal	Input	This is the vertical synchronizing signal input for CRT display
	EPROM			This is connected to V_{SS}.
R, G, B, I, OUT	Single-chip	Video signal	Output	This is a 5-bit output pin for CRT display. The output structure is CMOS output. This is in common with ports $P5_2$-$P5_6$
	EPROM			These pins are setting to open
$P6_0$-$P6_7$	Single-chip	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is N-channel open drain This port is in common with PWM output pins PWM0-PWM7
	EPROM	Input port P6	Input	All pins are connected to V_{SS}
D-A	Single-chip	D-A output	Output	This is an output pin for 14-bit PWM
	EPROM			This pin is setting to open

EPROM MODE

The M37102E8-XXXSP/FP features an EPROM mode in addition to its normal modes. When the $\overline{RESET}$ signal level is low ("L") and CNV_{SS}/V_{PP} signal level is high ("H"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1 to 3 give the pin connections in the EPROM mode. When in the EPROM mode, ports P0, P1, P2, $P3_0$, $P3_1$ and CNV_{SS} are used for the PROM (equivalent to the M5L27256). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5L27256. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 1. Pin function in EPROM mode

	M37102E8-XXXSP/FP	M5L27256
V_{CC}	V_{CC}	V_{CC}
V_{PP}	CNV_{SS}	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports P0, $P1_0$-$P1_6$	A_0-A_{14}
Data I/O	Port P2	D_0-D_7
$\overline{CE}$	$P3_1$	$\overline{CE}$
$\overline{OE}$	$P3_0$	$\overline{OE}$

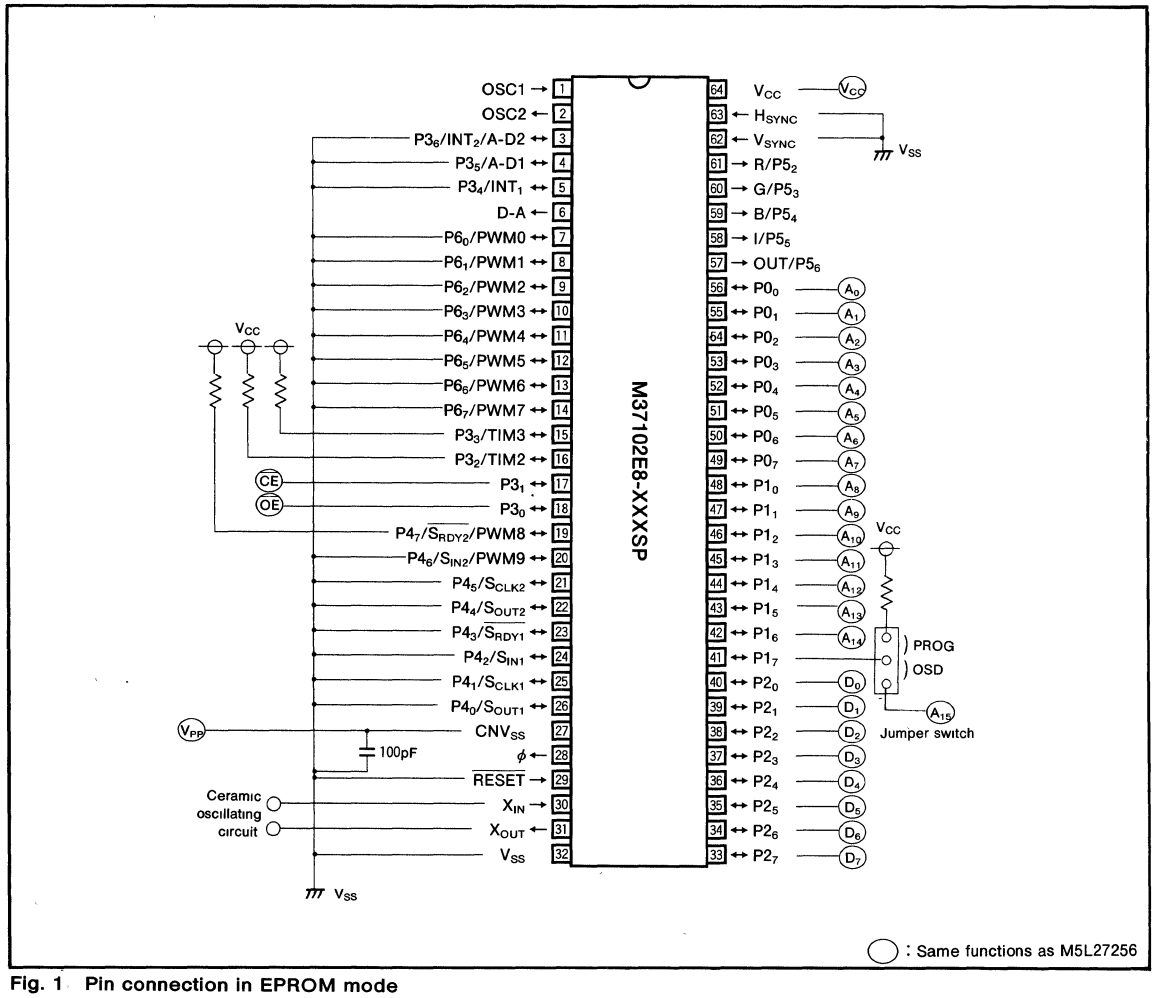


Fig. 1 Pin connection in EPROM mode

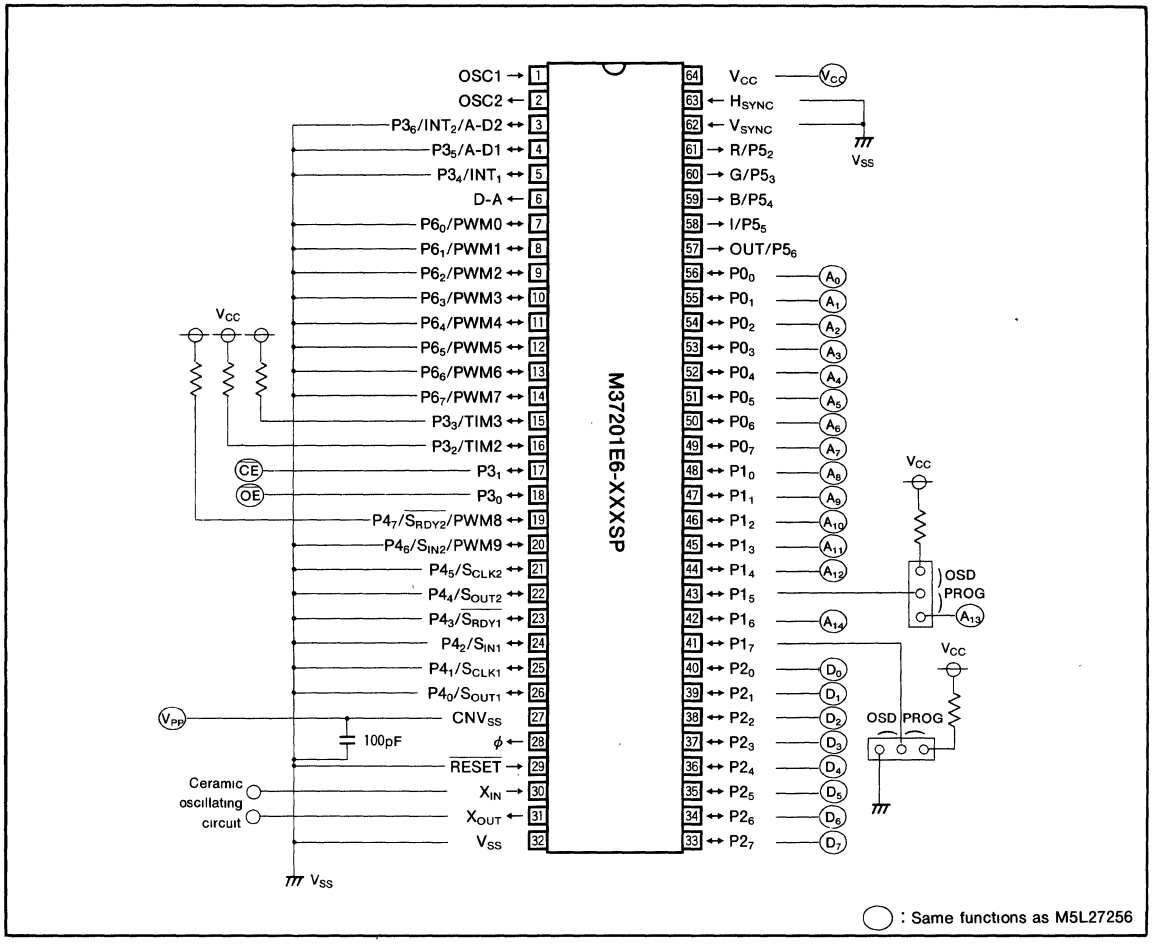


Fig. 2 Pin connection in EPROM mode

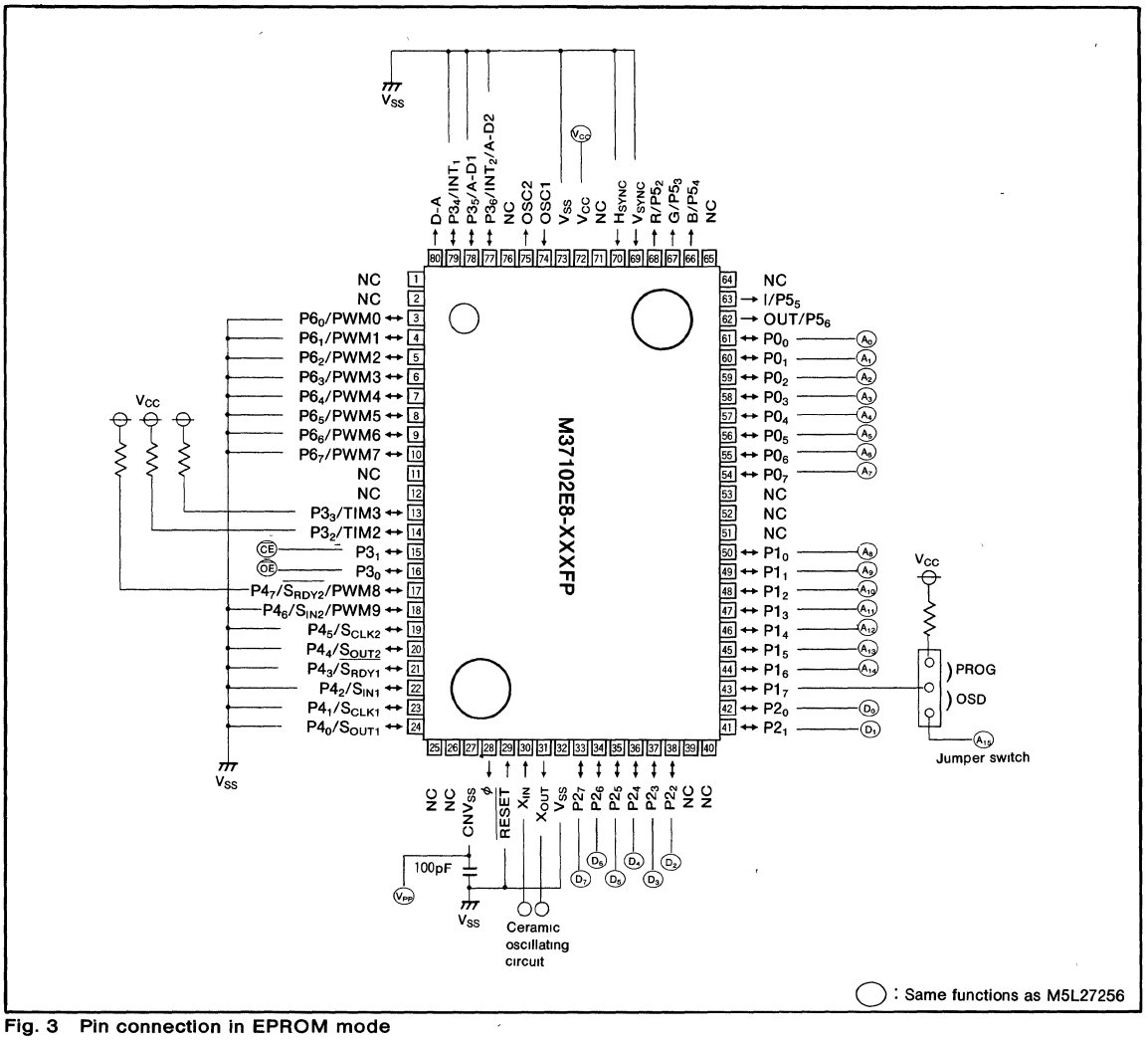


Fig. 3 Pin connection in EPROM mode

PROM READING, WRITING AND ERASING

Reading

To read the PROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level, and supply 0V to the $\overline{RESET}$ pin, 5V to the V_{CC} pin and the CNV_{SS} (V_{PP}) pin. Input the address of the data (A_0-A_{14}) to be read and the data will be output to the I/O pins D_0-D_7. The data I/O pins will be floating when the $\overline{OE}$ pin is in the "H" state.

Writing

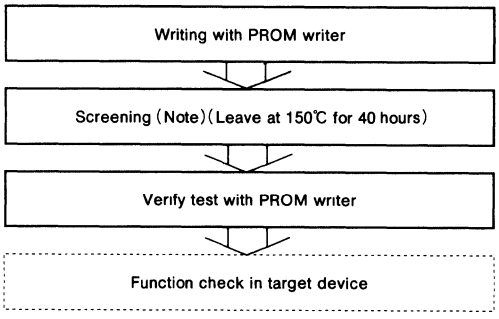
To write to the PROM, set the $\overline{OE}$ pin to an "H" level, and supply 0V to the $\overline{RESET}$ pin, 6V to the V_{CC} pin and 12.5V to the V_{PP} pin. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins A_0-A_{14}, and the data to be written is input to pins D_0-D_7. Set the $\overline{CE}$ pin to a "L" level to begin writing.

NOTES ON HANDLING

(1) Since a high voltage is used to write data, care should be taken when turning on the PROM writer's power.

(2) For the programmable microcomputer (shipped in blank or OTP type), Mitsubishi does not perform PROM write test and screening in the assembly process and following process. To improve reliability after write, performing write and test according to the flow below before use is recommended.

(3) In EPROM mode, address A_{15} is set to "H" automatically.



Note : Since the screening temperature is higher than storage temperature, never expose to 150℃ exceeding 100 hours.

Table 2. I/O signal in each mode

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	Data I/O
Read-out	V_{IL}	V_{IL}	5V	5V	Output
Output disable	V_{IL}	V_{IH}	5V	5V	Floating
Programming	V_{IL}	V_{IH}	12.5V	6V	Input
Programming verify	V_{IH}	V_{IL}	12.5V	6V	Output
Program disable	V_{IH}	V_{IH}	12.5V	6V	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "off" state	−0.3 to 6	V
V_I	Input voltage CNV_{SS}		−0.3 to 6	V
V_I	Input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_6$, $P4_0$-$P4_7$, $P6_0$-$P6_7$, H_{SYNC}, V_{SYNC}, $\overline{RESET}$		−0.3 to V_{CC}+0.3	V
V_O	Output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_6$, $P4_0$-$P4_5$, R, G, B, I, OUT, D-A, X_{OUT}, OSC2		−0.3 to V_{CC}+0.3	V
V_O	Output voltage $P4_6$, $P4_7$, $P6_0$-$P6_7$		−0.3 to 13	V
I_{OH}	Circuit current R, G, B, I, OUT, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$, $P3_1$, D-A		0 to 1(Note 1)	mA
I_{OL1}	Circuit current R, G, B, I, OUT, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$-$P3_6$, $P4_0$-$P4_3$, D-A		0 to 2(Note 2)	mA
I_{OL2}	Circuit current $P6_0$-$P6_7$, $P4_6$, $P4_7$		0 to 1(Note 2)	mA
I_{OL3}	Circuit current $P2_4$-$P2_7$		0 to 10(Note 3)	mA
I_{OL4}	Circuit current $P4_4$, $P4_5$		0 to 3(Note 2)	mA
Pd	Power dissipation	T_a=25℃	550	mW
Topr	Operating temperature		−10 to 70	℃
Tstg	Storage temperature		−40 to 125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=−10 to 70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage(Note 4) During the CRT operation	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	"H" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_6$, $P4_0$-$P4_3$, $P4_6$,$P4_7$, $P6_0$-$P6_7$, H_{SYNC}, V_{SYNC}, $\overline{RESET}$, X_{IN}, OSC1	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P4_4$, $P4_5$	0.7V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, $P3_5$, $P4_0$, $P4_3$-$P4_5$, $P4_7$	0		0.4V_{CC}	V
V_{IL}	"L" input voltage $P3_2$-$P3_4$, $P3_6$, $P4_1$, $P4_2$, $P4_6$, H_{SYNC}, V_{SYNC}, $\overline{RESET}$, X_{IN}, OSC1	0		0.2V_{CC}	V
I_{OH}	"H" average output current (Note 1) R,G,B,I,OUT,$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$			1	mA
I_{OL1}	"L" average output current (Note 2) R,G,B,I,OUT,$P0_0$-$P0_7$, $P2_0$-$P2_3$, $P3_0$-$P3_6$, $P4_0$-$P4_3$, D-A			2	mA
I_{OL2}	"L" average output current (Note 2) $P6_0$-$P6_7$, $P4_6$, $P4_7$			1	mA
I_{OL3}	"L" average output current (Note 3) $P2_4$-$P2_7$			10	mA
I_{OL4}	"L" average output current (Note 2) $P4_4$, $P4_5$			3	mA
f_{CPU}	Oscillating frequency (for CRT operation)(Note 5)	3.6	4.0	4.4	MHz
f_{CRT}	Oscillating frequency (for CRT display)	6.0	7.0	8.0	MHz
fhs	Input frequency $P3_2$-$P3_4$, $P3_6$, $P4_5$			100	kHz
fhs	Input frequency $P4_1$			1	MHz

Note 1 : The total current that flows out of the IC should be 20mA (max.)
2 : The total of I_{OL1}, I_{OL2} and I_{OL4} should be 30mA (max.)
3 : The total of I_{OL} of port $P2_4$-$P2_7$ should be 20mA (max)
4 : Apply 0.022μF or greater capacitance externally between the V_{CC}−V_{SS} power supply pins so as to reduce power source noise
Also apply 0.068μF or greater capacitance externally between the V_{CC}−CNV_{SS} pins.
5 : Use the crystal oscillator or ceramic resonator for CPU oscillation circuit

ELECTRIC CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10 to 70℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Supply current	V_{CC}=5.5V, f(X_{IN})=4MHz CRT OFF		10	20	mA
		V_{CC}=5.5V, f(X_{IN})=4MHz CRT ON		20	30	
		At stop mode			300	μA
V_{OH}	"H" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$, $P3_1$, R, G, B, I, OUT	V_{CC}=4.5V I_{OH}=−0.5mA	2.4			V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_3$, $P3_0$-$P3_6$, $P4_0$-$P4_3$, R, G, B, I, OUT, D-A	V_{CC}=4.5V I_{OL}=0.5mA			0.4	V
	"L" output voltage $P6_0$-$P6_7$, $P4_6$, $P4_7$	V_{CC}=4.5V I_{OL}=0.5mA			0.4	
	"L" output voltage $P2_4$-$P2_7$	V_{CC}=4.5V I_{OL}=10.0mA			3.0	
	"L" output voltage $P4_4$, $P4_5$	V_{CC}=4.5V I_{OL}=3mA			0.4	
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$	V_{CC}=5.0V		0.5	0.7	V
	Hysteresis (Note 1) H_{SYNC}, V_{SYNC}, $P3_2$-$P3_4$, $P3_6$, $P4_1$, $P4_2$, $P4_4$-$P4_6$	V_{CC}=5.0V		0.5	1.3	
I_{OZH}	"H" input leak current $\overline{RESET}$, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_6$, $P4_0$-$P4_5$	V_{CC}=5.5V V_O=5.5V			5	μA
	"H" input leak current $P6_0$-$P6_7$, $P4_6$, $P4_7$	V_{CC}=5.5V V_O=12V			10	
I_{OZL}	"L" input leak current $\overline{RESET}$, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_6$, $P4_0$-$P4_7$, $P6_0$-$P6_7$	V_{CC}=5.5V V_O=0V			5	μA

Note 1. $P3_2$-$P3_4$, $P3_6$ have the hysteresis when these pins are used as interrupt input pins or timer input pins.
$P4_1$, $P4_2$, $P4_4$-$P4_6$ have the hysteresis when these pins are used as serial I/O ports