M37120M6-XXXFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DISCRIPTION

The M37120M6-XXXFP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in an 80-pin plastic molded QFP. This single-chip microcomputer is useful for appliance controllers.

In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

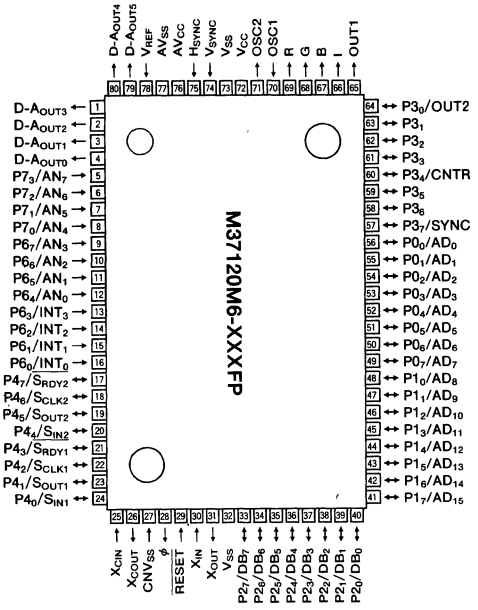
FEATURES

- Number of basic instructions 71
- Memory size
  - ROM ..... 12288 bytes
  - RAM ..... 256 bytes
- Instruction execution time
  - ..... 1μs (minimum instructions at 4MHz frequency)
- Single power supply
  - f(X_{IN})=4MHz ..... 5V$\pm$10%
- Power dissipation
  - normal operation mode
  - (at 4MHz frequency) 75mW
- Subroutine nesting ..... 128levels (Max.)
- Interrupt 14types, 14vectors
- 8-bit timer 4
- Programmable I/O ports
  - (Ports P0, P1, P2, P3, P4) 40
- Input ports (Ports P6, P7) 12
- Serial I/O (8-bit) 2
- A-D converter (8-bit resolution) 8channels
- D-A converter (8-bit resolution) 6channels
- Watchdog timer
- 72-character on screen display function
  - Number of character ..... 24 characters×3 lines
  - Kinds of character 126
- Two clock generating circuits
  - (One is for main clock, the other is for clock function)

APPLICATION

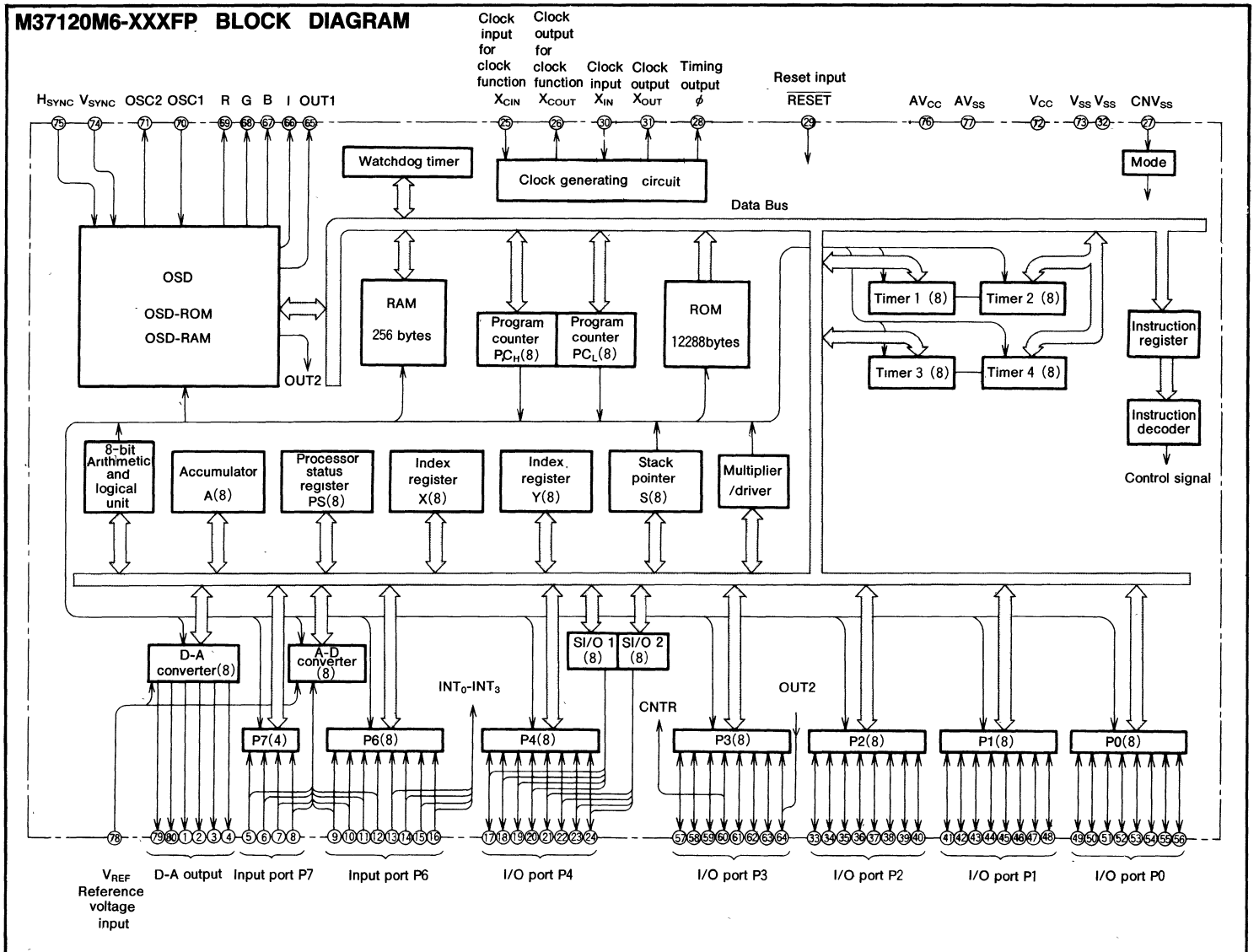
TV, VCR

PIN CONFIGURATION (TOP VIEW)



Outline 80P6N

M37120M6-XXXFP BLOCK DIAGRAM



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FUNCTIONS OF M37120M6-XXXFP

Parameter			Functions
Number of basic instructions			71
Instruction execution time			1μs (minimum instructions, at 4MHz frequency).
Clock frequency			4MHz
Memory size	ROM		12288bytes
	RAM		256bytes
Input/Output port	P0, P1, P2, P3	I/O	8-bit×4
	P4	I/O	8-bit×1
	P6	Input	8-bit×1
	P7	Input	4-bit×1
	I, B, G, R, OUT1	Output	1-bit×5 (for CRT display function)
	V_{SYNC}, H_{SYNC}	Input	1-bit×2 (for CRT display function)
	D-A_{OUT0}—D-A_{OUT5}	Output	1-bit×6
Serial I/O			8-bit×2
Timers			8-bit timer×4
Subroutine nesting			128 (maximum)
Interrupt			Four external interrupts, nine internal interrupts, one software interrupt
Clock generating circuit			Two built-in circuits (ceramic or quartz crystal oscillator)
Supply voltage			5V±10%
Operating temperature range			−10 to 70℃
Device structure			CMOS silicon gate
Package			80-pin plastic molded QFP
CRT display function	Number of character		24 characters×3lines
	Kinds of character		126 (12×16 dots)

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}
AV_{CC}, AV_{SS}	Analog power supply		Power supply input for A-D and D-A converters.
CNV_{SS}	CNV_{SS}		This is connect to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	The function of this pin can be selected either timing output or resetout output
X_{CIN}	Clock input for clock function	Input	This is the I/O pins of the clock generating circuit for the clock function To control generating frequency, an external ceramic or quartz crystal oscillator is connected between the X_{CIN} and X_{COUT} pins If an external clock is used, the clock source should be connected to the X_{CIN} pin and the X_{COUT} pin should be left open This clock can be used as a program controlled the system clock
X_{COUT}	Clock output for clock function	Output	
$D\text{-}A_{OUT0}$ —$D\text{-}A_{OUT5}$	D-A output	Output	Analog signal from D-A converter is output
V_{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D and D-A converters
$P0_0$—$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output At reset, this port is set to input mode The output structure is CMOS output
$P1_0$—$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0
$P2_0$—$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0
$P3_0$—$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0 Port $P3_0$ is in common with CRT input pin and $P3_4$ is in common with counter input pin
$P4_0$—$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same function as port P0, but the output structure is N-channel open drain.
$P6_0$—$P6_7$	Input port P6	Input	Port P6 is an 8-bit input port $P6_0$—$P6_3$ are in common with interrupt input pins and $P6_4$—$P6_7$ are in common with analog input pins
$P7_0$—$P7_3$	Input port P7	Input	Port P7 is a 4-bit input port and in common with analog input pins
OSC1, OSC2	Clock input for CRT display Clock output for CRT display	Input Output	This is the I/O pins of the clock generating circuit for the CRT display To control generating frequency, external condensers and registers are connected
H_{SYNC}	H_{SYNC} input	Input	This is the horizontal synchronizing signal input for CRT display.
V_{SYNC}	V_{SYNC} input	Input	This is the vertical synchronizing signal input for CRT display
I, B, G, R, OUT1	CRT output	Output	This is a 5-bit output pin for CRT display

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The M37120 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Programming Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions are provided.

The WIT instruction can be used.

The STP instruction can be used.

CPU Mode Register

The CPU mode register is allocated to address $00FB_{16}$. Bits 0 and 1 of this register are processor mode bits. This register also has a stack page selection bit.

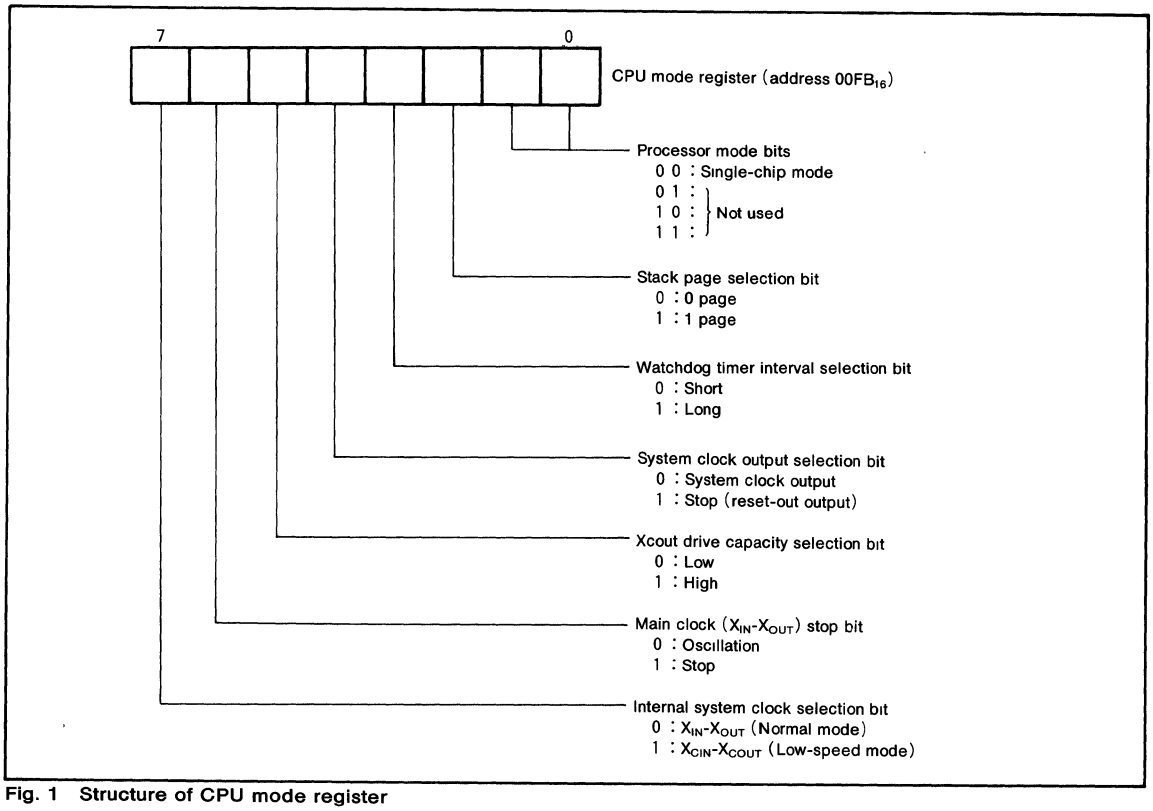


Fig. 1 Structure of CPU mode register

MEMORY

• Special Function Register (SFR) Area

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• RAM

RAM is used for data storage as well as a stack area.

• ROM

ROM is used for storing user programs as well as the interrupt vector area.

• RAM for display

RAM for display is used for specifing the character codes and colors to display.

• ROM for display

ROM for display is used for storing character data.

• Interrupt Vector Area

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• Zero Page

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

• Special Page

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

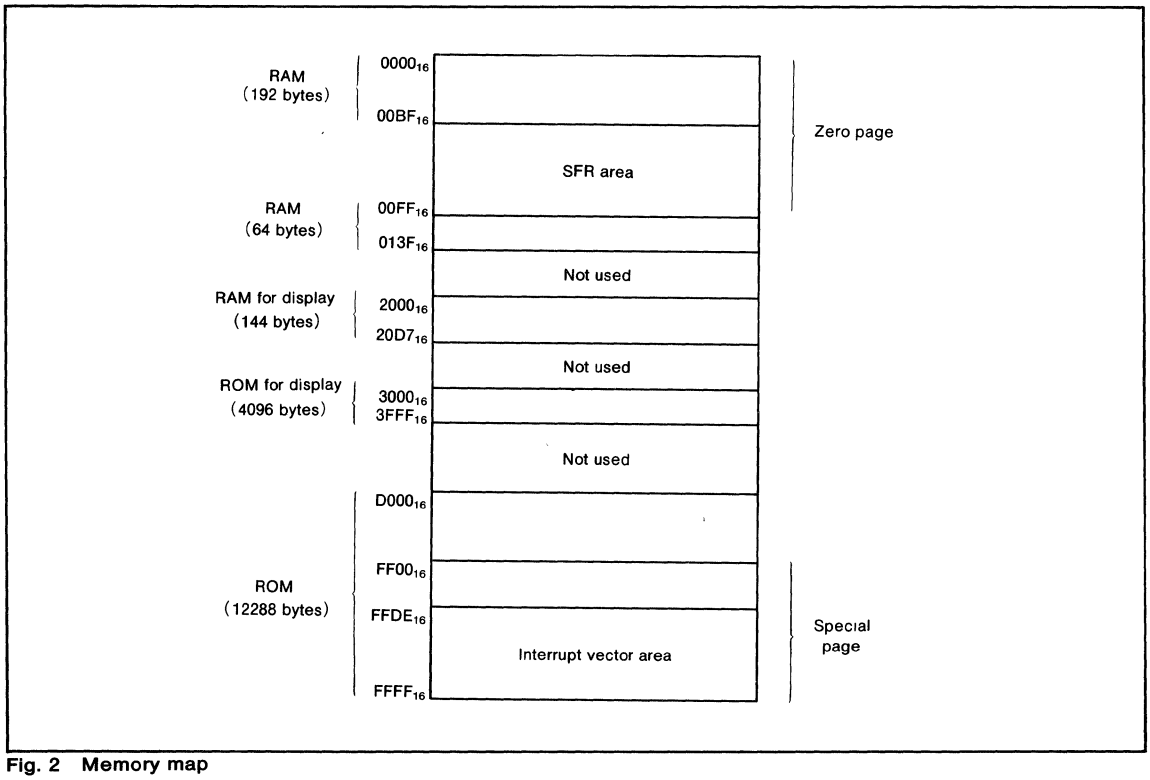


Fig. 2 Memory map

$00C0_{16}$	Port P0
$00C1_{16}$	Port P0 directional register
$00C2_{16}$	Port P1
$00C3_{16}$	Port P1 directional register
$00C4_{16}$	Port P2
$00C5_{16}$	Port P2 directional register
$00C6_{16}$	Port P3
$00C7_{16}$	Port P3 directional register
$00C8_{16}$	Port P4
$00C9_{16}$	Port P4 directional register
$00CA_{16}$	Port P6
$00CB_{16}$	Port P7
$00CC_{16}$	
$00CD_{16}$	
$00CE_{16}$	
$00CF_{16}$	
$00D0_{16}$	
$00D1_{16}$	
$00D2_{16}$	
$00D3_{16}$	A-D control register
$00D4_{16}$	INT edge selection register
$00D5_{16}$	A-D conversion result register
$00D6_{16}$	D-A conversion register 5
$00D7_{16}$	D-A conversion register 4
$00D8_{16}$	D-A conversion register 3
$00D9_{16}$	D-A conversion register 2
$00DA_{16}$	D-A conversion register 1
$00DB_{16}$	D-A conversion register 0
$00DC_{16}$	Serial I/O1 mode register
$00DD_{16}$	Serial I/O1 register
$00DE_{16}$	Serial I/O2 mode register
$00DF_{16}$	Serial I/O2 register

$00E0_{16}$	Horizontal position register
$00E1_{16}$	Vertical position register of block 1
$00E2_{16}$	Vertical position register of block 2
$00E3_{16}$	Vertical position register of block 3
$00E4_{16}$	Character size register
$00E5_{16}$	Border selection register
$00E6_{16}$	Color register 0
$00E7_{16}$	Color register 1
$00E8_{16}$	Color register 2
$00E9_{16}$	Color register 3
$00EA_{16}$	CRT control register
$00EB_{16}$	Display block counter
$00EC_{16}$	CRT port control register
$00ED_{16}$	
$00EE_{16}$	
$00EF_{16}$	Watchdog timer
$00F0_{16}$	Timer 1
$00F1_{16}$	Timer 2
$00F2_{16}$	Timer 3
$00F3_{16}$	Timer 4
$00F4_{16}$	
$00F5_{16}$	
$00F6_{16}$	
$00F7_{16}$	
$00F8_{16}$	Timer 12 mode register
$00F9_{16}$	Timer 34 mode register
$00FA_{16}$	
$00FB_{16}$	CPU mode register
$00FC_{16}$	Interrupt request register 1
$00FD_{16}$	Interrupt request register 2
$00FE_{16}$	Interrupt control register 1
$00FF_{16}$	Interrupt control register 2

Fig. 3 SFR (Special function register) memory map

INTERRUPTS

Interrupts can be caused by 14 different events consisting of four external, nine internal, and one software events.

Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed, interrupt disable flag I is set, and the program jumps to the address specified in the vector table. The interrupt request bit is cleared automatically. The reset and BRK instruction interrupt can never be disabled. Other interrupts are disabled when the interrupt disable flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figure 3 shows the structure of the interrupt request registers 1 and 2 and interrupt control registers 1 and 2.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt disable flag is "0". The interrupt request bit can be clear with a program, but not set. The interrupt enable bit can be set and clear with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 5 shows interrupts control.

Table 1. Interrupt vector address and priority.

Event	Priority	Vector addresses	Remarks
RESET	1	$FFFF_{16}$, $FFFE_{16}$	Non-maskable
V_{SYNC} interrupt	2	$FFFD_{16}$, $FFFC_{16}$	By V_{SYNC} signal of OSD
CRT interrupt	3	$FFFB_{16}$, $FFFA_{16}$	By display completion of character block
INT_0 interrupt	4	$FFF9_{16}$, $FFF8_{16}$	External interrupt (polarity programmable)
INT_1 interrupt	5	$FFF7_{16}$, $FFF6_{16}$	External interrupt (polarity programmable)
INT_2 interrupt	6	$FFF5_{16}$, $FFF4_{16}$	External interrupt (polarity programmable)
INT_3 interrupt	7	$FFF3_{16}$, $FFF2_{16}$	External interrupt (polarity programmable)
Timer 1 interrupt	8	$FFF1_{16}$, $FFF0_{16}$	
Timer 2 interrupt	9	$FFEF_{16}$, $FFEE_{16}$	
Timer 3 interrupt	10	$FFED_{16}$, $FFEC_{16}$	
Timer 4 interrupt	11	$FFEB_{16}$, $FFEA_{16}$	
Serial I/O 1 interrupt	12	$FFE9_{16}$, $FFE8_{16}$	
Serial I/O 2 interrupt	13	$FFE7_{16}$, $FFE6_{16}$	
A-D conversion completion interrupt	14	$FFE5_{16}$, $FFE4_{16}$	
Disable to use.		$FFE3_{16}$, $FFE2_{16}$	
Disable to use.		$FFE1_{16}$, $FFE0_{16}$	
BRK instruction interrupt	15	$FFDF_{16}$, $FFDE_{16}$	Non-maskable software interrupt

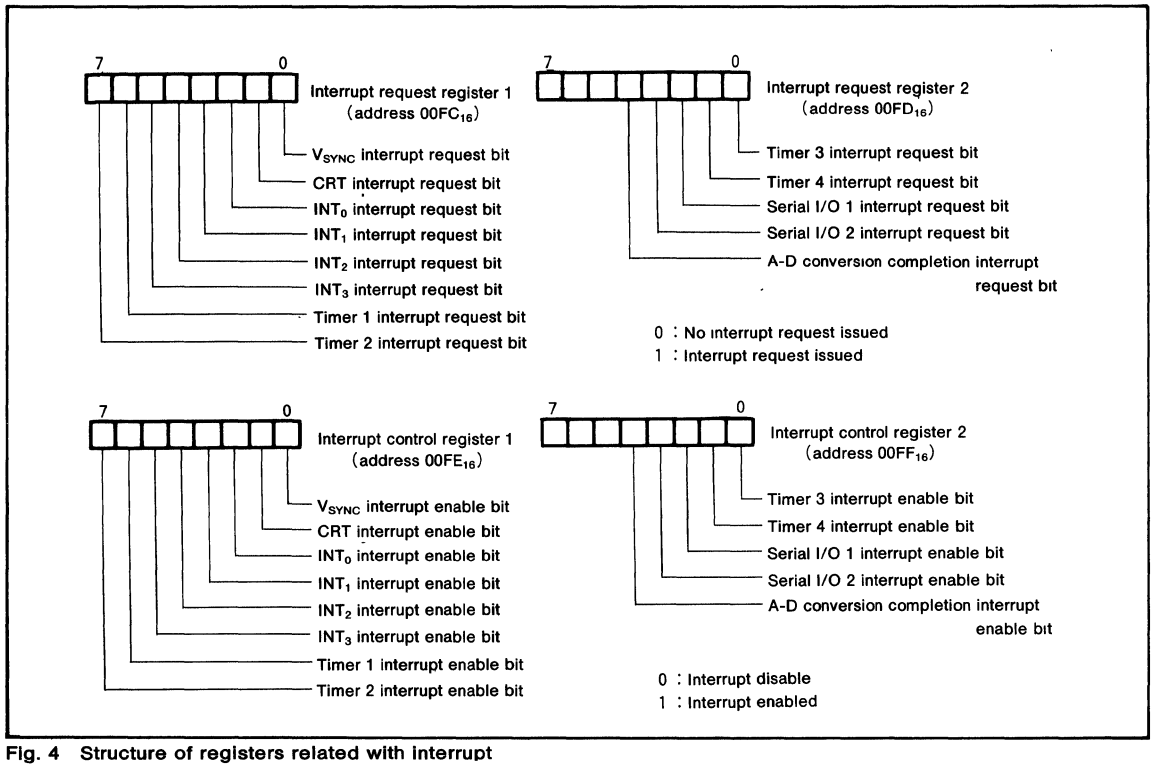


Fig. 4 Structure of registers related with interrupt

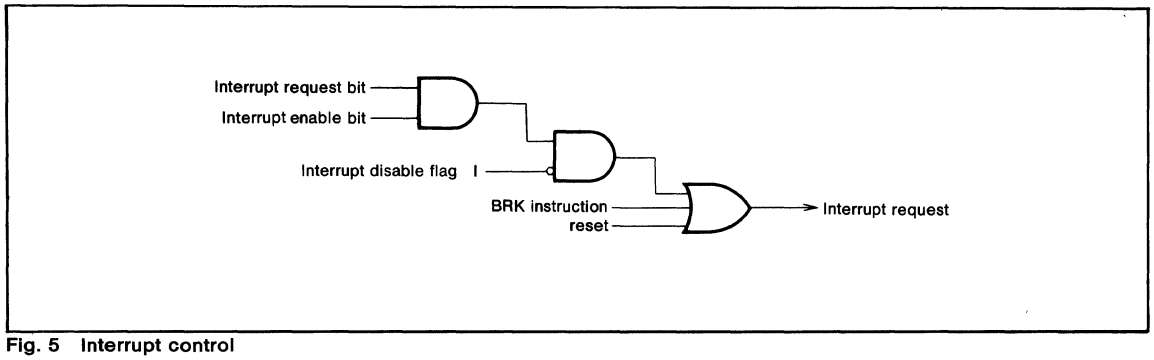


Fig. 5 Interrupt control

TIMER

The M37120M6-XXXFP has four timers; timer 1, timer 2, timer 3 and timer 4.

A block diagram of timer 1 through 4 is shown in Figure 6.

The count source for timer 1 through 4 can be selected by using bit 0, 1, 4 of the timer 12 mode register (address $00F8_{16}$) and bit 0, 1 of the timer 34 mode register (address $00F9_{16}$), as shown in Figure 7.

All of the timers are down count timers and have 8-bit latches. When a timer reaches "0" and the next count pulse is input to a timer, the contents of the reload latch are loaded into the timer. The division ratio of the timer is 1/(n +1), where n is the contents of timer latch.

Also all of the timers have interrupt generating functions. The timer interrupt request bit is set at the next count pulse after the timer reaches "0" (see interrupt section).

The starting and stopping of timers are controlled by bit 2, 3 of the timer 12 mode register and the timer 34 mode register. If the corresponding bit is "0", the timer starts counting, and the corresponding bit is "1", the timer stops.

At a reset or stop mode, FF_{16} is automatically set in timer 3 and 07_{16} in timer 4. And timer 4, timer 3 and the clock (ϕ divided by 8) are connected in series. Reset or stop mode is cleared by timer 4 overflow.

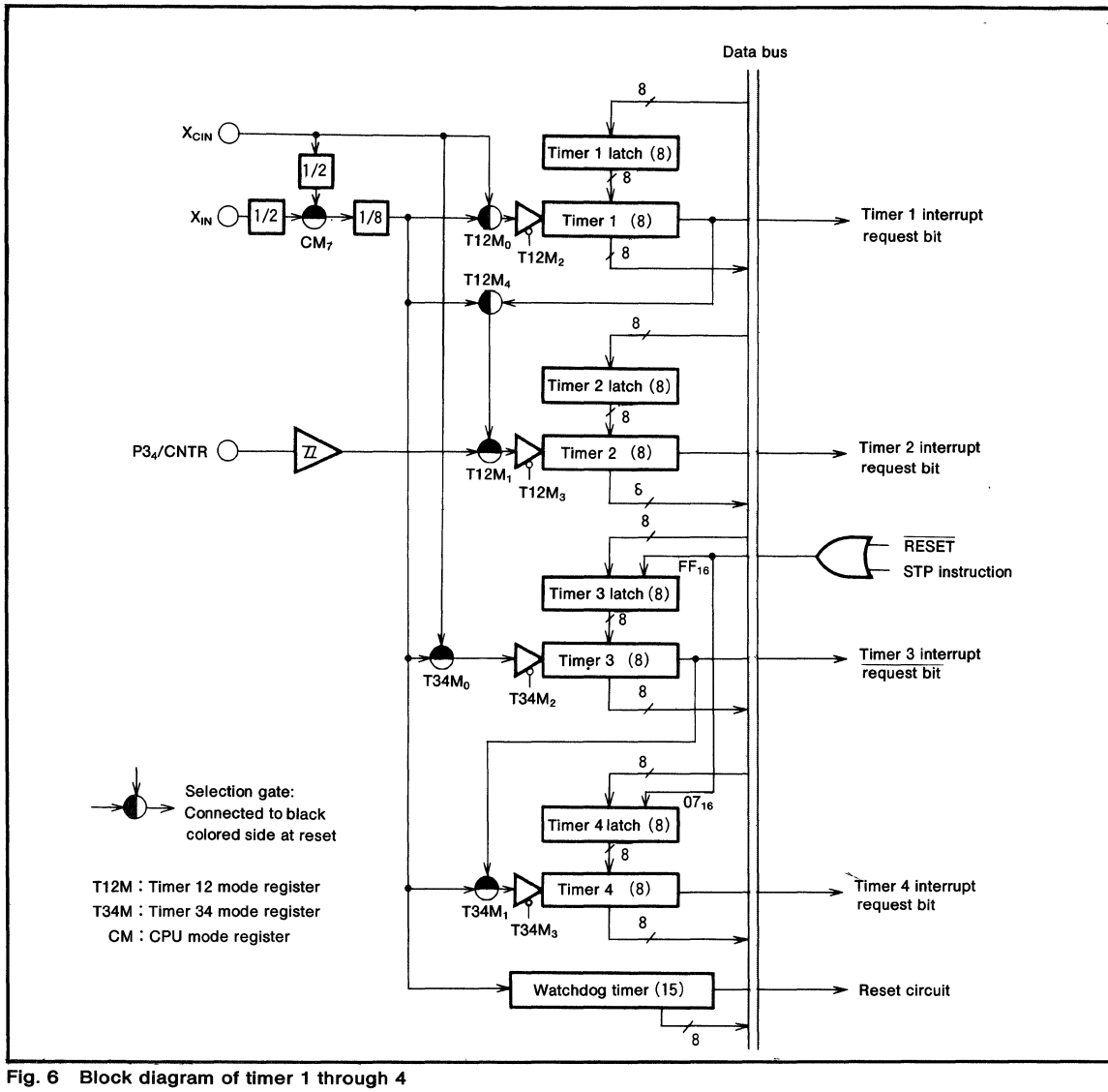


Fig. 6 Block diagram of timer 1 through 4

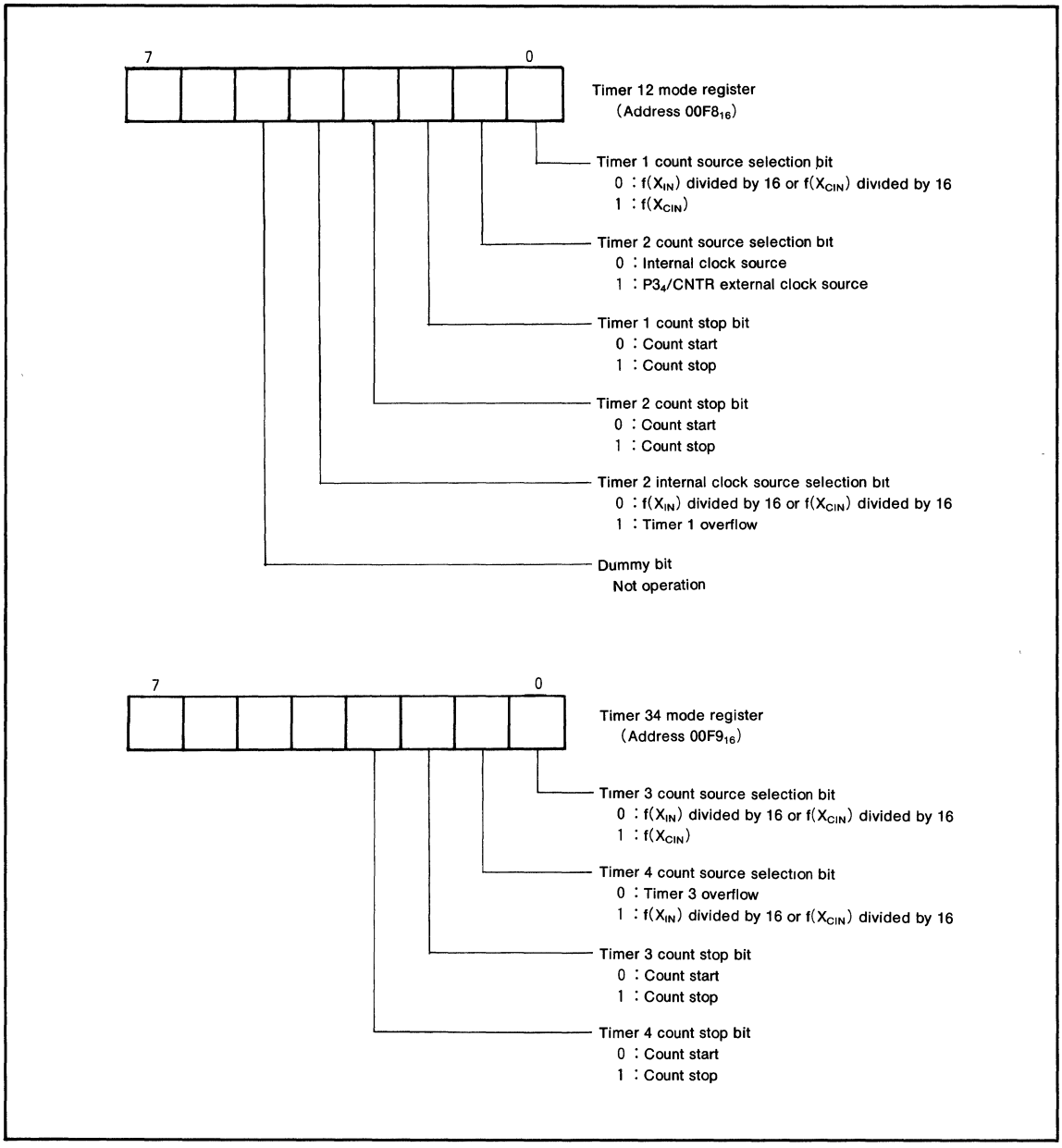


Fig. 7 Structure of timer mode registers

SERIAL I/O

M37120 has two serial I/Os which can operate in clock synchronous (Serial I/O 1, Serial I/O 2). Serial I/O 1 and 2 have the same funciton.

The block diagram of serial I/O is shown in Figure 8. In the serial I/O mode the receive ready signal ($\overline{S_{RDY}}$), synchronous input/output clock (S_{CLK}), and the serial I/O (S_{OUT}, S_{IN}), pins are used as port P4.

The serial I/O mode register 1 and 2 (addresses $00DC_{16}$ and $00DE_{16}$) are 8-bit registers. But the bits 7 and 6 are not used. Bit 0, 1, 2 of these registers are used to select a synchronous clock source. Bits 3 and 4 decide whether P4 will be used as a serial I/O or not. When bit 3 is "1", $P4_2$, $P4_6$ become I/O pins of the synchronous clock. When an internal syncronous clock is selected, the clock is output from $P4_2$, $P4_6$. If the external synchronous clock is selected, the clock is input to $P4_2$, $P4_6$. And $P4_1$, $P4_5$ will be a serial output, and $P4_0$, $P4_4$ will be a serial input. To use $P4_0$, $P4_4$ as serial input, set the directional register bit which correspond to $P4_0$, $P4_4$, to "0". For more information on the directional register, refer to the I/O pin section.

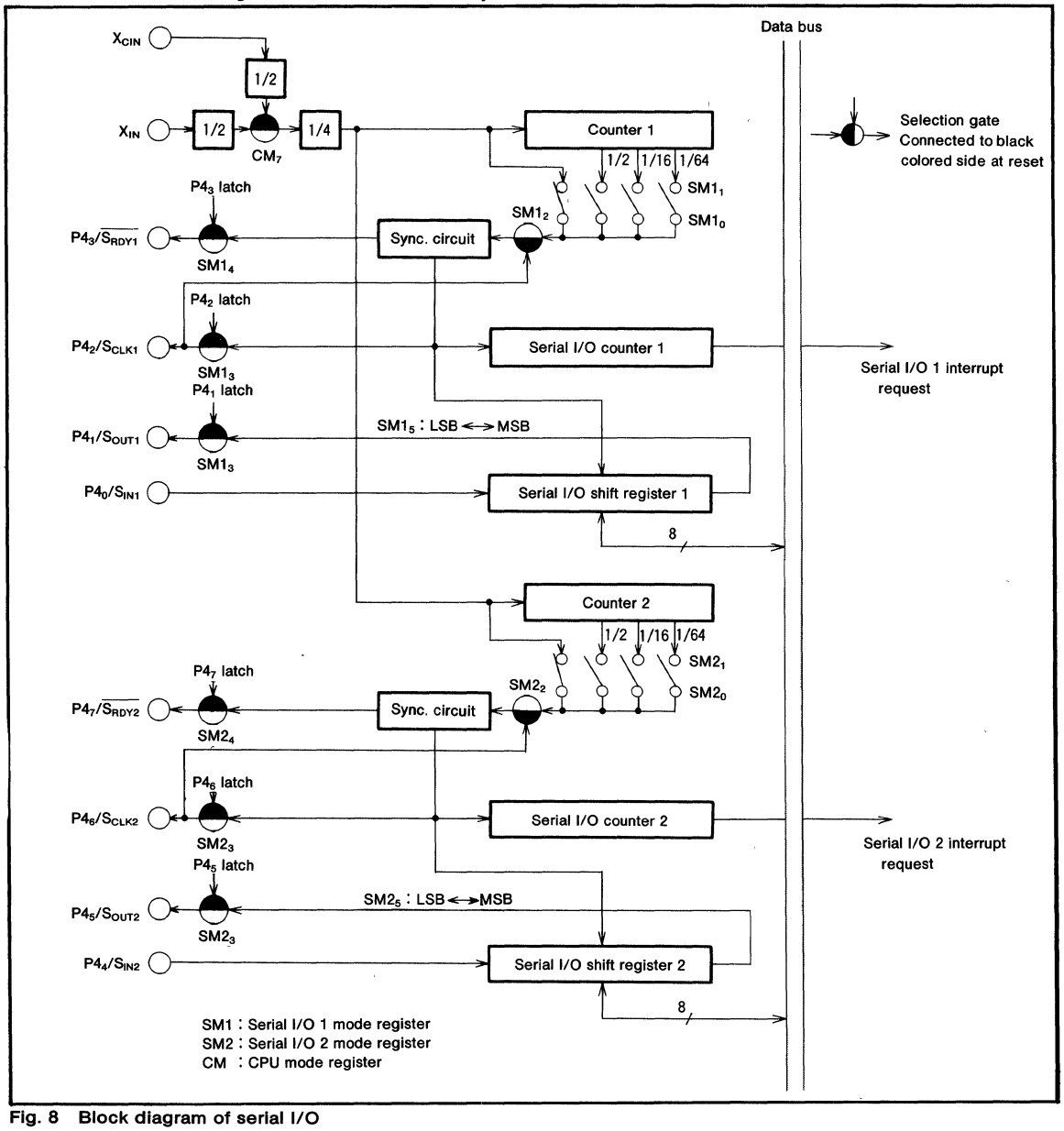


Fig. 8 Block diagram of serial I/O

To use the serial I/O, bit 3 of serial I/O mode register 1 and 2 needs to be set to "1", if it is "0" $P4_2$, $P4_6$ will function as a normal I/O. Bit 4 determines if $P4_3$, $P4_7$ are used as output pins for the receive data ready signal (bit 4 = "1", $\overline{S_{RDY}}$) or used as a normal I/O pin (bit 4 = "0"). Bit 5 is transfer direction selection bit. M37120 can be changed transfer direction by using this bit.

The function of serial I/O differs depending on the clock source; external clock or internal clock.

Internal clock- The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register. After the falling edge of write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M37120M6-XXXFP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to $P4_1$, $P4_5$. During the rising edge of this clock, data can be input from $P4_0$, $P4_4$ and the data in the serial I/O register will be shifted 1 bit. After the transfer clock has counted 8 times, the serial I/O counter will be "0" and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External Clock- If an external clock is used, the interrupt request bit will be set after the transfer clock has counted 8 times but the transfer clock will not stop. Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 500kHz at a duty cycle of 50%.

Timing diagrams are shown in Figure 9.

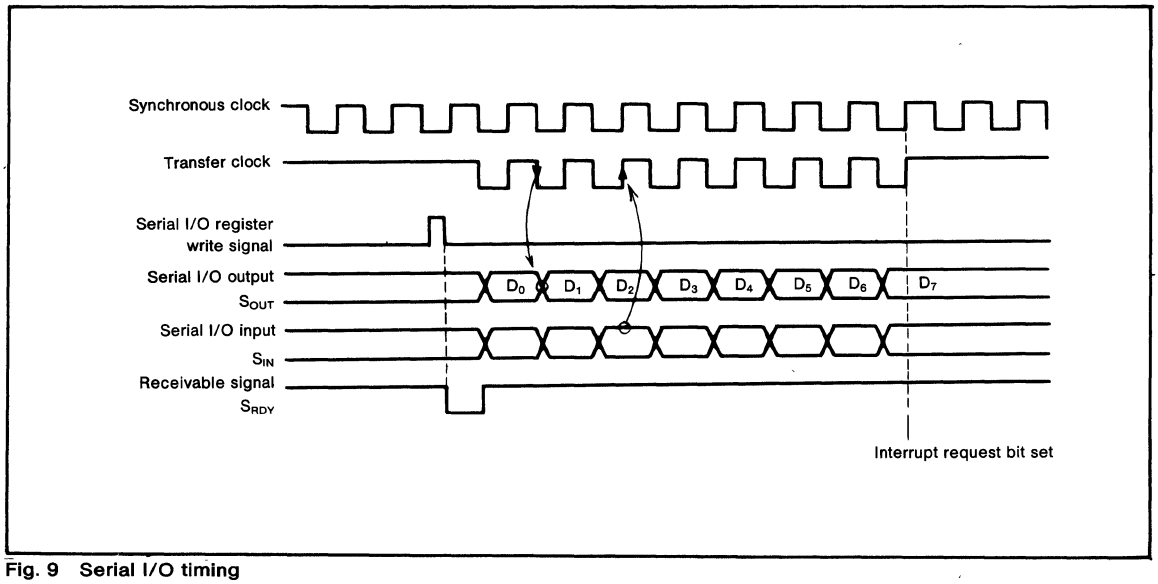


Fig. 9 Serial I/O timing

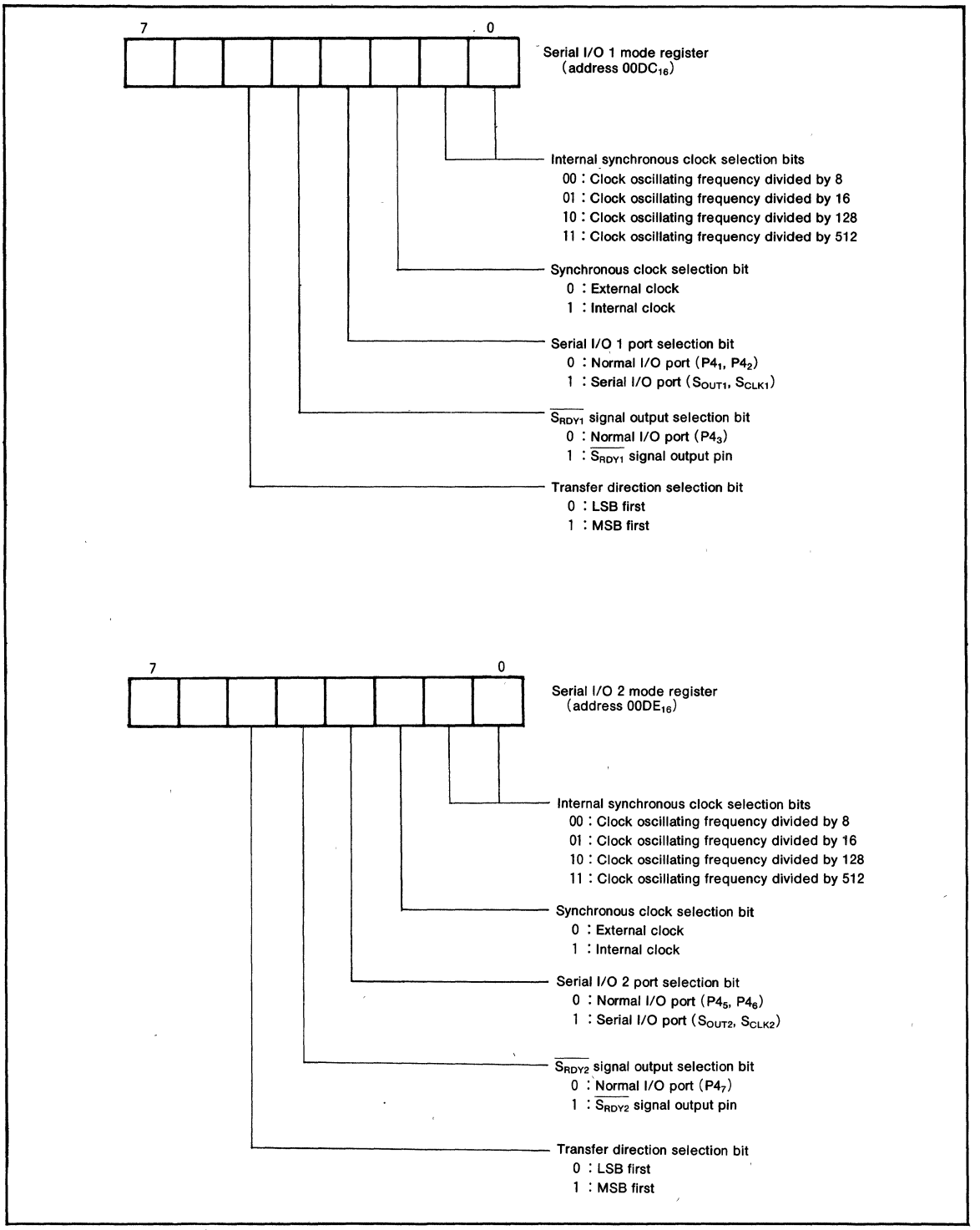


Fig. 10 Structure of serial I/O mode registers

A-D CONVERTER

The A-D converter circuit is shown in Figure 12. The analog input ports of the A-D converter (AN_0-AN_7) are in common with in port $P6_4$-$P6_7$, $P7_0$-$P7_3$.

The A-D control register is located at address $00D3_{16}$. One of the eight analog inputs is selected by bits 0, 1 and 2 of this register. The AN pins, not to use as analog input, uses as normal I/O ports.

Bit 0, 1 and 2, and corresponding to analog input pin is shown in Figure 11. A-D conversion is accomplished by first selecting bit 0, 1 and 2 of the A-D control register for the analog input pin.

A-D conversion starts by setting "0" to bit 3 of the A-D control register. When A-D conversion is finished, an interrupt is generated. After A-D interrupt is accepted, the result of A-D conversion can be read from the A-D register.

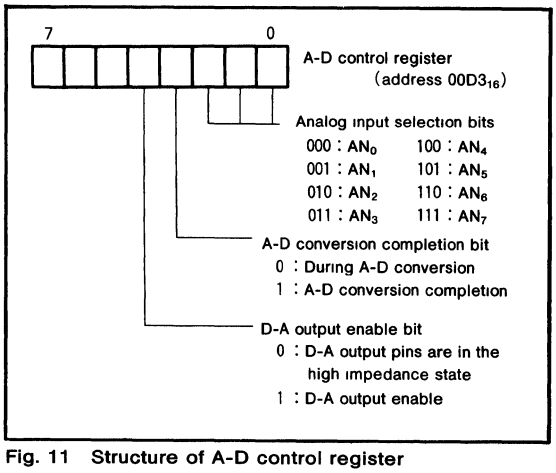


Fig. 11 Structure of A-D control register

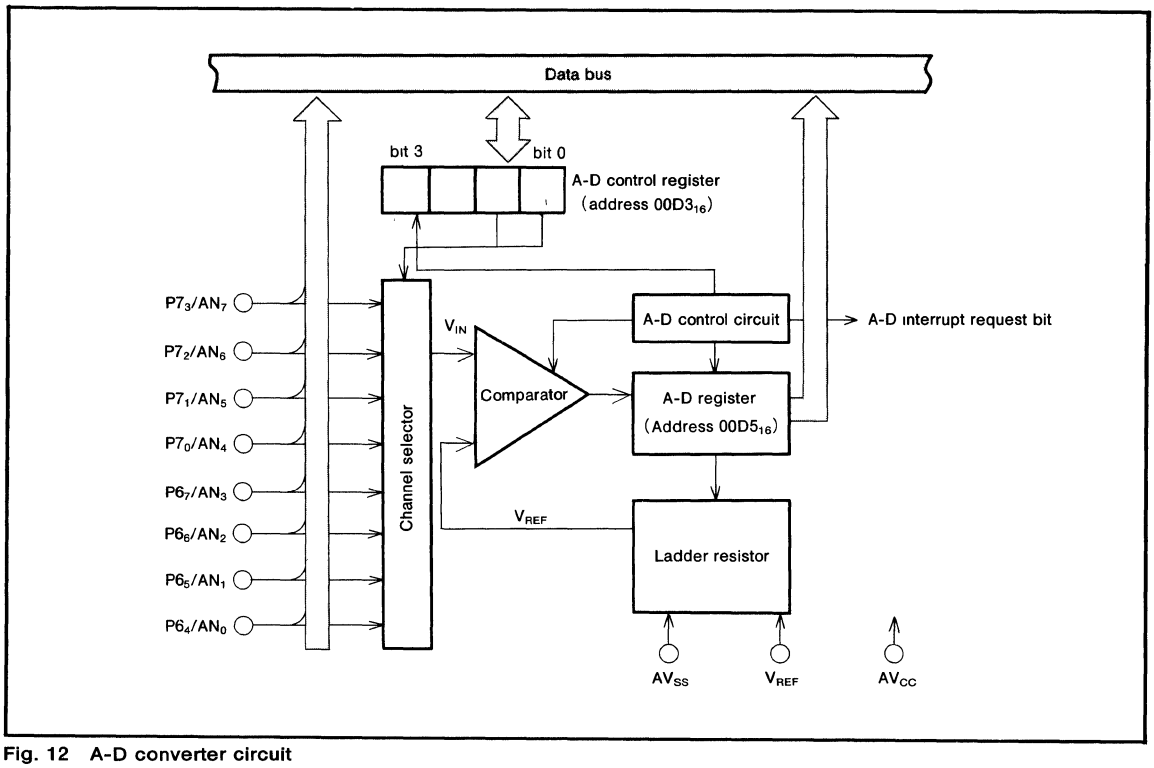


Fig. 12 A-D converter circuit

D-A CONVERTER

Six 8-bit resolution D-A converter channels are provided. Figure 13 shows a block diagram of the D-A converter.

D-A conversion is performed by setting a value in the D-A conversion register (addresses $00D6_{16}$ to $00DB_{16}$). The result of D-A conversion is output from the D-A output pin.

The output analog voltage V_{DA} is determined by the value n (decimal) set in the D-A conversion register as follows:

$V_{DA}=V_{REF} \times n/256$ (n=0 to 255)

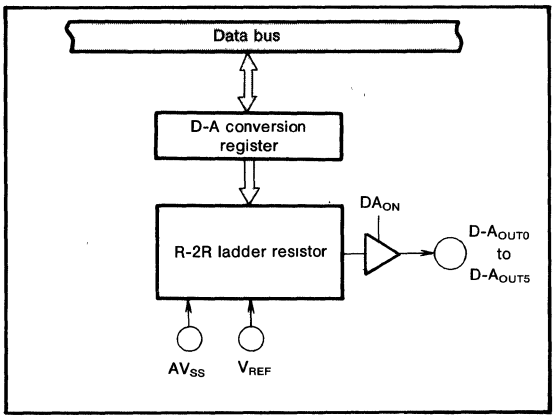


Fig. 13 D-A converter block diagram

CRT DISPLAY FUNCTIONS

(1) Outline of CRT Display Functions

Table 2 outlines the CRT display functions. The M37120M6-XXXFP incorporates a 24 columns × 3 lines CRT display control circuit. CRT display is controlled by the CRT display control register.

Up to 126 kinds of characters can be displayed, and colors can be specified for each character. Four colors can be displayed on one screen. A combination of up to 15 colors can be obtained by using each output signal (R, G, B, and I).

Characters are displayed in a 12×16 dot configuration to obtain smooth character patterns. (See Figure 14)

The following shows the procedure how to display characters on the CRT screen.

① Set the character to be displayed in display RAM.
② Set the display color by using the color register.
③ Specify the color register in which the display color is set by using the display RAM.
④ Specify the vertical position and character size by using the vertical position register and the character size register.
⑤ Specify the horizontal position by using the horizontal position register.
⑥ Write the display enable bit to the designated block display flag of the CRT control register. When this is done, the CRT starts operation according to the input of the V_{SYNC} signal.

The CRT display circuit has an extended display mode. This mode allows multiple lines (more than 3 lines) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Figure 15 shows a block diagram of the CRT display control circuit. Figure 16 shows the structure of the CRT control register.

Table 2. Outline of CRT display functions

Parameter		Functions
Number of display character		24characters× 3 lines
Character configuration		12×16 dots (See Figure 14)
Kinds of character		126
character size		4 size selectable
Color	Kinds of color	15(maximum)
	Coloring unit	Character
Display expansion		Possible (multiple lines)

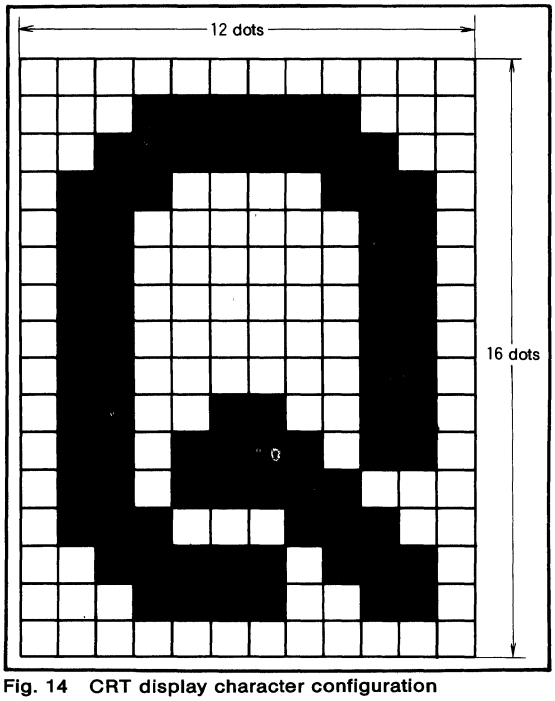


Fig. 14 CRT display character configuration

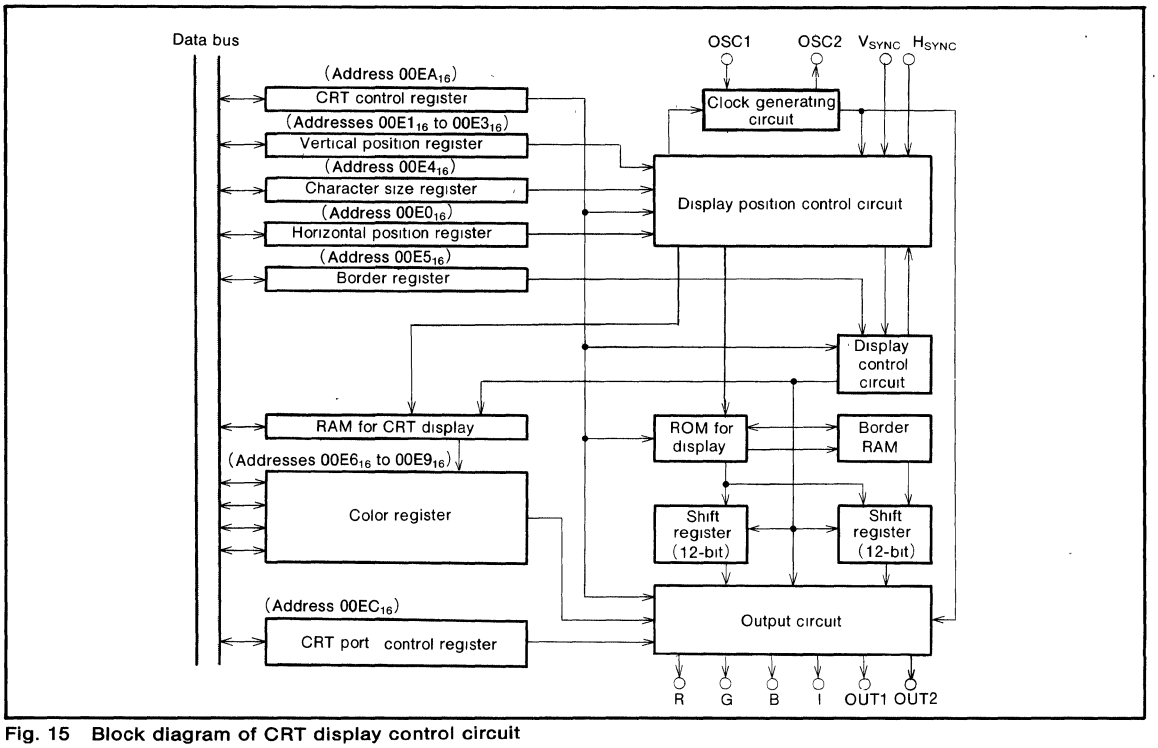
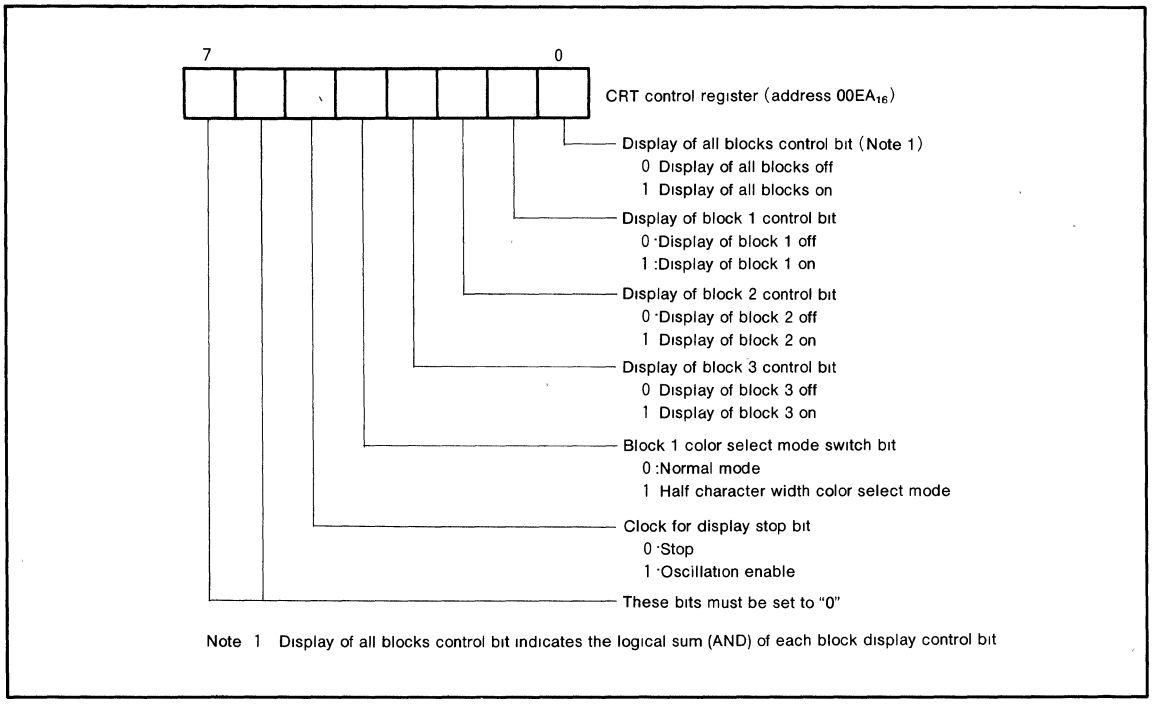


Fig. 15 Block diagram of CRT display control circuit



Note 1 Display of all blocks control bit indicates the logical sum (AND) of each block display control bit

Fig. 16 Structure of CRT control register

(2) Display Position

The display positions of characters are specified in units called a "block." There are three blocks, block 1 to block 3. Up to 24 characters can be displayed in one block. (See (4) Display Memory.)

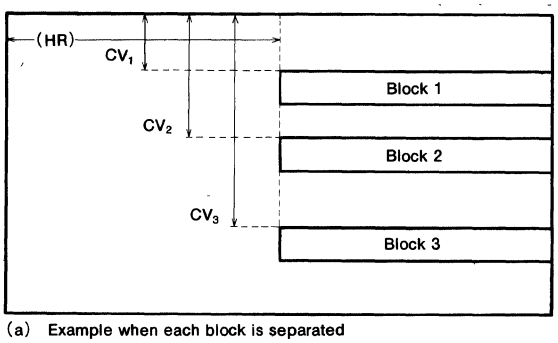
The display position of each block in both horizontal and vertical directions can be set by software.

The horizontal direction is common to all blocks, and is selected from 64-step display positions in units of 4Tc (Tc =oscillation cycle for display).

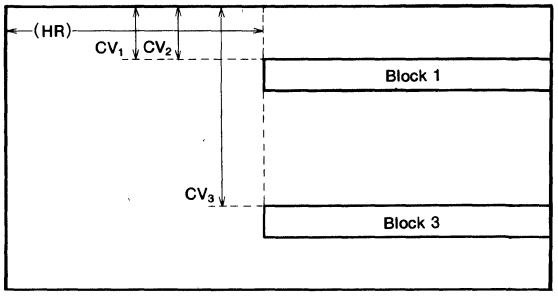
The display position in the vertical direction is selected from 128-step display positions for each block in units of four scanning lines.

If the display start position of a block overlaps with some other block ((b) in Figure 17), a block of the smaller block No. (1 to 3) is displayed.

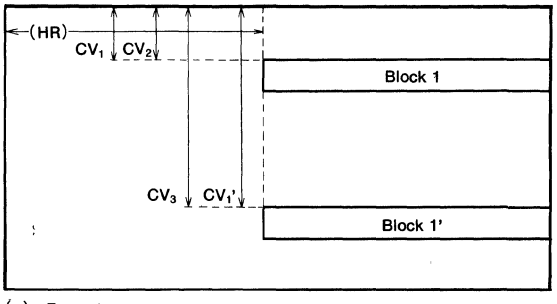
If when one block is displaying, some other block is displayed at the same display position ((c) in Figure 17), the former block is overridden and the latter is displayed.



(a) Example when each block is separated



(b) Example when the display start position of a block overlaps with some other block



(c) Example when one block is displaying some other block is superimposed

Fig. 17 Display position

The vertical position can be specified from 128-step positions (four scanning lines per step) for each block by setting values 00_{16} to $7F_{16}$ to bits 0 to 6 in the vertical position register (addresses $00E1_{16}$ to $00E3_{16}$). Figure 18 shows the structure of the vertical position register.

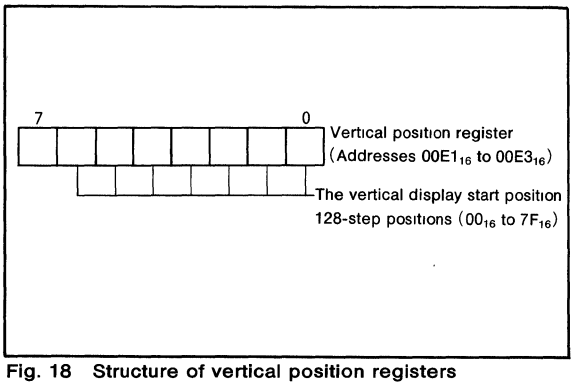


Fig. 18 Structure of vertical position registers

The horizontal direction is common to all blocks, and can be specified from 64-step display positions (4Tc per step (Tc=oscillation cycle for display)) by setting values 00_{16} to $3F_{16}$ to bits 0 to 5 in the horizontal position register (address $00E0_{16}$). Figure 19 shows the structure of the horizontal position register.

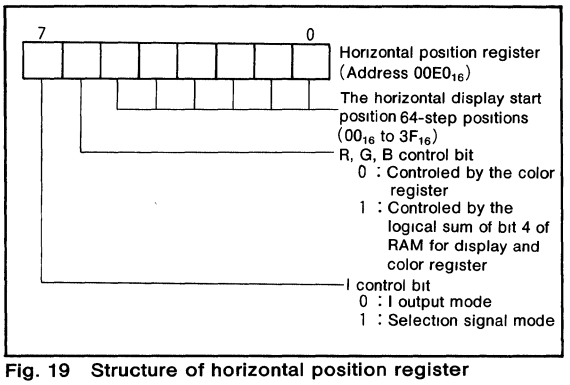


Fig. 19 Structure of horizontal position register

(3) Character Size

The size of characters to be displayed can be selected from four sizes for each block. Use the character size register (address $00E4_{16}$) to set a character size.

The character size in block 1 can be specified by using bits 0 and 1 in the character size register; the character size in block 2 can be specified by using bits 2 and 3; the character size in block 3 can be specified by using bits 4 and 5. Figure 20 shows the structure of the character size register.

The character size can be selected from four sizes: small size, medium size, large size, and extra large size. Each character size is determined by the number of scanning lines in the height (vertical) direction and the cycle of display oscillation (=Tc) in the width (horizontal) direction.

The small size consists of [one scanning line] × [1 Tc]; the medium size consists of [two scanning lines] × [2 Tc]; the large size consists of [three scanning lines] × [3 Tc]; the extra large size consists of [four scanning lines] × [4 Tc].

Table 3 shows the relationship between the set values in the character size register and the character sizes.

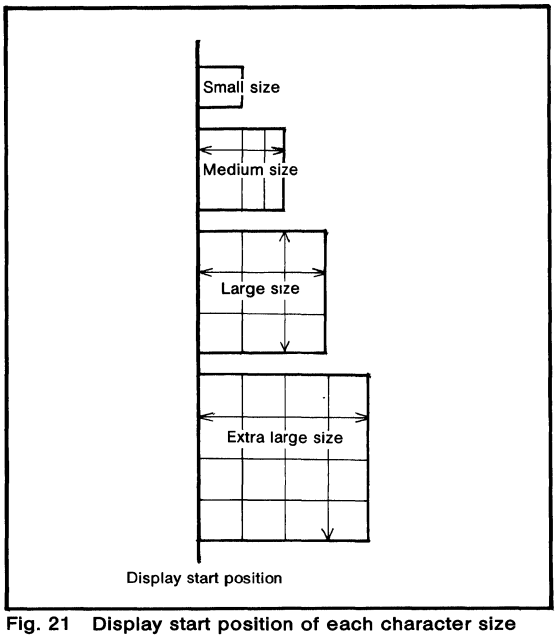


Fig. 21 Display start position of each character size (horizontal direction)

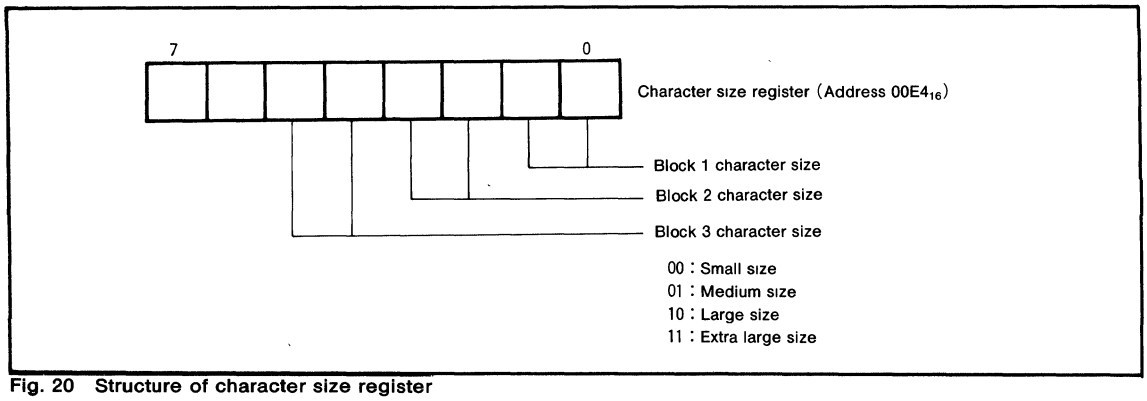


Fig. 20 Structure of character size register

Table 3. The relationship between the set values in the character size register and the character sizes

Set values in the character size register		Character	Width (horizontal)	Height (vertical)
CSn_1	CSn_0	size	direction	direction
0	0	Small	1 T_C	1
0	1	Medium	2 T_C	2
1	0	Large	3 T_C	3
1	1	Extra large	4 T_C	4

Note : The display start position in the horizontal direction is not affected by the character size In other words, the horizontal start position is common to all blocks even when the character size varies with each block (See Figure 21)

(4) Display Memory

There are two types of display memory : ROM for CRT display (addresses 3000_{16} to $3FFF_{16}$) used to store character dot data (masked) and RAM fof CRT display (addresses 2000_{16} to $20D7_{16}$) used to specify the colors of characters to be displayed. The following describes each type of display memory.

① ROM for CRT display (addresses 3000_{16} to $3FFF_{16}$)

The. CRT display ROM containns dot pattern data for characters to be displayed. For characters stored in this ROM to be actually displayed, it is necessary to specify them by writing the character code inherent to each character (code determined based on the addresses in the CRT display ROM) into the CRT display RAM.

The CRT display ROM has a capacity of 4K bytes. Because 32 bytes are required for one character data, the ROM can contain up to 128 kinds of characters. Actually, however, because two characters are required for test pattern use, the ROM can contain up to 126 kinds of characters for display use.

The CRT display ROM space is broadly divided into two areas. The [vertical 16 dots] × [horizontal (left side) 8 dots] data of display characters are stored in addresses 3000_{16} to $37FF_{16}$; the [vertical 16 dots] × [horizontal (right side) 4 dots] data of display characters are stored in addresses 3800_{16} to $3FFF_{16}$. (See Figure 22) Note however that the four upper bits in the data to be written to addresses 3800_{16} to $3FFF_{16}$ must be set to "1" (by writing data $F0_{16}$ to FF_{16}).

The character code used to specify a character to be displayed is determined based on the address in the CRT display ROM in which that character is stored.

Assume that data for one character is stored at $3XX0_{16}$ to $3XXF_{16}$ (XX denotes 00_{16} to $7F_{16}$) and $3YY0_{16}$ to $3YYF_{16}$ (YY denotes 80_{16} to FF_{16}), then the character code for it is "XX_{16}."

In other words, character code for any given character is configured with two middle digits of the four-digit (hex- notated) addresses (3000_{16} to $37FF_{16}$) where data for that character is stored.

Table 4 lists the character codes.

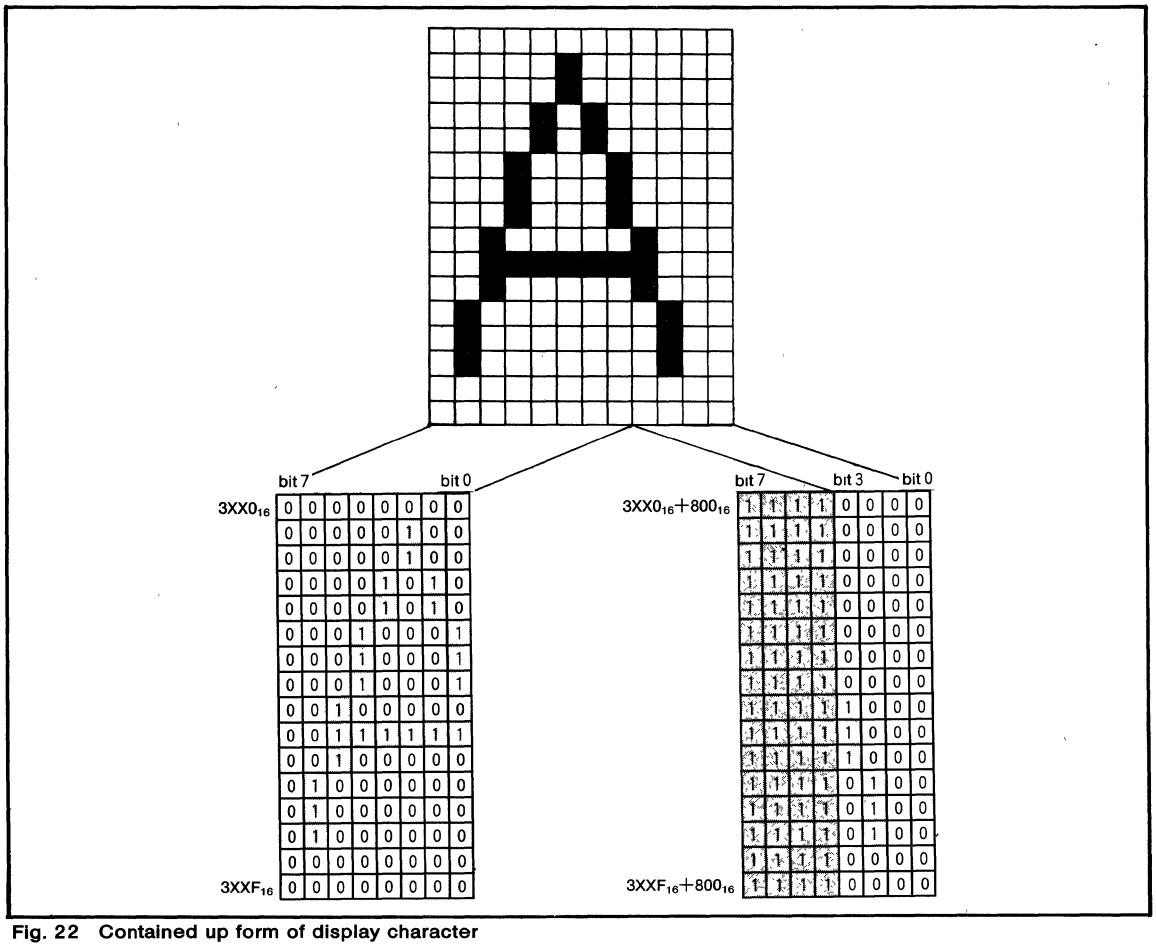


Fig. 22 Contained up form of display character

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Table 4. List of the character code

Character code	Contained up address of character data	
	Left 8 dots lines	Right 4 dots lines
00_{16}	3000_{16} to $300F_{16}$	3800_{16} to $380F_{16}$
01_{16}	3010_{16} to $301F_{16}$	3810_{16} to $381F_{16}$
02_{16}	3020_{16} to $302F_{16}$	3820_{16} to $382F_{16}$
03_{16}	3030_{16} to $303F_{16}$	3830_{16} to $383F_{16}$
:	:	:
10_{16}	3100_{16} to $310F_{16}$	3900_{16} to $390F_{16}$
11_{16}	3110_{16} to $311F_{16}$	3910_{16} to $391F_{16}$
:	:	:
$4F_{16}$	$34F0_{16}$ to $34FF_{16}$	$3CF0_{16}$ to $3CFF_{16}$
50_{16}	3500_{16} to $350F_{16}$	$3D00_{16}$ to $3D0F_{16}$
:	:	:
$7D_{16}$	$37D0_{16}$ to $37DF_{16}$	$3FD0_{16}$ to $3FDF_{16}$
$7E_{16}$ (Note)	$37E0_{16}$ to $37EF_{16}$	$3FE0_{16}$ to $3FEF_{16}$
$7F_{16}$ (Note)	$37F0_{16}$ to $37FF_{16}$	$3FF0_{16}$ to $3FFF_{16}$

Note : The test patterns are contained up in addresses $37E0_{16}$ to $37FF_{16}$ and $3FE0_{16}$ to $3FFF_{16}$

② RAM for CRT display (addresses 2000_{16} to $20D7_{16}$)
The CRT display RAM is allocated at addresses 2000_{16} to $20D7_{16}$, and is divided into a display character code specifying part and display color specifying part for each block. Table 5 shows the contents of the CRT display RAM.
When a character is to be display at the first character (leftmost) position in block 1, for example, it is necessary to write the character code to the seven low-order bits (bits 0 to 6) in address 2000_{16} and the color register No. to the two low-order bits (bits 0 and 1) in address 2080_{16}. The color register No. to be written here is one of the four registers in which the color to be displayed is set in advance. For details on color registers, refer to (5) Color Registers.
The structure of the CRT display RAM is shown in Figure 23. Write the character patterns at Table 6 and 7, when M37120M6-XXXFP is mask-ordered.

Table 5. The contents of RAM for CRT display

Block	Display position (from left)	Character code specification	Color specification
Block 1	1st column	2000_{16}	2080_{16}
	2nd column	2001_{16}	2081_{16}
	3rd column	2002_{16}	2082_{16}
	:	:	:
	22th column	2015_{16}	2095_{16}
	23th column	2016_{16}	2096_{16}
	24th column	2017_{16}	2097_{16}
Not used		2018_{16} : $201F_{16}$	2098_{16} : $209F_{16}$
Block 2	1st column	2020_{16}	$20A0_{16}$
	2nd column	2021_{16}	$20A1_{16}$
	3rd column	2022_{16}	$20A2_{16}$
	:	:	:
	22th column	2035_{16}	$20B5_{16}$
	23th column	2036_{16}	$20B6_{16}$
	24th column	2037_{16}	$20B7_{16}$
Not used		2038_{16} : $203F_{16}$	$20B8_{16}$: $20BF_{16}$
Block 3	1st column	2040_{16}	$20C0_{16}$
	2nd column	2041_{16}	$20C1_{16}$
	3rd column	2042_{16}	$20C2_{16}$
	:	:	:
	22th column	2055_{16}	$20D5_{16}$
	23th column	2056_{16}	$20D6_{16}$
	24th column	2057_{16}	$20D7_{16}$
Not used		2058_{16} : $207F_{16}$	

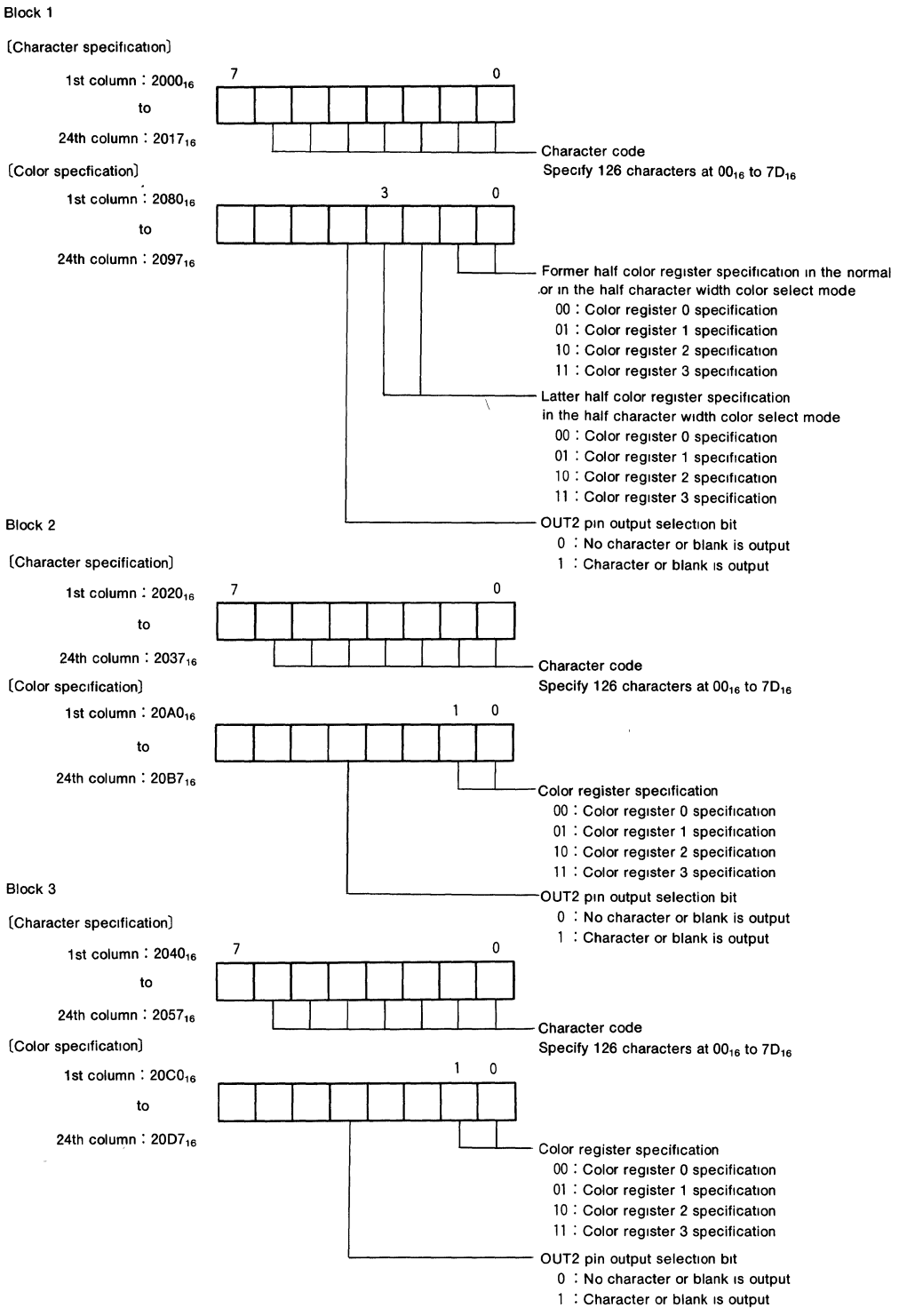


Fig. 23 Structure of RAM for CRT display

Table 6. Test character pattern 1

Address	Data	Address	Data
$37E0_{16}$	40_{16}	$3FE0_{16}$	$F0_{16}$
$37E1_{16}$	04_{16}	$3FE1_{16}$	$F0_{16}$
$37E2_{16}$	00_{16}	$3FE2_{16}$	$F4_{16}$
$37E3_{16}$	20_{16}	$3FE3_{16}$	$F0_{16}$
$37E4_{16}$	02_{16}	$3FE4_{16}$	$F0_{16}$
$37E5_{16}$	00_{16}	$3FE5_{16}$	$F2_{16}$
$37E6_{16}$	10_{16}	$3FE6_{16}$	$F0_{16}$
$37E7_{16}$	01_{16}	$3FE7_{16}$	$F0_{16}$
$37E8_{16}$	80_{16}	$3FE8_{16}$	$F0_{16}$
$37E9_{16}$	08_{16}	$3FE9_{16}$	$F0_{16}$
$37EA_{16}$	00_{16}	$3FEA_{16}$	$F8_{16}$
$37EB_{16}$	40_{16}	$3FEB_{16}$	$F0_{16}$
$37EC_{16}$	04_{16}	$3FEC_{16}$	$F0_{16}$
$37ED_{16}$	00_{16}	$3FED_{16}$	$F4_{16}$
$37EE_{16}$	20_{16}	$3FEE_{16}$	$F0_{16}$
$37EF_{16}$	02_{16}	$3FEF_{16}$	$F0_{16}$

Table 7. Test character pattern 2

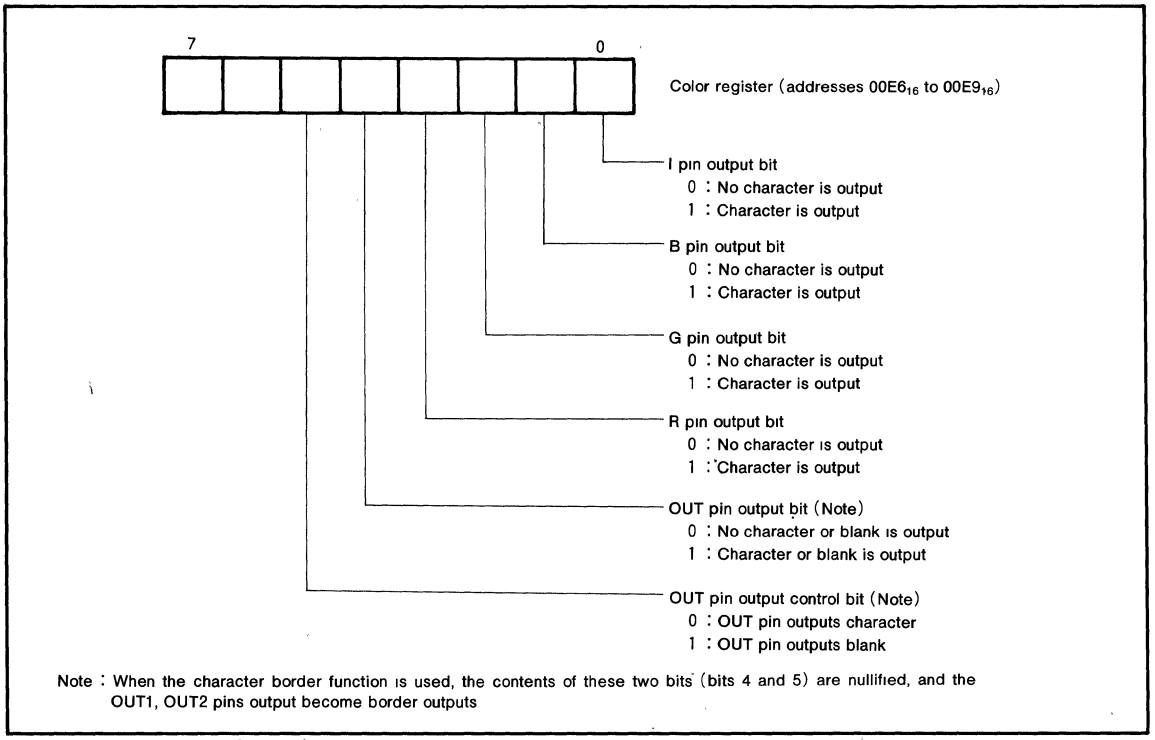
Address	Data	Address	Data
$37F0_{16}$	00_{16}	$3FF0_{16}$	$F0_{16}$
$37F1_{16}$	00_{16}	$3FF1_{16}$	$F0_{16}$
$37F2_{16}$	00_{16}	$3FF2_{16}$	$F0_{16}$
$37F3_{16}$	00_{16}	$3FF3_{16}$	$F0_{16}$
$37F4_{16}$	00_{16}	$3FF4_{16}$	$F0_{16}$
$37F5_{16}$	00_{16}	$3FF5_{16}$	$F0_{16}$
$37F6_{16}$	00_{16}	$3FF6_{16}$	$F0_{16}$
$37F7_{16}$	00_{16}	$3FF7_{16}$	$F0_{16}$
$37F8_{16}$	00_{16}	$3FF8_{16}$	$F0_{16}$
$37F9_{16}$	00_{16}	$3FF9_{16}$	$F0_{16}$
$37FA_{16}$	00_{16}	$3FFA_{16}$	$F0_{16}$
$37FB_{16}$	00_{16}	$3FFB_{16}$	$F0_{16}$
$37FC_{16}$	00_{16}	$3FFC_{16}$	$F0_{16}$
$37FD_{16}$	00_{16}	$3FFD_{16}$	$F0_{16}$
$37FE_{16}$	00_{16}	$3FFE_{16}$	$F0_{16}$
$37FF_{16}$	00_{16}	$3FFF_{16}$	$F0_{16}$

(5) Color Registers

The color of a displayed character can be specified by setting the color to one of the four color registers (CO0 to CO3: addresses $00E6_{16}$ to $00E9_{16}$) and then specifying that color register with the CRT display RAM.

There are four color outputs : R, G, B, and I. By using a combination of these outputs, it is possible to set 2^4-1 (when no output) = 15 colors. However, because only four color registers are available, up to four colors can be displayed at one time.

R, G, B, and I outputs are set by using bits 0 to 3 in the color register. Bit 4 in the color register is used to set a character or blank output; bit 5 is used to specify whether a character output or blank output. Figure 24 shows the structure of the color registers.



Note : When the character border function is used, the contents of these two bits (bits 4 and 5) are nullified, and the OUT1, OUT2 pins output become border outputs

Fig. 24 Structure of color registers

(6) Half Character Width Color Select Mode

By setting "1" to bit 4 in the CRT control register (address $00EA_{16}$) it is possible to specify colors in units of a half character size (vertical 16 dots×horizontal 6 dots) for characters in block 1 only.

In the half character width color select mode, colors of display characters in block 1 are specified as follows:

① The left half of the character is set to the color of the color register that is specified by bits 0 and 1 at the color register specifying addresses in the CRT display RAM (addresses 2080_{16} to 2097_{16}).

② The right half of the character is set to the color of the color register that is specified by bits 2 and 3 at the color register specifying address in the CRT display RAM (addresses 2080_{16} to 2097_{16}).

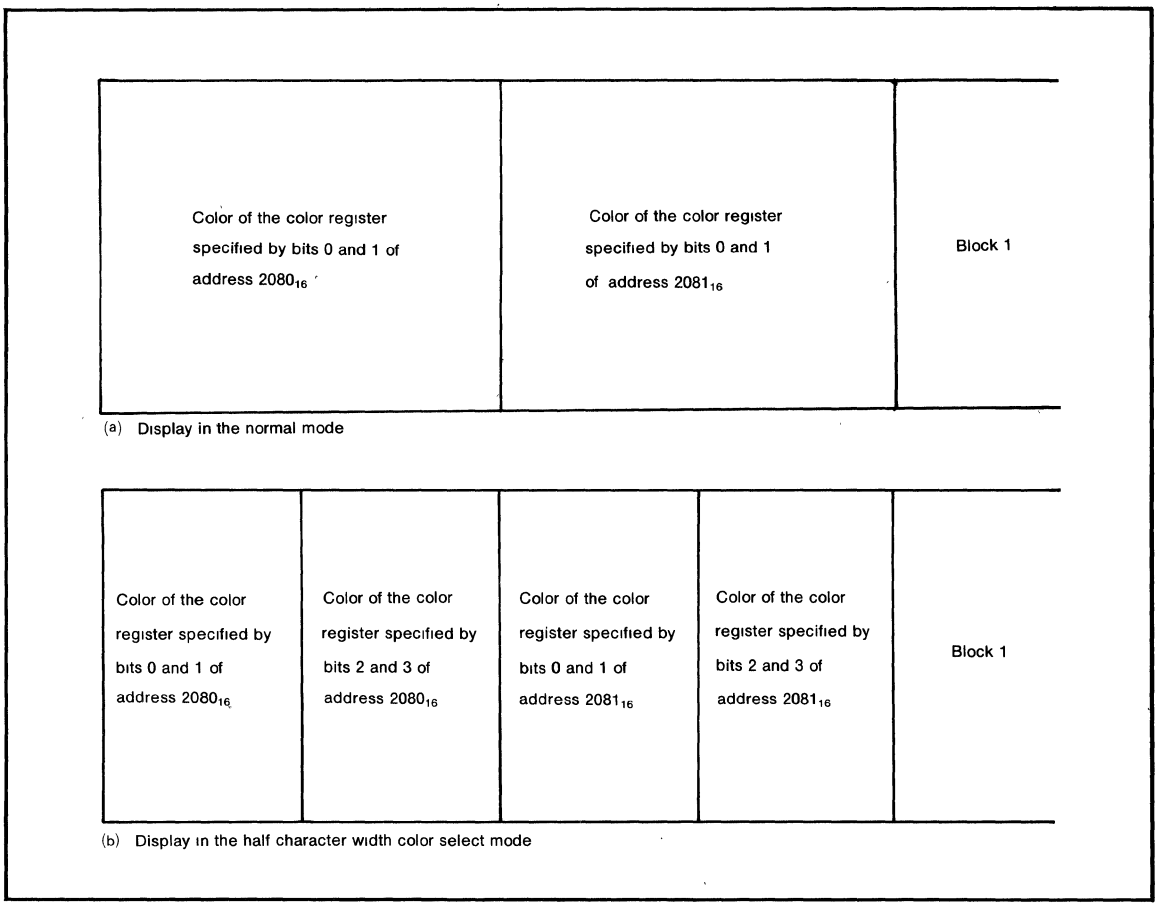


Fig. 25 Difference between normal color select mode and half character width color select mode.

(7) Multiline Display

The M37120M6-XXXFP can normally display three lines on the CRT screen by displaying three blocks at different horizontal positions.

In addition, it allows up to 16 lines to be displayed by using a CRT interrupt and display block counter.

The CRT interrupt works in such a way that when display of one block is terminated, an interrupt request is generated. In other words, character display for a certain block is initiated when the scanning line reaches the display position for that block (specified with vertical and horizontal position registers) and when the range of that block is exceeded, an interrupt is applied.

The display block counter is used to count the number of blocks that have just been displayed. Each time the display of one block is terminated, the contents of the counter are incremented by one.

For multiline display, it is necessary to enable the CRT interrupt (by clearing the interrupt disable flag to "0" and setting the CRT interrupt enable bit (= bit 4 at address $00FE_{16}$) to "1"), then execute the following processing in the CRT interrupt handling routine.

① Read the value of the display block counter.

② The block for which display is terminated (i.e., the cause of CRT interrupt generation) can be determined by the value read in ①.

③ Replace the display character data and display position of that block with the character data (contents of CRT display RAM) and display position (contents of vertical position and horizontal position registers) to be displayed next.

Figure 26 shows the structure of the display block counter.

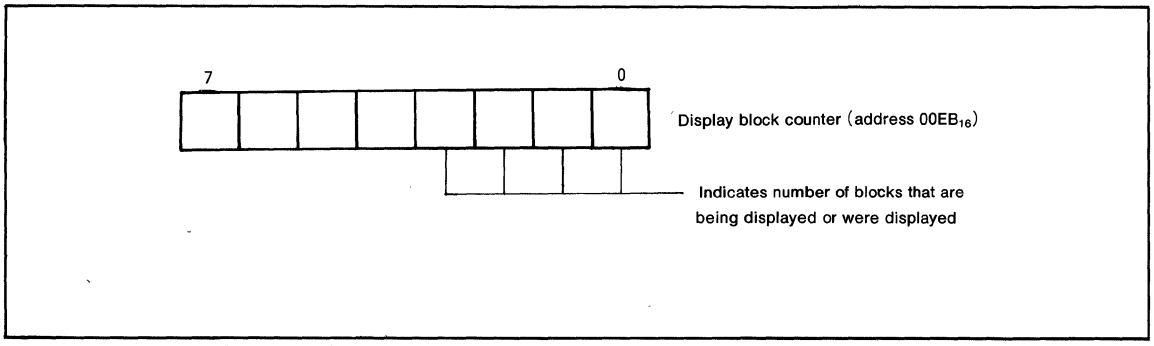


Fig. 26 Structure of display block counter

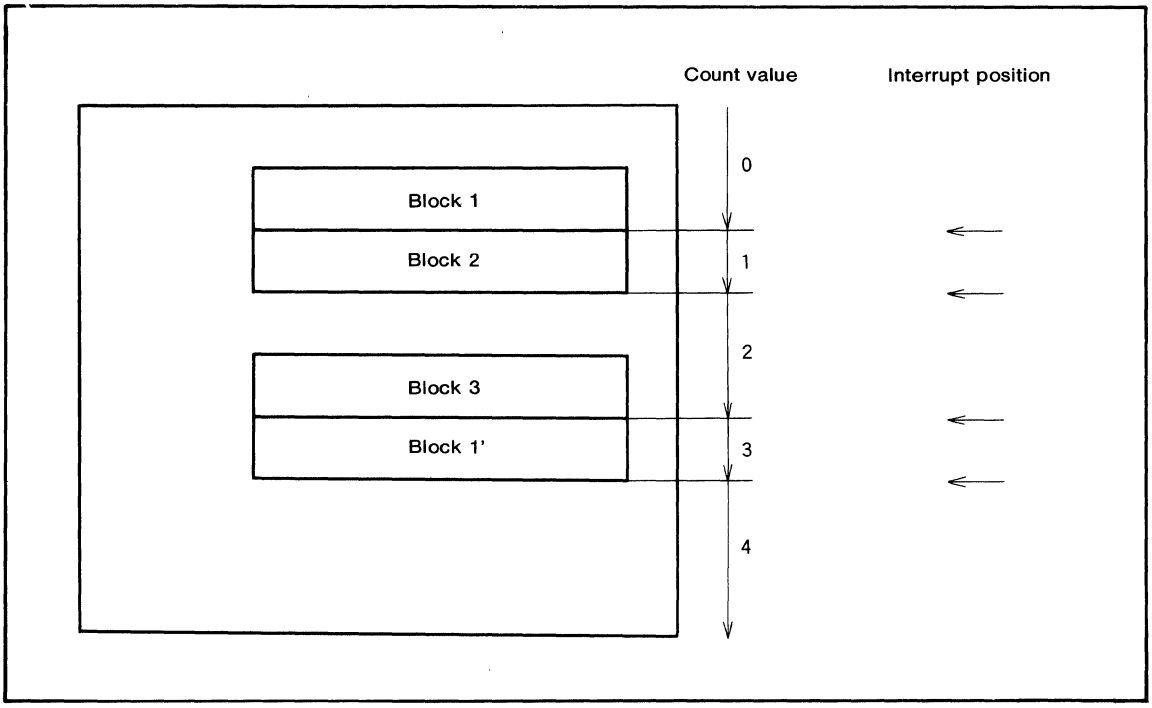


Fig. 27 Timing of CRT interrupt and count value of display block counter

(8) Character Border Function

A border of a one clock (one dot) equivalent size can be added to a character to be displayed in both horizontal and vertical directions.

The border is output from the OUT1, OUT2 pins. In this case, bits 4 and 5 in the color registers (contents output from the OUT pins) are nullified, and the border is output from the OUT pins instead.

Border can be specified in units of block by using the border selection register (address $00E5_{16}$). Table 8 shows the relationship between the values set in the border selection register and the character border function. Figure 29 shows the structure of the border selection register.

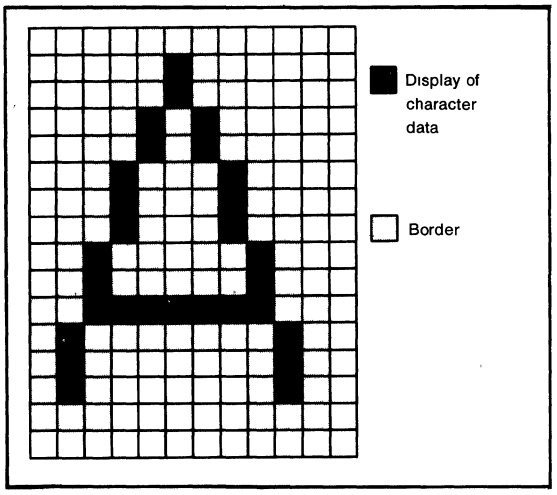


Fig. 28 Example of border

Table 8. The relationship between the values set in the border selection register and the character border function

Border selection register		Functions	Example of output
MDn1	MDn0		
X	0	Normal	R, G, B, I output OUT1, OUT2 output
0	1	Border including character	R, G, B, I output OUT1, OUT2 output
1	1	Border not including character	R, G, B, I output OUT1, OUT2 output

X : An X indicates either "0" or "1"

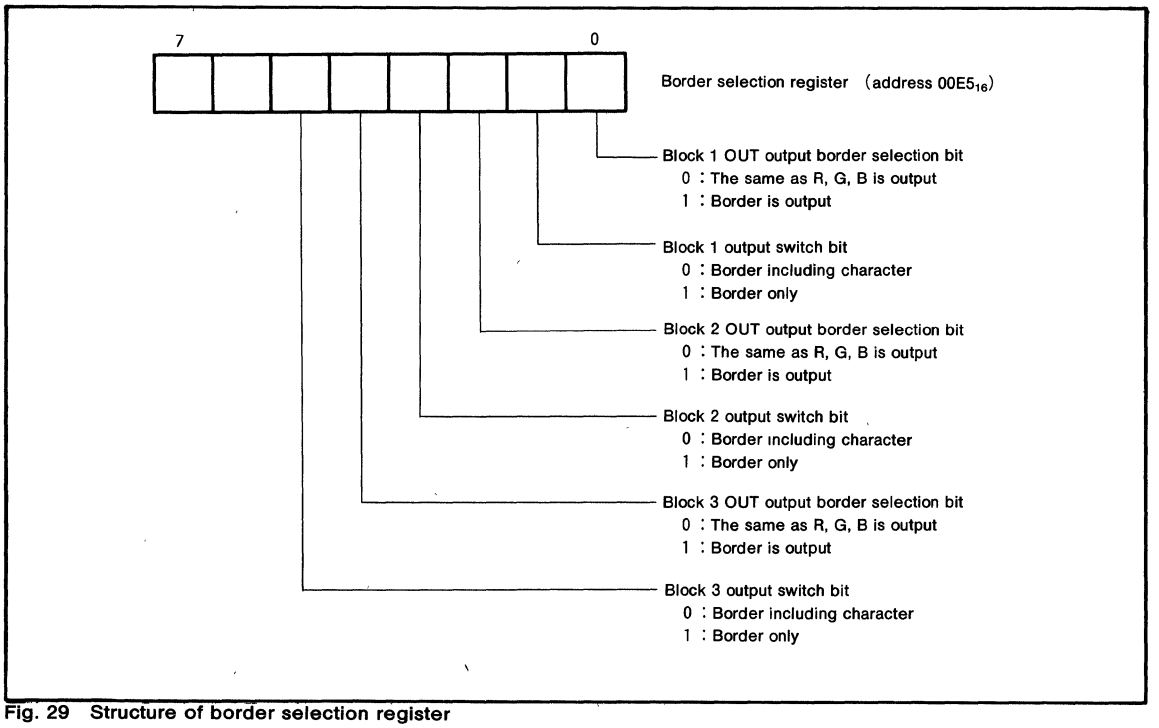


Fig. 29 Structure of border selection register

(9) CRT Output Pin Control

CRT output pins R, G, B, I, and OUT1 become output enable by setting bit 6 of CRT port control register. OUT2 is in common with port $P3_0$. This pin become output enable when bit 7 of CRT port control register is set after setting bit 0 of port P3 directional register.

The polarities of CRT outputs (R, G, B, I, and OUT1, as well as H_{SYNC} and V_{SYNC}) can be specified by using the CRT port control register (address $00EC_{16}$).

Use bits 0 to 4 in the CRT port control register to set the output polarities of H_{SYNC}, V_{SYNC}, R/G/B, I, and OUT1. When these bits are cleared to "0", a positive polarity is selected; when the bits are set to "1", a negative polarity is selected.

Figure 30 shows the structure of the CRT port control register.

(10) OUT2 Control

Because function selection (such as character or blank output control, border selection, etc.) of OUT1 is the same as that of OUT2, OUT2 outputs the same data of OUT1.

OUT2 can output characters in specified character area by specifying bit 4 of RAM for display. This function is no use when blank output is setting by color register.

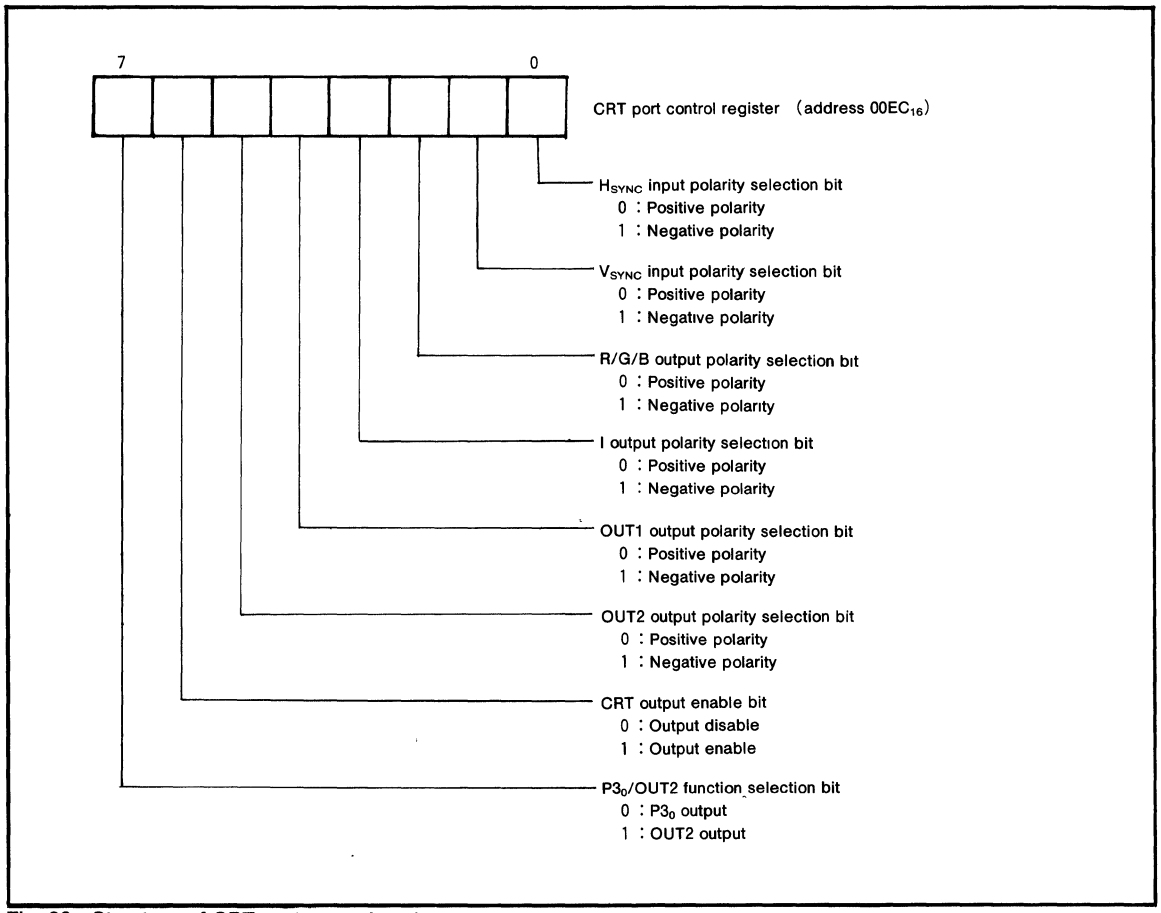


Fig. 30 Structure of CRT port control register

WATCHDOG TIMER

The watchdog timer provides a method of returning to reset status if a runaway or other cause prevents a program from running a loop normally.

The watchdog timer is a 15-bit counter consisting of a lower seven bits and an upper eight bits (address $00EF_{16}$). At reset or after the watchdog timer is written to, $7FFF_{16}$ is set in this timer and it starts to count.

When the MSB reaches "0", an internal reset is generated. Therefore programs should normally be written to ensure that the watchdog timer is written to before this bit reaches "0". If address $00EF_{16}$ is read, the value in the upper eight bits of the counter is read. Directly after a reset, the watchdog timer is stopped.

The count source of the lower seven bits is a signal that is the system clock ϕ divided by eight. The count source of the upper eight bits can be selected as either the overflow signal from the 7-bit counter or a signal that is the system clock ϕ divided by eight, depending on the value of bit 3 of the CPU mode register (address $00FB_{16}$).

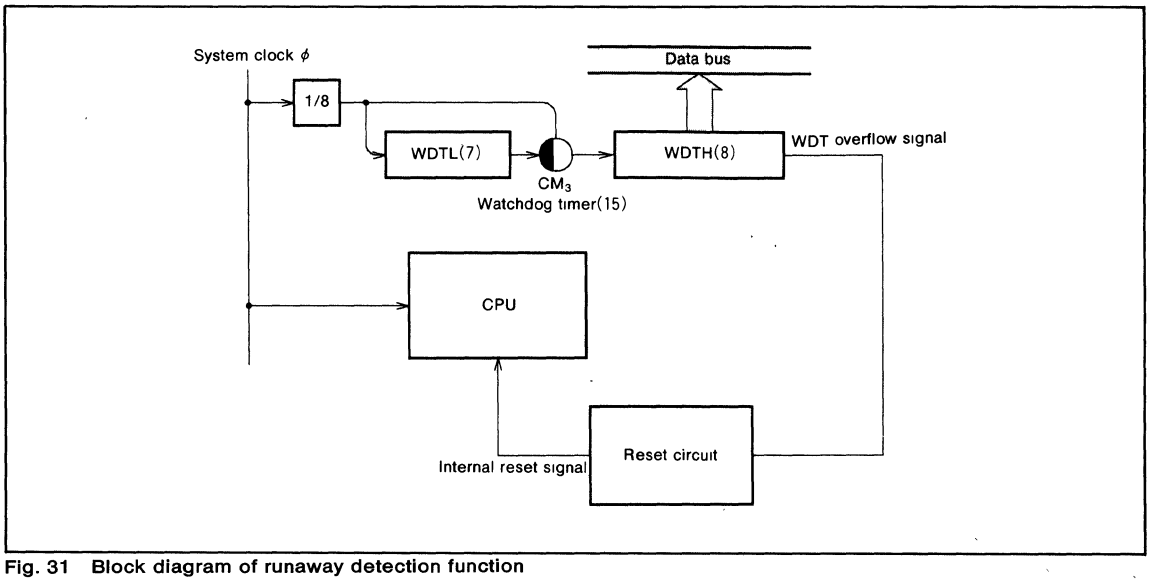


Fig. 31 Block diagram of runaway detection function

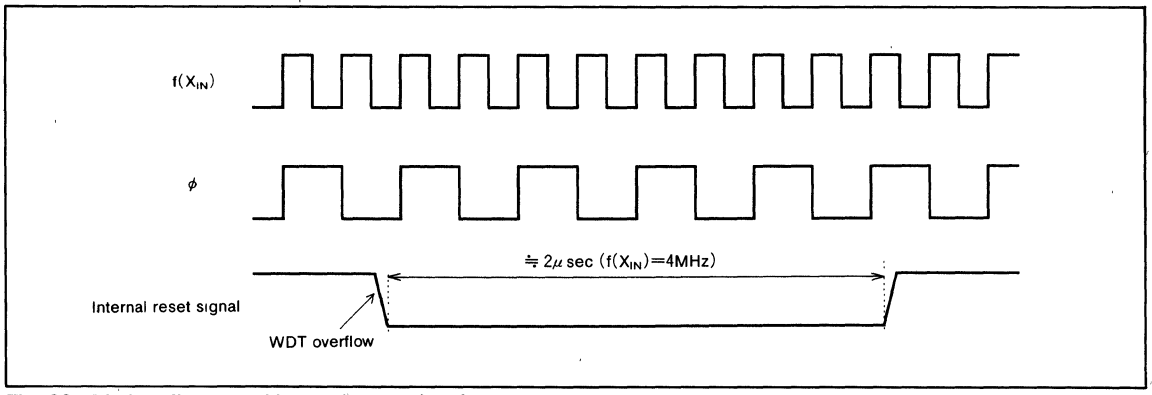


Fig. 32 Timing diagram of internal reset signal

RESET CIRCUIT

The M37120M6-XXXFP is reset according to the sequence shown in Figure 34. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for no less than 2μs while the power voltage is between 4 and 5.5V and the crystal oscillator oscillation is stable and then returned to "H" level.

The internal initializations following reset are shown in Figure 33.

Immediately after reset, the count of X_{IN} is stopped and X_{CIN} divided by 2 is selected as an internal clock. FF_{16} is set timer 3 and 07_{16} is set to timer 4 and timer 3 and timer 4 are connected. Also X_{CIN} divided by 16 is selected as the timer 3 count source. Reset is cleared by timer 4 overflow.

	Address	
(1) Port P0 directional register	(D0)(C1$_{16}$)	00$_{16}$
(2) Port P1 directional register	(D1)(C3$_{16}$)	00$_{16}$
(3) Port P2 directional register	(D2)(C5$_{16}$)	00$_{16}$
(4) Port P3 directional register	(D3)(C7$_{16}$)	00$_{16}$
(5) Port P4 directional register	(D4)(C9$_{16}$)	00$_{16}$
(6) A-D control register	(D3$_{16}$)	01000
(7) INT edge selection register	(D4$_{16}$)	0000
(8) D-A conversion register 5	(D6$_{16}$)	00$_{16}$
(9) D-A conversion register 4	(D7$_{16}$)	00$_{16}$
(10) D-A conversion register 3	(D8$_{16}$)	00$_{16}$
(11) D-A conversion register 2	(D9$_{16}$)	00$_{16}$
(12) D-A conversion register 1	(DA$_{16}$)	00$_{16}$
(13) D-A conversion register 0	(DB$_{16}$)	00$_{16}$
(14) Serial I/O 1 mode register	(SM1)(DC$_{16}$)	000000
(15) Serial I/O 2 mode register	(SM2)(DE$_{16}$)	000000
(16) CRT port control register	(EC$_{16}$)	00$_{16}$
(17) Display block counter	(EB$_{16}$)	0000
(18) CRT control register	(EA$_{16}$)	00$_{16}$
(19) Color register 3	(E9$_{16}$)	000000
(20) Color register 2	(E8$_{16}$)	000000
(21) Color register 1	(E7$_{16}$)	000000
(22) Color register 0	(E6$_{16}$)	000000
(23) Horizontal position register	(E0$_{16}$)	00$_{16}$
(24) Watchdog timer	(EF$_{16}$)	FF$_{16}$
(25) Timer 12 mode register	(T12M)(F8$_{16}$)	000000
(26) Timer 34 modu register	(T34M)(F9$_{16}$)	0000
(27) CPU mode register	(CM)(FB$_{16}$)	11111100
(28) Interrupt request register 1	(FC$_{16}$)	00$_{16}$
(29) Interrupt request register 2	(FD$_{16}$)	000000
(30) Interrupt control register 1	(FE$_{16}$)	00$_{16}$
(31) Interrupt control register 2	(FF$_{16}$)	000000
(32) Processor status register		1
(33) Program counter	(PC$_H$)	Contents of address FFFF$_{16}$
	(PC$_L$)	Contents of address FFFE$_{16}$

Note : Since the contents of both registers other than those listed above (including timers and the serial I/O register) and the RAM are undefined at reset, it is necessary to set initial values.

Fig. 33 Internal state of microcomputer at reset

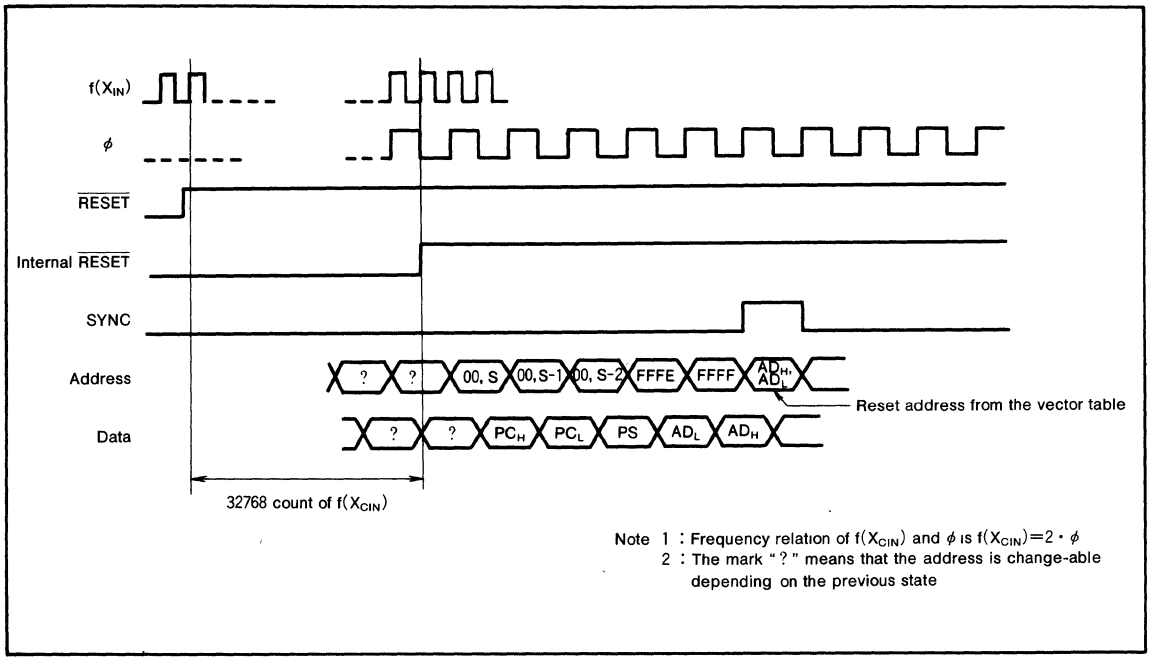


Fig. 34 Timing diagram at reset

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS outputs and pull-up transistor options available. As shown in Figure 3, P0 can be accessed as memory through zero page address $00C0_{16}$. Port P0's directional register allows each bit to be programmed individually as input or output. The directional register (zero page address $00C1_{16}$) can be programmed as input with "0", or as output with "1". When in the output mode, the data to be output is latched to the port register and output. When data is read from the output port, the otuput pin level is not read, only the latched data of the port register is read. Therefore, a previously output value can be read correctly even though the output voltage level has been shifted up or down. Port pins set as input are in the high impedance state so the signal level can be read. When data is written into the input port, the data is latched only to the output register and the pin still remains in the high impedance state.

(2) Port P1

Port P1 has the same function as P0.

(3) Port P2

Port P2 has the same function as P0.

(4) Port P3

Port P3 has the same functions P0 except that part of P3 is common with the CRT output pin and counter input pin.

(5) Port P4

Port P4 has the same function as P0. The output structure is N-channel open drain.

(6) Port P6

Port P6 has the same functions as P0. The lower 4-bit of this port are in common with interrupt input pins and the higher 4-bit of this port are in common with analog input pins.

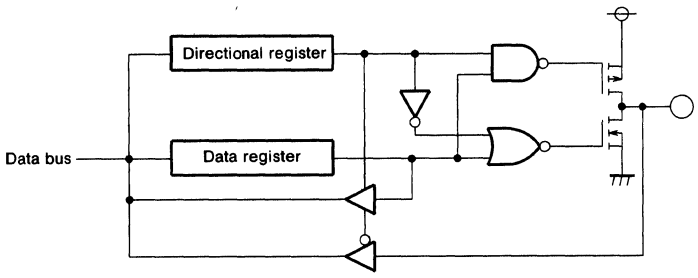
(7) Port P7

Port P7 is a 4-bit input port This port is in common with analog input pins.

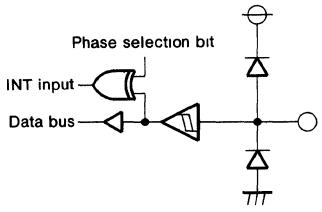
(8) I/O pins for CRT display function

H_{SYNC}, V_{SYNC} are input pins for deciding the display location. R, G, B, I, OUT1 and OUT2 are output the pattern of CRT display.

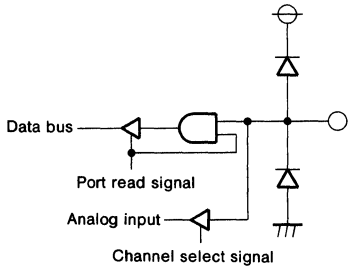
• Port P0, P1, P2, P3



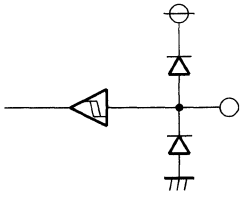
• Port $P6_0$, $P6_1$, $P6_2$, $P6_3$



• Port $P6_4$, $P6_5$, $P6_6$, $P6_7$, P7



• H_{SYNC}, V_{SYNC} input



• R, G, B, I, OUT1 output

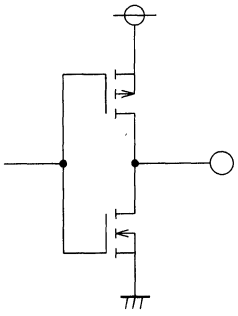
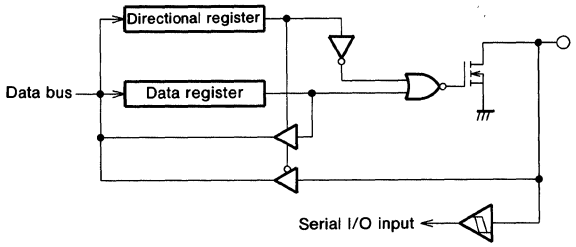
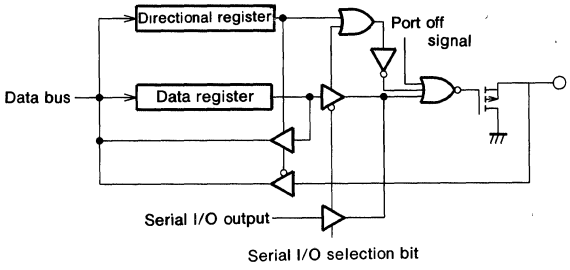


Fig. 35 Block diagram of Ports P0, P1, P2, P3, P6, P7, H_{SYNC}, V_{SYNC}, R, G, B, I, OUT1

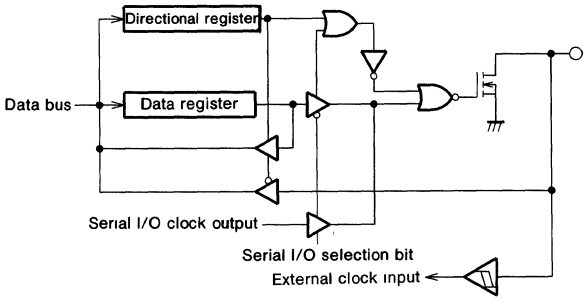
• Port $P4_0$, $P4_4$



• Port $P4_1$, $P4_5$



• Port $P4_2$, $P4_6$



• Port $P4_3$, $P4_7$

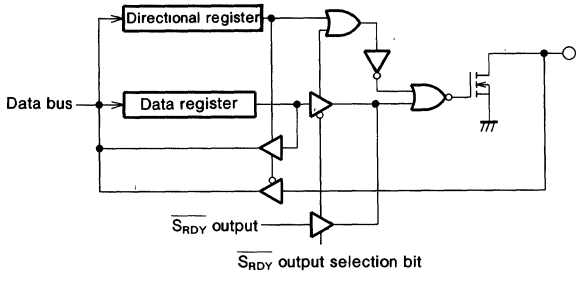


Fig. 36 Block diagram of Ports P4

CLOCK GENERATING CIRCUIT

The M37120M6-XXXFP has two internal clock generating circuits. Figure 40 shows a block diagram of the clock generating circuits. Normally, the frequency applied to the clock input pin X_{IN} divided by two is used as the internal clock (timing output) ϕ. Bit 7 of CPU mode register can be used to switch the internal clock ϕ to 1/2 the frequency applied to the clock input pin X_{CIN}.

Figure 37 shows a circuit example using a ceramic (or crystal) oscillator. Use the manufacturer's recommended values for constants such as capacitance which will differ depending on each oscillator. When using an external clock signal, input from the X_{IN} (X_{CIN}) pin and leave the X_{OUT} (X_{COUT}) pin open. A circuit example is shown in Figure 38.

An external clock signal cannot be supplied to the X_{CIN} pin open.

The M37120M6-XXXFP has two low power dissipation modes; stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case timer 3 and timer 4 are forcibly connected and $\phi/8$ is selected as timer 3 input. When restarting oscillation, FF_{16} is automatically set in timer 3 and 07_{16} in timer 4 in order to enable the oscillator to stabilize. Before executing the STP instruction, the timer 3 count stop bit and timer 4 count stop bit must be set to supply ("0"), timer 3 interrupt enable bit and timer 4 interrupt enable bit must be set to disable ("0").

Oscillation is restarted (release the stop mode) when INT, or serial I/O interrupt is received. The interrupt enable bit of the interrupt used to release the stop mode must be set to "1". When restarting oscillation with an interrupt or reset, the internal clock ϕ is held "H" until timer 4 overflows and is not supplied to the CPU.

The microcomputer enters an wait mode when the WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode release) when the microcomputer is reset or when it receives an interrupt.

Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode must be set to "1" before executing the WIT instruction.

Low power dissipation operation is also achieved when the X_{IN} clock is stopped and the internal clock ϕ is generated from the X_{CIN} clock ($36\mu A$ or less at $f(X_{CIN})=32kHz$, $V_{CC}=3V$). X_{IN} clock oscillation is stopped when the bit 6 of CPU mode register (address $00FB_{16}$) is set and restarted when it is cleared. However, the wait time until the oscillation stabilizes must be generated with a program when restarting. Figure 41 shows the transition of states for the system clock.

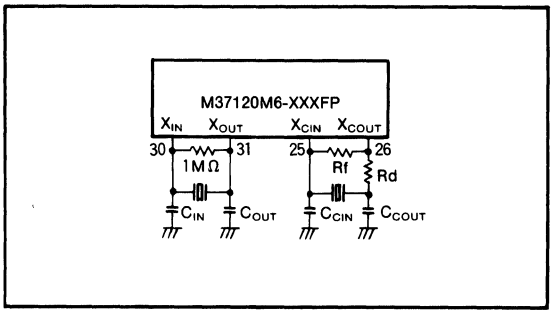


Fig. 37 Example ceramic resonator circuit

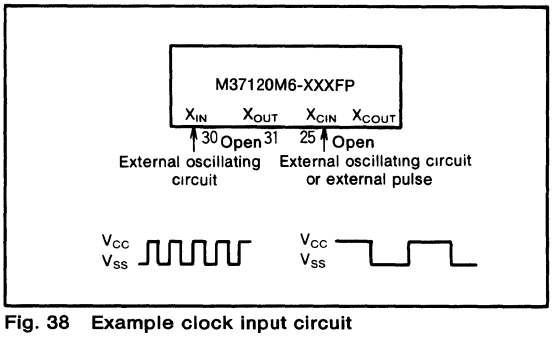


Fig. 38 Example clock input circuit

TIMER OSCILLATION CIRCUIT

Power is supplied to the timer clock oscillation circuit via a step-down regulator circuit to reduce the power consumption when the M37120M6-XXXFP is operating in timer mode. Since this step-down regulator circuit reduces the voltage applied to the V_{CC} pin to 1.4V (standard), the user can design a low-power timer mode. Bit 5 (CM_5) of the CPU mode register can be used to provide two-stage setting for the oscillation circuit: low-power mode when CM_5= 0 and high-power mode when $CM_5 = 1$. Note that high-power mode is set after a reset, so the program must switch to low-power mode to enable low-power-consumption mode, after allowing time for the oscillation to stabilize.

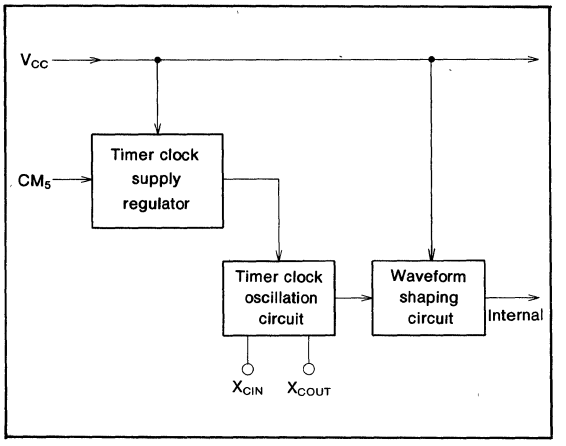


Fig. 39 Block diagram of the timer clock oscillation circuit

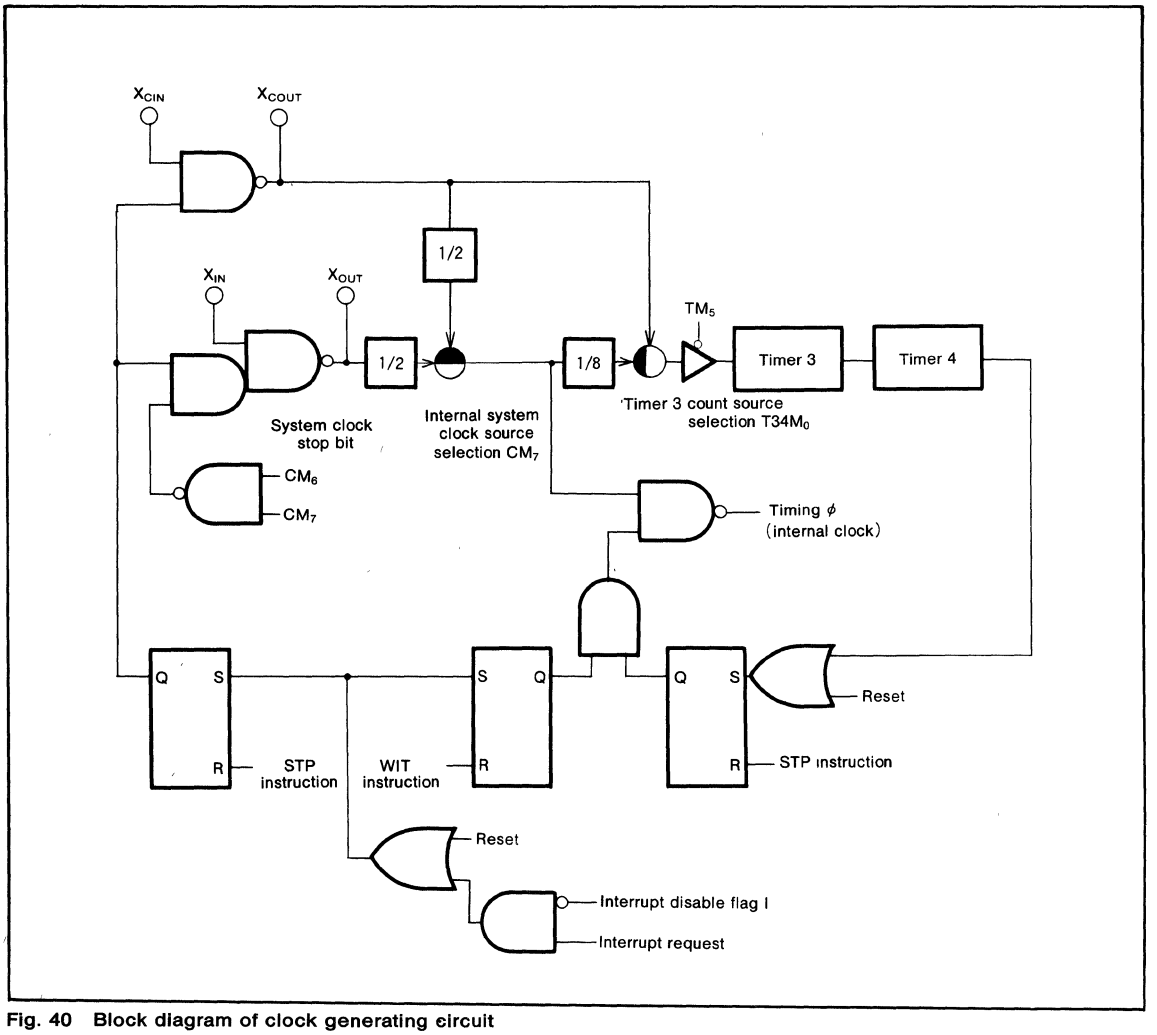
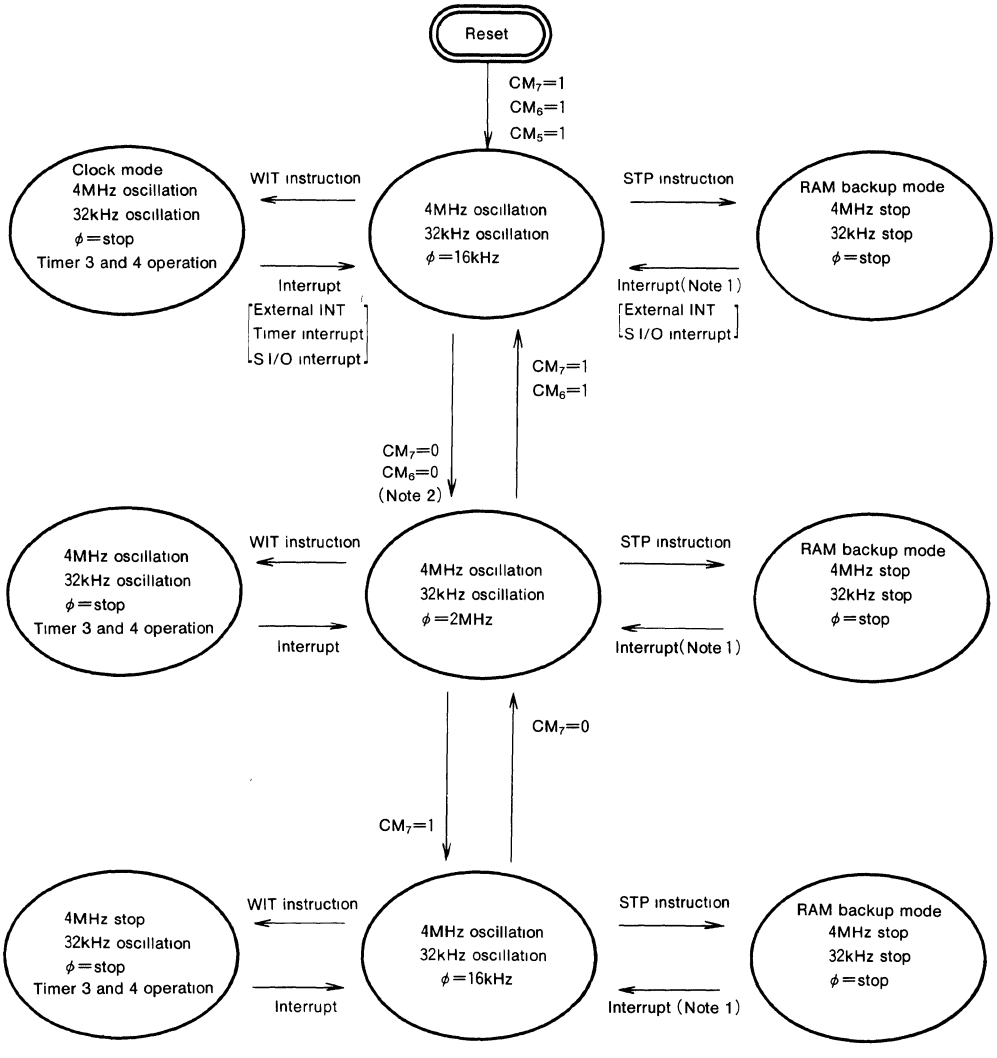


Fig. 40 Block diagram of clock generating circuit

MITSUBISHI ELECTRIC



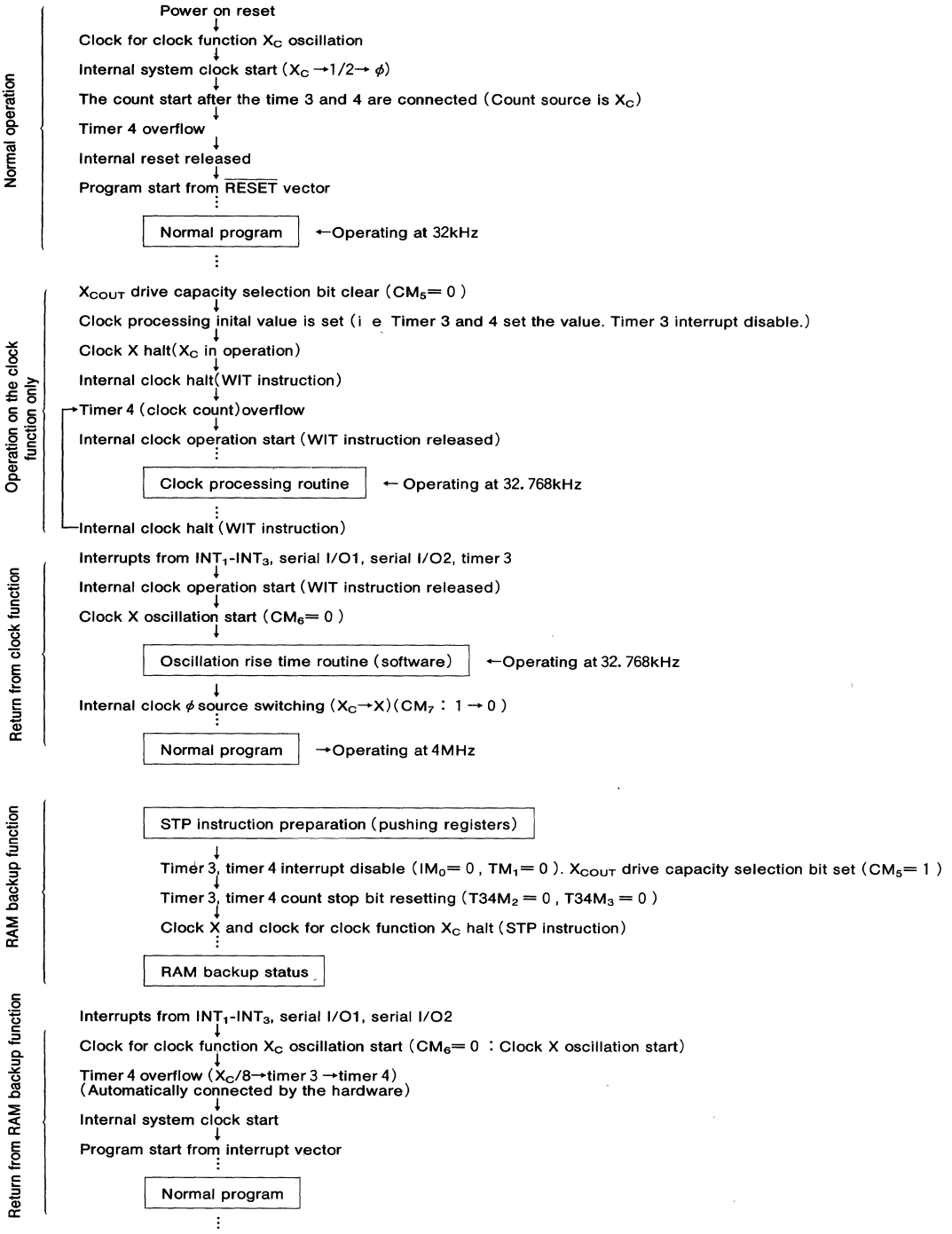
The above example assumes that signals of 4MHz and 32kHz are being applied to pins X_{IN} X_{CIN} respectively ϕ signifies the internal clock.

Note 1 : Approximately latency time are automatically generated upon release from the STP instruction due to connections of timer 3 and 4

2 : The software must provided enough time for the oscillation (4MHz) to stabilize

Fig. 41 Transition of states for the system clock

<An example of flow for system>



PROGRAMMING NOTES

(1) The frequency ratio of the timer is 1/(n+1).
(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as an NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
(3) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as an NOP) is needed before the SEC, CLC, or CLD instructions are executed.
(4) An NOP instruction must be used after the exection of a PLP instruction.
(5) When the interrupt is processed, confirm the interrupt enable bit is enable state after into the interrupt routine. If so, check the request flag after that.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.
(1) mask ROM confirmation form
(2) mask specification form
(3) ROM data ..... EPROM 3 sets

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "off" state	−0.3 to 7.0	V
V_I	Input voltage $\overline{RESET}$		−0.3 to 7.0	V
V_I	Input voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_7$, $P4_0$−$P4_7$, $P6_0$−$P6_7$, $P7_0$−$P7_3$, X_{IN}, X_{CIN}, V_{REF}, V_{SYNC}, H_{SYNC}		−0.3 to V_{CC}+0.3	V
V_O	Output voltage X_{COUT}		−0.3 to 2.5V (at high power mode) −0.3 to 1.5V (at low power mode)	V
V_O	Output voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_7$, $P4_0$−$P4_7$, R, G, B, I, OUT1, X_{OUT}, ϕ, D-A_{OUT0} to D-A_{OUT5}		−0.3 to V_{CC}+0.3	V

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=AV_{CC}=5V±10%, T_a=−10 to 70°C unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage	$f(X_{IN})$=4MHz (Note 1)	4.0	5.0	5.5	V
		$f(X_{CIN})$=32kHz (Note 2)	2.5	5.0	5.5	
V_{SS}	Supply voltage		0	0	0	V
V_{IH}	"H" input voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_7$, $P4_0$−$P4_7$, $P6_0$−$P6_7$, $P7_0$−$P7_3$, X_{IN}, OSC1, $\overline{RESET}$, H_{SYNC}, V_{SYNC}		0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_7$, $P4_0$−$P4_7$, $P6_0$−$P6_7$, $P7_0$−$P7_3$, X_{IN}, OSC1, H_{SYNC}, V_{SYNC}		0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0.15V_{CC}	V
V_{REF}	Reference voltage input V_{REF}		4.0		V_{CC}	V
V_{IA}	Analog input voltage AN_0−AN_7		0		V_{REF}	V
$I_{OH(avg)}$	"H" average output current (Note 3) $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_7$, R, G, B, I, OUT1				1	mA
$I_{OL(avg)}$	"L" average output current (Note 4) $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_7$, $P4_0$−$P4_7$, R, G, B, I, OUT1				2	mA
$f(X_{IN})$	Clock oscillating frequency for main clock (Note 5)				4.2	MHz
$f(X_{CIN})$	Clock oscillating frequency for clock function (Note 5)				32.768	kHz
f(OSC1)	Clock oscillating frequency for OSD		6.0	7.0	8.0	MHz

Note 1 : At OSD operating, maximum value is 4.5V
2 : It is only at clock operation mode
Any other operation mode, maximum value is 4.0V
3 : The total of input current from IC should be 20mA max.
4 : The total of input current from IC should be 30mA max.
5 : Oscillation frequency is at 50% duty cycle.

ELECTRICAL CHARACTERISTICS (V_{CC}=AV_{CC}=5V±10%, T_a=−10 to 70℃ unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max.	
V_{OH}	"H" output voltage $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P2_0$—$P2_7$, $P3_0$—$P3_7$, ϕ, R, G, B, I, OUT1	V_{CC}=4.5V I_{OH}=−0.5mA	2.4			V
V_{OL}	"L" output voltage $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P2_0$—$P2_7$, $P3_0$—$P3_7$, $P4_0$—$P4_7$, ϕ, R, G, B, I, OUT1	V_{CC}=4.5V I_{OL}=0.5mA			0.4	V
$V_{T+}-V_{T-}$	Hysteresis H_{SYNC}, V_{SYNC}, $P6_0$—$P6_3$, $P4_0$, $P4_2$, $P4_4$, $P4_6$, $P3_4$ (Note 1)	V_{CC}=5.0V		0.5		V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$	V_{CC}=5.0V		0.5		V
I_{IL}	"L" input current $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P2_0$—$P2_7$, $P3_0$—$P3_7$, $P4_0$—$P4_7$, $P6_0$—$P6_7$, $P7_0$—$P7_3$, H_{SYNC}, V_{SYNC}, $\overline{RESET}$	V_{CC}=5.5V V_I=0V			5	μA
I_{IH}	"H" input current $P0_0$—$P0_7$, $P1_0$—$P1_7$, $P2_0$—$P2_7$, $P3_0$—$P3_7$, $P4_0$—$P4_7$, $P6_0$—$P6_7$, $P7_0$—$P7_3$, H_{SYNC}, V_{SYNC}, $\overline{RESET}$	V_{CC}=5.5V V_I=5.5V			5	μA
V_{RAM}	RAM retention voltage	At stop mode	2.0		5.5	V
I_{CC}	Supply current	At system operation, X_{IN}=4MHz, X_{CIN}=32kHz, f(OSC1)=7MHz, Output transistors are at "off" state		13	24	mA
		At system operation, V_{CC}=3.0V, X_{IN}=stop, X_{CIN}=32kHz, Output transistors are at "off" state		18	36	μA
		At low−speed operation mode, V_{CC}=3.0V, X_{IN}=stop, X_{CIN}=32kHz, At wait mode (CM_5=0), Output transistors are at "off" state		2	8	
		At stop mode, X_{IN}=X_{CIN}=stop, Output transistors are at "off" state		1	10	
I_{ACC}	Analog power supply			0.5	1.0	mA

Note 1 : $P4_0$, $P4_2$, $P4_4$, $P4_6$ have the hysteresis only when these are used for serial I/O pins
$P3_4$ has the hysteresis only when this is used for a timer input pin

A-D CONVERTER CHARACTERISTICS

(V_{CC}=AV_{CC}=5V, V_{SS}=AV_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=AV_{CC}=V_{REF}=5.0V		±1.5	±3.0	LSB
T_{CONV}	Conversion time				24.5	μs
V_{IA}	Analog input voltage		AV_{SS}		V_{REF}	V
V_{REF}	Reference input voltage		4.0		V_{CC}	V
R_{LADDER}	Ladder resistance value	V_{REF}=5.0V		40		kΩ
$I_{VREF(AD)}$	Reference input current (Note 1)	V_{REF}=5.0V			0.3	mA
V_{AVCC}	Analog power supply input voltage			V_{CC}		V
V_{AVSS}	Analog power supply input voltage			0		V

Note 1 : The total of I_{VREF} is the sum of $I_{VREF(AD)}$ and $I_{VREF(DA)}$.

D-A CONVERTER CHARACTERISTICS

(V_{CC}=AV_{CC}= 5 V, V_{SS}=AV_{SS}= 0 V, T_a =25℃, f(X_{IN})= 4 MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max	
—	Resolution				8	Bits
—	Full scale deviation	V_{CC}=AV_{CC}=V_{REF}=5.0V			1.0	%
T_{SU}	Set time				3	μs
V_{REF}	Reference input voltage		4		V_{CC}	V
R_{OUT}	Output resistance		1	2	4	kΩ
V_{AVSS}	Analog power supply input voltage			0		V
$I_{VREF(DA)}$	Reference power input current (Note 1)		0	2.5	5.0	mA

Note 1 : The total of I_{VREF} is the sum of $I_{VREF(AD)}$ and $I_{VREF(DA)}$.
$I_{VREF(DA)}$ is the reference power input current flowing when channel 1 of the DA converter is operating. (The other five DA converter register values are 00_{16})