M37225M6/M8/MA/MC–XXXSP, M37225ECSP

SNGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER with ON-SCREEN DISPLAY CONTROLLER

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1. DESCRIPTION

The M37225M6/M8/MA/MC–XXXSP are single-chip microcomputers designed with CMOS silicon gate technology. They have a OSD, I^2C-BUS interface, PWM output, and 12 V withstand, so it is useful for a channel selection system for TV.

The features of the M37225ECSP are similar to those of the M37225M6-XXXSP except that the chip has a built-in PROM which can be written electrically. The differences amang M37225M6/M8/MA/MC–XXXSP are the ROM, RAM size. Accordingly, the following descriptions will be for the M37225M6-XXXSP.

2. FEATURES

- Number of basic instructions 71
- Memory size
  - ROM ..... 24K bytes (M37225M6-XXXSP)
    32K bytes (M37225M8-XXXSP)
    40K bytes (M37225MA–XXXSP)
    48K bytes (M37225MC–XXXSP, M37225ECSP)
  - RAM ..... 1024 bytes (M37225M6/M8-XXXSP)
    2048 bytes (M37225MA/MC–XXXSP, M37225ECSP)
  - (✻ ROM correction memory included)
- Minimum instruction execution time
  ..... 0.5 µs (at 8 MHz oscillation frequency)
- Power source voltage ..... 5 V ± 10 %
- Subroutine nesting ..... 128 levels (Max.)
- Interrupts ..... 16 types, 16 vectors
- 8-bit timers 4
- Programmable I/O ports (Ports P0, P1, P2, $P3_0$–$P3_2$, $P3_5$) 28
- Input ports (Ports $P3_3$, $P3_4$, $P5_0$, $P5_1$) 4
- Output ports (Ports $P5_2$–$P5_5$) 4
- 12 V withstand ports 6
- LED drive ports 4
- Serial I/O ..... 8-bit × 1 channel
- Multi-master I^2C-BUS interface ..... 1 (2 systems)
- A-D converter (8-bit resolution) ..... 8 channels
- PWM output circuit ..... 14-bit × 2, 8-bit × 6
- Power dissipation
  In operating ..... 165 mW
  (at V_{CC} = 5.5V, 8 MHz oscillation frequency, and OSD on)
- ROM correction function ..... 3 vectors
- Immediate return mode from wait state
- OSD function
  - Display characters ..... 24 characters × 2 lines
    (It is possible to display 3 lines or more by software)
  - Kinds of characters ..... 381 kinds
  - Character display area 16 × 20 dots
  - Kinds of character sizes ..... Block display: 3 kinds
    SPRITE display: 1 kinds
  - Kinds of character colors. ..... 8 colors (R, G, B)
  - Coloring unit ..... character, character background, raster
  - Display position
    Horizontal: 64 levels Vertical :255 levels
  - Attribute ..... Border (all-bordered, shadow-bordered), BUTTON
  - SPRITE display function
  - Wallpaper function
  - Window function
  - Corresponding to bi-scan mode

3. APPLICATION

TV

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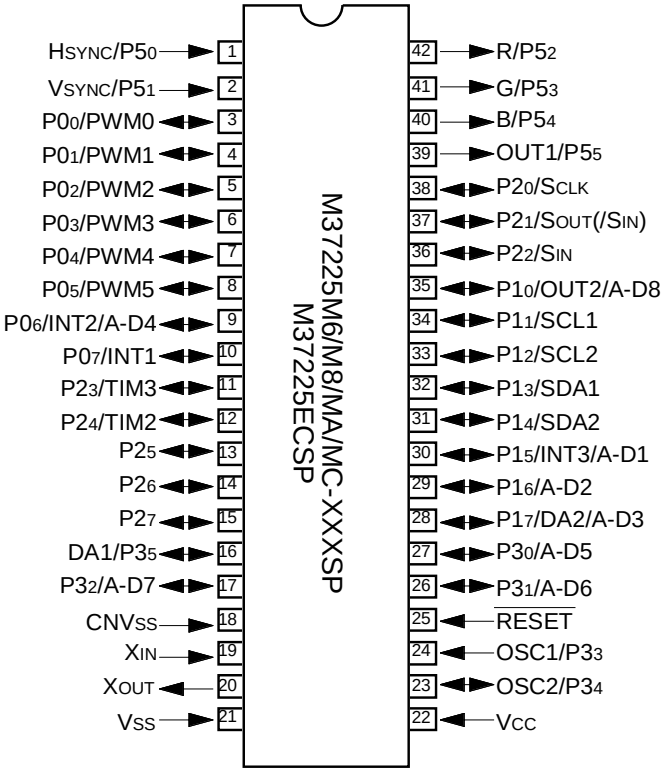
4. PIN CONFIGURATION



Outline 42P4B

Fig. 4.1 Pin Configuration (Top View)

5. FUNCTIONAL BLOCK DIAGRAM

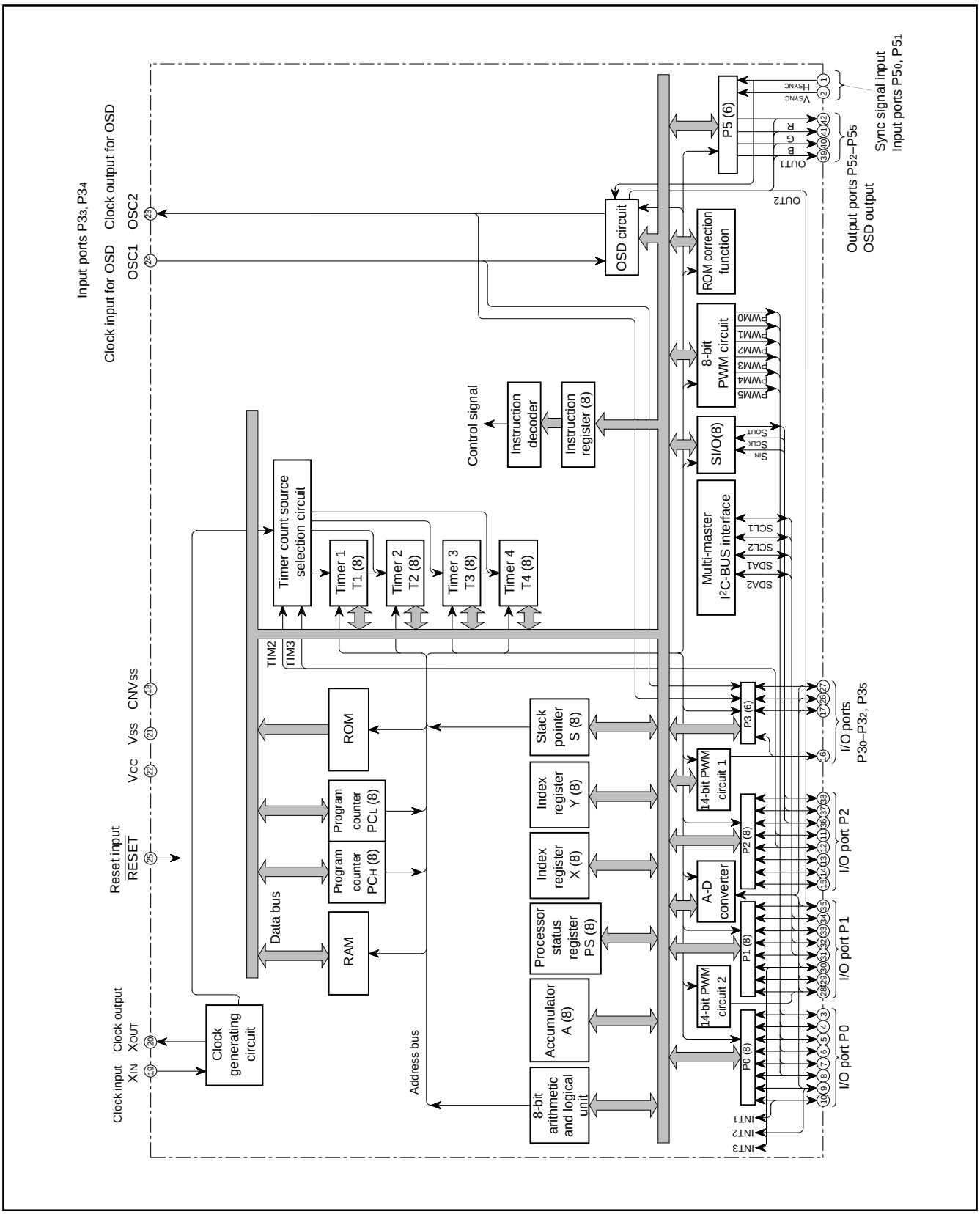


Fig. 5.1 Functional Block Diagram of M37225

6. PERFORMANCE OVERVIEW

Table 6.1 Performance Overview

Parameter				Functions
Number of basic instructions				71
Instruction execution time				0.5 μs (the minimum instruction execution time, at 8 MHz oscillation frequency)
Clock frequency				8 MHz (maximum)
Memory size	ROM	M37225M6-XXXSP		24K bytes
		M37225M8-XXXSP		32K bytes
		M37225MA-XXXSP		40K bytes
		M37225MC-XXXSP, M37225ECSP		48K bytes
	RAM	M37225M6/M8-XXXSP		1024 bytes (ROM correction memory included)
		M37225MA/MC-XXXSP, M37225ECSP		2048 bytes (ROM correction memory included)
	OSD ROM			15K bytes
	OSD RAM			96 bytes
Input/Output ports	$P0_0$–$P0_5$		I/O	6-bit × 1 (N-channel open-drain output structure, can be used as PWM output pins)
	$P0_6$, $P0_7$		I/O	2-bit × 1 (N-channel open-drain output structure, can be used as INT input pins, A-D input pin)
	P1		I/O	8-bit × 1 (CMOS input/output structure, can be used as OSD output pin, INT input pin, A-D input pins, DA output pin, multi-master I^2C-BUS interface)
	P2		I/O	8-bit × 1 (CMOS input/output structure, can be used as serial I/O pins, timer external clock input pins)
	$P3_0$, $P3_1$, $P3_5$		I/O	3-bit × 1 (CMOS output structure, or N-channel open-drain output structure, can be used as A-D input pins, DA output pin)
	$P3_2$		I/O	1-bit × 1 (N-channel open-drain output structure, can be used as A-D input pin)
	$P3_3$, $P3_4$		Input	2-bit × 1 (Can be used as OSD clock input/output pins)
	$P5_0$, $P5_1$		Input	2-bit × 1 (N-channel open-drain output structure, can be used as horizonal • vertical synchronous sibnal input pins)
	$P5_2$–$P5_5$		Output	4-bit × 1 (CMOS output structure, can be used as OSD output pins)
Serial I/O				8-bit × 1
Multi-master I^2C-BUS interface				1 (2 systems)
A-D converter				8 channels (8-bit resolution)
PWM output circuit				14-bit × 2, 8-bit × 6
Timers				8-bit timer × 4
ROM correction function				3 vectors
Subroutine nesting				128 levels (maximum)
Interrupt				<16 types> INT external interrupt × 3, Internal timer interrupt × 6, Serial I/O interrupt × 1, OSD interrupt × 1, Multi-master I^2C-BUS interface interrupt × 1, f(X_{IN})/4096 interrupt × 1, SPRITE OSD interrupt × 1, A-D conversion interrupt × 1, V_{SYNC} interrupt × 1, BRK instruction interrupt × 1, reset × 1
Clock generating circuit				2 built-in circuits (externally connected to a ceramic resonator or a quartz-crystal oscillator)

Table 6.2 Performance Overview (Continued)

Parameter		Functions
OSD function	Number of display characters	24 characters × 2 lines
	Dot structure	16 × 20 dots
	Kinds of characters	381 kinds
	Kinds of character sizes	3 kinds
	Character font coloring	1 screen : 8 kinds (per character unit)
	Display position	Horizontal : 64 levels, Vertical : 255 levels
Power source voltage		5V ± 10%
Power dissipation	OSD ON	165 mW typ. (at oscillation frequency f(XIN) = 8 MHz, fOSC = 8 MHz)
	OSD OFF	110 mW typ. (at oscillation frequency f(XIN) = 8 MHz)
	In stop mode	1.65 mW (maximum)
Operating temperature range		–10 °C to 70 °C
Device structure		CMOS silicon gate process
Package		42-pin plastic molded SDIP

7. PIN DESCRIPTION

Table 7.1 Pin Description

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Power source		Apply voltage of 5 V ± 10 % to (typical) V_{CC}, and 0 V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a LOW for 2 µs or more (under normal V_{CC} conditions). If more time is needed for the quartz-crystal oscillator to stabilize, this LOW condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic resonator or a quartz-crystal oscillator is connected between pins X_{IN} and X_{OUT}. If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
$P0_0$/PWM0–$P0_5$/PWM5, $P0_6$/INT2/A-D4, $P0_7$/INT1	I/O port P0	I/O	Port P0 is an 8-bit I/O port with direction register allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open-drain output. (See note 1)
	PWM output	Output	Pins $P0_0$–$P0_5$ are also used as PWM output pins PWM0–PWM5 respectively. The output structure is N-channel open-drain output.
	External interrupt input	Input	Pins $P0_6$ and $P0_7$ are also used as INT external interrupt input pins INT2 and INT1 respectively.
	Analog input	Input	$P0_6$ pin is also used as analog input pin A-D4.
$P1_0$/OUT2/A-D8, $P1_1$/SCL1, $P1_2$/SCL2, $P1_3$/SDA1, $P1_4$/SDA2, $P1_5$/INT3/A-D1, $P1_6$/A-D2, $P1_7$/DA2/A-D3	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0. The output structure is CMOS output. (See note 1)
	OSD output	Output	Pins $P1_0$ is also used as OSD output pin OUT2. The output structure is CMOS output.
	Multi-master I^2C-BUS interface	I/O	Pins $P1_1$–$P1_4$ are used as SCL1, SCL2, SDA1 and SDA2 respectively, when multi-master I^2C-BUS interface is used. The output structure is N-channel open-drain output.
	Analog input	Input	Pins $P1_0$, $P1_5$–$P1_7$ are also used as analog input pin A-D8, A-D1–A-D3 respectively.
	External interrupt input	Input	$P1_5$ pin is also used as INT external interrupt input pin INT3.
	DA output	Output	Pins $P1_7$ is also used as 14-bit PWM output pin DA2. The output structure is CMOS output.
$P2_0$/S_{CLK}, $P2_2$/S_{IN}, $P2_3$/TIM3, $P2_4$/TIM2, $P2_5$–$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0. The $P2_1$/S_{OUT}(/S_{IN}), output structure is CMOS output. (See note 1)
	Serial I/O synchronous clock input/output port	I/O	$P2_0$ pin is also used as serial I/O synchronous clock input/output pin S_{CLK}. The output structure is N-channel open-drain output.
	Serial I/O data input/output	I/O	$P2_1$ pin is also used as serial I/O data input/output pin S_{OUT} (/S_{IN}). The output structure is N-channel open-drain output.
	Serial I/O data input	Input	$P2_2$ pin is also used as serial I/O data input pin S_{IN}.
	External clock input for timer	Input	Pins $P2_3$ and $P2_4$ are also used as timer external clock input pins TIM3 and TIM2 respectively.
$P3_0$/A-D5, $P3_1$/A-D6, $P3_2$/A-D7, DA1/$P3_5$	I/O port P3	I/O	Ports $P3_0$–$P3_2$ and $P3_5$ are a 3-bit I/O port and has basically the same functions as port 0 (see note 1). Either CMOS output or N-channel open-drain output structure can be selected as ports $P3_0$, $P3_1$ and $P3_5$. The output structure of port $P3_2$ is N-channel open-drain output structure.(See notes 1, 2)
	Analog input	Input	Pins $P3_0$–$P3_2$ are also used as analog input pins A-D5–A-D7 respectively.
	DA output	Output	$P3_5$ pin is also used as 14-bit PWM output pin DA1. The output structure is CMOS output. At reset, output is undefined.
OSC1/$P3_3$, OSC2/$P3_4$,	Input port P3	Input	Pins $P3_3$ and $P3_4$ are a 2-bit input port.
	Clock input for OSD	Input	$P3_3$ pin is also used as OSD clock input pin OSC1.
	Clock output for OSD	Output	$P3_4$ pin is also used as OSD clock output pin OSC2. The output structure is CMOS output.

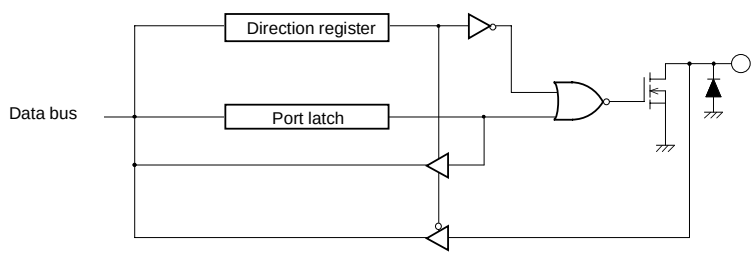
Table 7.2 Pin Description (continued)

Pin	Name	Input/ Output	Functions
H_{SYNC}/$P5_0$, V_{SYNC}/$P5_1$	Input port P5	Input	Ports $P5_0$ and $P5_1$ are a 2-bit input port.
	H_{SYNC} input	Input	This is a horizontal synchronizing signal input for OSD.
	V_{SYNC} input	Input	This is a vertical synchronizing signal input for OSD.
R/$P5_2$, G/$P5_3$, B/$P5_4$, OUT1/$P5_5$	Output port P5	Output	Ports $P5_2$–$P5_5$ are a 4-bit output port. The output structure is CMOS output.
	OSD output	Output	Pins $P5_2$–$P5_5$ are also used as OSD output pins R, G, B, OUT1 respectively. The output structure is CMOS output. At reset, output is LOW.

Notes 1: Port Pi (i = 0 to 3) has the port Pi direction register which can be used to program each bit as an input (“0”) or an output (“1”). The pins programmed as “1” in the direction register are output pins. When pins are programmed as “0,” they are input pins. When pins are programmed as output pins, the output data are written into the port latch and then output. When data is read from the output pins, the output pin level is not read but the data of the port latch is read. This allows a previously-output value to be read correctly even if the output LOW voltage has risen, for example, because a light emitting diode was directly driven. The input pins are in the floating state, so the values of the pins can be read. When data is written into the input pin, it is written only into the port latch, while the pin remains in the floating state.

2: To switch output structures, set by the following bits.
$P3_0$: bit 6 of port P3 direction register
$P3_1$: bit 7 of port P3 direction register
$P3_5$: bit 5 of port $P3_5$ output mode control register
When “0,” CMOS output; when “1,” N-channel open-drain output.

Ports $P0_0$–$P0_5$

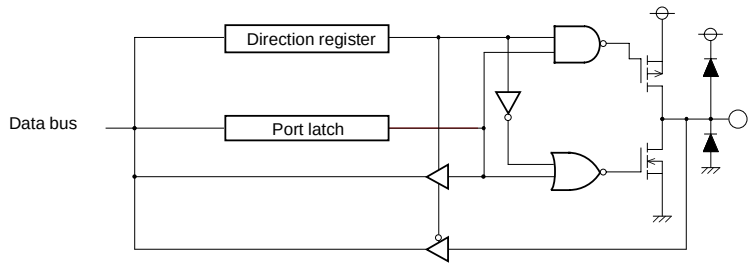


N-channel open-drain output

Ports $P0_0$–$P0_5$

Note : Each port is also used as follows :
$P0_0$–$P0_5$: PWM0–PWM5

Ports P1, P2, $P3_0$, $P3_1$



CMOS output

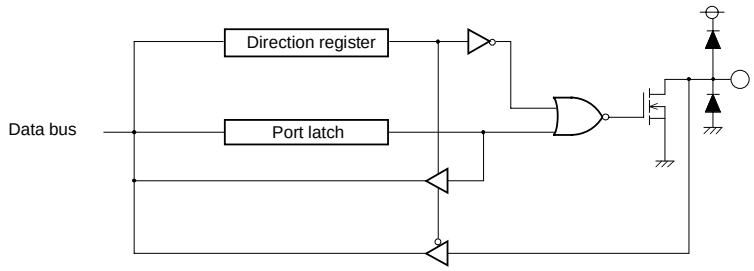
Ports P1, P2, $P3_0$, $P3_1$, $P3_5$

Notes 1: Each port is also used as follows :

$P1_0$: OUT2/AD8	$P2_2$: SIN
$P1_1$: SCL1	$P2_3$: TIM3
$P1_2$: SCL2	$P2_4$: TIM2
$P1_3$: SDA1	$P3_0$: A-D5
$P1_4$: SDA2	$P3_1$: A-D6
$P1_5$: INT3/A-D1	$P3_5$: DA1
$P1_6$: A-D2	
$P1_7$: DA2/A-D3	
$P2_0$: SCLK	
$P2_1$: SOUT/(SIN)	

2: Either CMOS output or N-channel open-drain output structure can be selected as ports $P3_0$, $P3_1$ and $P3_5$ (when selecting N-channel open-drain, it is the same with N-channel open-drain output below).

Ports $P0_6$, $P0_7$, $P3_2$



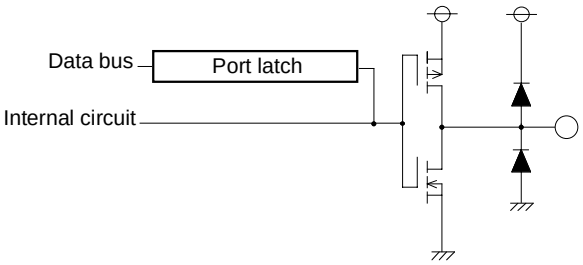
N-channel open-drain output

Ports $P0_6$, $P0_7$, $P3_2$

Note : Each port is also used as follows :
$P0_6$: INT2/A-D4
$P0_7$: INT1

Fig. 7.1 I/O Pin Block Diagram (1)

$P5_2$–$P5_5$

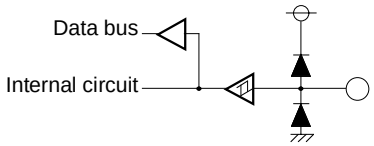


CMOS output

Ports $P5_2$–$P5_5$

Note : Each pin is also used as follows :
$P5_2$: R
$P5_3$: G
$P5_4$: B
$P5_5$: OUT1

$P5_0$, $P5_1$

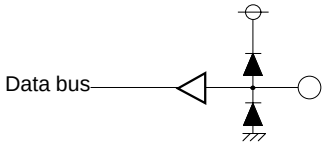


Schmidt input

Ports $P5_0$, $P5_1$

Note : Each pin is also used as follows :
$P5_0$: HSYNC
$P5_1$: VSYNC

$P3_3$, $P3_4$



Input

Ports $P3_3$, $P3_4$

Note : Each pin is also used as follows :
$P3_3$: OSC1
$P3_4$: OSC2

Fig. 7.2 I/O Pin Block Diagram (2)

8. FUNCTIONAL DESCRIPTION
8.1 CENTRAL PROCESSING UNIT (CPU)

This microcomputer uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the SERIES 740 <Software> User's Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

The FST, SLW instruction cannot be used.

The MUL, DIV, WIT and STP instructions can be used.

8.1.1 CPU Mode Register

The CPU mode register contains the stack page selection bit and internal system clock selection bit. The CPU mode register is allocated at address 00FB16.

CPU Mode Register

b7 b6 b5 b4 b3 b2 b1 b0

0 0 1 1 1 0 0

CPU mode register (CM) [Address 00FB16]

B	Name	Functions	After reset	R	W
0, 1	Processor mode bits (CM0, CM1)	b1 b0 0 0: Single-chip mode 0 1: 1 0: 1 1: } Not available	0	R	W
2	Stack page selection bit (CM2) (See note)	0: 0 page 1: 1 page	1	R	W
3 to 5	Fix these bits to "1."		1	R	W
6, 7	Fix these bits to "0."		0	R	W

Note: This bit is set to "1" after the reset release.

Fig. 8.1.1 CPU Mode Register

8.2 MEMORY

8.2.1 Special Function Register (SFR) Area

The special function register (SFR) area in the zero page contains control registers such as I/O ports and timers.

8.2.2 RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

8.2.3 ROM

ROM is used for storing user programs as well as the interrupt vector area.

8.2.4 OSD RAM

RAM for display is used for specifying the character codes and colors to display.

8.2.5 OSD ROM

ROM for display is used for storing character data.

8.2.6 Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

8.2.7 Zero Page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

8.2.8 Special Page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

8.2.9 ROM Correction Vector

This is used as the program jump destination addresses for ROM correction.

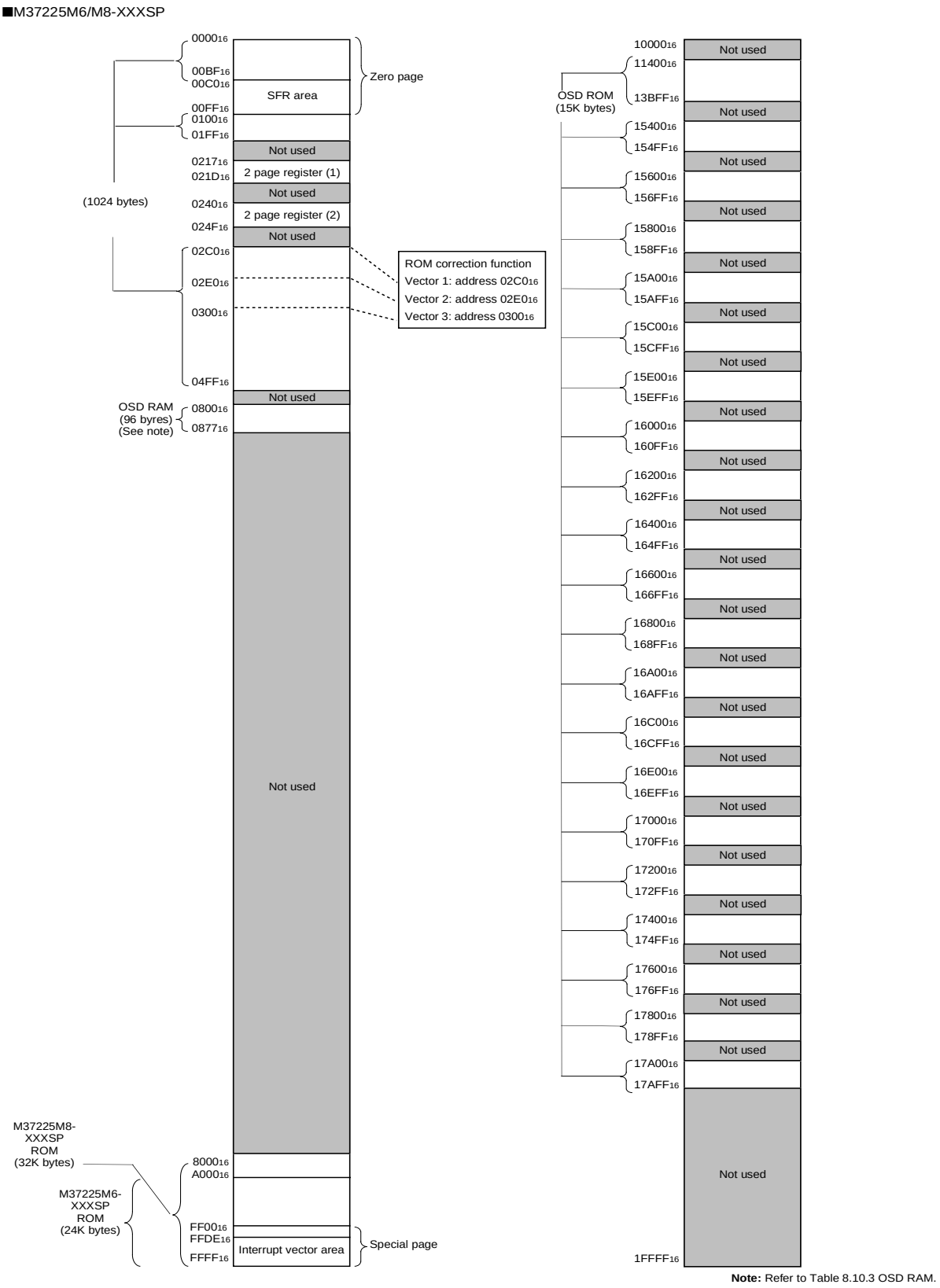


Fig. 8.2.1 Memory Map (M37225M6/M8-XXXSP)

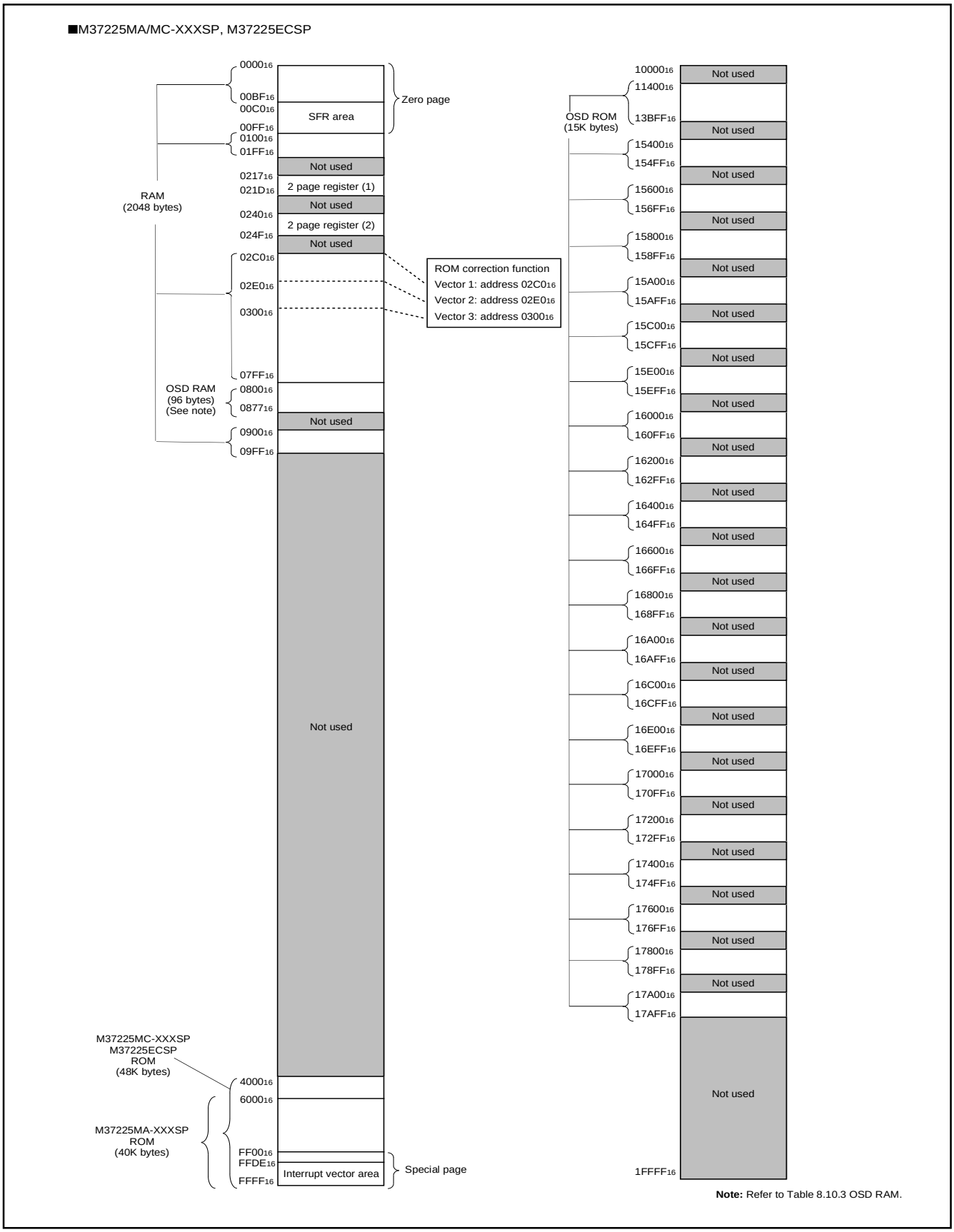


Fig. 8.2.2 Memory Map (M37225MA/MC-XXXSP, M37225ECSP)

■ SFR area (addresses $C0_{16}$ to DF_{16})

< Bit allocation >

: } Function bit

Name : } Function bit

: No function bit

0 : Fix to this bit to "0" (do not write to "1")

1 : Fix to this bit to "1" (do not write to "0")

< State immediately after reset >

0 : "0" immediately after reset

1 : "1" immediately after reset

? : Indeterminate immediately after reset

Address	Register	Bit allocation b7							b0	State immediately after reset b7							b0
$C0_{16}$	Port P0 (P0)									?							
$C1_{16}$	Port P0 direction register (D0)									00_{16}							
$C2_{16}$	Port P1 (P1)									?							
$C3_{16}$	Port P1 direction register (D1)									00_{16}							
$C4_{16}$	Port P2 (P2)									?							
$C5_{16}$	Port P2 direction register (D2)									00_{16}							
$C6_{16}$	Port P3 (P3)			P35	P34IN	P33IN	P32	P31	P30	?							
$C7_{16}$	Port P3 direction register (D3)	P31S	P30S	P35D			P32D	P31D	P30D	0	0	0	?	?	0	0	0
$C8_{16}$										?							
$C9_{16}$	Port P35 output mode control register (P3S)	0	0	P35S						0	0	0	0	?	?	?	?
CA_{16}	Port P5 (P5)			P55 OUT	P54 OUT	P53 OUT	P52 OUT	P51 IN	P50 IN	0	0	?	?	?	?	?	?
CB_{16}	OSD port control register (PF)	0	OUT2 SEL	P55 SEL	P54 SEL	P53 SEL	P52 SEL	0	0	00_{16}							
CC_{16}	Test register					1	1			0	0	0	0	1	1	?	?
CD_{16}	Interrupt input polarity register (IP)	0	0	POL3	POL2	POL1	0	OCG1	OCG0	00_{16}							
CE_{16}	DA1-H register (DA1-H)									?							
CF_{16}	DA1-L register (DA1-L)									0	0	?	?	?	?	?	?
$D0_{16}$	PWM0 register (PWM0)									?							
$D1_{16}$	PWM1 register (PWM1)									?							
$D2_{16}$	PWM2 register (PWM2)									?							
$D3_{16}$	PWM3 register (PWM3)									?							
$D4_{16}$	PWM4 register (PWM4)									?							
$D5_{16}$	PWM output control register 1 (PW)	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0	00_{16}							
$D6_{16}$	PWM output control register 2 (PN)	0	0	PN5	PN4	PN3	PN2	0	0	00_{16}							
$D7_{16}$	I^2C data shift register (S0)	D7	D6	D5	D4	D3	D2	D1	D0	?							
$D8_{16}$	I^2C address register (S0D)	SAD6	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0	RBW	00_{16}							
$D9_{16}$	I^2C status register (S1)	MST	TRX	BB	PIN	AL	AAS	AD0	LRB	0	0	0	1	0	0	0	?
DA_{16}	I^2C control register (S1D)	BSEL1	BSEL0	10BIT SAD	ALS	ESO	BC2	BC1	BC0	00_{16}							
DB_{16}	I^2C clock control register (S2)	ACK	ACK BIT	FAST MODE	CCR4	CCR3	CCR2	CCR1	CCR0	00_{16}							
DC_{16}	Serial I/O mode register (SM)		SM6	SM5	0	SM3	SM2	SM1	SM0	00_{16}							
DD_{16}	Serial I/O register (SIO)									?							
DE_{16}	AD conversion register (AD)									?							
DF_{16}	AD control register (ADCON)	0		0	ADVREF	ADSTR	ADIN2	ADIN1	ADIN0	08_{16}							

Fig. 8.2.3 Memory Map of Special Function Register (SFR) (1)

■ SFR area (addresses $E0_{16}$ to FF_{16})

< Bit allocation >

: Function bit

Name :

: No function bit

0 : Fix to this bit to "0" (do not write to "1")

1 : Fix to this bit to "1" (do not write to "0")

< State immediately after reset >

0 : "0" immediately after reset

1 : "1" immediately after reset

? : Indeterminate immediately after reset

Address	Register	Bit allocation b7							b0	State immediately after reset b7							b0
$E0_{16}$	Block H register (BHP)			BHP5	BHP4	BHP3	BHP2	BHP1	BHP0	00_{16}							
$E1_{16}$	Block 1V register (B1VP)	B1VP7	B1VP6	B1VP5	B1VP4	B1VP3	B1VP2	B1VP1	B1VP0	?							
$E2_{16}$	Block 2V register (B2VP)	B2VP7	B2VP6	B2VP5	B2VP4	B2VP3	B2VP2	B2VP1	B2VP0	?							
$E3_{16}$	SPRITE control register (SC)	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00_{16}							
$E4_{16}$	SPRITE H register (SHP)	SHP7	SHP6	SHP5	SHP4	SHP3	SHP2	SHP1	SHP0	00_{16}							
$E5_{16}$	SPRITE V register (SVP)	SVP7	SVP6	SVP5	SVP4	SVP3	SVP2	SVP1	SVP0	?							
$E6_{16}$	Color register 1 (CO1)		CO16	CO15	CO14	CO13	CO12	CO11	CO10	0	?	?	?	?	?	?	?
$E7_{16}$	Color register 2 (CO2)		CO26	CO25	CO24	CO23	CO22	CO21	CO20	0	?	?	?	?	?	?	?
$E8_{16}$	Color register 3 (CO3)		CO36	CO35	CO34	CO33	CO32	CO31	CO30	0	?	?	?	?	?	?	?
$E9_{16}$	Color register 4 (CO4)		CO46	CO45	CO44	CO43	CO42	CO41	CO40	0	?	?	?	?	?	?	?
EA_{16}	OSD control register (OC)	OC7	OC6	OC5	OC4	OC3	OC2	OC1	OC0	00_{16}							
EB_{16}	OSD I/O polarity control register (OPC)	OPC7	OPC6	OPC5	OPC4	OPC3	OPC2	OPC1	OPC0	00_{16}							
EC_{16}	Color register 5 (CO5)		CO56	CO55	CO54	CO53	CO52	CO51	CO50	0	?	?	?	?	?	?	?
ED_{16}	Color register 6 (CO6)		CO66	CO65	CO64	CO63	CO62	CO61	CO60	0	?	?	?	?	?	?	?
EE_{16}	Color register 7 (CO7)		CO76	CO75	CO74	CO73	CO72	CO71	CO70	0	?	?	?	?	?	?	?
EF_{16}	Color register 8 (CO8)		CO86	CO85	CO84	CO83	CO82	CO81	CO80	0	?	?	?	?	?	?	?
$F0_{16}$	Timer 1 (T1)									FF_{16}							
$F1_{16}$	Timer 2 (T2)									07_{16}							
$F2_{16}$	Timer 3 (T3)									FF_{16}							
$F3_{16}$	Timer 4 (T4)									07_{16}							
$F4_{16}$	Timer mode register 1 (TM1)			TM15	TM14	TM13	TM12	TM11	TM10	00_{16}							
$F5_{16}$	Timer mode register 2 (TM2)			TM25	TM24	TM23	TM22	TM21	TM20	00_{16}							
$F6_{16}$	PWM5 register (PWM5)									?							
$F7_{16}$	Test register	00_{16}								?							
$F8_{16}$	Test register	00_{16}								?							
$F9_{16}$	Block 1 control register (B1C)				B1C4	B1C3	B1C2	B1C1	B1C0	0	0	0	?	?	?	?	?
FA_{16}	Block 2 control register (B2C)				B2C4	B2C3	B2C2	B2C1	B2C0	0	0	0	?	?	?	?	?
FB_{16}	CPU mode register (CM)	0	0	1	1	1	CM2	0	0	$3C_{16}$							
FC_{16}	Interrupt request register 1 (IREQ1)	IT3R	IICR	VSCR	OSDR	TM4R	TM3R	TM2R	TM1R	00_{16}							
FD_{16}	Interrupt request register 2 (IREQ2)	0	ADR		MSR	SPR	S1R	IT2R	IT1R	00_{16}							
FE_{16}	Interrupt control register 1 (ICON1)	IT3E	IICE	VSCE	OSDE	TM4E	TM3E	TM2E	TM1E	00_{16}							
FF_{16}	Interrupt control register 2 (ICON2)		ADE	0	MSE	SPE	S1E	IT2E	IT1E	00_{16}							

Fig. 8.2.4 Memory Map of Special Function Register (SFR) (2)

■ 2 page register area (addresses 210_{16} to $21F_{16}$, 240_{16} to $24F_{16}$)

< Bit allocation >

: Function bit

Name :

: No function bit

0 : Fix to this bit to "0" (do not write to "1")

1 : Fix to this bit to "1" (do not write to "0")

< State immediately after reset >

0 : "0" immediately after reset

1 : "1" immediately after reset

? : Indeterminate immediately after reset

Address	Register	Bit allocation b7	b6	b5	b4	b3	b2	b1	b0	State immediately after reset b7	b6	b5	b4	b3	b2	b1	b0
210_{16}										?							
211_{16}										?							
212_{16}										?							
213_{16}										?							
214_{16}										?							
215_{16}										?							
216_{16}										?							
217_{16}	ROM correction address 1 (high-order)									00_{16}							
218_{16}	ROM correction address 1 (low-order)									00_{16}							
219_{16}	ROM correction address 2 (high-order)									00_{16}							
$21A_{16}$	ROM correction address 2 (low-order)									00_{16}							
$21B_{16}$	ROM correction enable register (RCR)	0	0	0	0	0	RCR2	RCR1	RCR0	00_{16}							
$21C_{16}$	ROM correction address 3 (high-order)									00_{16}							
$21D_{16}$	ROM correction address 3 (low-order)									00_{16}							
$21E_{16}$										?							
$21F_{16}$										?							
240_{16}	Left border control register (LBR)		LBR6	LBR5	LBR4	LBR3	LBR2	LBR1	LBR0	00_{16}							
241_{16}	Right border control register (RBR)		RBR6	RBR5	RBR4	RBR3	RBR2	RBR1	RBR0	00_{16}							
242_{16}										?							
243_{16}										?							
244_{16}										?							
245_{16}	Top border control register (TBR)	TBR7	TBR6	TBR5	TBR4	TBR3	TBR2	TBR1	TBR0	?							
246_{16}	Bottom border control register (BBR)	BBR7	BBR6	BBR5	BBR4	BBR3	BBR2	BBR1	BBR0	?							
247_{16}	Test register	00_{16}								00_{16}							
248_{16}										?							
249_{16}										?							
$24A_{16}$										?							
$24B_{16}$										?							
$24C_{16}$										?							
$24D_{16}$										?							
$24E_{16}$	DA2-H register (DA2H)									?							
$24F_{16}$	DA2-L register (DA2L)									0	0	?	?	?	?	?	?

Fig. 8.2.5 Memory Map of 2 Page Register Area

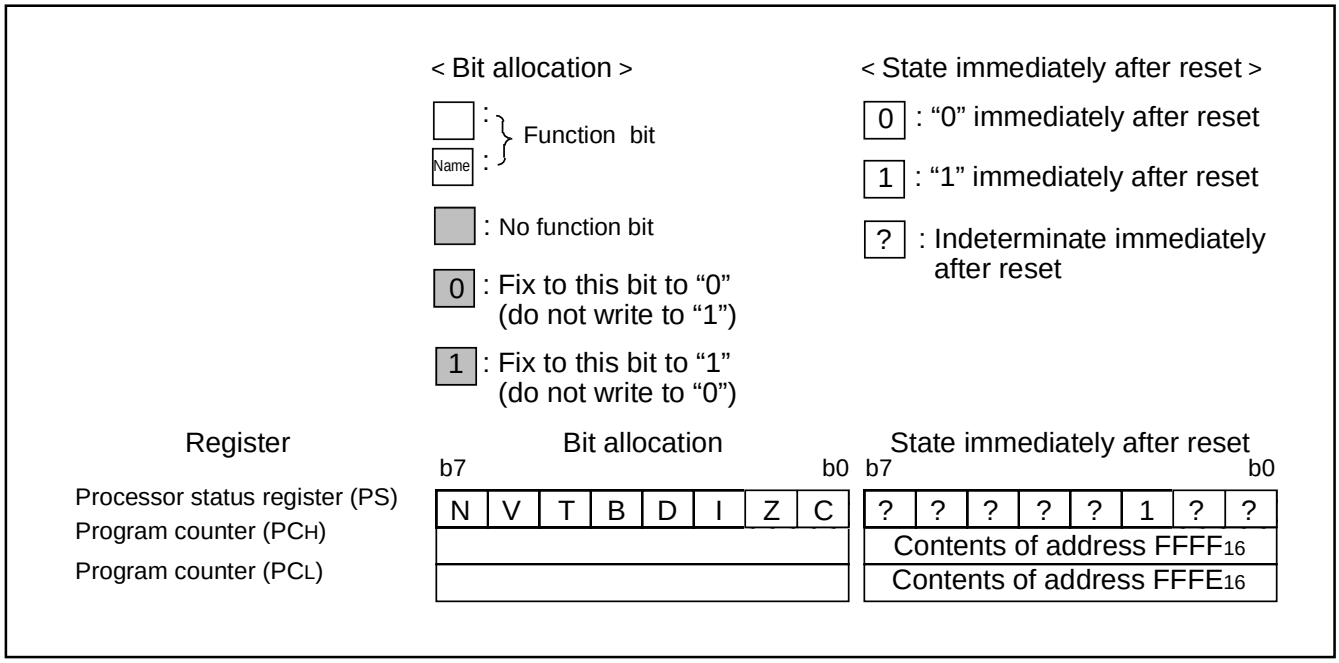


Fig. 8.2.6 Internal State of Processor Status Register and Program Counter at Reset

8.3 INTERRUPTS

Interrupts can be caused by 16 different sources consisting of 3 external, 14 internal, 1 software, and reset. Interrupts are vectored interrupts with priorities as shown in Table 8.3.1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted,

① The contents of the program counter and processor status register are automatically stored into the stack.

② The interrupt disable flag I is set to "1" and the corresponding interrupt request bit is set to "0."

③ The jump destination address stored in the vector address enters the program counter.

Other interrupts are disabled when the interrupt disable flag is set to "1."

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figures 8.3.2 to 8.3.6 show the interrupt-related registers.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1," interrupt request bit is "1," and the interrupt disable flag is "0." The interrupt request bit can be set to "0" by a program, but not set to "1." The interrupt enable bit can be set to "0" and "1" by a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 8.3.1 shows interrupt control.

8.3.1 Interrupt Causes

(1) VSYNC, OSD, SPRITE OSD Interrupts

The VSYNC interrupt is an interrupt request synchronized with the vertical sync signal.

The OSD interrupt occurs after character block display to the CRT is completed.

The SPRITE OSD interrupt occurs at the completion of SPRITE display.

(2) INT1 to INT3 External Interrupts

The INT1 to INT3 interrupts are external interrupt inputs, the system detects that the level of a pin changes from LOW to HIGH or from HIGH to LOW, and generates an interrupt request. The input active edge can be selected by bits 3 to 5 of the interrupt input polarity register (address $00CD_{16}$) : when this bit is "0," a change from LOW to HIGH is detected; when it is "1," a change from HIGH to LOW is detected. Note that both bits are cleared to "0" at reset.

(3) Timers 1 to 4 Interrupts

An interrupt is generated by an overflow of timers 1 to 4.

Table 8.3.1 Interrupt Vector Addresses and Priority

Priority	Interrupt Source	Vector Addresses	Remarks
1	Reset	$FFFF_{16}$, $FFFE_{16}$	Non-maskable
2	OSD interrupt	$FFFD_{16}$, $FFFC_{16}$	
3	INT2 external interrupt	$FFFB_{16}$, $FFFA_{16}$	Active edge selectable
4	INT1 external interrupt	$FFF9_{16}$, $FFF8_{16}$	Active edge selectable
5	SPRITE OSD interrupt	$FFF7_{16}$, $FFF6_{16}$	
6	Timer 4 interrupt	$FFF5_{16}$, $FFF4_{16}$	
7	f(XIN)/4096 interrupt	$FFF3_{16}$, $FFF2_{16}$	
8	VSYNC interrupt	$FFF1_{16}$, $FFF0_{16}$	
9	Timer 3 interrupt	$FFEF_{16}$, $FFEE_{16}$	
10	Timer 2 interrupt	$FFED_{16}$, $FFEC_{16}$	
11	Timer 1 interrupt	$FFEB_{16}$, $FFEA_{16}$	
12	Serial I/O interrupt	$FFE9_{16}$, $FFE8_{16}$	
13	Multi-master I^2C-BUS interface interrupt	$FFE7_{16}$, $FFE6_{16}$	
14	INT3 external interrupt	$FFE5_{16}$, $FFE4_{16}$	Active edge selectable
15	A-D conversion interrupt	$FFE3_{16}$, $FFE2_{16}$	
16	BRK instruction interrupt	$FFDF_{16}$, $FFDE_{16}$	Non-maskable

(4) Serial I/O Interrupt

This is an interrupt request from the clock synchronous serial I/O function.

(5) f(XIN)/4096 Interrupt

The f (XIN)/4096 interrupt occurs regularly with a f(XIN)/4096 period. Set bit 0 of the PWM mode register 1 to “0.”

(6) Multi-master I2C-BUS Interface Interrupt

This is an interrupt request related to the multi-master I2C-BUS interface.

(7) A-D Conversion Interrupt

The A-D conversion interrupt occurs at the completion of A-D conversion.

(8) BRK Instruction Interrupt

This software interrupt has the least significant priority. It does not have a corresponding interrupt enable bit, and it is not affected by the interrupt disable flag I (non-maskable).

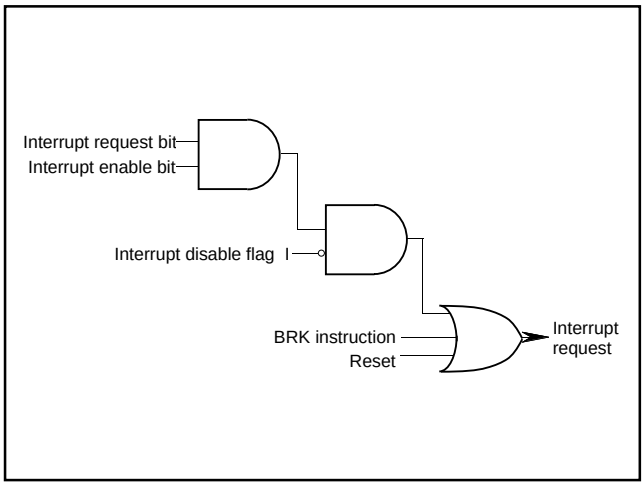


Fig. 8.3.1 Interrupt Control

Interrupt Request Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 1 (IREQ1) [Address 00FC16]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt request bit (TM1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
1	Timer 2 interrupt request bit (TM2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
2	Timer 3 interrupt request bit (TM3R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
3	Timer 4 interrupt request bit (TM4R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
4	OSD interrupt request bit (OSDR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
5	VSYNC interrupt request bit (VSCR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
6	Multi-master I2C-BUS interface interrupt request bit (IICR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
7	INT3 external interrupt request bit (IT3R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻

✻: "0" can be set by software, but "1" cannot be set.

Fig. 8.3.2 Interrupt Request Register 1

Interrupt Request Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 2 (IREQ2) [Address 00FD16]

B	Name	Functions	After reset	R	W
0	INT1 external interrupt request bit (IT1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
1	INT2 external interrupt request bit (IT2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
2	Serial I/O interrupt request bit (S1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
3	SPRITE OSD interrupt request bit (SPR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
4	f(XIN)/4096 interrupt request bit (MSR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
5	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—
6	A-D conversion interrupt request bit (ADR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
7	Fix this bit to "0."		0	R	W

✻: "0" can be set by software, but "1" cannot be set.

Fig. 8.3.3 Interrupt Request Register 2

Interrupt Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 1 (ICON1) [Address 00FE16]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt enable bit (TM1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	Timer 2 interrupt enable bit (TM2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Timer 3 interrupt enable bit (TM3E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3	Timer 4 interrupt enable bit (TM4E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
4	OSD interrupt enable bit (OSDE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
5	VSYNC interrupt enable bit (VSCE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
6	Multi-master I2C-BUS interface interrupt enable bit (IICE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
7	INT3 external interrupt enable bit (IT3E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W

Fig. 8.3.4 Interrupt Control Register 1

Interrupt Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 2 (ICON2) [Address 00FF16]

B	Name	Functions	After reset	R	W
0	INT1 external interrupt enable bit (IT1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	INT2 external interrupt enable bit (IT2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Serial I/O interrupt enable bit (S1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3	SPRITE OSD interrupt enable bit (SPE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
4	f(XIN)/4096 interrupt enable bit (MSE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
5	Fix this bit to “0.”		0	R	W
6	A-D conversion interrupt enable bit (ADE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—

Fig. 8.3.5 Interrupt Control Register 2

Interrupt Input Polarity Register

b7	b6	b5	b4	b3	b2	b1	b0
0	0				0		

Interrupt input polarity register (IP) [Address $00CD_{16}$]

b	Name	Function	After reset	R	W
0, 1	OSD clock selection bits (OCG0, OCG1)	b1 b0: 0 0 — The clock for OSD is supplied by connecting RC or LC across the pins OSC1 and OSC2. However, it is not corresponding to the bi-scan mode. 0 1 — Since the main clock is used as the clock for OSD, the oscillation frequency is limited. Because of this, the character size in width (horizonal) direction is also limited. In this case, pins OSC1 and OSC2 are also used as input ports $P3_3$ and $P3_4$ respectively. OSD oscillation frequency = $f(X_{IN})$ 1 0 — The clock for OSD is supplied by connecting LC across the pins OSC1 and OSC2. In the bi-scan mode, be sure to set this. 1 1 — The clock for OSD is supplied by connecting the following across the pins OSC1 and OSC2. However, it is not corresponding to the bi-scan mode. • a ceramic resonator only for OSD and a feedback resistor • a quartz-crystal oscillator only for OSD and a feedback resistor	0	R	W
2	Fix this bit to “0.”		0	R	W
3	INT1 polarity switch bit (POL1)	0 : Positive polarity 1 : Negative polarity	0	R	W
4	INT2 polarity switch bit (POL2)	0 : Positive polarity 1 : Negative polarity	0	R	W
5	INT3 polarity switch bit (POL3)	0 : Positive polarity 1 : Negative polarity	0	R	W
6, 7	Fix these bits to “0.”		0	R	W

Fig. 8.3.6 Interrupt Input Polarity Register

8.4 TIMERS

This microcomputer has 4 timers: timers 1 to 4. All timers are 8-bit timers with the 8-bit timer latch. The timer block diagram is shown in Figure 8.4.3.

All of the timers count down and their divide ratio is 1/(n+1), where n is the value of timer latch. By writing a count value to the corresponding timer latch (addresses $00F0_{16}$ to $00F3_{16}$: timers 1 to 4), the value is also set to a timer, simultaneously.

The count value is decremented by 1. The timer interrupt request bit is set to "1" by a timer overflow at the next count pulse, after the count value reaches "00_{16}."

8.4.1 Timer 1

Timer 1 can select one of the following count sources:

- f(X_{IN})/16
- f(X_{IN})/4096 or f(X_{CIN})/4096

The count source of timer 1 is selected by setting bit 0 of timer mode register 1 (address $00F4_{16}$).

Timer 1 interrupt request occurs at timer 1 overflow.

8.4.2 Timer 2

Timer 2 can select one of the following count sources:

- f(X_{IN})/16
- Timer 1 overflow signal
- External clock from the TIM2 pin

The count source of timer 2 is selected by setting bits 4 and 1 of timer mode register 1 (address $00F4_{16}$). When timer 1 overflow signal is a count source for the timer 2, the timer 1 functions as an 8-bit prescaler.

Timer 2 interrupt request occurs at timer 2 overflow.

8.4.3 Timer 3

Timer 3 can select one of the following count sources:

- f(X_{IN})/16
- External clock from the H_{SYNC} pin
- External clock from the TIM3 pin

The count source of timer 3 is selected by setting bits 5 and 0 of timer mode register 2 (address $00F5_{16}$).

Timer 3 interrupt request occurs at timer 3 overflow.

8.4.4 Timer 4

Timer 4 can select one of the following count sources:

- f(X_{IN})/16
- f(X_{IN})/2
- Timer 3 overflow signal

The count source of timer 3 is selected by setting bits 1 and 4 of timer mode register 2 (address $00F5_{16}$). When timer 3 overflow signal is a count source for the timer 4, the timer 3 functions as an 8-bit prescaler.

Timer 4 interrupt request occurs at timer 4 overflow.

At reset, timers 3 and 4 are connected by hardware and "FF_{16}" is automatically set in timer 3; "07_{16}" in timer 4. The f(X_{IN})/16 is selected as the timer 3 count source. The internal reset is released by timer 4 overflow in this state and the internal clock is connected.

At execution of the STP instruction, timers 3 and 4 are connected by hardware and "FF_{16}" is automatically set in timer 3; "07_{16}" in timer 4. However, the f(X_{IN})/16 is not selected as the timer 3 count source. So set both bit 0 of timer mode register 2 (address $00F5_{16}$) and bit 6 at address $00C7_{16}$ to "0" before execution of the STP instruction (f(X_{IN})/16 is selected as the timer 3 count source). The internal STP state is released by timer 4 overflow in this state and the internal clock is connected.

As a result of the above procedure, the program can start under a stable clock.

However, when setting "1" to bit 5 of timer mode register 1 (address $00F4_{16}$), timers 3 and 4 are not set the above value, the STP state is set by executing the STP instruction. This allows to program the time to return from the STP state.

The timer-related registers is shown in Figures 8.4.1 and 8.4.2.

Timer Mode Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Timer mode register 1 (TM1) [Address 00F4$_{16}$]

B	Name	Functions	After reset	R	W
0	Timer 1 count source selection bit 1 (TM10)	0: f(XIN)/16 1: f(XIN)/4096	0	R	W
1	Timer 2 count source selection bit 1 (TM11)	0: Interrupt clock source 1: External clock from TIM2 pin	0	R	W
2	Timer 1 count stop bit (TM12)	0: Count start 1: Count stop	0	R	W
3	Timer 2 count stop bit (TM13)	0: Count start 1: Count stop	0	R	W
4	Timer 2 internal count source selection bit 2 (TM14)	0: f(XIN)/16 1: Timer 1 overflow	0	R	W
5	<At execution of STP instruction> Timers 3 and 4 auto set disable bit (TM15)	0: Auto set enabled 1: Auto set disabled	0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Fig. 8.4.1 Timer Mode Register 1

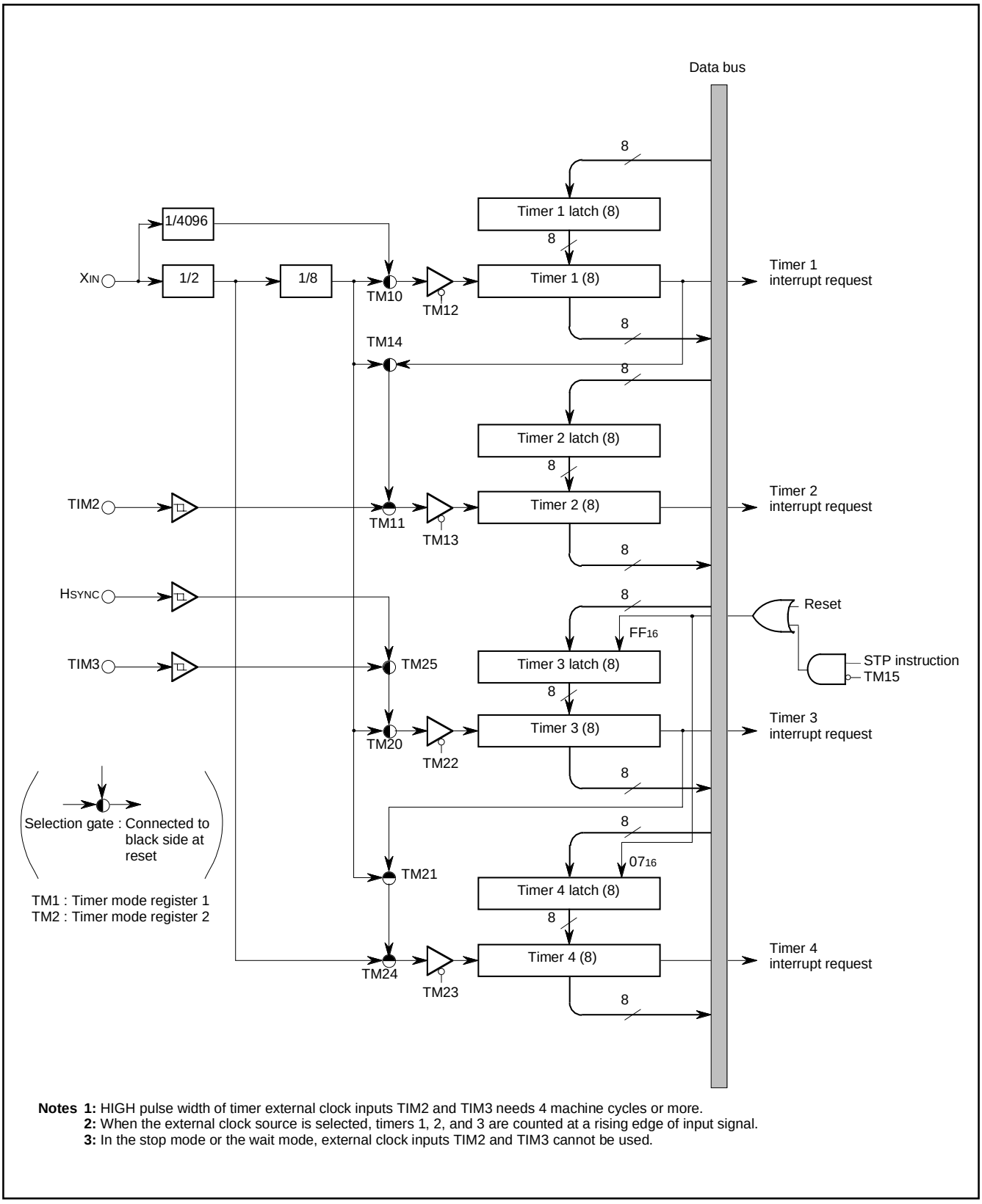
Timer Mode Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Timer mode register 2 (TM2) [Address 00F5$_{16}$]

B	Name	Functions	After reset	R	W
0	Timer 3 count source selection bit (TM20)	0 : f(XIN)/16 1 : External clock source	0	R	W
1	Timer 4 internal interrupt count source selection bit (TM21)	0 : Timer 3 overflow signal 1 : f(XIN)/16	0	R	W
2	Timer 3 count stop bit (TM22)	0: Count start 1: Count stop	0	R	W
3	Timer 4 count stop bit (TM23)	0: Count start 1: Count stop	0	R	W
4	Timer 4 count source selection bit (TM24)	0: Internal clock source 1: f(XIN)/2	0	R	W
5	Timer 3 external count source selection bit (TM25)	0: TIM3 pin input 1: HSYNC pin input	0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Fig. 8.4.2 Timer Mode Register 2



Notes 1: HIGH pulse width of timer external clock inputs TIM2 and TIM3 needs 4 machine cycles or more.
2: When the external clock source is selected, timers 1, 2, and 3 are counted at a rising edge of input signal.
3: In the stop mode or the wait mode, external clock inputs TIM2 and TIM3 cannot be used.

Fig. 8.4.3 Timer Block Diagram

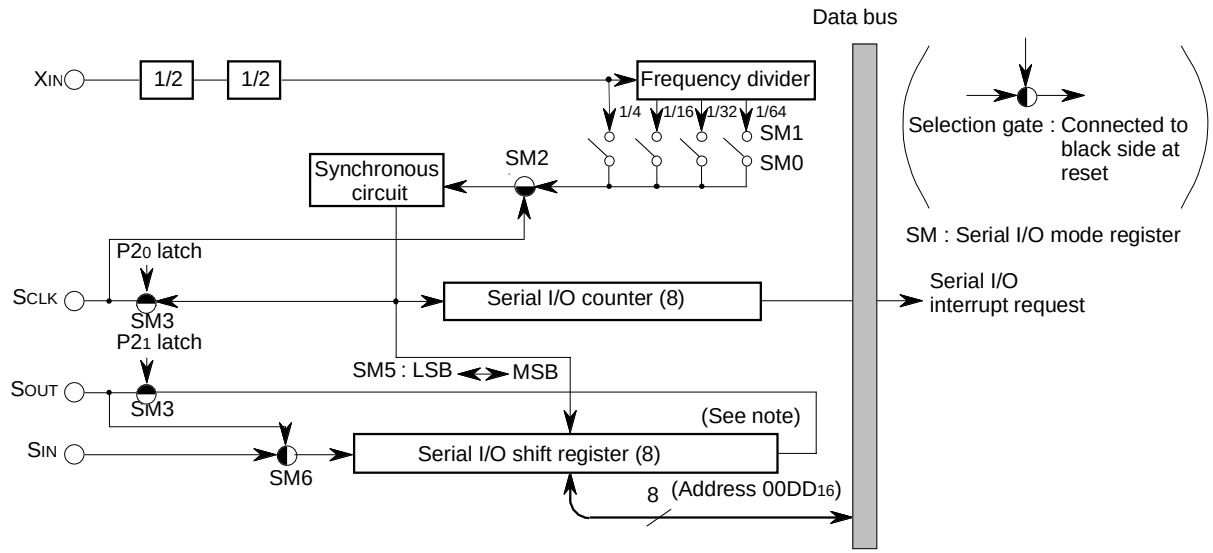
8.5 SERIAL I/O

This microcomputer has a built-in serial I/O which can either transmit or receive 8-bit data serially in the clock synchronous mode.

The serial I/O block diagram is shown in Figure 8.5.1. The synchronous clock I/O pin (SCLK), and data output pin (SOUT) also function as port P4, data input pin (SIN) also functions as port P2.

Bit 3 of the serial I/O mode register (address 00DC16) selects whether the synchronous clock is supplied internally or externally (from the SCLK pin). When an internal clock is selected, bits 1 and 0 select whether f(XIN) or f(XCIN) is divided by 4, 16, 32, or 64. To use SIN pin for serial I/O, set the corresponding bit of the port P2 direction register (address 00C516) to "0."

The operation of the serial I/O is described below. The operation of the serial I/O differs depending on the clock source; external clock or internal clock.



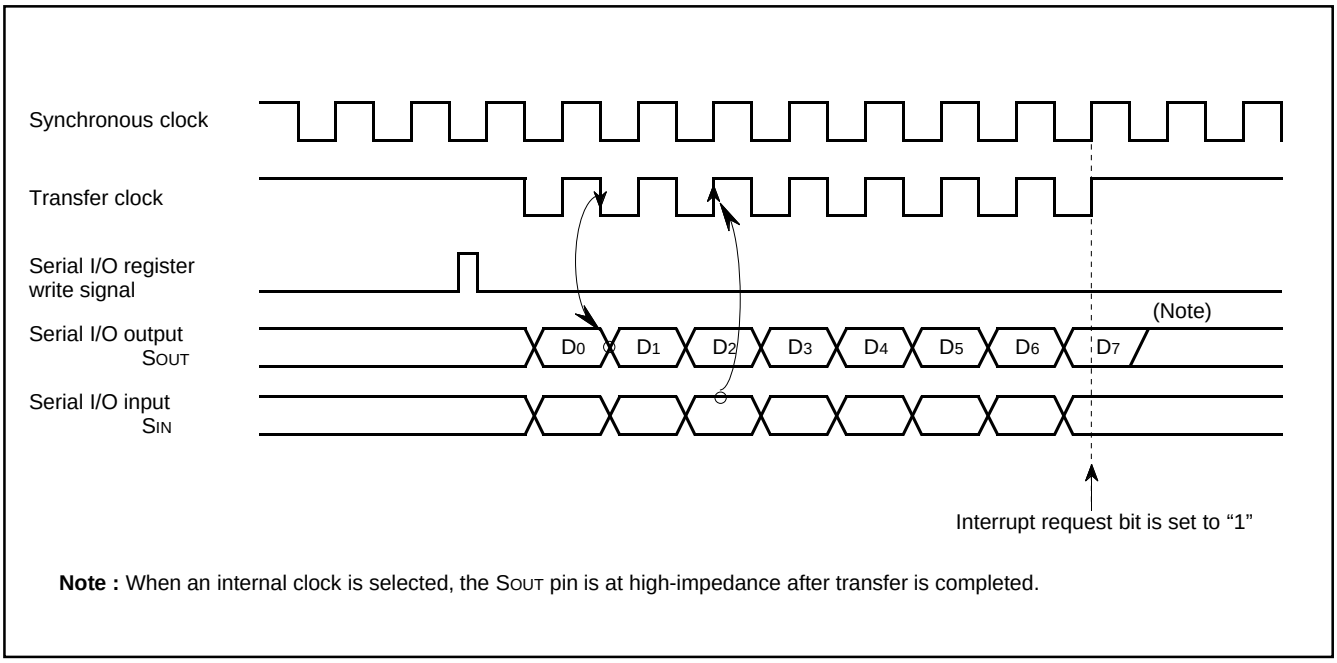
Note : When the data is set in the serial I/O register (address 00DD16), the register functions as the serial I/O shift register.

Fig. 8.5.1 Serial I/O Block Diagram

Internal clock : The serial I/O counter is set to “7” during the write cycle into the serial I/O register (address 00DD16), and the transfer clock goes HIGH forcibly. At each falling edge of the transfer clock after the write cycle, serial data is output from the SOUT pin. Transfer direction can be selected by bit 5 of the serial I/O mode register. At each rising edge of the transfer clock, data is input from the SIN pin and data in the serial I/O register is shifted 1 bit.
After the transfer clock has counted 8 times, the serial I/O counter becomes “0” and the transfer clock stops at HIGH. At this time the interrupt request bit is set to “1.”

External clock : The an external clock is selected as the clock source, the interrupt request is set to “1” after the transfer clock has been counted 8 counts. However, transfer operation does not stop, so the clock should be controlled externally. Use the external clock of 1 MHz or less with a duty cycle of 50%.
The serial I/O timing is shown in Figure 8.5.2. When using an external clock for transfer, the external clock must be held at HIGH for initializing the serial I/O counter. When switching between an internal clock and an external clock, do not switch during transfer. Also, be sure to initialize the serial I/O counter after switching.

Notes 1: On programming, note that the serial I/O counter is set by writing to the serial I/O register with the bit managing instructions, such as SEB and CLB.
2: When an external clock is used as the synchronous clock, write transmit data to the serial I/O register when the transfer clock input level is HIGH.



Note : When an internal clock is selected, the SOUT pin is at high-impedance after transfer is completed.

Fig. 8.5.2 Serial I/O Timing (for LSB first)

Serial I/O Mode Register

b7	b6	b5	b4	b3	b2	b1	b0
			0				

Serial I/O mode register (SM) [Address 00DC16]

B	Name	Functions	After reset	R	W
0, 1	Internal synchronous clock selection bits (SM0, SM1)	b1 b0 0 0: f(XIN)/4 0 1: f(XIN)/16 1 0: f(XIN)/32 1 1: f(XIN)/64	0	R	W
2	Synchronous clock selection bit (SM2)	0: External clock 1: Internal clock	0	R	W
3	Serial I/O port selection bit (SM3)	0: P20, P21 1: SCLK, SOUT	0	R	W
4	Fix this bit to “0.”		0	R	W
5	Transfer direction selection bit (SM5)	0: LSB first 1: MSB first	0	R	W
6	Serial input pin selection bit (SM6)	0: Input signal from SIN pin. 1: Input signal from SOUT pin.	0	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—

Fig. 8.5.3 Serial I/O Mode Register

8.5.1 Serial I/O Common Transmission/Reception mode

By writing “1” to bit 6 of the serial I/O mode register, signals SIN and SOUT are switched internally to be able to transmit or receive the serial data.

Figure 8.5.4 shows signals on serial I/O common transmission/reception mode.

Note: When receiving the serial data after writing “FF16” to the serial I/O register.

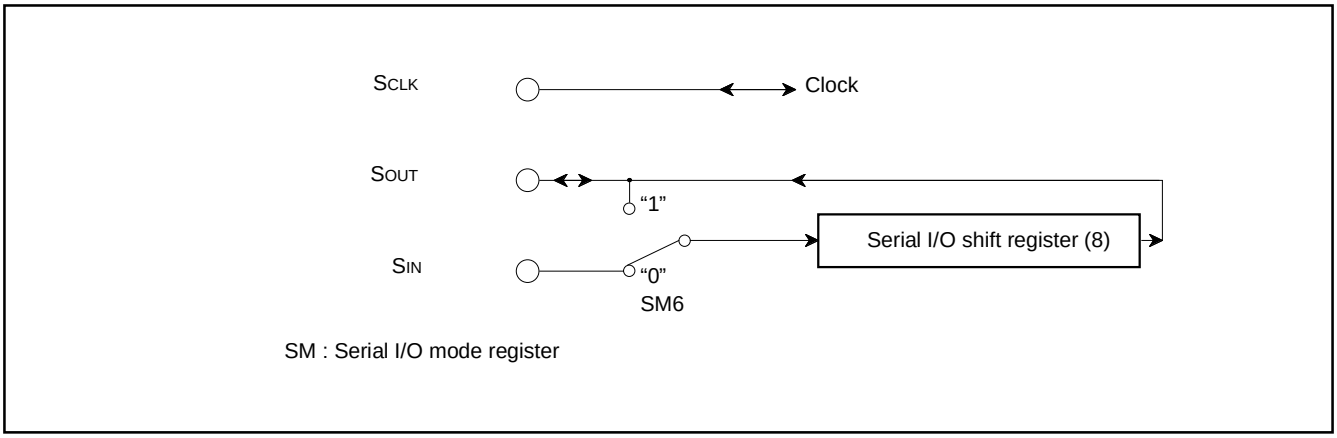


Fig. 8.5.4 Signals on Serial I/O Common Transmission/Reception Mode

8.6 MULTI-MASTER I²C-BUS INTERFACE

The multi-master I²C-BUS interface is a serial communications circuit, conforming to the Philips I²C-BUS data transfer format. This interface, offering both arbitration lost detection and a synchronous functions, is useful for the multi-master serial communications.

Figure 8.6.1 shows a block diagram of the multi-master I²C-BUS interface and Table 8.6.1 shows multi-master I²C-BUS interface functions.

This multi-master I²C-BUS interface consists of the I²C address register, the I²C data shift register, the I²C clock control register, the I²C control register, the I²C status register and other control circuits.

Table 8.6.1 Multi-master I²C-BUS Interface Functions

Item	Function
Format	In conformity with Philips I²C-BUS standard: 10-bit addressing format 7-bit addressing format High-speed clock mode Standard clock mode
Communication mode	In conformity with Philips I²C-BUS standard: Master transmission Master reception Slave transmission Slave reception
SCL clock frequency	16.1 kHz to 400 kHz (at ϕ = 4 MHz)

ϕ : System clock = f(XIN)/2

Note : We are not responsible for any third party's infringement of patent rights or other rights attributable to the use of the control function (bits 6 and 7 of the I²C control register at address 00DA16) for connections between the I²C-BUS interface and ports (SCL1, SCL2, SDA1, SDA2).

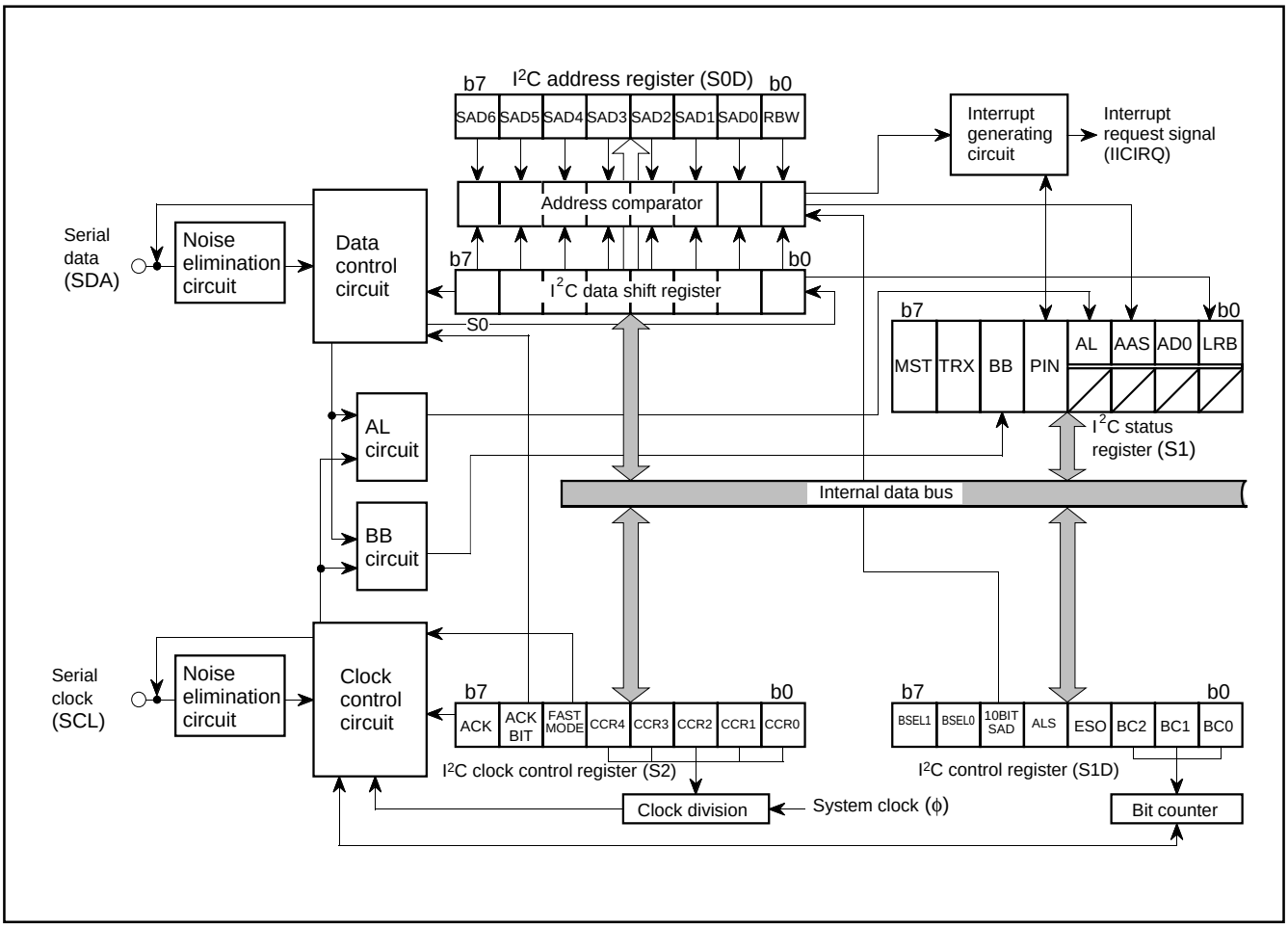


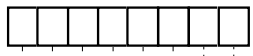
Fig. 8.6.1 Block Diagram of Multi-master I²C-BUS Interface

8.6.1 I²C Data Shift Register

The I²C data shift register (S0 : address 00D7₁₆) is an 8-bit shift register to store receive data and write transmit data.
When transmit data is written into this register, it is transferred to the outside from bit 7 in synchronization with the SCL clock, and each time one-bit data is output, the data of this register are shifted one bit to the left. When data is received, it is input to this register from bit 0 in synchronization with the SCL clock, and each time one-bit data is input, the data of this register are shifted one bit to the left.
The I²C data shift register is in a write enable status only when the ESO bit of the I²C control register (address 00DA₁₆) is "1." The bit counter is reset by a write instruction to the I²C data shift register. When both the ESO bit and the MST bit of the I²C status register (address 00D9₁₆) are "1," the SCL is output by a write instruction to the I²C data shift register. Reading data from the I²C data shift register is always enabled regardless of the ESO bit value.

Note: To write data into the I²C data shift register after setting the MST bit to "0" (slave mode), keep an interval of 8 machine cycles or more.

I²C Address Register



I²C address register (S0D) [Address 00D8₁₆]

B	Name	Functions	After reset	R	W
0	Read/write bit (RBW)	<Only in 10-bit addressing (in slave) mode> The last significant bit of address data is compared. 0: Wait the first byte of slave address after START condition (read state) 1: Wait the first byte of slave address after RESTART condition (write state)	0	R	—
1 to 7	Slave address (SAD0 to SAD6)	<In both modes> The address data is compared.	0	R	W

Fig. 8.6.2 Data Shift Register

8.6.2 I²C Address Register

The I²C address register (address 00D8₁₆) consists of a 7-bit slave address and a read/write bit. In the addressing mode, the slave address written in this register is compared with the address data to be received immediately after the START condition are detected.

(1) Bit 0: read/write bit (RBW)

Not used when comparing addresses, in the 7-bit addressing mode. In the 10-bit addressing mode, the first address data to be received is compared with the contents (SAD6 to SAD0 + RBW) of the I²C address register.
The RBW bit is cleared to "0" automatically when the stop condition is detected.

(2) Bits 1 to 7: slave address (SAD0–SAD6)

These bits store slave addresses. Regardless of the 7-bit addressing mode and the 10-bit addressing mode, the address data transmitted from the master is compared with the contents of these bits.

I²C Address Register

b7 b6 b5 b4 b3 b2 b1 b0

I²C address register (S0D) [Address 00D8₁₆]

B	Name	Functions	After reset	R	W
0	Read/write bit (RBW)	<Only in 10-bit addressing (in slave) mode> The last significant bit of address data is compared. 0: Wait the first byte of slave address after START condition (read state) 1: Wait the first byte of slave address after RESTART condition (write state)	0	R	—
1 to 7	Slave address (SAD0 to SAD6)	<In both modes> The address data is compared.	0	R	W

Fig. 8.6.3 I²C Address Register

8.6.3 I²C Clock Control Register

The I²C clock control register (address 00DB16) is used to set ACK control, SCL mode and SCL frequency.

(1) Bits 0 to 4: SCL frequency control bits (CCR0–CCR4)

These bits control the SCL frequency.

(2) Bit 5: SCL mode specification bit (FAST MODE)

This bit specifies the SCL mode. When this bit is set to "0," the standard clock mode is set. When the bit is set to "1," the high-speed clock mode is set.

(3) Bit 6: ACK bit (ACK BIT)

This bit sets the SDA status when an ACK clock* is generated. When this bit is set to "0," the ACK return mode is set and SDA goes to LOW at the occurrence of an ACK clock. When the bit is set to "1," the ACK non-return mode is set. The SDA is held in the HIGH status at the occurrence of an ACK clock.
However, when the slave address matches the address data in the reception of address data at ACK BIT = "0," the SDA is automatically made LOW (ACK is returned). If there is a mismatch between the slave address and the address data, the SDA is automatically made HIGH (ACK is not returned).

*ACK clock: Clock for acknowledgement

(4) Bit 7: ACK clock bit (ACK)

This bit specifies a mode of acknowledgment which is an acknowledgment response of data transmission. When this bit is set to "0," the no ACK clock mode is set. In this case, no ACK clock occurs after data transmission. When the bit is set to "1," the ACK clock mode is set and the master generates an ACK clock upon completion of each 1-byte data transmission.The device for transmitting address data and control data releases the SDA at the occurrence of an ACK clock (make SDA HIGH) and receives the ACK bit generated by the data receiving device.

Note: Do not write data into the I²C clock control register during transmission. If data is written during transmission, the I²C clock generator is reset, so that data cannot be transmitted normally.

I²C Clock Control Register

b7 b6 b5 b4 b3 b2 b1 b0

I²C clock control register (S2) [Address 00DB16]

B	Name	Functions			After reset	R	W
0 to 4	SCL frequency control bits (CCR0 to CCR4)	Setup value of CCR4–CCR0	Standard clock mode	High speed clock mode	0	R	W
		00 to 02	Setup disabled	Setup disabled			
		03	Setup disabled	333			
		04	Setup disabled	250			
		05	100	400 (See note)			
		06	83.3	166			
		⋮	500/CCR value	1000/CCR value			
		1D	17.2	34.5			
		1E	16.6	33.3			
		1F	16.1	32.3			
		(at ϕ = 4 MHz, unit : kHz)					
5	SCL mode specification bit (FAST MODE)	0: Standard clock mode 1: High-speed clock mode			0	R	W
6	ACK bit (ACK BIT)	0: ACK is returned. 1: ACK is not returned.			0	R	W
7	ACK clock bit (ACK)	0: No ACK clock 1: ACK clock			0	R	W

Note: At 400 kHz in the high-speed clock mode, the duty is as below .
"0" period : "1" period = 3 : 2
In the other cases, the duty is as below.
"0" period : "1" period = 1 : 1

Fig. 8.6.4 I²C Address Register

8.6.4 I²C Control Register

The I²C control register (address 00DA16) controls the data communication format.

(1) Bits 0 to 2: bit counter (BC0–BC2)

These bits decide the number of bits for the next 1-byte data to be transmitted. An interrupt request signal occurs immediately after the number of bits specified with these bits are transmitted.
When a START condition is received, these bits become "0002" and the address data is always transmitted and received in 8 bits.

(2) Bit 3: I²C interface use enable bit (ESO)

This bit enables usage of the multimaster I²C BUS interface. When this bit is set to "0," the use disable status is provided, so the SDA and the SCL become high-impedance. When the bit is set to "1," use of the interface is enabled.
When ESO = "0," the following is performed.

- PIN = "1," BB = "0" and AL = "0" are set (they are bits of the I²C status register at address 00D916).
- Writing data to the I²C data shift register (address 00D716) is disabled.

(3) Bit 4: data format selection bit (ALS)

This bit decides whether or not to recognize slave addresses. When this bit is set to "0," the addressing format is selected, so that address data is recognized. When a match is found between a slave address and address data as a result of comparison or when a general call (refer to "8.6.5 I²C Status Register," bit 1) is received, transmission processing can be performed. When this bit is set to "1," the free data format is selected, so that slave addresses are not recognized.

(4) Bit 5: addressing format selection bit (10BIT SAD)

This bit selects a slave address specification format. When this bit is set to "0," the 7-bit addressing format is selected. In this case, only the high-order 7 bits (slave address) of the I²C address register (address 00D816) are compared with address data. When this bit is set to "1," the 10-bit addressing format is selected, all the bits of the I²C address register are compared with address data.

(5) Bits 6 and 7: connection control bits between I²C-BUS interface and ports (BSEL0, BSEL1)

These bits controls the connection between SCL and ports or SDA and ports (refer to Figure 8.6.5).

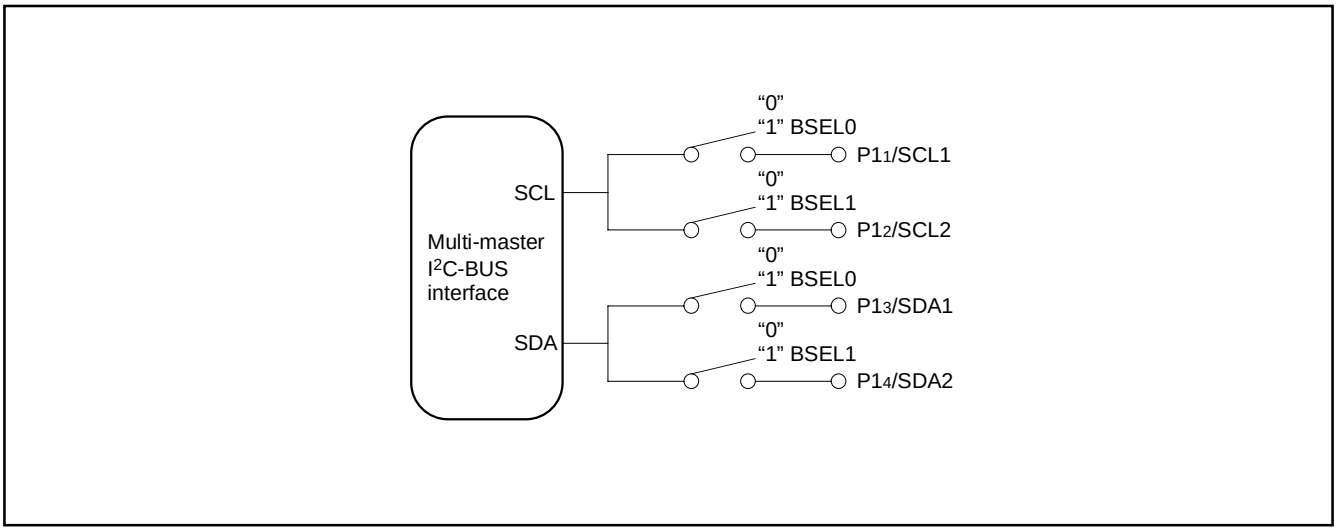


Fig. 8.6.5 Connection Port Control by BSEL0 and BSEL1

I²C Control Register

b7 b6 b5 b4 b3 b2 b1 b0

I²C control register (S1D) [Address 00DA16]

B	Name	Functions	After reset	R	W
0 to 2	Bit counter (Number of transmit/recieve bits) (BC0 to BC2)	b2 b1 b0 0 0 0: 8 0 0 1: 7 0 1 0: 6 0 1 1: 5 1 0 0: 4 1 0 1: 3 1 1 0: 2 1 1 1: 1	0	R	W
3	I²C-BUS interface use enable bit (ESO)	0: Disabled 1: Enabled	0	R	W
4	Data format selection bit(ALS)	0: Addressing format 1: Free data format	0	R	W
5	Addressing format selection bit (10BIT SAD)	0: 7-bit addressing format 1: 10-bit addressing format	0	R	W
6, 7	Connection control bits between I²C-BUS interface and ports (BSEL0, BSEL1)	b7 b6 Connection port (See note) 0 0: None 0 1: SCL1, SDA1 1 0: SCL2, SDA2 1 1: SCL1, SDA1, SCL2, SDA2	0	R	W

Note: When using ports P11-P14 as I²C-BUS interface, the output structure changes automatically from CMOS output to N-channel open-drain output.

Fig. 8.6.6 I²C Control Register

8.6.5 I²C Status Register

The I²C status register (address 00D9₁₆) controls the I²C-BUS interface status. The low-order 4 bits are read-only bits and the high-order 4 bits can be read out and written to.

(1) Bit 0: last receive bit (LRB)

This bit stores the last bit value of received data and can also be used for ACK receive confirmation. If ACK is returned when an ACK clock occurs, the LRB bit is set to "0." If ACK is not returned, this bit is set to "1." Except in the ACK mode, the last bit value of received data is input. The state of this bit is changed from "1" to "0" by executing a write instruction to the I²C data shift register (address 00D7₁₆).

(2) Bit 1: general call detecting flag (AD0)

This bit is set to "1" when a general call* whose address data is all "0" is received in the slave mode. By a general call of the master device, every slave device receives control data after the general call. The AD0 bit is set to "0" by detecting the STOP condition or START condition.

*General call: The master transmits the general call address "00₁₆" to all slaves.

(3) Bit 2: slave address comparison flag (AAS)

This flag indicates a comparison result of address data.

- In the slave receive mode, when the 7-bit addressing format is selected, this bit is set to "1" in one of the following conditions.
  - The address data immediately after occurrence of a START condition matches the slave address stored in the high-order 7 bits of the I²C address register (address 00D8₁₆).
  - A general call is received.
- In the slave reception mode, when the 10-bit addressing format is selected, this bit is set to "1" with the following condition.
  - When the address data is compared with the I²C address register (8 bits consists of slave address and RBW), the first bytes match.
- The state of this bit is changed from "1" to "0" by executing a write instruction to the I²C data shift register (address 00D7₁₆).

(4) Bit 3: arbitration lost* detecting flag (AL)

n the master transmission mode, when a device other than the microcomputer sets the SDA to "L,", arbitration is judged to have been lost, so that this bit is set to "1." At the same time, the TRX bit is set to "0," so that immediately after transmission of the byte whose arbitration was lost is completed, the MST bit is set to "0." When arbitration is lost during slave address transmission, the TRX bit is set to "0" and the reception mode is set. Consequently, it becomes possible to receive and recognize its own slave address transmitted by another master device.

*Arbitration lost: The status in which communication as a master is disabled.

(5) Bit 4: I²C-BUS interface interrupt request bit (PIN)

This bit generates an interrupt request signal. Each time 1-byte data is transmitted, the state of the PIN bit changes from "1" to "0." At the same time, an interrupt request signal is sent to the CPU. The PIN bit is set to "0" in synchronization with a falling edge of the last clock (including the ACK clock) of an internal clock and an interrupt request signal occurs in synchronization with a falling edge of the PIN bit. When detecting the STOP condition in slave, the multi-master I²C-BUS interface interrupt request bit (IR) is set to "0" (interrupt request) regardless of falling of PIN bit. When the PIN bit is "0," the SCL is kept in the "0" state and clock generation is disabled. Figure 8.6.8 shows an interrupt request signal generating timing chart.
The PIN bit is set to "1" in any one of the following conditions.

- Writing "1" to the PIN bit
- Executing a write instruction to the I²C data shift register (address 00D7₁₆).
- When the ESO bit is "0"
- At reset

Note: It takes 8 BCLK cycles or more until PIN bit become "1" after write instructions are executed to these registers.

The conditions in which the PIN bit is set to "0" are shown below:

- Immediately after completion of 1-byte data transmission (including when arbitration lost is detected)
- Immediately after completion of 1-byte data reception
- In the slave reception mode, with ALS = "0" and immediately after completion of slave address or general call address reception
- In the slave reception mode, with ALS = "1" and immediately after completion of address data reception

(6) Bit 5: bus busy flag (BB)

This bit indicates the status of use of the bus system. When this bit is set to "0," this bus system is not busy and a START condition can be generated. When this bit is set to "1," this bus system is busy and the occurrence of a START condition is disabled by the START condition duplication prevention function (See note).
This flag can be written by software only in the master transmission mode. In the other modes, this bit is set to "1" by detecting a START condition and set to "0" by detecting a STOP condition. When the ESO bit of the I²C control register (address 00DA₁₆) is "0" and at reset, the BB flag is kept in the "0" state.

(7) Bit 6: communication mode specification bit (transfer direction specification bit: TRX)

This bit decides the direction of transfer for data communication. When this bit is "0," the reception mode is selected and the data of a transmitting device is received. When the bit is "1," the transmission mode is selected and address data and control data are output into the SDA in synchronization with the clock generated on the SCL.
When the ALS bit of the I²C control register (address 00DA₁₆) is "0" in the slave reception mode is selected, the TRX bit is set to "1" (transmit) if the least significant bit (R/$\overline{W}$ bit) of the address data transmitted by the master is "1." When the ALS bit is "0" and the R/$\overline{W}$ bit is "0," the TRX bit is cleared to "0" (receive).
The TRX bit is cleared to "0" in one of the following conditions.

- When arbitration lost is detected.
- When a STOP condition is detected.
- When occurence of a START condition is disabled by the START condition duplication prevention function (Note).
- With MST = "0" and when a START condition is detected.
- With MST = "0" and when ACK non-return is detected.
- At reset

(8) Bit 7: Communication mode specification bit (master/slave specification bit: MST)

This bit is used for master/slave specification for data communication. When this bit is “0,” the slave is specified, so that a START condition and a STOP condition generated by the master are received, and data communication is performed in synchronization with the clock generated by the master. When this bit is “1,” the master is specified and a START condition and a STOP condition are generated, and also the clocks required for data communication are generated on the SCL.

The MST bit is cleared to “0” in one of the following conditions.

- Immediately after completion of 1-byte data transmission when arbitration lost is detected
- When a STOP condition is detected.
- When occurence of a START condition is disabled by the START condition duplication preventing function (Note).
- At reset

Note: The START condition duplication prevention function disables the START condition generation, reset of bit counter reset, and SCL output, when the following condition is satisfied:
a START condition is set by another master device.

I^2C Status Register

b7 b6 b5 b4 b3 b2 b1 b0

I^2C status register (S1) [Address $00D9_{16}$]

B	Name	Functions	After reset	R	W
0	Last receive bit (LRB) (See note)	0 : Last bit = “0 ” 1 : Last bit = “1 ” (See note)	Indeterminate	R	—
1	General call detecting flag (AD0) (See note)	0 : No general call detected 1 : General call detected (See note)	0	R	—
2	Slave address comparison flag (AAS) (See note)	0 : Address mismatch 1 : Address match (See note)	0	R	—
3	Arbitration lost detecting flag (AL) (See note)	0 : Not detected 1 : Detected (See note)	0	R	—
4	I^2C-BUS interface interrupt request bit (PIN)	0 : Interrupt request issued 1 : No interrupt request issued	1	R	W
5	Bus busy flag (BB)	0 : Bus free 1 : Bus busy	0	R	W
6, 7	Communication mode specification bits (TRX, MST)	b7 b6 0 0 : Slave recieve mode 0 1 : Slave transmit mode 1 0 : Master recieve mode 1 1 : Master transmit mode	0	R	W

Note : These bits and flags can be read out, but cannnot be written.

Fig. 8.6.7 I^2C Status Register

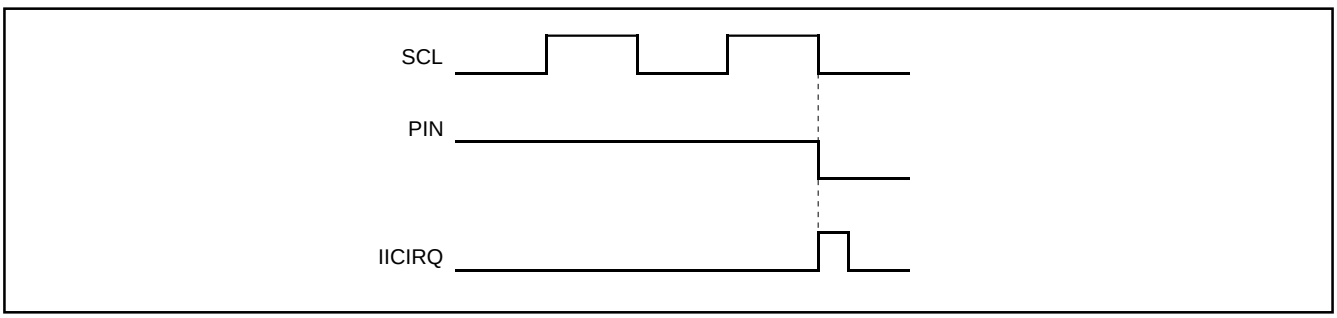


Fig. 8.6.8 Interrupt Request Signal Generation Timing

8.6.6 START Condition Generation Method

When the ESO bit of the I²C control register (address 00DA16) is "1," execute a write instruction to the I²C status register (address 00D916) to set the MST, TRX and BB bits to "1." A START condition will then be generated. After that, the bit counter becomes "0002" and an SCL for 1 byte is output. The START condition generation timing and BB bit set timing are different in the standard clock mode and the high-speed clock mode. Refer to Figure 8.6.9 for the START condition generation timing diagram, and Table 8.6.2 for the START condition/STOP condition generation timing table.

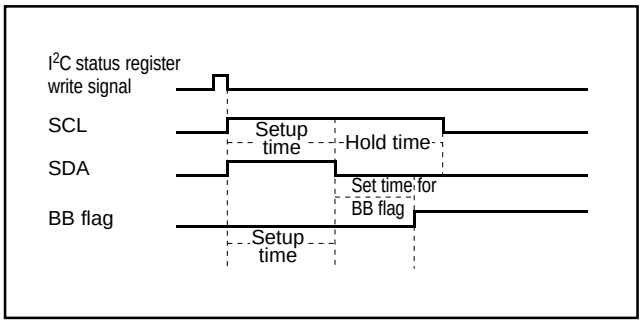


Fig. 8.6.9 START Condition Generation Timing Diagram

8.6.7 STOP Condition Generation Method

When the ESO bit of the I²C control register (address 00DA16) is "1," execute a write instruction to the I²C status register (address 00D916) for setting the MST bit and the TRX bit to "1" and the BB bit to "0". A STOP condition will then be generated. The STOP condition generation timing and the BB flag reset timing are different in the standard clock mode and the high-speed clock mode. Refer to Figure 8.6.10 for the STOP condition generation timing diagram, and Table 8.6.2 for the START condition/STOP condition generation timing table.

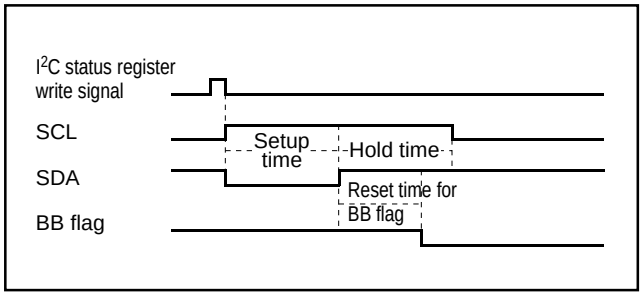


Fig. 8.6.10 STOP Condition Generation Timing Diagram

Table 8.6.2 START Condition/STOP Condition Generation Timing Table

Item	Standard Clock Mode	High-speed Clock Mode
Setup time (START condition)	5.0 µs (20 cycles)	2.5 µs (10 cycles)
Setup time (STOP condition)	4.25 µs (17 cycles)	1.75 µs (7 cycles)
Hold time	5.0 µs (20 cycles)	2.5 µs (10 cycles)
Set/reset time for BB flag	3.0 µs (12 cycles)	1.5 µs (6 cycles)

Note: Absolute time at ϕ = 4 MHz. The value in parentheses denotes the number of ϕ cycles.

8.6.8 START/STOP Condition Detect Conditions

The START/STOP condition detect conditions are shown in Figure 8.6.11 and Table 8.6.3. Only when the 3 conditions of Table 8.6.3 are satisfied, a START/STOP condition can be detected.

Note: When a STOP condition is detected in the slave mode (MST = 0), an interrupt request signal "IICIRQ" is generated to the CPU.

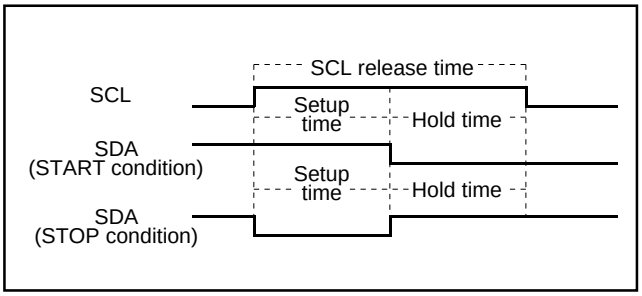


Fig. 8.6.11 START Condition/STOP Condition Detect Timing Diagram

Table 8.6.3 START Condition/STOP Condition Detect Conditions

Standard Clock Mode	High-speed Clock Mode
6.5 µs (26 cycles) < SCL release time	1.0 µs (4 cycles) < SCL release time
3.25 µs (13 cycles) < Setup time	0.5 µs (2 cycles) < Setup time
3.25 µs (13 cycles) < Hold time	0.5 µs (2 cycles) < Hold time

Note: Absolute time at ϕ = 4 MHz. The value in parentheses denotes the number of ϕ cycles.

8.6.9 Address Data Communication

There are two address data communication formats, namely, 7-bit addressing format and 10-bit addressing format. The respective address communication formats is described below.

(1) 7-bit addressing format

To meet the 7-bit addressing format, set the 10BIT SAD bit of the I^2C control register (address $00DA_{16}$) to "0." The first 7-bit address data transmitted from the master is compared with the high-order 7-bit slave address stored in the I^2C address register (address $00D8_{16}$). At the time of this comparison, address comparison of the RBW bit of the I^2C address register (address $00D8_{16}$) is not made. For the data transmission format when the 7-bit addressing format is selected, refer to Figure 8.6.12, (1) and (2).

(2) 10-bit addressing format

To meet the 10-bit addressing format, set the 10BIT SAD bit of the I^2C control register (address $00DA_{16}$) to "1." An address comparison is made between the first-byte address data transmitted from the master and the 7-bit slave address stored in the I^2C address register (address $00D8_{16}$). At the time of this comparison, an address comparison between the RBW bit of the I^2C address register (address $00D8_{16}$) and the R/$\overline{W}$ bit which is the last bit of the address data transmitted from the master is made. In the 10-bit addressing mode, the R/$\overline{W}$ bit which is the last bit of the address data not only specifies the direction of communication for control data but also is processed as an address data bit.

When the first-byte address data matches the slave address, the AAS bit of the I^2C status register (address $00D9_{16}$) is set to "1." After the second-byte address data is stored into the I^2C data shift register (address $00D7_{16}$), make an address comparison between the second-byte data and the slave address by software. When the address data of the 2nd bytes matches the slave address, set the RBW bit of the I^2C address register (address $00D8_{16}$) to "1" by software. This processing can match the 7-bit slave address and R/$\overline{W}$ data, which are received after a RESTART condition is detected, with the value of the I^2C address register (address $00D8_{16}$). For the data transmission format when the 10-bit addressing format is selected, refer to Figure 8.6.12, (3) and (4).

8.6.10 Example of Master Transmission

An example of master transmission in the standard clock mode, at the SCL frequency of 100 kHz and in the ACK return mode is shown below.

① Set a slave address in the high-order 7 bits of the I^2C address register (address $00D8_{16}$) and "0" in the RBW bit.
② Set the ACK return mode and SCL = 100 kHz by setting "85_{16}" in the I^2C clock control register (address $00DB_{16}$).
③ Set "10_{16}" in the I^2C status register (address $00D9_{16}$) and hold the SCL at the HIGH.
④ Set a communication enable status by setting "48_{16}" in the I^2C control register (address $00DA_{16}$).
⑤ Set the address data of the destination of transmission in the high-order 7 bits of the I^2C data shift register (address $00D7_{16}$) and set "0" in the least significant bit.
⑥ Set "$F0_{16}$" in the I^2C status register (address $00D9_{16}$) to generate a START condition. At this time, an SCL for 1 byte and an ACK clock automatically occurs.
⑦ Set transmit data in the I^2C data shift register (address $00D7_{16}$). At this time, an SCL and an ACK clock automatically occurs.
⑧ When transmitting control data of more than 1 byte, repeat step ⑦.
⑨ Set "$D0_{16}$" in the I^2C status register (address $00D9_{16}$). After this, if ACK is not returned or transmission ends, a STOP condition will be generated.

8.6.11 Example of Slave Reception

An example of slave reception in the high-speed clock mode, at the SCL frequency of 400 kHz, in the ACK non-return mode, using the addressing format, is shown below.

① Set a slave address in the high-order 7 bits of the I^2C address register (address $00D8_{16}$) and "0" in the RBW bit.
② Set the no ACK clock mode and SCL = 400 kHz by setting "25_{16}" in the I^2C clock control register (address $00DB_{16}$).
③ Set "10_{16}" in the I^2C status register (address $00D9_{16}$) and hold the SCL at the HIGH.
④ Set a communication enable status by setting "48_{16}" in the I^2C control register (address $00DA_{16}$).
⑤ When a START condition is received, an address comparison is made.
⑥ •When all transmitted address are"0" (general call):
AD0 of the I^2C status register (address $00D9_{16}$) is set to "1"and an interrupt request signal occurs.
•When the transmitted addresses match the address set in ①:
ASS of the I^2C status register (address $00D9_{16}$) is set to "1" and an interrupt request signal occurs.
•In the cases other than the above:
AD0 and AAS of the I^2C status register (address $00D9_{16}$) are set to "0" and no interrupt request signal occurs.
⑦ Set dummy data in the I^2C data shift register (address $00D7_{16}$).
⑧ When receiving control data of more than 1 byte, repeat step ⑦.
⑨ When a STOP condition is detected, the communication ends.

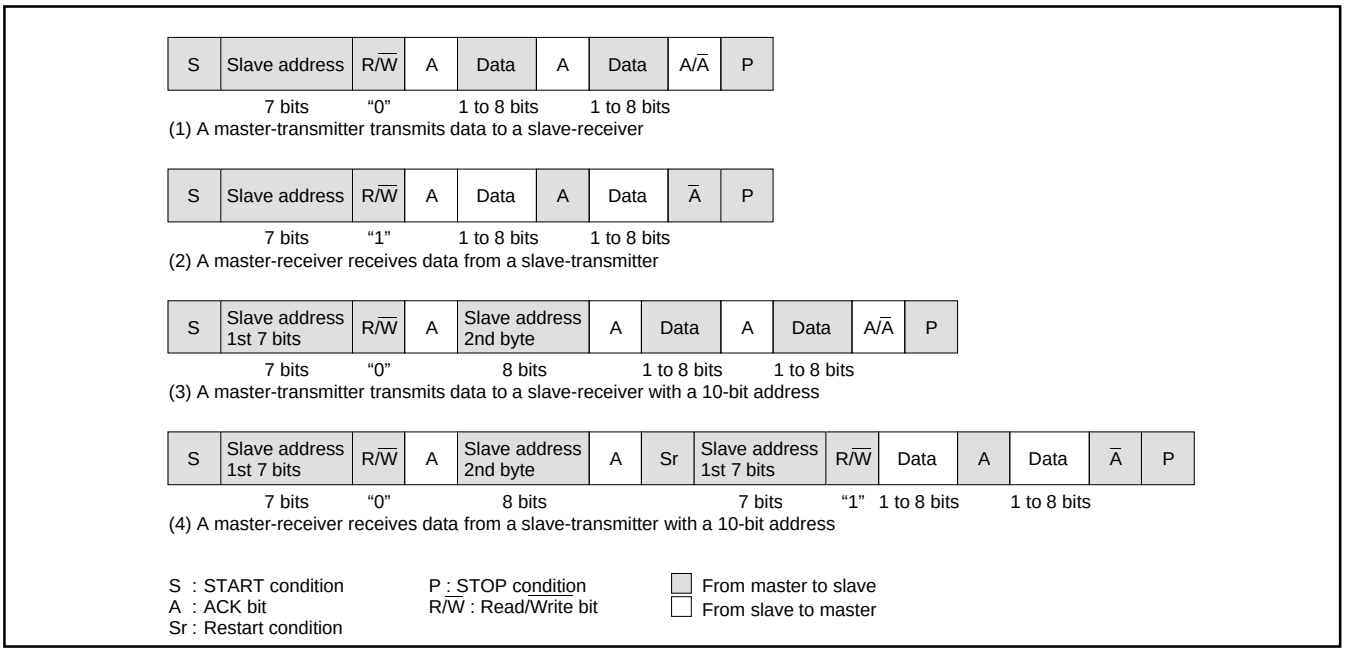


Fig. 8.6.12 Address Data Communication Format

8.6.12 Precautions when using multi-master I²C-BUS interface

(1) Read-modify-write instruction

The precautions when the raead-modify-write instruction such as SEB, CLB etc. is executed for each register of the multi-master I²C-BUS interface are described below.

•I²C data shift register (S0)

When executing the read-modify-write instruction for this register during transfer, data may become a value not intended.

•I²C address register (S0D)

When the read-modify-write instruction is executed for this register at detecting the STOP condition, data may become a value not intended. It is because hardware changes the read/write bit (RBW) at the above timing.

•I²C status register (S1)

Do not execute the read-modify-write instruction for this register because all bits of this register are changed by hardware.

•I²C control register (S1D)

When the read-modify-write instruction is executed for this register at detecting the START condition or at completing the byte transfer, data may become a value not intended. Because hardware changes the bit counter (BC0–BC2) at the above timing.

•I²C clock control register (S2)

The read-modify-write instruction can be executed for this register.

(2) START condition generating procedure using multi-master

①Procedure example (The necessary conditions of the generating procedure are described as the following ② to ⑤).

```
                •
                •
        LDA     —               (Taking out of slave address value)
        SEI                     (Interrupt disabled)
        BBS   5,S1,BUSBUSY      (BB flag confirming and branch process)
BUSFREE:
        STA   S0                (Writing of slave address value)
        LDM #$F0, S1            (Trigger of START condition generating)
        CLI                     (Interrupt enabled)
                •
                •
BUSBUSY:
        CLI                     (Interrupt enabled)
                •
                •
```

②Use "STA," "STX" or "STY" of the zero page addressing instruction for writing the slave address value to the I²C data shift register.

③Use "LDM" instruction for setting trigger of START condition generating.

④Write the slave address value of above ② and set trigger of START condition generating of above ③ continuously shown the above procedure example.

⑤Disable interrupts during the following three process steps:

- BB flag confirming
- Writing of slave address value
- Trigger of START condition generating

When the condition of the BB flag is bus busy, enable interrupts immediately.

(3) RESTART condition generating procedure

①Procedure example (The necessary conditions of the generating procedure are described as the following ② to ⑥.)

Execute the following procedure when the PIN bit is “0.”

```
        •
        •
LDM   #$00, S1     (Select slave receive mode)
LDA   —            (Taking out of slave address value)
SEI                (Interrupt disabled)
STA   S0           (Writing of slave address value)
LDM   #$F0, S1     (Trigger of RESTART condition generating)
CLI                (Interrupt enabled)
        •
        •
```

②Select the slave receive mode when the PIN bit is “0.” Do not write “1” to the PIN bit. Neither “0” nor “1” is specified for the writing to the BB bit.

The TRX bit becomes “0” and the SDA pin is released.

③The SCL pin is released by writing the slave address value to the I^2C data shift register. Use “STA,” “STX” or “STY” of the zero page addressing instruction for writing.

④Use “LDM” instruction for setting trigger of RESTART condition generating.

⑤Write the slave address value of above ③ and set trigger of RESTART condition generating of above ④ continuously shown the above procedure example.

⑥Disable interrupts during the following two process steps:

- Writing of slave address value
- Trigger of RESTART condition generating

(4) STOP condition generating procedure

①Procedure example (The necessary conditions of the generating procedure are described as the following ② to ④.)

```
        •
        •
SEI                (Interrupt disabled)
LDM   #$C0, S1     (Select master transmit mode)
NOP                (Set NOP)
LDM   #$D0, S1     (Trigger of STOP condition generating)
CLI                (Interrupt enabled)
        •
        •
```

②Write “0” to the PIN bit when master transmit mode is select.

③Execute “NOP” instruction after setting of master transmit mode. Also, set trigger of STOP condition generating within 10 cycles after selecting of master trasmit mode.

④Disable interrupts during the following two process steps:

- Select of master transmit mode
- Trigger of STOP condition generating

(5) Writing to I^2C status register

Do not execute an instruction to set the PIN bit to “1” from “0” and an instruction to set the MST and TRX bits to “0” from “1” simultaneously. It is because it may enter the state that the SCL pin is released and the SDA pin is released after about one machine cycle. Do not execute an instruction to set the MST and TRX bits to “0” from “1” simultaneously when the PIN bit is “1.” It is because it may become the same as above.

(6) Process of after STOP condition generating

Do not write data in the I^2C data shift register S0 and the I^2C status register S1 until the bus busy flag BB becomes “0” after generating the STOP condition in the master mode. It is because the STOP condition waveform might not be normally generated. Reading to the above registers do not have the problem.

8.7 PWM OUTPUT FUNCTION

This microcomputer is equipped with two 14-bit PWMs (DA1, DA2) and six 8-bit PWMs (PWM0–PWM5). DA1 and DA2 have a 14-bit resolution with the minimum resolution bit width of 0.25 μs and a repeat period of 4096 μs (for f(X_{IN}) = 8 MHz). PWM0–PWM5 have the same circuit structure and an 8-bit resolution with minimum resolution bit width of 4 μs and repeat period of 1024 μs (for f(X_{IN}) = 8 MHz).

Figure 8.7.1 shows the PWM block diagram. The PWM timing generating circuit applies individual control signals to DA1, DA2 and PWM0–PWM5 using f(X_{IN}) divided by 2 as a reference signal.

8.7.1 Data Setting

When outputting DA1, first set the high-order 8 bits to the DA1-H register (address $00CE_{16}$), then the low-order 6 bits to the DA1-L register (address $00CF_{16}$). When outputting DA1, first set the high-order 8 bits to the DA2-H register (address $024E_{16}$), then the low-order 6 bits to the DA2-L register (address $024F_{16}$). When outputting PWM0–PWM5, set 8-bit output data to the PWMi register (i means 0 to 5; addresses $00D0_{16}$ to $00D4_{16}$, $00F6_{16}$).

8.7.2 Transferring Data from Registers to PWM Circuit

Data transfer from the 8-bit PWM register to the 8-bit PWM circuit is executed at writing data to the register.

The signal output from the 8-bit PWM output pin corresponds to the contents of this register.

Also, data transfer from the DA1 register (addresses $00CE_{16}$ and $00CF_{16}$) to the 14-bit PWM circuit is executed at writing data to the DA1-L register (address $00CF_{16}$). Reading from the DA1-H register (address $00CE_{16}$) means reading this transferred data. Data transfer from the DA2 register (addresses $024E_{16}$ and $024F_{16}$) to the 14-bit PWM circuit is executed at writing data to the DA2-L register (address $024F_{16}$). Reading from the DA2-H register (address $024E_{16}$) means reading this transferred data. Accordingly, it is possible to confirm the data being output from the DAi (i = 1, 2) output pin by reading the DAi (i = 1, 2) register.

8.7.3 Operating of 8-bit PWM

The following explains PWM operation.

First, set the bit 0 of PWM output control register 1 (address $00D5_{16}$) to “0” (at reset, bit 0 is already set to “0” automatically), so that the PWM count source is supplied.

PWM0–PWM5 are also used as pins $P0_0$–$P0_5$, respectively. For PWM0–PWM5, set the corresponding bits of the ports P0 direction register to “1” (output mode). And select each output polarity by bit 3 of PWM output control register 2 (address $00D6_{16}$). Then, set bits 2 to 7 of PWM output control register 1 to “1” (PWM output).

The PWM waveform is output from the PWM output pins by setting these registers.

Figure 8.7.2 shows the 8-bit PWM timing. One cycle (T) is composed of 256 (2^8) segments. The 8 kinds of pulses, relative to the weight of each bit (bits 0 to 7), are output inside the circuit during 1 cycle. Refer to Figure 8.7.2 (a). The 8-bit PWM outputs waveform which is the logical sum (OR) of pulses corresponding to the contents of bits 0 to 7 of the 8-bit PWM register. Several examples are shown in Figure 8.7.2 (b). 256 kinds of output (HIGH area: 0/256 to 255/256) are selected by changing the contents of the PWM register. A length of entirely HIGH output cannot be output, i.e. 256/256.

8.7.4 Operating of 14-bit PWM

For DA1, as with 8-bit PWM, set the bit 0 of PWM output control register 1 (address $00D5_{16}$) to “0” (at reset, bit 0 is already set to “0” automatically), so that the PWM count source is supplied. Next, select the output polarity by bit 2 of PWM output control register 2 (address $00D6_{16}$). Then, the 14-bit PWM outputs from the DA1 output pin by setting bit 1 of PWM output control register 1 to “0” (at reset, this bit already set to “0” automatically) to select the DA1 output.

For DA2 as with DA1, set the bit 0 of PWM output control register 1 (address $00D5_{16}$) to “0” (at reset, bit 0 is already set to “0” automatically), so that PWM count source is supplied. Next, select the output polarity by bit 4 of PWM output control register 2 (address $00D6_{16}$). Then, the 14-bit PWM outputs from the DA2 output pin by setting bit 5 of PWM output control register 1 to “0” (at reset, this bit already set to “0” automatically) to select the DA2 output.

The output example of the 14-bit PWM is shown in Figure 8.7.3.

The 14-bit PWM divides the data of the DAi latch (i = 1, 2) into the low-order 6 bits and the high-order 8 bits.

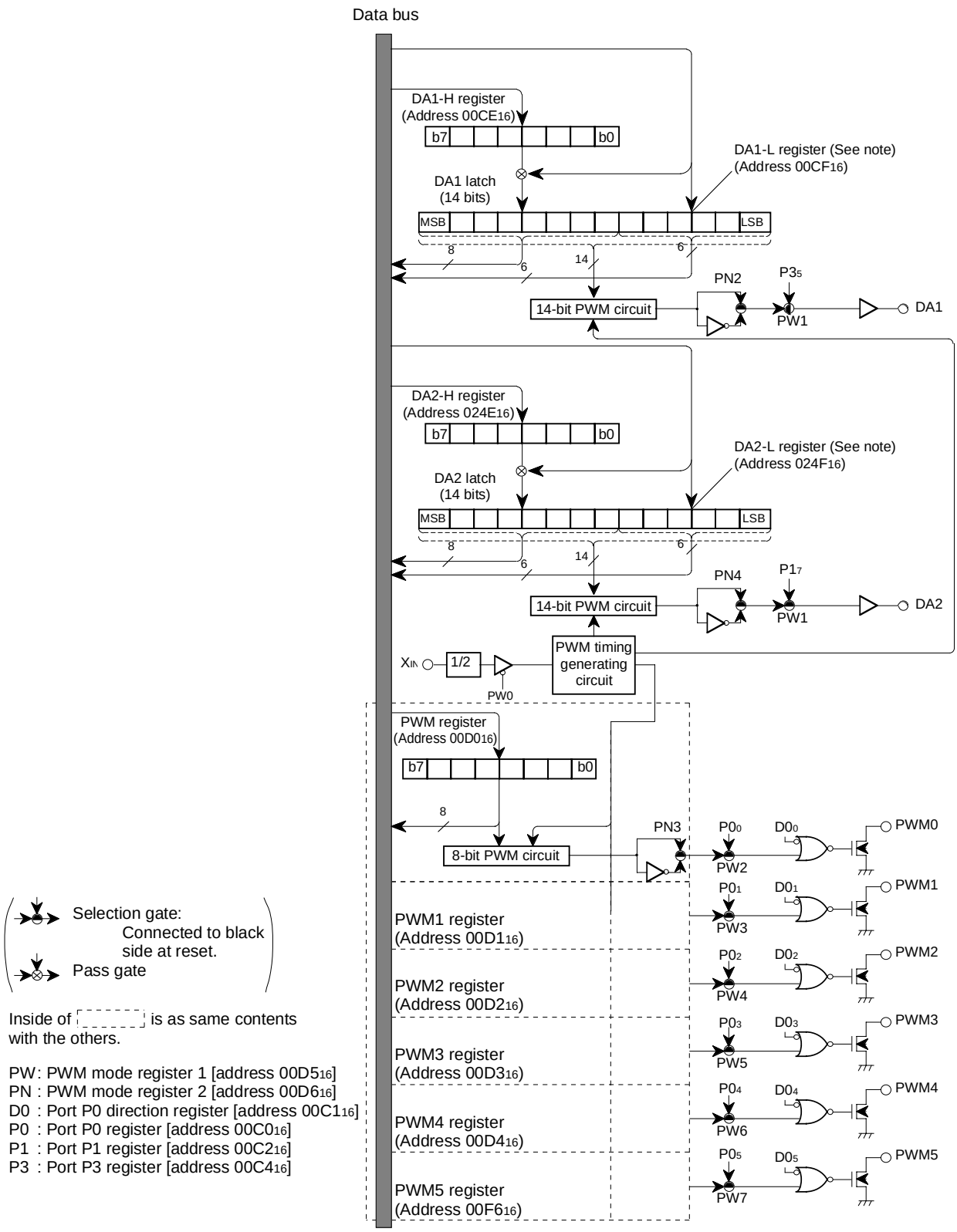
The fundamental waveform is determined with the high-order 8-bit data “D_H.” A HIGH area with a length t × D_H (HIGH area of fundamental waveform) is output every short area of “t” = 256τ = 64 μs (τ is the minimum resolution bit width of 250 ns). The HIGH level area increase interval (t_m) is determined with the low-order 6-bit data “D_L.” The HIGH are of smaller intervals “t_m” shown in Table 5 is longer by t than that of other smaller intervals in PWM repeat period “T” = 64t. Thus, a rectangular waveform with the different HIGH width is output from the DAi pins (i = 1, 2). Accordingly, the PWM output changes by τ unit pulse width by changing the contents of the DAi-H and DAi-L registers (i = 1, 2). A length of entirely HIGH cannot be output, i. e. 256/256.

8.7.5 Output after Reset

At reset, the output of ports $P0_0$–$P0_5$ and $P1_7$ are in the high-impedance state, and the contents of the PWM register and the PWM circuit are undefined. Note that after reset, the PWM output is undefined until setting the PWM register.

Table 8.7.1 Relation Between the Low-order 6-bit Data and High-level Area Increase Interval

Low-order 6 bits of Data	Area Longer by τ than That of Other t_m (m = 0 to 63)
0 0 0 0 0 0 (LSB)	Nothing
0 0 0 0 0 1	m = 32
0 0 0 0 1 0	m = 16, 48
0 0 0 1 0 0	m = 8, 24, 40, 56
0 0 1 0 0 0	m = 4, 12, 20, 28, 36, 44, 52, 60
0 1 0 0 0 0	m = 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62
1 0 0 0 0 0	m = 1, 3, 5, 7, ... 57, 59, 61, 63



Note: DAi-L register is also used as low-order 6 bits of DAi latch (i = 1, 2).

Fig. 8.7.1 PWM Block Diagram

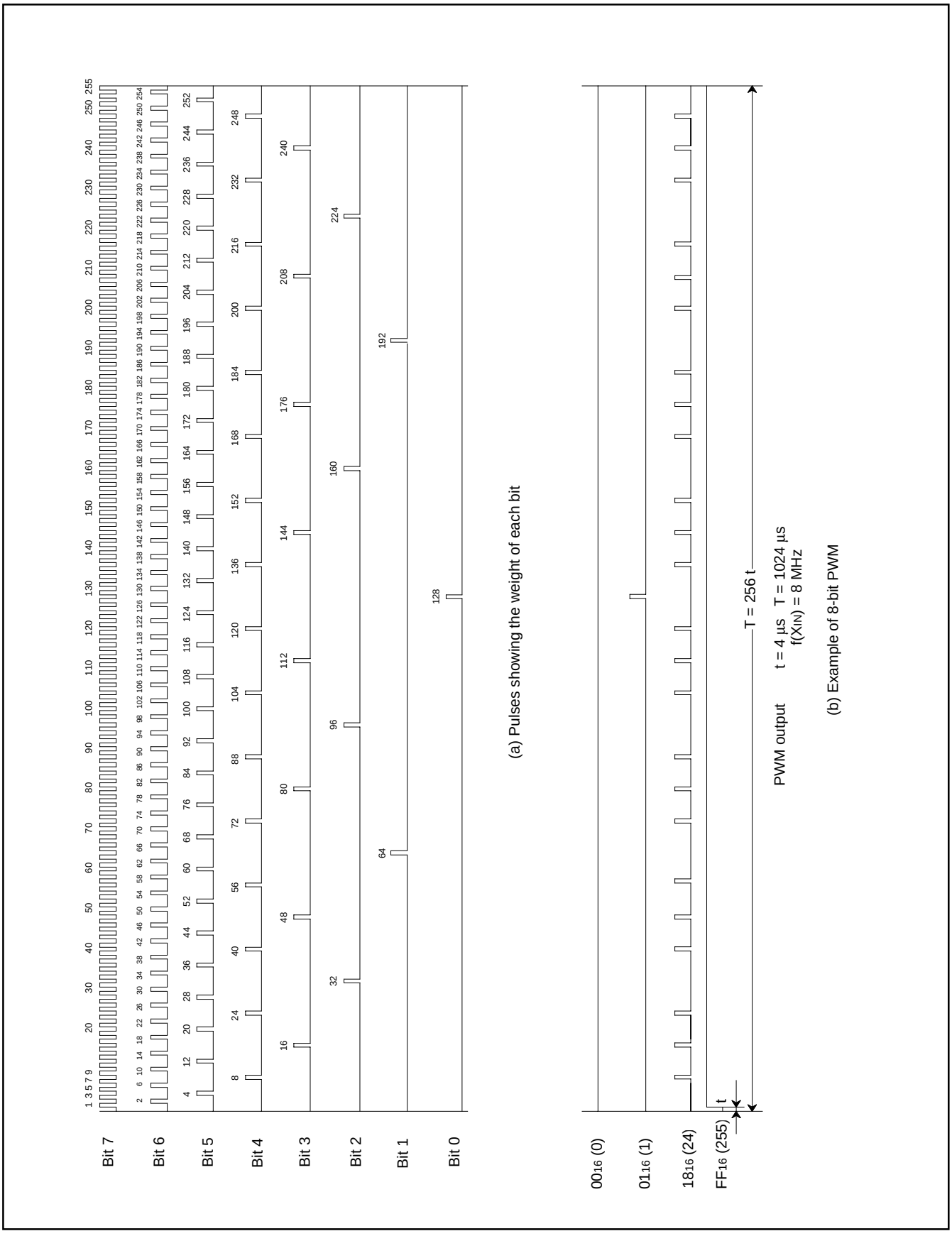
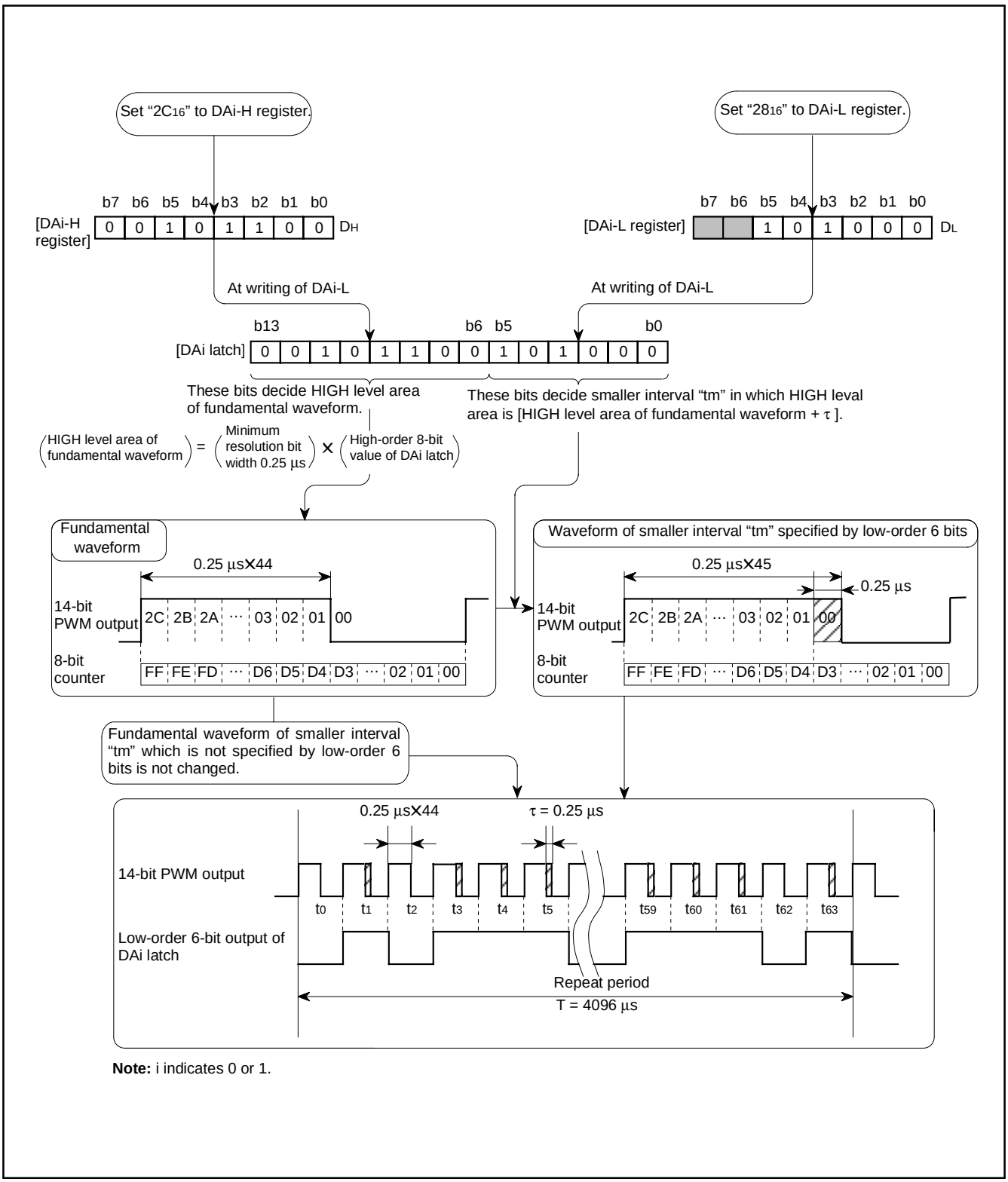


Fig. 8.7.2 PWM Timing



Note: i indicates 0 or 1.

Fig. 8.7.3 14-bit PWM Timing (f(XIN) = 8 MHz)

PWM Output Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

PWM output control register 1 (PW) [Address 00D5$_{16}$]

B	Name	Functions	After reset	R	W
0	DA1, DA2, PWM count source selection bit (PW0)	0 : Count source supply 1 : Count source stop	0	R	W
1	DA1 output/P3$_5$ selection bit (PW1)	0 : DA1 output 1 : P3$_5$ output	0	R	W
2	P0$_0$/PWM0 output selection bit (PW2)	0: P0$_0$ output 1: PWM0 output	0	R	W
3	P0$_1$/PWM1 output selection bit (PW3)	0: P0$_1$ output 1: PWM1 output	0	R	W
4	P0$_2$/PWM2 output selection bit (PW4)	0: P0$_2$ output 1: PWM2 output	0	R	W
5	P0$_3$/PWM3 output selection bit (PW5)	0: P0$_3$ output 1: PWM3 output	0	R	W
6	P0$_4$/PWM4 output selection bit (PW6)	0: P0$_4$ output 1: PWM4 output	0	R	W
7	P0$_5$/PWM5 output selection bit (PW7)	0: P0$_5$ output 1: PWM5 output	0	R	W

Fig. 8.7.4 PWM Output Control Register 1

PWM Output Control Register 2

b7 b6 b5 b4 b3 b2 b1 b0

0 0 0 0

PWM output control register 2 (PN) [Address 00D6$_{16}$]

B	Name	Functions	After reset	R	W
0, 1	Fix these bits to “0.”		0	R	W
2	DA1 output polarity selection bit (PN3)	0 : Positive polarity 1 : Negative polarity	0	R	W
3	PWM output polarity selection bit (PN4)	0 : Positive polarity 1 : Negative polarity	0	R	W
4	DA2 output polarity selection bit (PN5)	0 : Output LOW 1 : Output HIGH	0	R	W
5	P1$_7$/DA2 output selection bit (PN5)	0 : P1$_7$ 1 : DA2	0	R	W
6, 7	Fix these bits to “0.”		0	R	W

Fig. 8.7.5 PWM Output Control Register 2

8.8 A-D CONVERTER

8.8.1 A-D Conversion Register (AD)

A-D conversion reigister is a read-only register that stores the result of an A-D conversion. This register should not be read during A-D conversion.

8.8.2 A-D Control Register (ADCON)

The A-D control register controls A-D conversion. Bits 2 to 0 of this register select analog input pins. When these pins are not used as anlog input pins, they are used as ordinary I/O pins. Bit 3 is the A-D conversion completion bit, A-D conversion is started by writing “0” to this bit. The value of this bit remains at “0” during an A-D conversion, then changes to “1” when the A-D conversion is completed.

Bit 4 controls connection between the resistor ladder and V_{CC}. When not using the A-D converter, the resistor ladder can be cut off from the internal V_{CC} by setting this bit to “0,” accordingly providing low-power dissipation.

8.8.3 Comparison Voltage Generator (Resistor Ladder)

The voltage generator divides the voltage between V_{SS} and V_{CC} by 256, and outputs the divided voltages to the comparator as the reference voltage V_{ref}.

8.8.4 Channel Selector

The channel selector connects an analog input pin, selected by bits 2 to 0 of the A-D control register, to the comparator.

8.8.5 Comparator and Control Circuit

The conversion result of the analog input voltage and the reference voltage “V_{ref}” is stored in the A-D conversion register. The A-D conversion completion bit and A-D conversion interrupt request bit are set to “1” at the completion of A-D conversion.

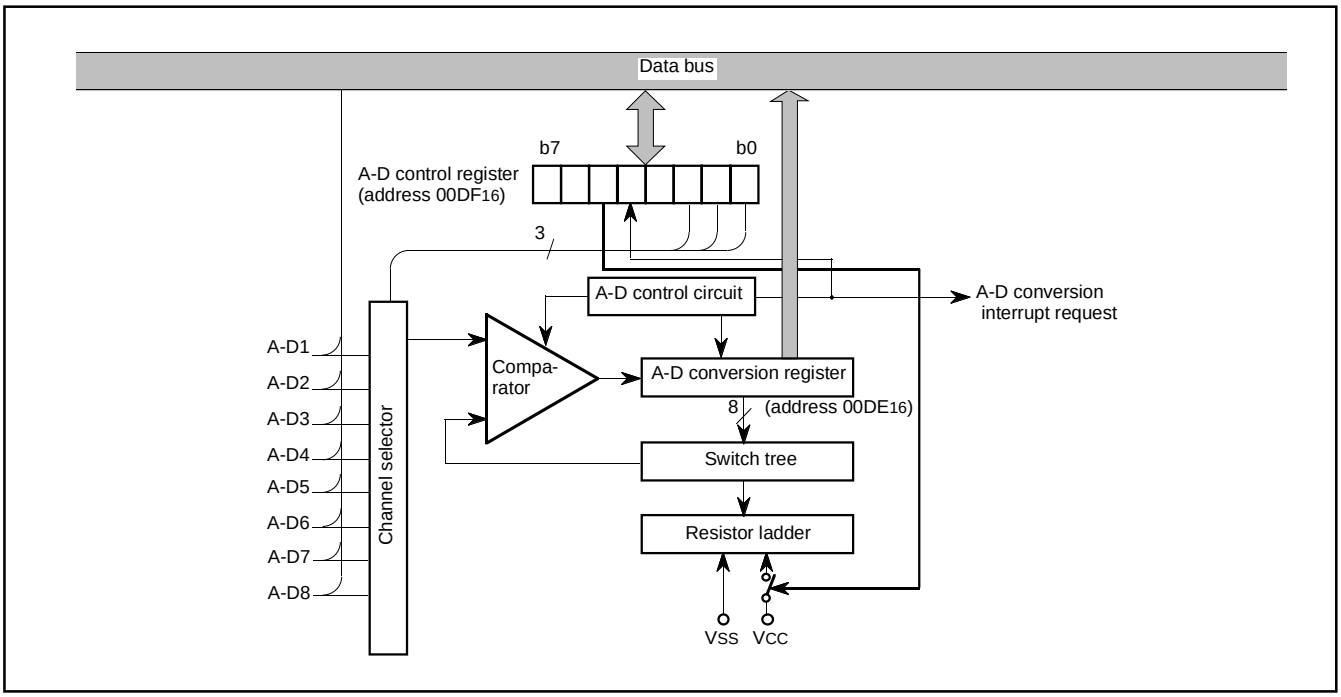


Fig. 8.8.1 A-D Converter Block Diagram

A-D Control Register

b7	b6	b5	b4	b3	b2	b1	b0
0		0					

A-D control register (ADCON) [Address 00DF16]

B	Name	Functions	After reset	R	W
0 to 2	Analog input pin selection bits (ADIN0 to ADIN2)	b2 b1 b0 0 0 0 : A-D1 0 0 1 : A-D2 0 1 0 : A-D3 0 1 1 : A-D4 1 0 0 : A-D5 1 0 1 : A-D6 1 1 0 : A-D7 1 1 1 : A-D8	0	R	W
3	A-D conversion completion bit (ADSTR)	0: Conversion in progress 1: Convertion completed	1	R	W
4	Vcc connection selection bit (ADVREF)	0: OFF 1: ON	0	R	W
5	Fix this bit to “0.”		0	R	W
6	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is indeterminate.		Indeterminate	R	—
7	Fix this bit to “0.”		0	R	W

Fig. 8.8.2 A-D Control Register

8.8.6 Conversion Method

① Set the A-D conversion interrupt request bit to “0” (even when A-D conversion is started, the A-D conversion interrupt reguest bit is not set to “0” automatically).
② When using A-D conversion interrupt, enable interrupts by setting A-D conversion interrupt enable bit to “1” and setting the interrupt disable flag to “0.”
③ Set the V_{CC} connection selection bit to “1” to connect V_{CC} to the resistor ladder.
④ Select analog input pins by the analog input selection bit of the A-D control register.
⑤ Set the A-D conversion completion bit to “0.” This write operation starts the A-D conversion. Do not read the A-D conversion register during the A-D conversion.
⑥ Verify the completion of the conversion by the state (“1”) of the A-D conversion completion bit, the state (“1”) of A-D conversion interrupt reguest bit, or the occurrence of an A-D conversion interrupt.
⑦ Read the A-D conversion register to obtain the conversion results.

Note : When the ladder resistor is disconnect from V_{CC}, set the V_{CC} connection selection bit to “0” between steps ⑥ and ⑦.

8.8.7 Internal Operation

When the A-D conversion starts, the following operations are automatically performed.

① The A-D conversion register is set to “00_{16}.”
② The most significant bit of the A-D conversion register becomes “1, ” and the comparison voltage “V_{ref}” is input to the comparator. At this point, V_{ref} is compared with the analog input voltage “V_{IN} .”
③ Bit 7 is determined by the comparison results as follows.
When $V_{ref} < V_{IN}$: bit 7 holds “1”
When $V_{ref} > V_{IN}$: bit 7 becomes “0”

With the above operations, the analog value is converted into a digital value. The A-D conversion terminates in a maximum of 50 machine cycles (8.5 µs at f(X_{IN}) = 8 MHz) after it starts, and the conversion result is stored in the A-D conversion register.

An A-D conversion interrupt request occurs at the same time as A-D conversion completion, the A-D conversion interrupt request bit becomes “1.” The A-D conversion completion bit also becomes “1.”

Table 8.8.1 Expression for V_{ref} and V_{REF}

A-D conversion register contents “n” (decimal notation)	Vref (V)
0	0
1 to 255	$\frac{V_{REF}}{256} \times (n - 0.5)$

Note: V_{REF} indicates the reference voltage (= Vcc).

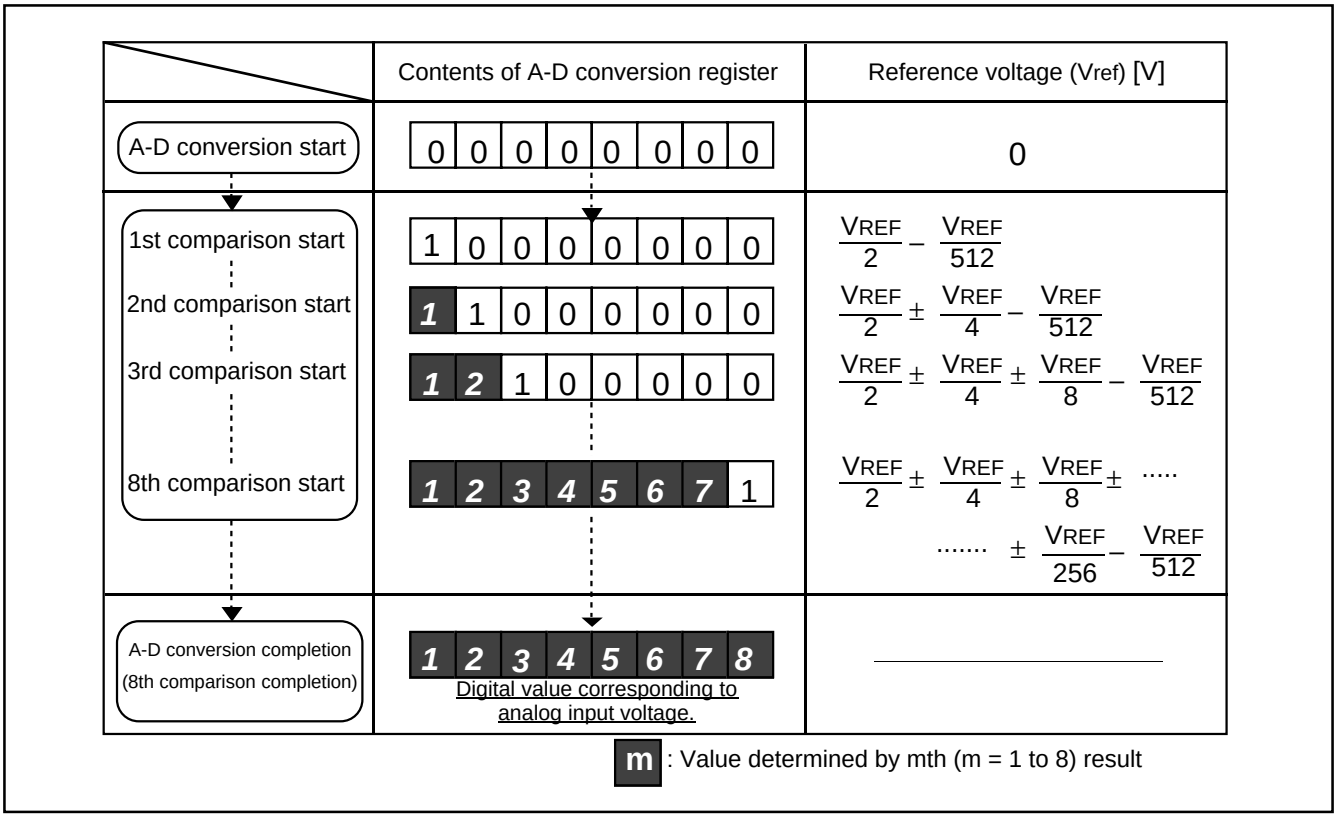


Fig. 8.8.3 Changes in A-D Conversion Register and Comparison Voltage during A-D Conversion

8.8.8 Definition of A-D Conversion Accuracy

The definition of A-D conversion accuracy is described below (refer to Figure 8.8.4).

(1) Relative Accuracy

•Zero transition error (V_{0T})

The deviation of the input voltage at which A-D conversion output data changes from "0" to "1," from the corresponding ideal A-D conversion characteristics between 0 and V_{REF}.

$$V_{0T} = \frac{(V_0 - 1/2 \times V_{REF}/256)}{1LSB} \quad [LSB]$$

• Full-scale transition error (V_{FST})

The deviation of the input voltage at which A-D conversion output data changes from "255" to "254," from the corresponding ideal A-D conversion characteristics between 0 and V_{REF}.

$$V_{FST} = \frac{(V_{REF} - 3/2 \times V_{REF}/256) - V_{254}}{1LSB} \quad [LSB]$$

• Non-linearity error

The deviation of the actual A-D conversion characteristics, from the ideal A-D conversion characteristics between V_0 and V_{254}.

$$\text{Non-linearity error} = \frac{V_n - (1LSB \times n + V_0)}{1LSB} \quad [LSB]$$

• EDifferential non-linearity error

The deviation of the input voltage required to change output data by "1," from the corresponding ideal A-D conversion characteristics between 0 and V_{REF}.

$$\text{Differential non-linearity error} = \frac{(V_{n+1} - V_n) - 1LSB}{1LSB} [LSB]$$

(2) Absolute Accuracy

• EAbsolute accuracy error

The deviation of the actual A-D conversion characteristics, from the ideal A-D conversion characteristics between 0 and V_{REF}.

$$\text{Absolute accuracy error} = \frac{V_n - 1LSB_A \times (n + 1/2)}{1LSB_A} \quad [LSB]$$

Note: The analog input voltage "Vn" at which A-D conversion output data changes from "n" to "n + 1" (n ; 0 to 254) is as follows (refer to Figure 8.8.4) :

$$1LSB \text{ with respect to relative accuracy} = \frac{V_{254} - V_0}{254} \quad [V]$$

$$1LSB_A \text{ with respect to absolute accuracy} = \frac{V_{REF}}{256} \quad [V]$$

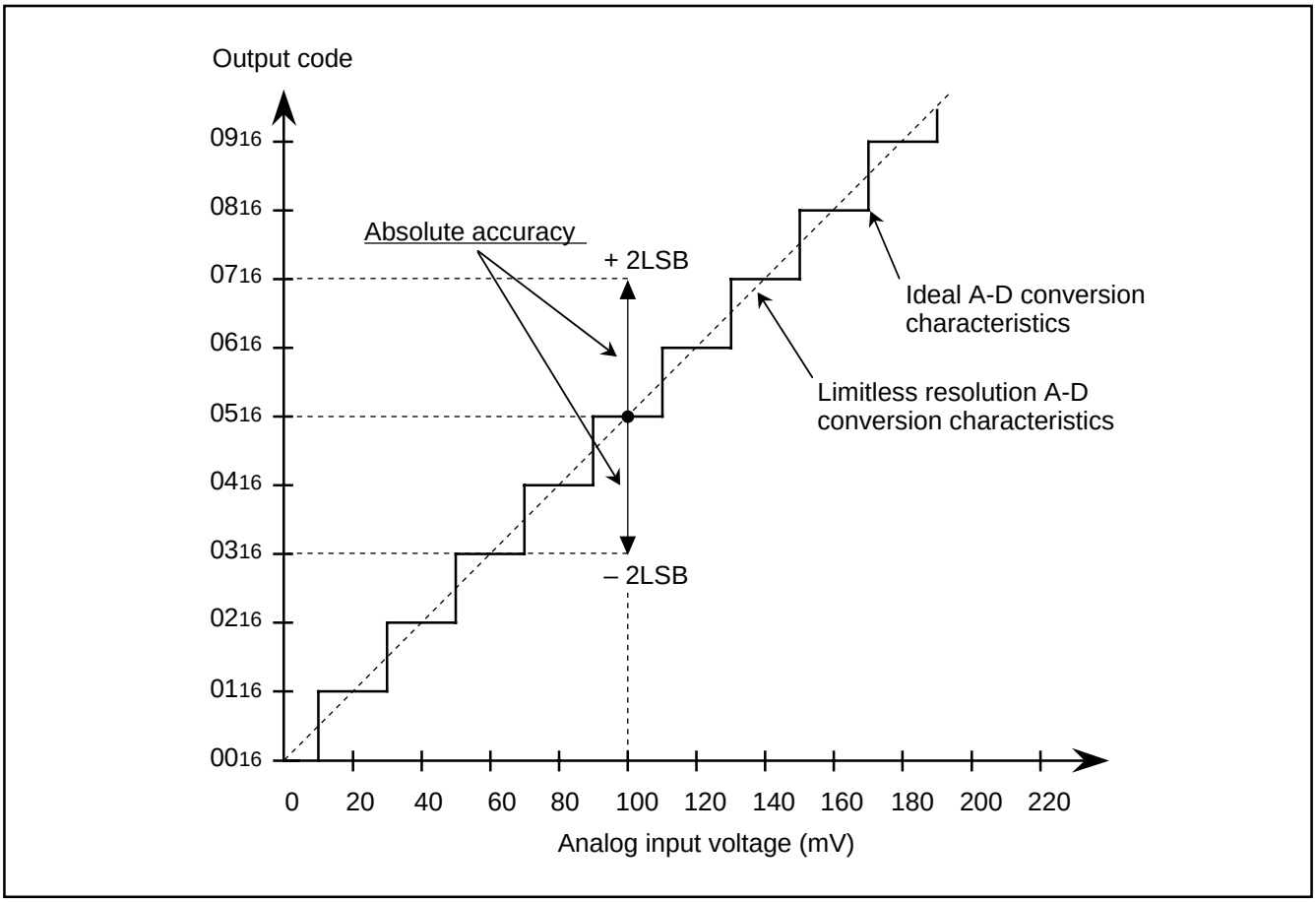


Fig. 8.8.4 Definition of A-D Conversion Accuracy

8.9 ROM CORRECTION FUNCTION

This can correct program data in ROM. Up to 3 addresses can be corrected, a program for correction is stored in the ROM correction vector in RAM as the top address. The ROM correction vectors are 3 vectors.

Vector 1 : address $02C0_{16}$
Vector 2 : address $02E0_{16}$
Vector 3 : address 0300_{16}

Set the address of the ROM data to be corrected into the ROM correction address register. When the value of the counter matches the ROM data address in the ROM correction vector as the top address, the main program branches to the correction program stored in the ROM memory for correction. To return from the correction program to the main program, the op code and operand of the JMP instruction (total of 3 bytes) are necessary at the end of the correction program. The ROM correction function is controlled by the ROM correction enable register.

Notes 1: Specify the first address (op code address) of each instruction as the ROM correction address.
2: Use the JMP instruction (total of 3 bytes) to return from the correction program to the main program.
3: Do not set the same ROM correction address to vectors 1 to 3.

ROM correction address 1 (high-order)	0217_{16}
ROM correction address 1 (low-order)	0218_{16}
ROM correction address 2 (high-order)	0219_{16}
ROM correction address 2 (low-order)	$021A_{16}$
ROM correction address 3 (high-order)	$021C_{16}$
ROM correction address 3 (low-order)	$021D_{16}$

Fig. 8.9.1 ROM Correction Address Registers

ROM Correction Enable Register

b7	b6	b5	b4	b3	b2	b1	b0
0	0	0	0	0			

ROM correction enable register (RCR) [Address $021B_{16}$]

B	Name	Functions	After reset	R	W
0	Vector 1 enable bit (RCR0)	0: Disabled 1: Enabled	0	R	W
1	Vector 2 enable bit (RCR1)	0: Disabled 1: Enabled	0	R	W
2	Vector 3 enable bit (RCR2)	0: Disabled 1: Enabled	0	R	W
3 to 7	Fix these bits to “0.”		0	R	W

Fig. 8.9.2 ROM Correction Enable Register

8.10 OSD FUNCTIONS

This OSD function can display the following 3 types:

- "Block display " (24 characters × 2 lines)
- "SPRITE display" (display only a character) or "Raster patterning display" (display a character on entire screen side by side)
- "Raster flat display" (coloring entire screen)

The above displays can be overlapped at the same time. The priority is :

SPRITE display > Block display > Raster flat display

or

Block display > Raster patterning display > Raster flat display

Note that raster patterning display and SPRITE display cannot be used simultaneously.

Figure 8.10.2 shows the block diagram of OSD circuit, Figure 8.10.3 shows the configuration of OSD character display area, Figure 8.10.4 shows the OSD control register.

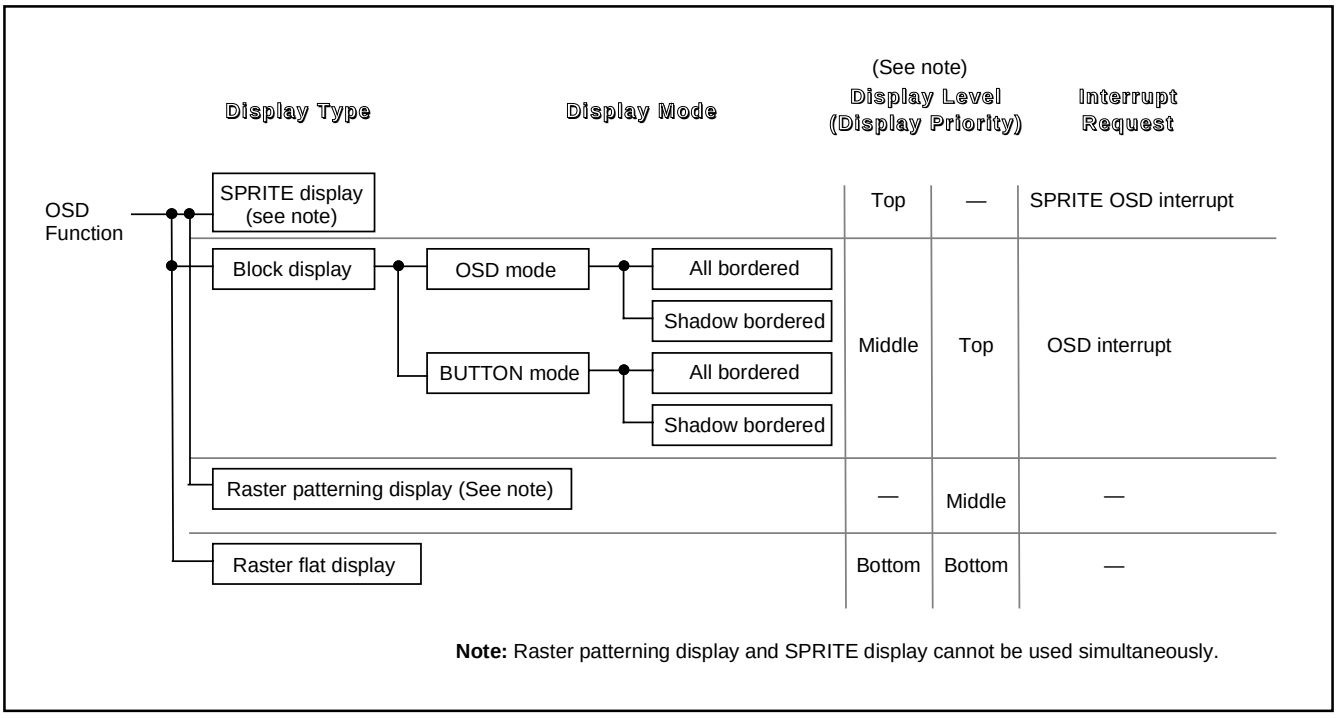


Fig. 8.10.1 Display Types of OSD Function

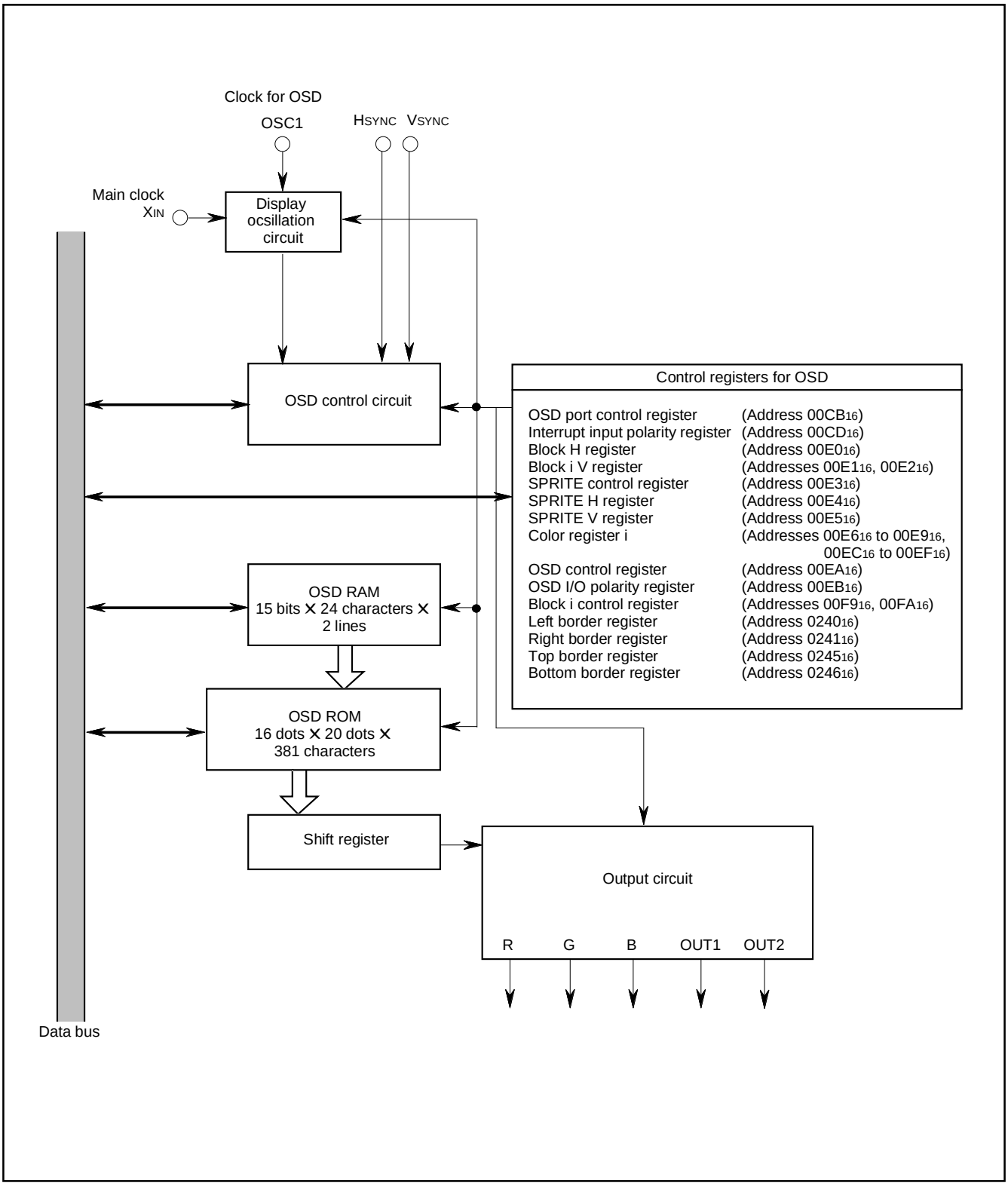


Fig. 8.10.2 Block Diagram of OSD Circuit

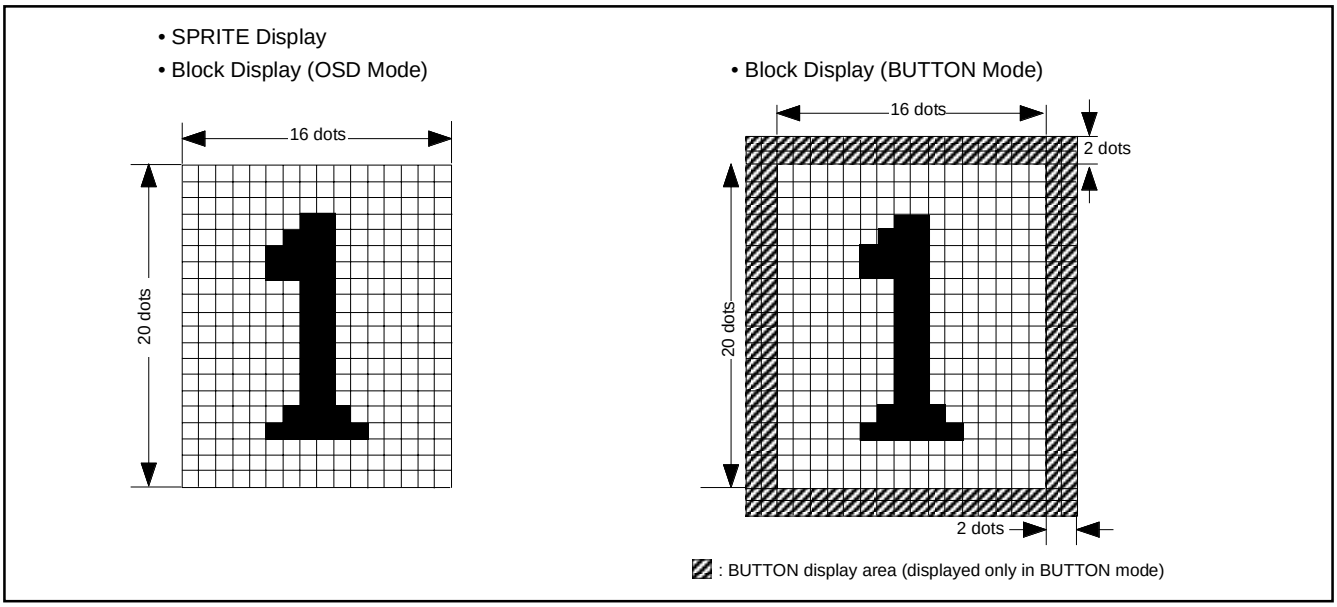


Fig. 8.10.3 Configuration of OSD Character Display Area

OSD Control Register

b7 b6 b5 b4 b3 b2 b1 b0

OSD control register (OC) [Address 00EA16]

B	Name	Functions	After reset	R	W
0	OSD control bit (OC0) (See note 1)	0 : All-blocks display OFF 1 : All-blocks display ON	0	R	W
1	Border type selection bit (OC1)	0 : All bordered 1 : Shadow bordered (See note 2)	0	R	W
2, 3	Window horizontal position minute adjustment bit (OC2, OC3)	b3 b2 (See notes 3 and 4) 0 0 : Standard 0 1 : Standard + 1TOSC 1 0 : Standard + 2TOSC 1 1 : Standard + 3TOSC	0	R	W
4	Window control bit (OC4)	0 : Window OFF 1 : Window ON	0	R	W
5	Scan mode selection bit (OC5)	0 : Normal scan mode 1 : Bi-scan mode (See note 5)	0	R	W
6	Raster color OUT1 control bit (OC6)	0 : No output 1 : Output	0	R	W
7	Raster color OUT2 control bit (OC7)	0 : No output 1 : Output	0	R	W

Notes 1 : Even this bit is switched during display, the display screen remains unchanged until a rising (falling) of the next VSYNC.
2 : Shadow border is output at right and bottom side of the font.
3 : TOSC = OSD oscillation cycle
4 : These bits are vallid for both left border and right border (for detail, refer to “(8) Window Function.”)
5 : When setting to bi-scan mode, connect LC between pins OSC1 and OSC2.

Fig. 8.10.4 OSD Control Register

(1) Clock for OSD

As a clock for display to be used for OSD, it is possible to select one of the following 3 types.

- Main clock from the pins XIN and XOUT
- Clock from the LC or RC oscillator supplied from the pins OSC1 and OSC2
- Clock from the ceramic resonator or the quartz-crystal oscillator from the pins OSC1 and OSC2

The clock for display to be used for OSD can be selected by bits 0 and 1 of the interrupt input polarity register (address $00CD_{16}$).
And besides, when selecting main clock, set the oscillation frequency to 8 MHz.

Interrupt Input Polarity Register

b7	b6	b5	b4	b3	b2	b1	b0
0	0				0		

Interrupt input polarity register (IP) [Address $00CD_{16}$]

b	Name	Function	After reset	R	W
0, 1	OSD clock selection bits (OCG0, OCG1)	b1 b0: 0 0 — The clock for OSD is supplied by connecting RC or LC across the pins OSC1 and OSC2. However, it is not corresponding to the bi-scan mode. 0 1 — Since the main clock is used as the clock for OSD, the oscillation frequency is limited. Because of this, the character size in width (horizonal) direction is also limited. In this case, pins OSC1 and OSC2 are also used as input ports $P3_3$ and $P3_4$ respectively. (OSD oscillation frequency = f(XIN)) 1 0 — The clock for OSD is supplied by connecting LC across the pins OSC1 and OSC2. In the bi-scan mode, be sure to set this. 1 1 — The clock for OSD is supplied by connecting the following across the pins OSC1 and OSC2. However, it is not corresponding to the bi-scan mode. • a ceramic resonator only for OSD and a feedback resistor • a quartz-crystal oscillator only for OSD and a feedback resistor	0	R	W
2	Fix this bit to "0."		0	R	W
3	INT1 polarity switch bit (POL1)	0 : Positive polarity 1 : Negative polarity	0	R	W
4	INT2 polarity switch bit (POL2)	0 : Positive polarity 1 : Negative polarity	0	R	W
5	INT3 polarity switch bit (POL3)	0 : Positive polarity 1 : Negative polarity	0	R	W
6, 7	Fix these bits to "0."		0	R	W

Fig. 8.10.5 Interrupt Input Polarity Register

(2) Scan mode

This microcomputer has the bi-scan mode for corresponding to HSYNC of double-speed frequency. In the bi-scan mode, the vertical start display position and the vertical dot size is two times as compared with the normal scan mode. The scan mode is selected by bit 5 of the OSD control register (refer to Figure 8.10.3).

Table 8.10.1 Setting for Scan Mode

Parameter \ Scan Mode	Normal Scan	Bi-Scan
Bit 5 of OSD Control Register	0	1
Vertical Display Start Position	Value of vertical position register × 1H	Value of vertical position register × 2H
Vertical Dot Size	1TOSC × 1H 2TOSC × 2H 3TOSC × 3H	1TOSC × 2H 2TOSC × 4H 3TOSC × 6H

Notes 1: TOSC = OSD oscillation cycle
2: H = HSYNC

(3) OSD input/output pin control

The OSD output pins R, G, B, OUT1 and OUT2 can also function as ports $P5_2$, $P5_3$, $P5_4$, $P5_5$, $P1_0$ respectively. Switch either OSD output function or port function by the OSD port control register (address $00CB_{16}$).

The input polarity of the HSYNC, VSYNC and output polarity of signals R, G, B, OUT1 and OUT2 can be specified with the OSD I/O polarity register (address $00EB_{16}$). Set a bit to "0" to specify positive polarity; set it to "1" to specify negative polarity.

Figure 8.10.6 shows the OSD I/O polarity register and Figure 8.10.7 shows the OSD port control register.

OSD I/O Polarity Register

b7 b6 b5 b4 b3 b2 b1 b0

OSD I/O polarity register (OPC) [Address $00EB_{16}$]

B	Name	Functions	After re	R	W
0	HSYNC input polarity switch bit (OPC0)	0 : Positive polarity input 1 : Negative polarity input	0	R	W
1	VSYNC input polarity switch bit (OPC1)	0 : Positive polarity input 1 : Negative polarity input	0	R	W
2	R/G/B output polarity switch bit (OPC2)	0 : Positive polarity output 1 : Negative polarity output	0	R	W
3	OUT1 output polarity switch bit (OPC3)	0 : Positive polarity output 1 : Negative polarity output	0	R	W
4	OUT2 output polarity switch bit (OPC4)	0 : Positive polarity output 1 : Negative polarity output	0	R	W
5	Raster color R control bit (OPC5)	0 : No output 1 : Output	0	R	W
6	Raster color G control bit (OPC6)	0 : No output 1 : Output	0	R	W
7	Raster color B control bit (OPC7)	0 : No output 1 : Output	0	R	W

Fig. 8.10.6 OSD I/O Polarity Register

OSD Port Control Register

b7 b6 b5 b4 b3 b2 b1 b0

0 0 0

OSD port control register (PF) [Address $00CB_{16}$]

b	Name	Functions	After reset	R	W
0, 1	Fix these bits to "0"		0	R	W
2	Port $P5_2$ output signal selection bit (P52SEL)	0 : R signal output 1 : Port $P5_2$ output	0	R	W
3	Port $P5_3$ output signal selection bit (P53SEL)	0 : G signal output 1 : Port $P5_3$ output	0	R	W
4	Port $P5_4$ output signal selection bit (P54SEL)	0 : B signal output 1 : Port $P5_4$ output	0	R	W
5	Port $P5_5$ output signal selection bit (P55SEL)	0 : OUT1 signal output 1 : Port $P5_5$ output	0	R	W
6	Port $P1_0$ output signal selection bit (OUT2SEL)	0 : Port $P1_0$ signal output 1 : OUT2 output	0	R	W
7	Fix this bit to "0"		0	R	W

Fig. 8.10.7 OSD Port Control Register

8.10.1 Block Display

There are 2 display modes and they are selected by a block unit. The display modes are selected by bits 0 to 2 of block i control register (i = 1, 2).
The features of each mode are described below.
There are an extended display mode. This mode allows multiple lines (3 lines or more) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Table 8.10.2 Features of Each Display Style of Block Display

Display style	Block display	
Parameter \ Display mode	OSD mode (On-screen display mode)	BUTTON mode (BUTTON display mode)
Number of display characters	24 characters × 2 lines	
Dot structure	16 × 20 dots	16 × 20 dots Character display area: (16 dots + 4 dots) × (20 dots + 4 dots)
Kinds of characters	381 kinds	
Kinds of character sizes	3 kinds	
Dot size	1TOSC × 1H, 2TOSC × 2H, 3TOSC × 3H (per block unit) (See notes 1, 2)	
Attribute	Border (per block unit)	■ Border (per block unit) ■ BUTTON display (per character unit) ■ Block shadow display (per character unit)
Character font coloring	1 screen: 8 kinds (per character unit)	
Character background coloring	1 screen: 8 kinds (per character unit)	
OSD output	R, G, B	
Raster coloring	Possible (per screen unit)	
Other functions	■ Corresponding to bi-scan ■ Window function (See note 3)	
Display position	Horizontal: 64 levels, Vertical: 255 levels	
Display expansion (multiline display)	Possible	

Notes 1: TOSC = OSD oscillation cycle
2: H = HSYNC
3: The SPRITE display is not effected by the window function.

Block i Control Register

b7 b6 b5 b4 b3 b2 b1 b0

Block i control register (BiC) (i = 1, 2) [Addresses 00F9$_{16}$, 00FA$_{16}$]

B	Name	Functions	After reset	R	W
0 to 2	Display mode selection bits (BiC0 to BiC2)	b2 b1 b0 — Display mode × 0 0 — Display OFF 0 0 1 — OSD mode (no border) 0 1 0 — BUTTON mode (no border) 1 0 1 — OSD mode (border) 1 1 0 — BUTTON mode (border)	Indeterminate	R	W
3, 4	Dot size selection bit (BiC3, BiC4)	b4 b3 — Dot size 0 0 — 1TOSC × 1H 0 1 — Do not set 1 0 — 2TOSC × 2H 1 1 — 3TOSC × 3H	Indeterminate	R	W
5 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Notes 1 : TOSC = OSD oscillation cycle
2 : H = HSYNC

Fig. 8.10.8 Block i Control Register (i = 1, 2)

(1) Display position

The display positions of characters are specified by a block. There are 2 blocks, blocks 1 and 2. Up to 24 characters can be displayed in each block (refer to “(3) Memory for OSD”).

The display position of each block can be set in both horizontal and vertical directions by software.

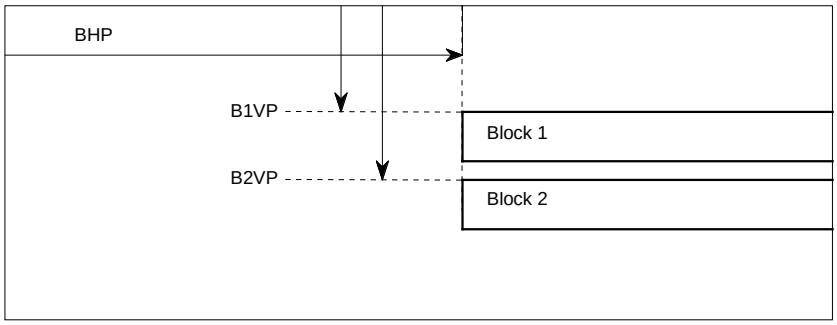
The display start position in the horizontal direction can be set for all blocks in common in 64-step display positions in units of 4TOSC (TOSC = OSD oscillation cycle).

The display start position in the vertical direction for each block can be set in 255-step display positions in units of 1 H (H = HSYNC cycle).

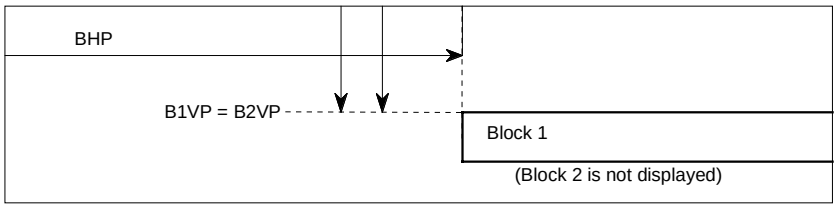
Blocks are displayed in conformance with the following rules:

- When the display position of block 1 is overlapped with block 2 (Figure 8.10.9 (b)), block 1 is displayed on the front.
- When another block display position appears while one block is . displayed (Figure 8.10.9 (c)), the block with a larger set value as the vertical display start position is displayed.

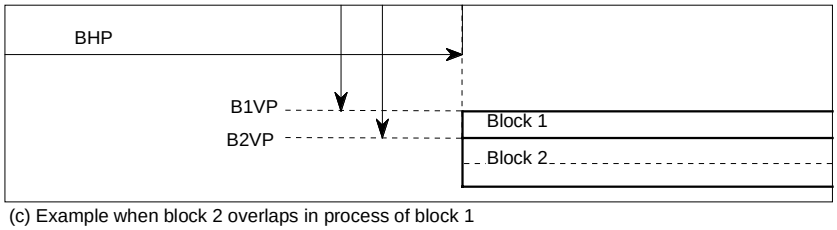
For the display position of SPRITE display, it is necessary to set independently, and it is possible to set display positions independently. Refer to “8.10.2 SPRITE Display.”



(a) Example when each block is separated



(b) Example when block 2 overlaps with block 1

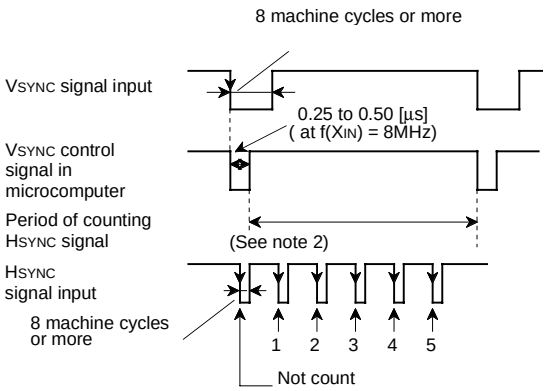


(c) Example when block 2 overlaps in process of block 1

Notes 1: B1VP or B2VP indicates the vertical display start position of display blocks 1 and 2.
2: BHP indicates the horizontal display start position of display blocks 1 and 2.

Fig. 8.10.9 Display Position

The vertical display start position is determined by counting the horizontal sync signal (HSYNC). At this time, when VSYNC and HSYNC are positive polarity (negative polarity), it starts to count the rising edge (falling edge) of HSYNC signal from after fixed cycle of rising edge (falling edge) of VSYNC signal. So interval from rising edge (falling edge) of VSYNC signal to rising edge (falling edge) of HSYNC signal needs enough time (2 machine cycles or more) for avoiding jitter. The polarity of HSYNC and VSYNC signals can select with the OSD I/O polarity register (address 00EB16).



When bits 0 and 1 of the I/O polarity control register (address 00EB16) are set to "1" (negative polarity)

Notes 1 : The vertical position is determined by counting falling edge of HSYNC signal after rising edge of VSYNC control signal in the microcomputer.
2 : Do not generate falling edge of HSYNC signal near rising edge of VSYNC control signal in microcomputer to avoid jitter.
3 : The pulse width of VSYNC and HSYNC needs 8 machine cycles or more.

Fig. 8.10.10 Supplement Explanation for Display Position

The vertical display start position for each block can be set in 255 steps (where each step is 1H (H: HSYNC cycle)) as values "0116" to "FF16" in block i V register (i = 1, 2) (addresses 00E116 to 00E216). When setting the block i V register to "0116," the display is started at 18H of count value of HSYNC signal. The vertical display start position here indicates the top position of character display area in OSD/BUTTON mode.
The block i V register is shown in Figures 8.10.11.

Block i V Register

b7 b6 b5 b4 b3 b2 b1 b0

Block i V register (BiVP) (i = 1, 2) [Addresses 00E116 and 00E216]

B	Name	Functions	After reset	R	W
0 to 7	Control bits of vertical display start positions (BiVP0 to BiVP7) (See note 1)	Vertical display start positions = Hdef + H × n (n: setting value, Hdef: 17H, H: HSYNC)	Indeterminate	R	W

Note: Set values except "0016" to BiVP.

Fig. 8.10.11 Block i V Register (i = 1, 2)

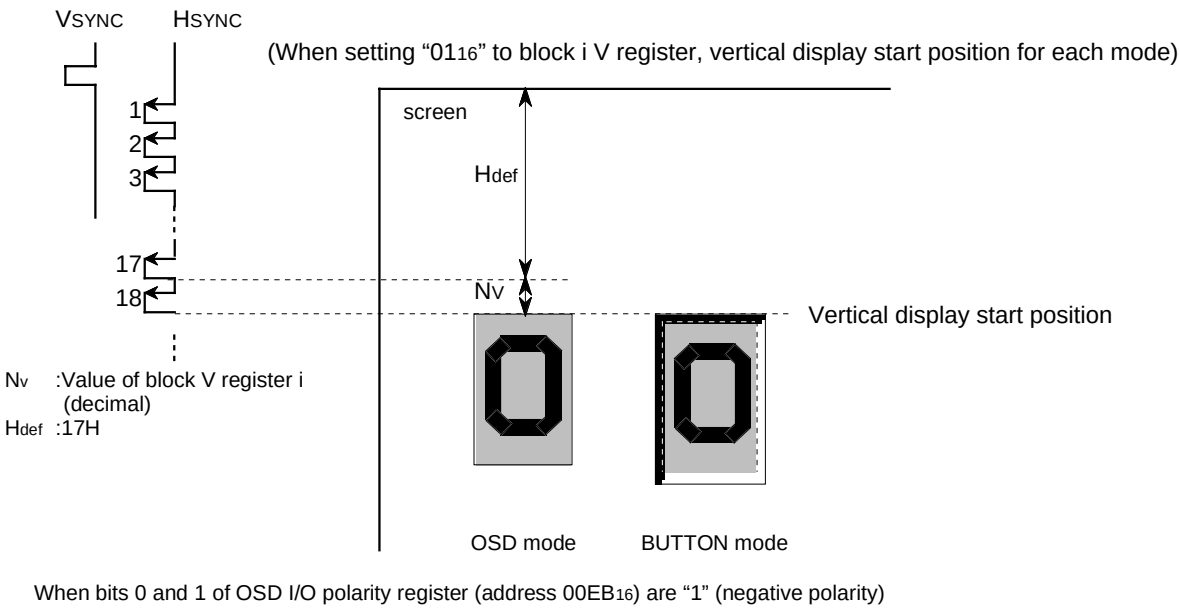


Fig. 8.10.12 Notes on Vertical Display Start Position

The horizontal display start position is common to all blocks, and can be set in 64 steps (where 1 step is 4TOSC, TOSC being the OSD oscillation cycle) as values "00₁₆" to "3F₁₆" in the block H register (address 00E0₁₆). The block H register is shown in Figure 8.10.13.

Block H Register

b7 b6 b5 b4 b3 b2 b1 b0

Horizontal position register (HP) [Address 00E0₁₆]

B	Name	Functions	After reset	R	W
0 to 5	Control bits of horizontal display start positions (BHP0 to BHP5) (See note 1)	Horizontal display start positions = T_{def1} + 4TOSC X n (n: setting value, T_{def1}: 31TOSC, TOSC: OSD oscillation cycle)	0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Note: The setting value synchronizes with the VSYNC.

Fig. 8.10.13 Block H Register

When setting the block H register to "00$_{16}$," it needs 31T_{OSC} (= T_{def1}) from a rising edge (negative polarity) of H_{SYNC} signal to horizontal display start position. The horizontal display start position here indicates the left position of the 1st character's BUTTON display area in BUTTON mode. When also changing character size, the horizontal display start position is the same. In OSD mode, display position is shifted for BUTTON display area (for 2 dots) from that of the same character size in BUTTON mode.

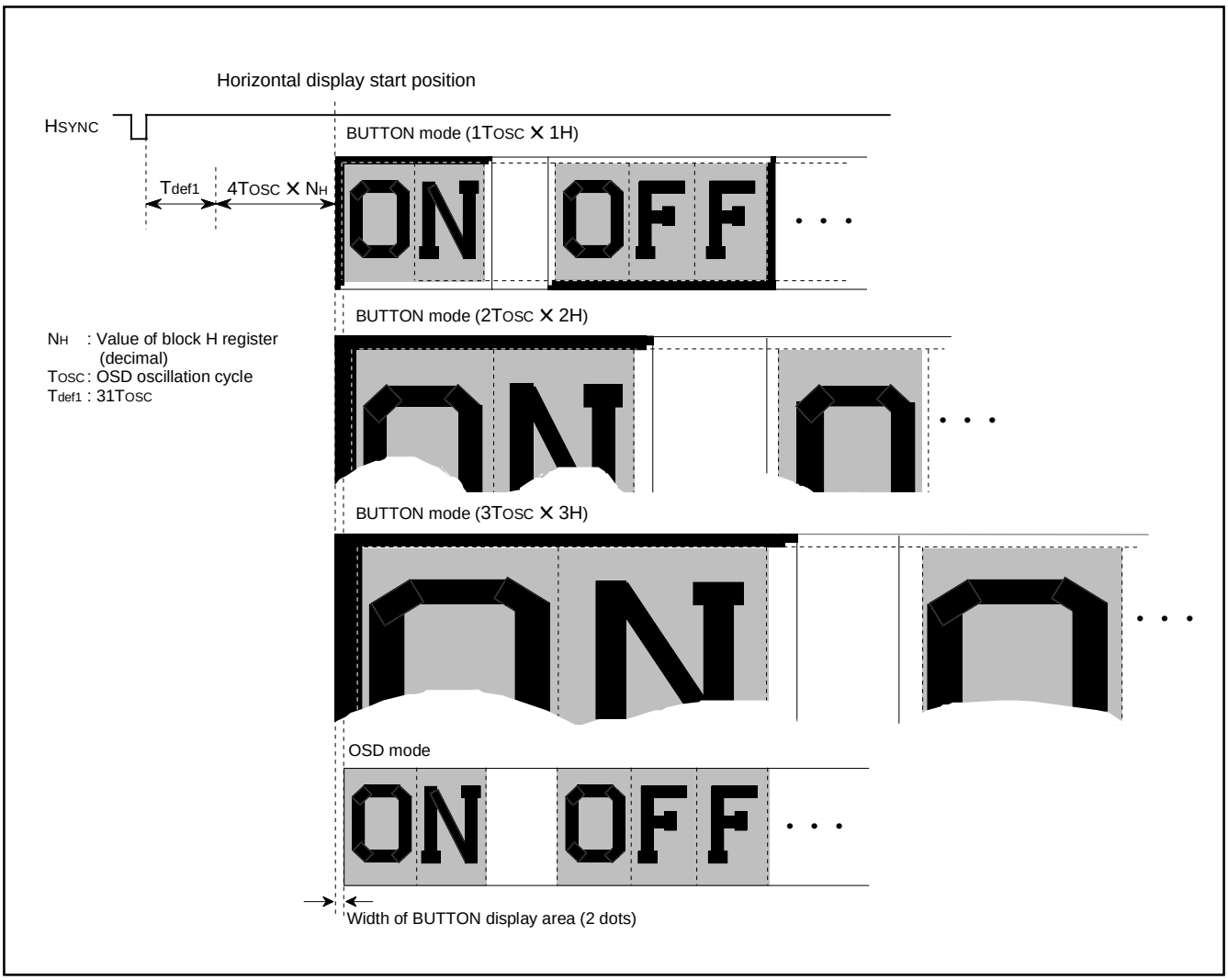


Fig. 8.10.14 Notes on Horizontal Display Start Position

(2) Dot size

The dot size can be selected by a block unit. The dot size in vertical direction is determined by dividing HSYNC in the vertical dot size control circuit. The dot size in horizontal is determined by dividing the following clock in the horizontal dot size control circuit : the clock gained by dividing the OSD clock source (OSC1, main clock from pin XIN) in the pre-divide circuit.
The dot size is specified by bits 3 and 4 of the block i control register.

Refer to Figure 8.10.8 (the block i control register).
The block diagram of dot size control circuit is shown in Figure 8.10.15.

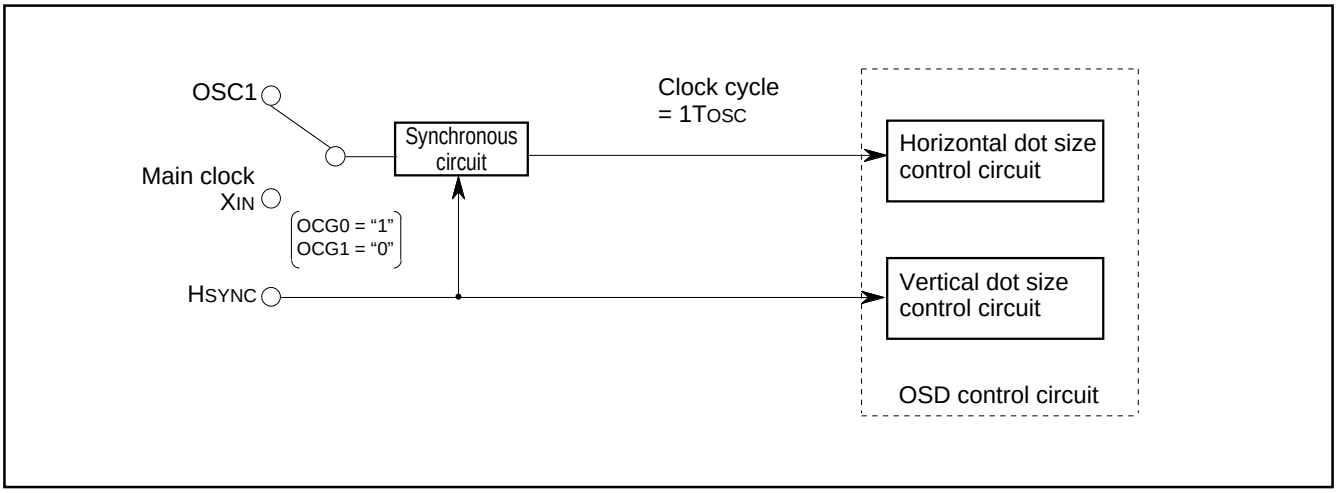


Fig. 8.10.15 Block Diagram of Dot Size Control Circuit

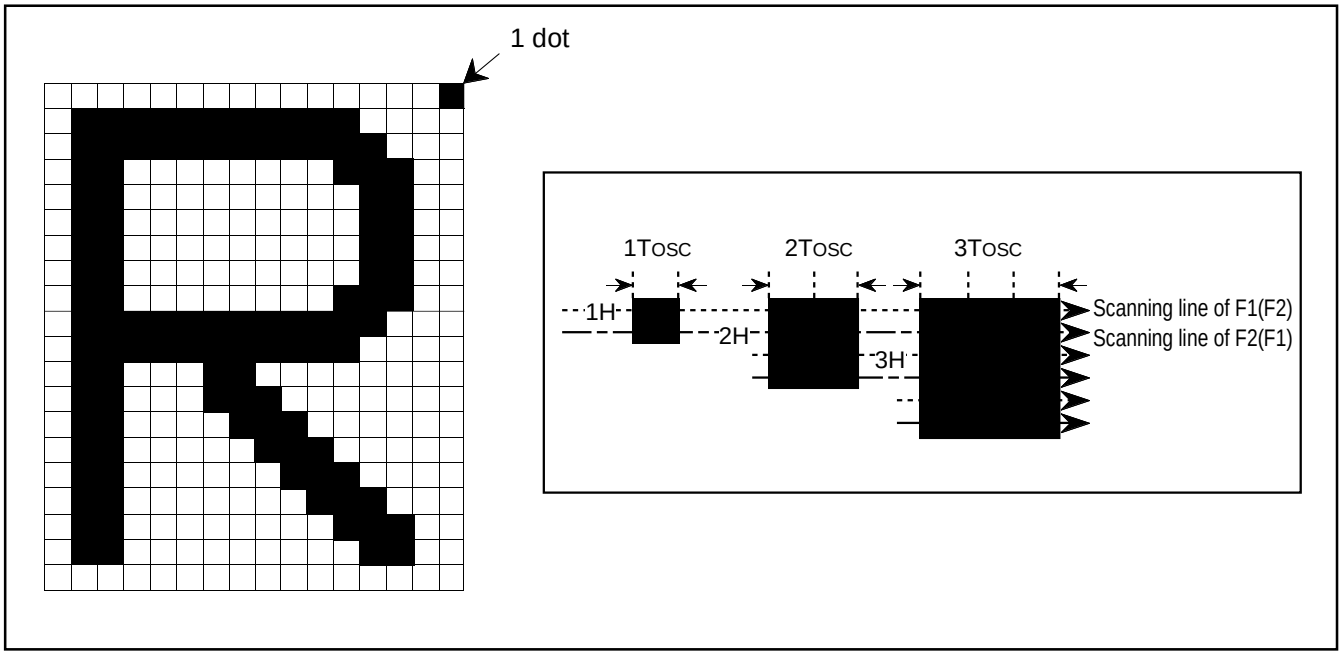


Fig. 8.10.16 Definition of Dot Sizes

(3) Memory for OSD

There are 2 types of memory for OSD : OSD ROM (addresses 1140_{16} to $13BFF_{16}$ and 1540_{16} to $17AFF_{16}$) used to specify character dot data and OSD RAM (addresses 0800_{16} to 0877) used to specify the characters, colors, and attribute. The following describes each type of memory.

① **OSD ROM (addresses 1140_{16} to $13BFF_{16}$, 1540_{16} to $17AFF_{16}$)**

The dot pattern data for OSD characters is stored in the character font area in the OSD ROM. To specify the kinds of the character font, it is necessary to write the character code (based on OSD ROM address) into the OSD RAM.

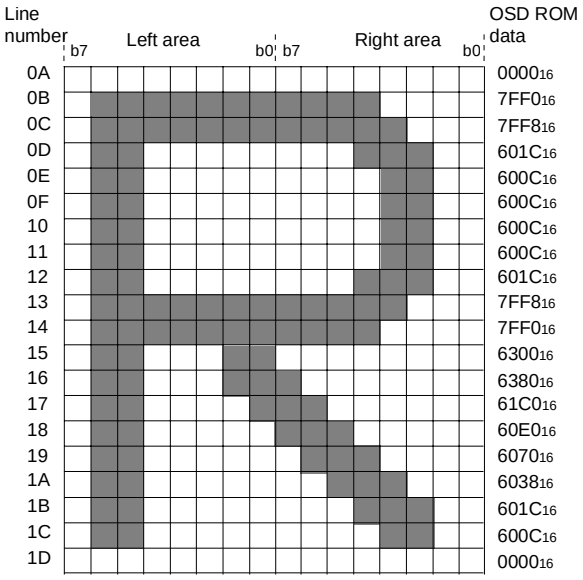
The modes are selected by bit 3 of the OSD control register 3 for each screen.

The character font data storing address is shown in Figure 8.10.17.

OSD ROM address of character font data

OSD ROM address bit	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
Line number / Character code / Font bit	1	0	Character code (high-order 1)	Line number					Character code (low-order 8 bits)								Font bit

Line number = "$0A_{16}$" to "$1D_{16}$"
Character code = "000_{16}" to "$17F_{16}$" ("$07F_{16}$", "080_{16}" and "$17F_{16}$" cannot be used.)
Font bit = 0: Left area
1: Right area



Character font

Fig. 8.10.17 Character Font Data Storing Address

Note: The 120-byte addresses corresponding to the character code "07F16," "08016" and "17F16" in OSD ROM are the test data storing area. Set "FF16" to the area. (We stores the test data to this area and the different data from "FF16" is stored for the actual products.)

<The test data storing area>
- 11000016 + (4 + 2n) × 10016 + FE16 to 11000016 + (5 + 2n) × 10016 + 0116
- 15000016 + (4 + 2n) × 10016 + FE16 and 15000016 + (4 + 2n) × 10016 + 0116 (n = 0 to 19)

Address area

addresses 114FE16 to 115016
addresses 116FE16 to 117016
⋮
addresses 138FE16 to 139016
addresses 13AFE16 to 13B016
addresses 154FE16 and 154FF16
addresses 156FE16 and 156FF16
⋮
addresses 178FE16 and 178FF16
addresses 17AFE16 and 17AFF16

② **OSD RAM (addresses 080016 to 087716)**

The OSD RAM for character is allocated at addresses 080016 to 084716, 085016 to 085716, 086016 to 086716, 087016 to 087716, and is divided into a display character code specification part 087016 to 087716, and color/attribute specification part for each block. Tables 8.10.3 shows the contents of the OSD RAM.

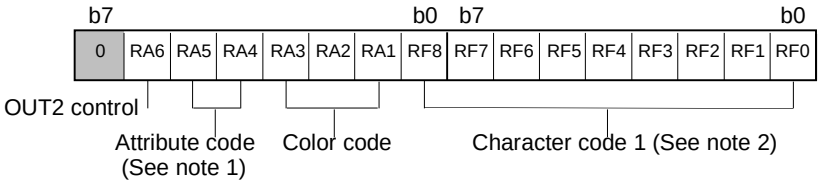
For example, to display 1 character position (the left edge) in block 1, write the character code in address 080016, write color/attribute code at 081016.

The structure of the OSD RAM is shown in Figure 8.10.18.

Table 8.10.3 Contents of OSD RAM

Block	Display Position (from left)	Character Code Specification	Color/Attribute Code Specification
Block 1	1st character	080016	081016
	2nd character	080116	081116
	3rd character	080216	081216
	:	:	:
	16th character	080F16	081F16
	17st character	084016	085016
	:	:	:
	24nd character	084716	085716
Block 2	1st character	082016	083016
	2nd character	082116	083116
	3rd character	082216	083216
	:	:	:
	16th character	082F16	083F16
	17st character	086016	087016
	:	:	:
	24nd character	086716	087716

Blocks 1 and 2



Mode / Bit	BUTTON Mode		OSD Mode	
	Bit name	Function	Bit name	Function
RF0	Character code	Character code in OSD ROM	Character code	Character code in OSD ROM
RF1				
RF2				
RF3				
RF4				
RF5				
RF6				
RF7				
RF8				
RA1	Color code	RA3 RA2 RA1 0 0 0: Color register 1 0 0 1: Color register 2 0 1 0: Color register 3 0 1 1: Color register 4 1 0 0: Color register 5 1 0 1: Color register 6 1 1 0: Color register 7 1 1 1: Color register 8	Color code	RA3 RA2 RA1 0 0 0: Color register 1 0 0 1: Color register 2 0 1 0: Color register 3 0 1 1: Color register 4 1 0 0: Color register 5 1 0 1: Color register 6 1 1 0: Color register 7 1 1 1: Color register 8
RA2				
RA3				
RA4	Attribute code	RA4 RA4 0 0: No BUTTON/block shadow display 0 1: ON BUTTON display 1 0: OFF BUTTON display 0 1: Block shadow display	Not used	———
RA5				
RA6	OUT2 control	0: OUT2 blank output OFF 1: OUT2 blank output ON	OUT2 control	0: OUT2 blank output OFF 1: OUT2 blank output ON
RA7	Fix to “0”		Fix to “0”	

Notes 1: Attribute code is valid in only BUTTON mode.
2: Do not use character codes “07F16,” “08016,” “17F16.”
And also, do not use character codes “18016” to “1FF16” (these codes are not included in OSD ROM area).

Fig. 8.10.18 Structure of OSD RAM

(4) Character color

Character colors are specified by RA1 to RA3 of OSD RAM.
Color data are set by color register i (CO1 to CO8: addresses $00E6_{16}$ to $00E9_{16}$, $00EC_{16}$ to $00EF_{16}$) in advance, and 8 kinds of color register i are specified by color codes.

(5) Character background color

Character background are specified by color register i as same as character color.

Note : The character background is displayed in the following part:
(character display area) – (character font) — (border) – (BUTTON display area)
Accordingly, the character background color and the color signal for these sections cannot be mixed.

(6) OUT1, OUT2 signals

OUT1 signal is used to erase a back ground TV image. The output waveform of OUT1 signal is controlled by combining the following bits; the display mode selection bits (bits 0 to 2 of the block i control register), the border type selection bit (bit 1 of the OSD control register), and the OUT1 output control bit (bit 6 of color register i).
Figure 8.10.20 and 8.10.21 shows the output example of R, G, B, and OUT1.
OUT2 signal is used to change the luminance of a background TV image. The output waveform of OUT2 signal is blank output and is controlled per character unit by RA6 of OSD RAM.

Color Register i

b7 b6 b5 b4 b3 b2 b1 b0

Color register i (CO1 to CO8) (i=1 to 8) [Addresses $00E6_{16}$ to $00E9_{16}$, $00EC_{16}$ to $00EF_{16}$]

B	Name	Functions	After reset	R	W
0	R signal output selection bit (COi0)	0: No output 1: Output	Indeterminate	R	W
1	G signal output selection bit (COi1)	0: No output 1: Output	Indeterminate	R	W
2	B signal output selection bit (COi2)	0: No output 1: Output	Indeterminate	R	W
3	R signal output (background) selection bit (COi3)	0: No output 1: Output	Indeterminate	R	W
4	G signal output (background) selection bit (COi4)	0: No output 1: Output	Indeterminate	R	W
5	B signal output (background) selection bit (COi5)	0: No output 1: Output	Indeterminate	R	W
6	OUT1 output control bit (COi6)	0: Character output 1: Blank output	Indeterminate	R	W
7	Nothing is assined. This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—

Fig. 8.10.19 Color register i (i = 1 to 8)

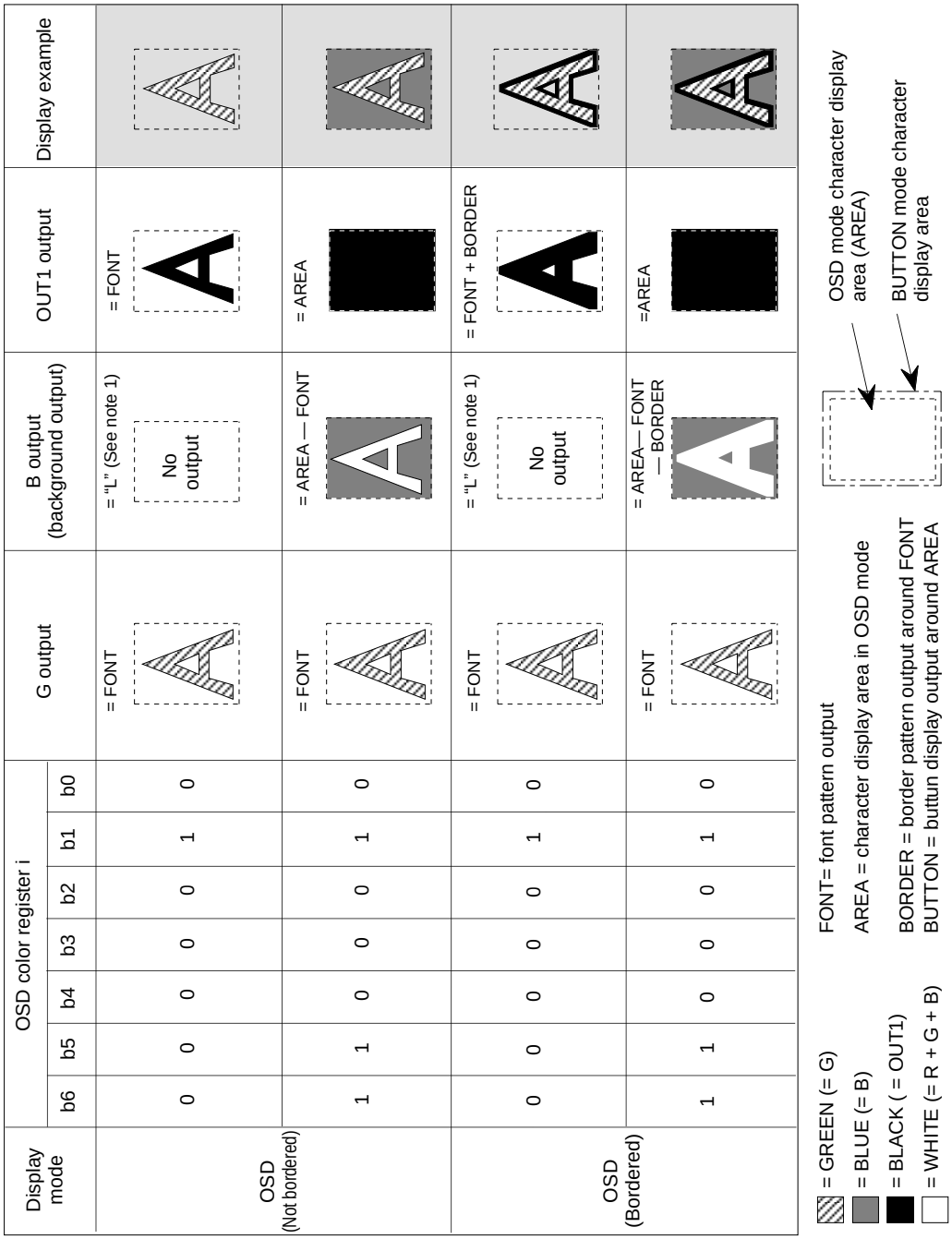


Fig. 8.10.20 Output Example of R, G, B and OUT1 (Character Color: Green, Character Background Color: Blue) (In OSD Mode)

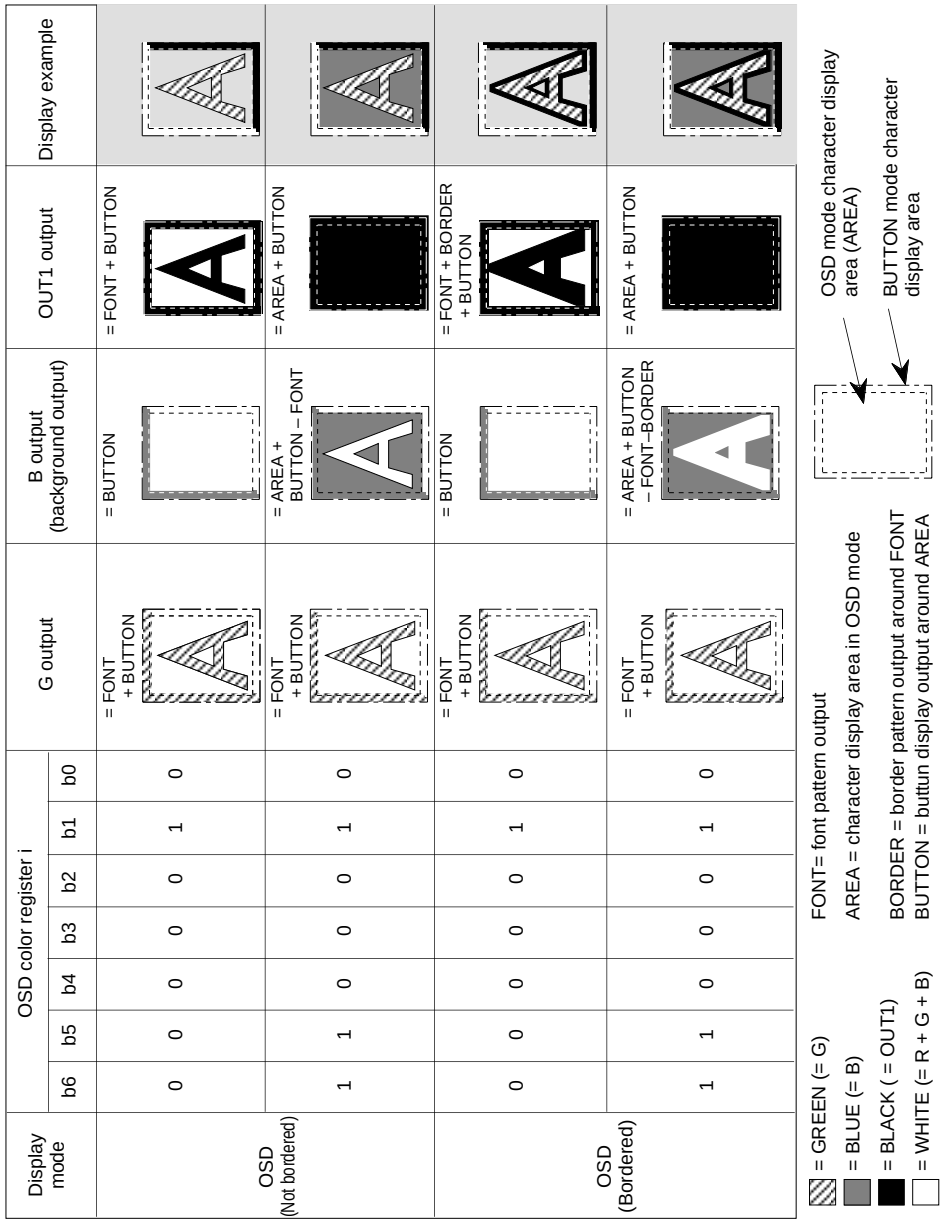


Fig. 8.10.21 Output Example of R, G, B and OUT1 (Character Color: Green, Character Background Color: Blue) (In BUTTON Mode)

(7) Attribute (block display)

The attributes (border, BUTTON display, block shadow display) are controlled to the character font. The display mode is specified per block unit by bits 0 to 2 of the block i control register. The attributes to be controlled are different depending on each mode.

OSD mode ..... Border

BUTTON mode ..... Border, BUTTON display, block shadow display

① **Border**

The border is output in the OSD and BUTTON modes. The all bordered (bordering around of character font) and the shadow bordered (bordering right and bottom sides of character font) are selected per screen unit by bit 1 of OSD control register (refer to Figure 8.10.4). The ON/OFF switch for borders can be controlled per block unit by bit 2 of the block i control register (refer to Figure 8.10.8).

The OUT1 signal is used for border output.

The horizontal size (x) of border is 1TOSC (TOSC: OSD oscillation cycle) regardless of the character font dot size. The vertical size (y) is 1H (2H in the bi-scan mode) regardless of character font.

Notes 1: The border dot area is the shaded area as shown in Figure 8.10.23. In BUTTON mode, it is possible to display in vertical out of character area of 20 dots.

2: When the border dot overlaps on the next character font, the character font has priority (refer to Figure 8.10.22 A). When the border dot overlaps on the next character back ground, the border has priority (refer to Figure 8.10.22 B).

3: The border in vertical out of character area is not displayed in OSD mode (refer to Figure 8.10.22).

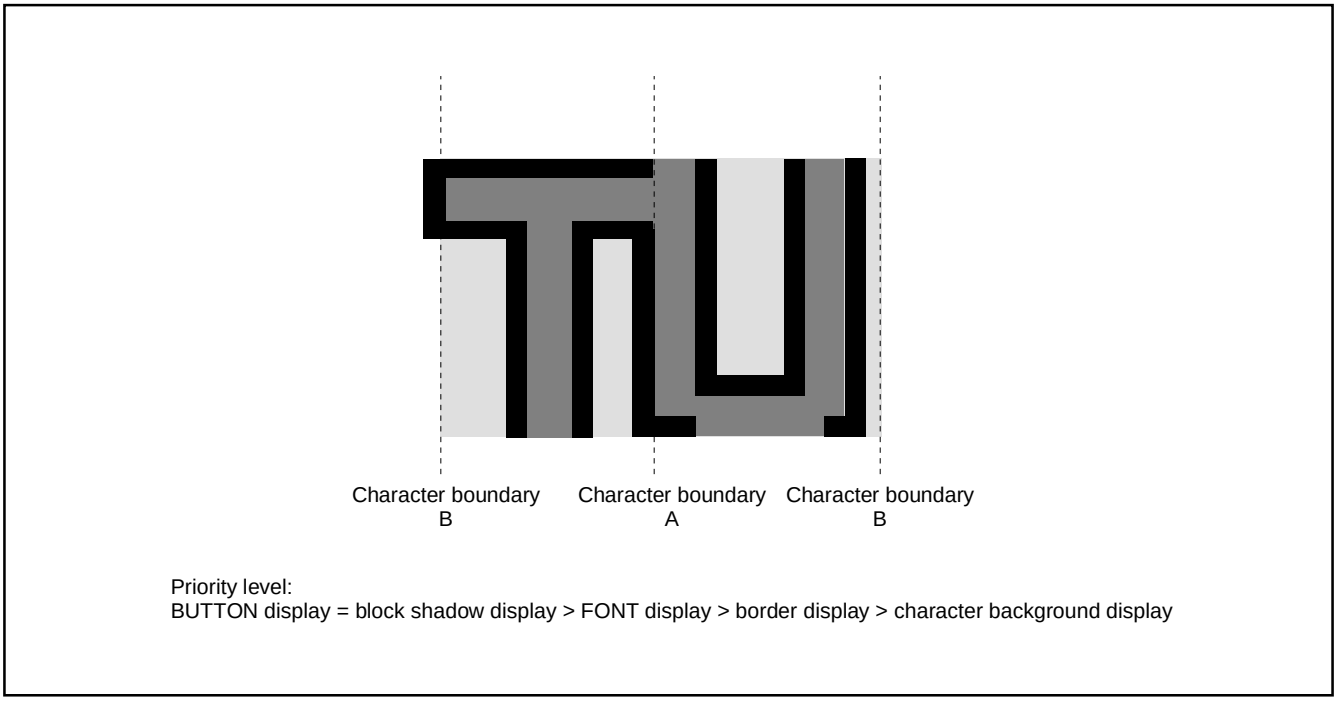
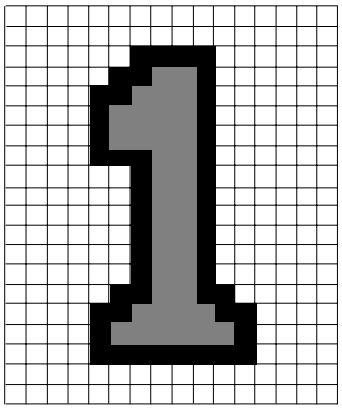
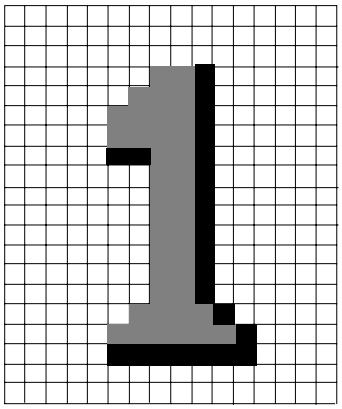


Fig. 8.10.22 Border Priority

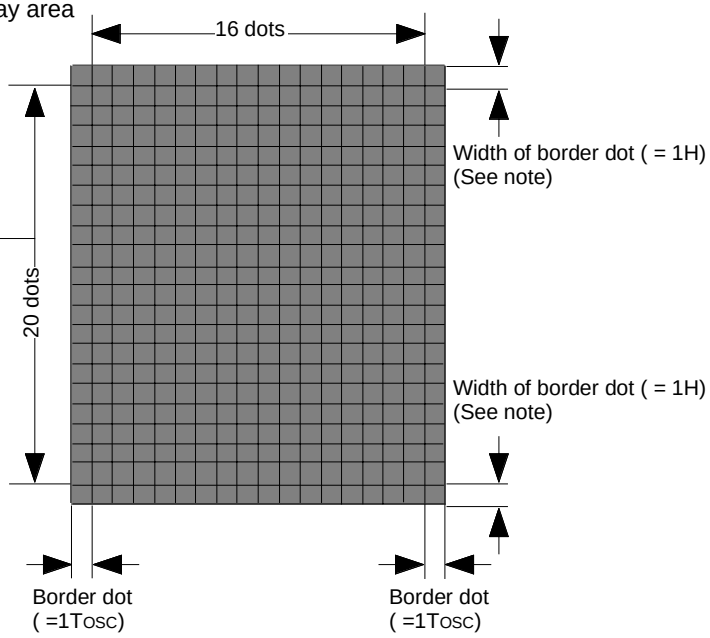
All border



Shadow border



Border display area



Note: It is possible in only BUTTON mode.

FONT

BORDER

This is display example when 1Tosc × 1H of dot size.

Fig. 8.10.23 Border Display Example and Border Area

② **BUTTON display**

There are 2 kinds of displays; ON BUTTON display and OFF BUTTON display. The BUTTON display is controlled per character unit by RA4 and RA5 of OSD RAM.

The BUTTON display area is around the character display area in the BUTTON mode. The ON/OFF BUTTON is displayed by outputting white (R + G + B) or black (OUT) to this area.

The horizontal size (x) of BUTTON display area is for 2 dots regardless of the character font dot size. The vertical size (y) is for 2 dots regardless of the vertical dot size of character font.

③ **Block shadow display**

The block shadow is displayed to the character display area in the BUTTON mode. The block shadow display is controlled per character unit by RA4 and RA5 of OSD RAM.

FIgure 8.10.24 shows each display example. The BUTTON/block shadow can be displayed to the character area where combined arbitrary (within 24 characters for a block). Set each character in this case, too. Set “0” to all attribute codes between ON BUTTON, OFF BUTTON and block shadow displays.

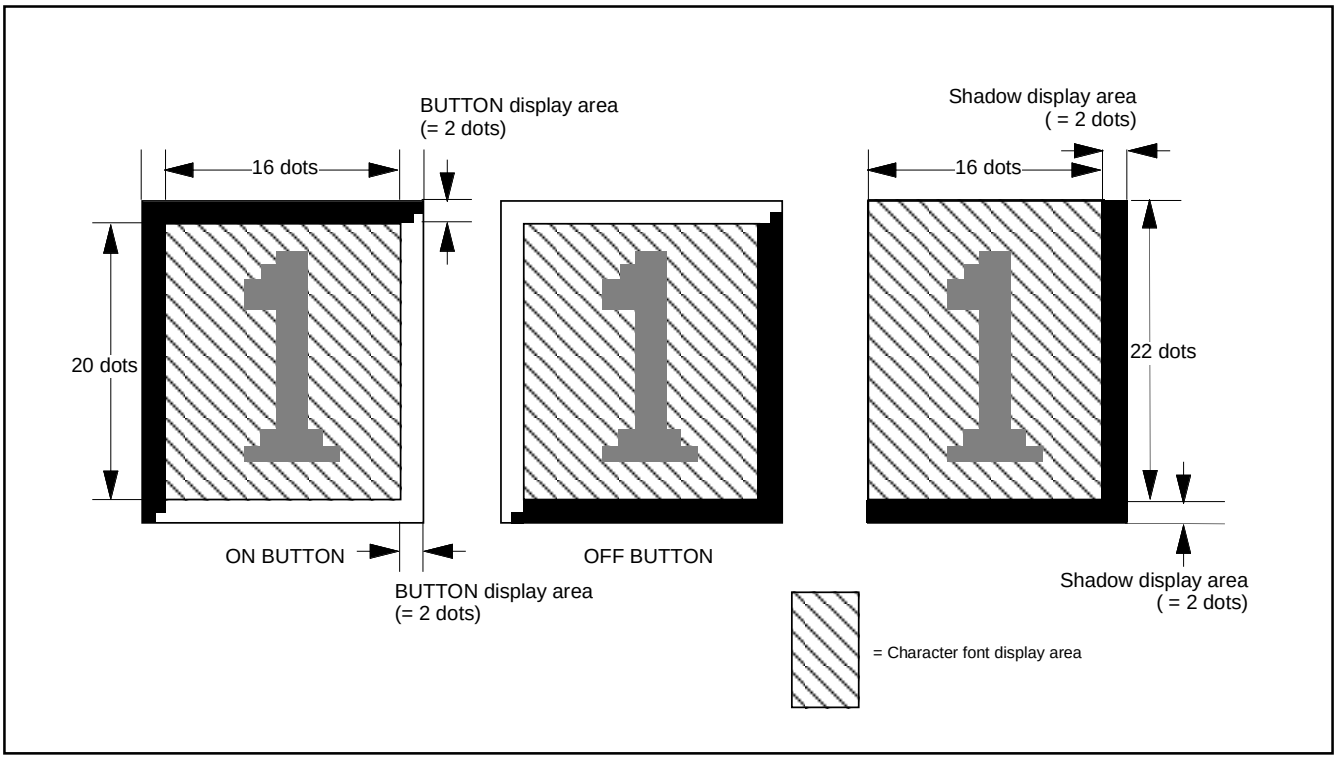


Fig. 8.10.24 ON/OFF BUTTON Display and Block Shadow Display

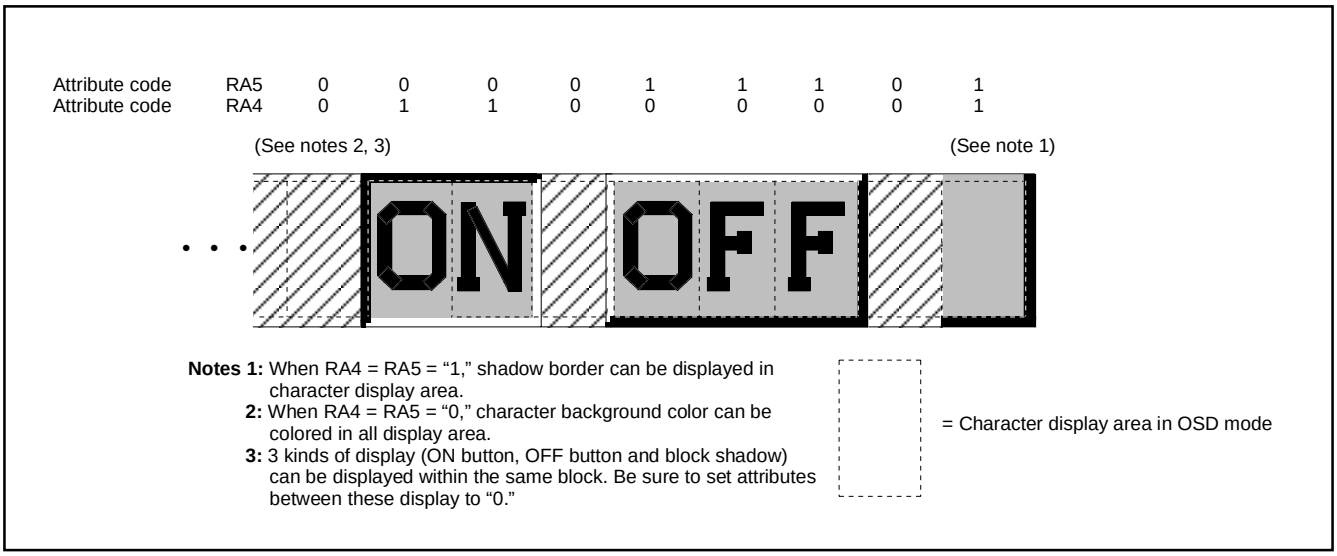


Fig. 8.10.25 Attribute Codes and Display Examples

(8) Multiline display

This microcomputer can ordinarily display 2 lines on the CRT screen by displaying 2 blocks at different vertical positions. In addition, it can display 3 lines or more by using OSD interrupts.

An OSD interrupt request occurs at the point at which display of each block has been completed. In other words, when a scanning line reaches the point of the display position (specified by the block i V registers) of a certain block, the character display of that block starts, and an interrupt occurs at the point at which the scanning line exceeds the block.

Notes 1: An OSD interrupt does not occur at the end of display when the block is not displayed. In other words, if a block is set to off display by the display control bit of the block control register i (addresses $00F9_{16}$ and $00FA_{16}$), an OSD interrupt request does not occur (refer to Figure 8.10.26 (A)).

2: When another block display appears while one block is displayed, an OSD interrupt request occurs only once at the end of the another block display (refer to Figure 8.10.26 (B)).

3: On the screen setting window, an OSD interrupt occurs even at the end of the block (off display) out of window (refer to Figure 12.11.36 (C)).

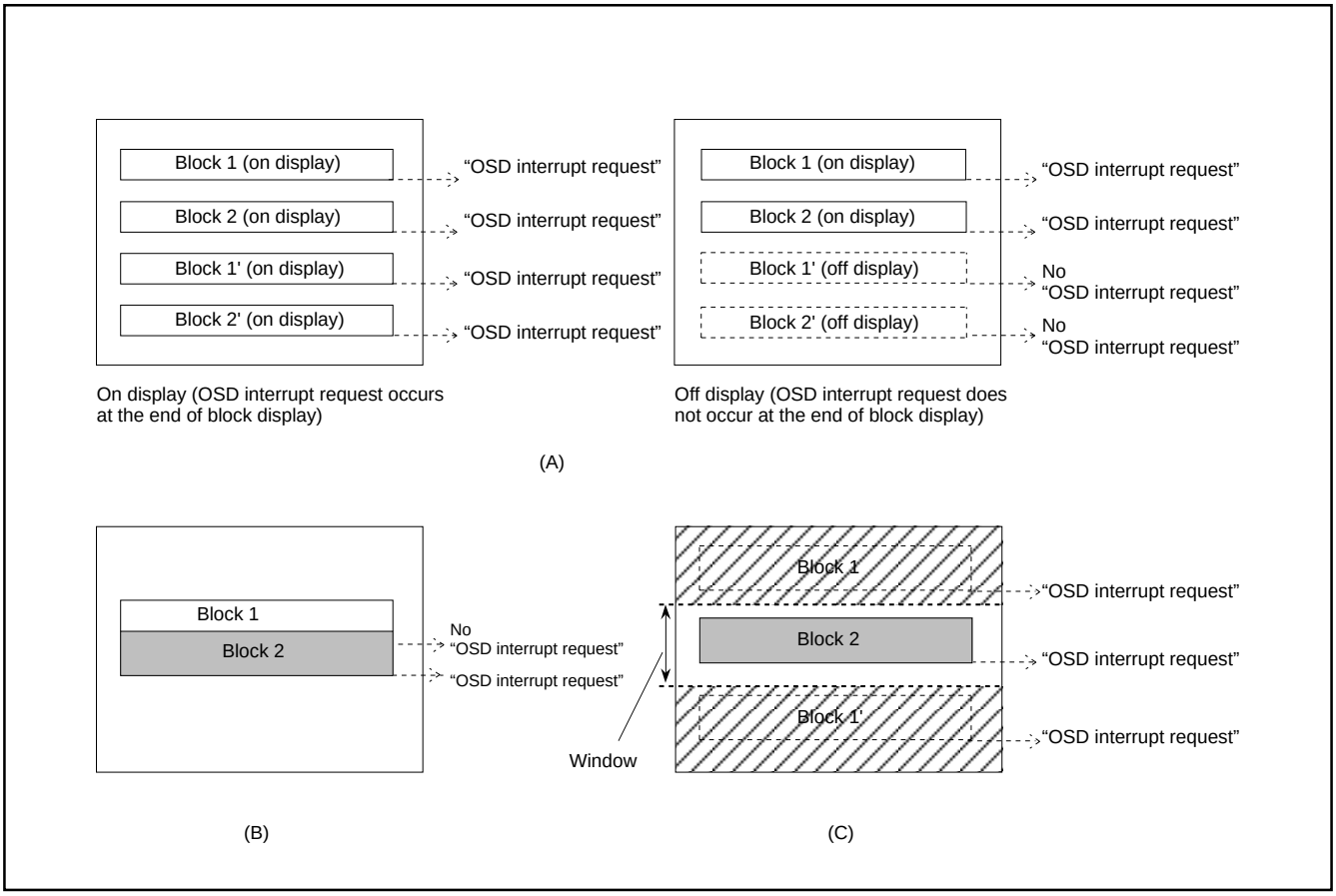


Fig. 8.10.26 Note on Occurence of OSD Interrupt

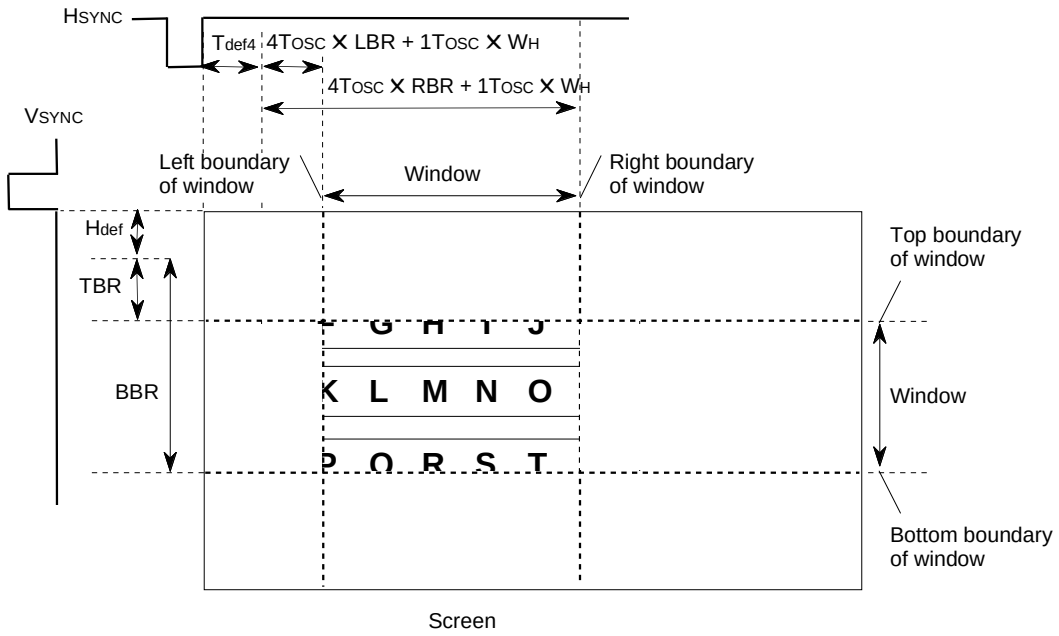
(9) Window function

The window function can be set windows on-screen, and output OSD within only the area where the window is set.

The ON/OFF for vertical window function is performed by bit 4 of the OSD control register. The top boundary is set by the top border control register (TBR) and the bottom boundary is set by bottom border control register (BBR). The left boundary is set by the left border control register (LBR), and the right boundary is set by the right border control register (RBR).

The left and right boundarys can be adjusted minutely by bits 2 and 3 of the OSD control register (address $00EA_{16}$).

Note: The SPRITE display is not effected by the window function.



LBR : Value of left border control register
RBR : Value of right border control register
WH : Value (0 to 3) of window horizontal position minute adjustment bit
TOSC : OSD oscillation cycle
Tdef4 : 4TOSC
TBR : Value of top border control register
BBR : Value of bottom border control register
Hdef : 17H
H : HSYNC

Fig. 8.10.27 Example of window function

Top Border Control Register

b7 b6 b5 b4 b3 b2 b1 b0

Top border control register (TBR) [Address 024516]

B	Name	Functions	After reset	R	W
0 to 7	Control bits of top border (TBR0 to TBR7)	Top border position = H_{def} + H × n (n: setting value, H_{def}: 17H, H: H_{SYNC})	Indeterminate	R	W

Notes 1: Set values except "00_{16}" to TBR.
2: Set values fit for TBR ≤ BBR.

Fig. 8.10.28 Top Border Control Register

Bottom Border Control Register

b7 b6 b5 b4 b3 b2 b1 b0

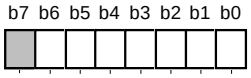
Bottom border control register (BBR) [Address 024616]

B	Name	Functions	After reset	R	W
0 to 7	Control bits of bottom border (BBR0 to BBR7)	Bottom border position = H_{def} + H × n (n: setting value, H_{def}: 17H, H: H_{SYNC})	Indeterminate	R	W

Notes 1: Set values except "00_{16}" to BBR.
2: Set values fit for TBR ≤ BBR.

Fig. 8.10.29 Bottom Border Control Register

Left Border Control Register



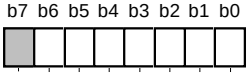
Left border control register (LBR) [Address 0240_{16}]

B	Name	Functions	After reset	R	W
0 to 6	Control bits of left border (LBR0 to LBR6)	Left border position = T_{def4} + 4TOSC × n + 1TOSC × WH (n: setting value, T_{def4}: 4TOSC, TOSC: OSD oscillation cycle, WH: value (0 to 3) of window horizontal position minute adjustment bit)	0	R	W
7	Nothing is assigned. This bit is write disable bit. When this bit is read out, the value is indeterminate.		0	R	—

Note: Set values fit for LBR ≤ RBR.

Fig. 8.10.30 Left BorderControl Register

Right Border Control Register



Right border control register (RBR) [Address 0241_{16}]

B	Name	Functions	After reset	R	W
0 to 6	Control bits of left border (RBR0 to RBR6)	Right border position = T_{def4} + 4TOSC × n + 1TOSC × WH (n: setting value, T_{def4}: 4TOSC, TOSC: OSD oscillation cycle, WH: value (0 to 3) of window horizontal position minute adjustment bit)	0	R	W
7	Nothing is assigned. This bit is write disable bit. When this bit is read out, the value is indeterminate.		0	R	—

Note: Set values fit for LBR ≤ RBR.

Fig. 8.10.31 Right Border Control Register

8.10.2 SPRITE Display

This is especially suitable for cursor and other displays as its function allows for display in any position, regardless of the validity of other OSDs or display positions. Each SPRITE font is ROM font consisting of 16 horizontal dots × 20 vertical dots, and there are 4 kinds. When SPRITE display overlaps with other OSDs, SPRITE display is always given priority.

To display SPRITE font, OSD ROM font data for 2 characters is used. These 2 fonts can be colored with any color and can be displayed by synthesizing as a character. The features and display example of SPRITE display are shown below.

Notes 1: The SPRITE display is not effected by the window function.
2: The SPRITE display cannot output character background color or OUT2.

Table 8.10.4 Features of SPRITE Display

Parameter	Features
Number of display characters	1 characters × 1 line (display by synthesizing 2 kinds of characters)
Dot structure	16 × 20 dots (See note 3)
Kinds of characters	4 kinds (Character code = "F8$_{16}$" to "FF$_{16}$") (See note 4)
Kinds of character sizes	1 kind
Dot size	1TOSC × 1H (See notes 5, 7, 8)
Character font coloring	Synthesis SPRITE fonts 1 and 2 (per SPRITE font unit)
OSD output	R, G, B
Other functions	Corresponding to bi-scan
Display position	Horizontal: 253 levels (See note 2), Vertical: 255 levels (See note 1)

Notes 1: It is possible to set in any position regardless of vertical display positions of the block display. The vertical display start positions of the SPRITE display is the same as that of the block display.
2: It is possible to set in any position regardless of horizontal display position of block display.
3: It is the same display area as OSD mode (refer to "Figure 8.10.3").
4: As for character font data storing address refer to "8.10.1 Block Display (3) Memory for OSD." The characters of character codes "F8$_{16}$" to "FF$_{16}$" can be also used for the block display.
5: Refer to "8.10.1 Block Display (2) Dot size." The dot size in the bi-scan mode is 1TOSC × 2H.
6: Refer to "8.10.1 Block Display (4) Character color." Only color registers 1 to 4 can be specified.
7: H = HSYNC
8: TOSC = OSD oscillation cycle

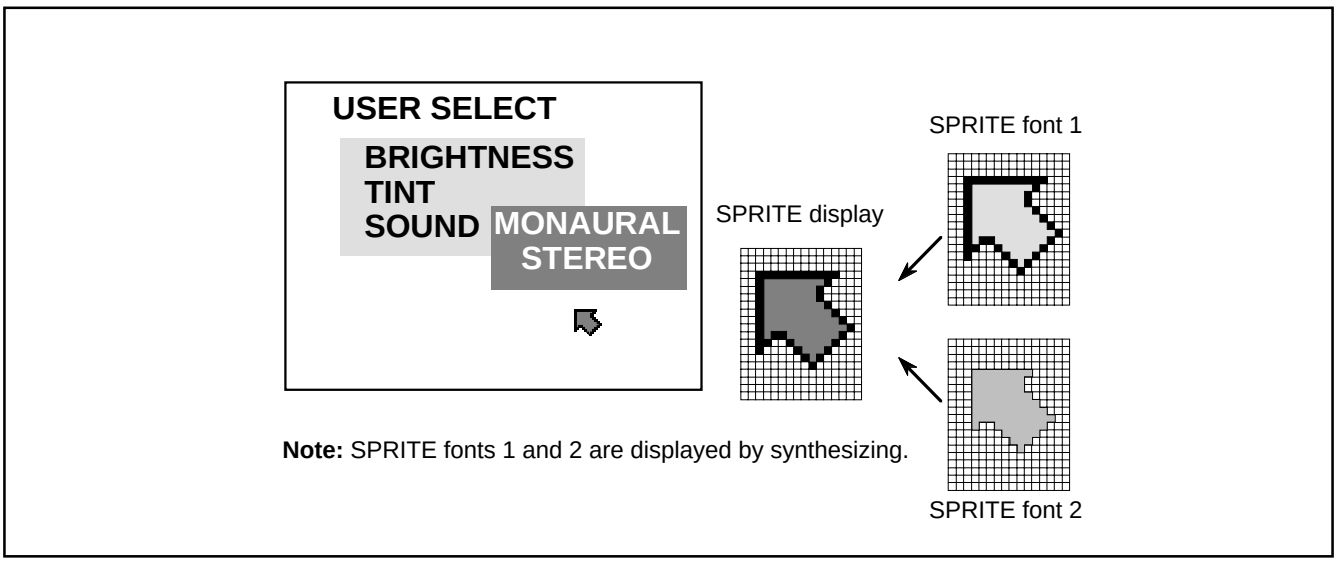


Fig. 8.10.32 SPRITE Display Example

SPRITE H Register

b7 b6 b5 b4 b3 b2 b1 b0

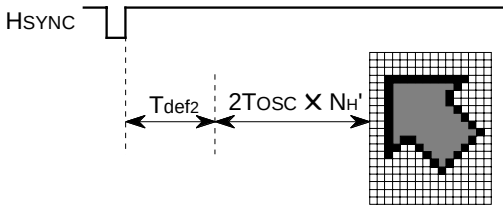
SPRITE H register (SHP) [Address $00E4_{16}$]

B	Name	Functions	After reset	R	W
0 to 7	Horizontal display start position control bits of SPRITE OSD (SHP0 to SHP7)	Horizontal display start position = T_{def2} + $2T_{OSC}$ × n (n: setting value, T_{def2}: $2T_{OSC}$, T_{OSC}: OSD oscillation cycle)	0	R	W

Notes 1: Set values except "00_{16}" to "02_{16}" to SHP.
2: When selecting raster patterning display, setting value is synchronized with V_{SYNC} signal; when selecting SPRITE display, it is not synchronized.

Fig. 8.10.33 SPRITE H Register

When setting the SPRITE H register to "03_{16}," the interval of T_{def2} + $2T_{OSC}$ × 3 = $8T_{OSC}$ is necessary from a rising edge (negative polarity) to horizontal display start position.



N_H' : value of SPRITE H register (decimal) (see note)
T_{OSC} : OSD oscillation cycle
T_{def2} : $2T_{OSC}$

Note: Do not set "0" to "2" to N_H'.

Fig. 8.10.34 Note on Horizontal Display Start Position of SPRITE Display

SPRITE V Register

b7 b6 b5 b4 b3 b2 b1 b0

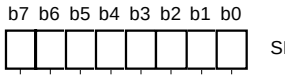
SPRITE V register (SVP) [Address $00E5_{16}$]

B	Name	Functions	After reset	R	W
0 to 7	Horizontal display start position control bits of SPRITE OSD (SVP0 to SVP7) (See note 1)	Horizontal display start position = H_{def} + H × n (n: setting value, H_{def}: 17H, H: H_{SYNC})	Indeterminate	R	W

Note: Set values except "00_{16}" to the SVP.

Fig. 8.10.35 SPRITE V Register

SPRITE Control Register



SPRITE control register (SC) [Address $00E3_{16}$]

B	Name	Functions	After reset	R	W
0, 1	SPRITE font 1 color register specification bit (SC0, SC1)	SC1 SC0 0 0: Color register 1 0 1: Color register 2 1 0: Color register 3 1 1: Color register 4	0	R	W
2, 3	SPRITE font 2 color register specification bit (SC2, SC3)	SC3 SC2 0 0: Color register 1 0 1: Color register 2 1 0: Color register 3 1 1: Color register 4	0	R	W
4, 5	SPRITE font selection bit (SC4, SC5)	SC5 SC4 Character code: SPRITE1 / SPRITE2 0 0: $F8_{16}$ / $F9_{16}$ 0 1: FA_{16} / FB_{16} 1 0: FC_{16} / FD_{16} 1 1: FE_{16} / FF_{16}	0	R	W
6, 7	SPRITE/raster patterning control bit (SC6, SC7) (See note)	SC7 SC6 0 0: Display OFF 0 1: Do not set 1 0: SPRITE display 1 1: Raster patterning display	0	R	W

Note : This bit is valid when bit 0 of the OSD control register to "1."

Fig. 8.10.35 SPRITE Control Register

8.10.3 Raster Display

The raster display is displayed on the lower layer than the SPRITE and block layers. There are 2 kinds of displays; the flat display and the patterning display.

In the raster flat display, an entire screen (raster) can be colored by setting the following bits; bits 5 to 7 of the OSD I/O polarity register and bits 6 and 7 of the OSD control register. Since each of the R, G, B, OUT1, and OUT2 pins can be switched to raster coloring output, 8 raster colors can be obtained.

In the raster patterning display, SPRITE fonts are displayed repeatedly on an entire screen (raster). At this time, set “1” to bits 6 and 7 of the SPRITE control register.

Horizontal display start positions of the raster patterning display are set by the SPRITE H register. At this time, setting value is synchronized with VSYNC signal.

Characters for patterning are set by bits 4 and 5 of the SPRITE control register and coloring are set by bits 0 to 3. The raster color is output on the background of SPRITE font.

Note that the raster patterning display and the SPRITE display cannot be used at the same time.

When the character color/the character background color overlaps with the raster color, the color (R, G, B, OUT1, OUT2), specified for the character color/the character background color, takes priority of the raster color. This ensures that the character color/the character background color is not mixed with the raster color.

The raster flat display example is shown in Figure 8.10.36, the raster patterning display example is shown in Figure 8.10.37.

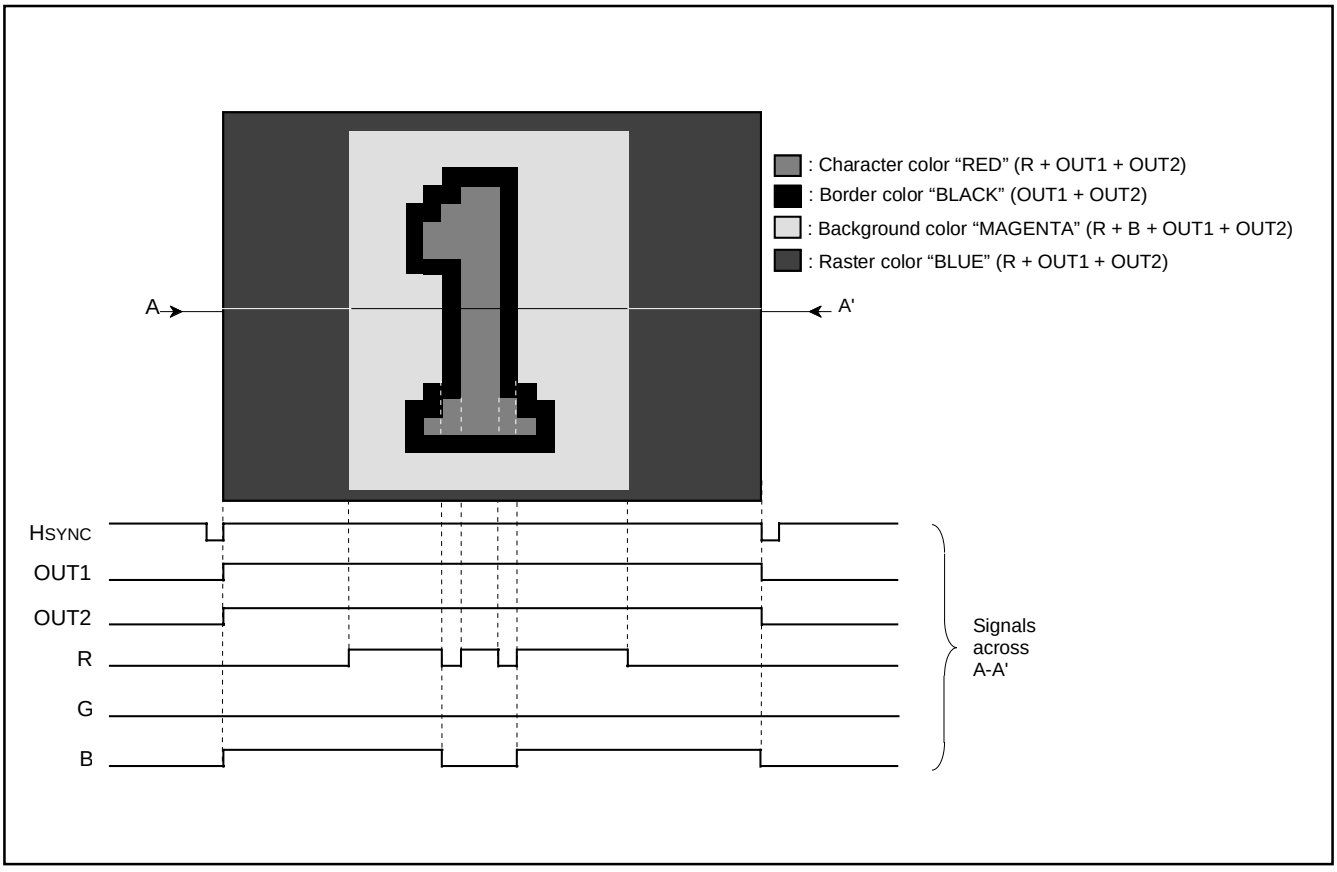
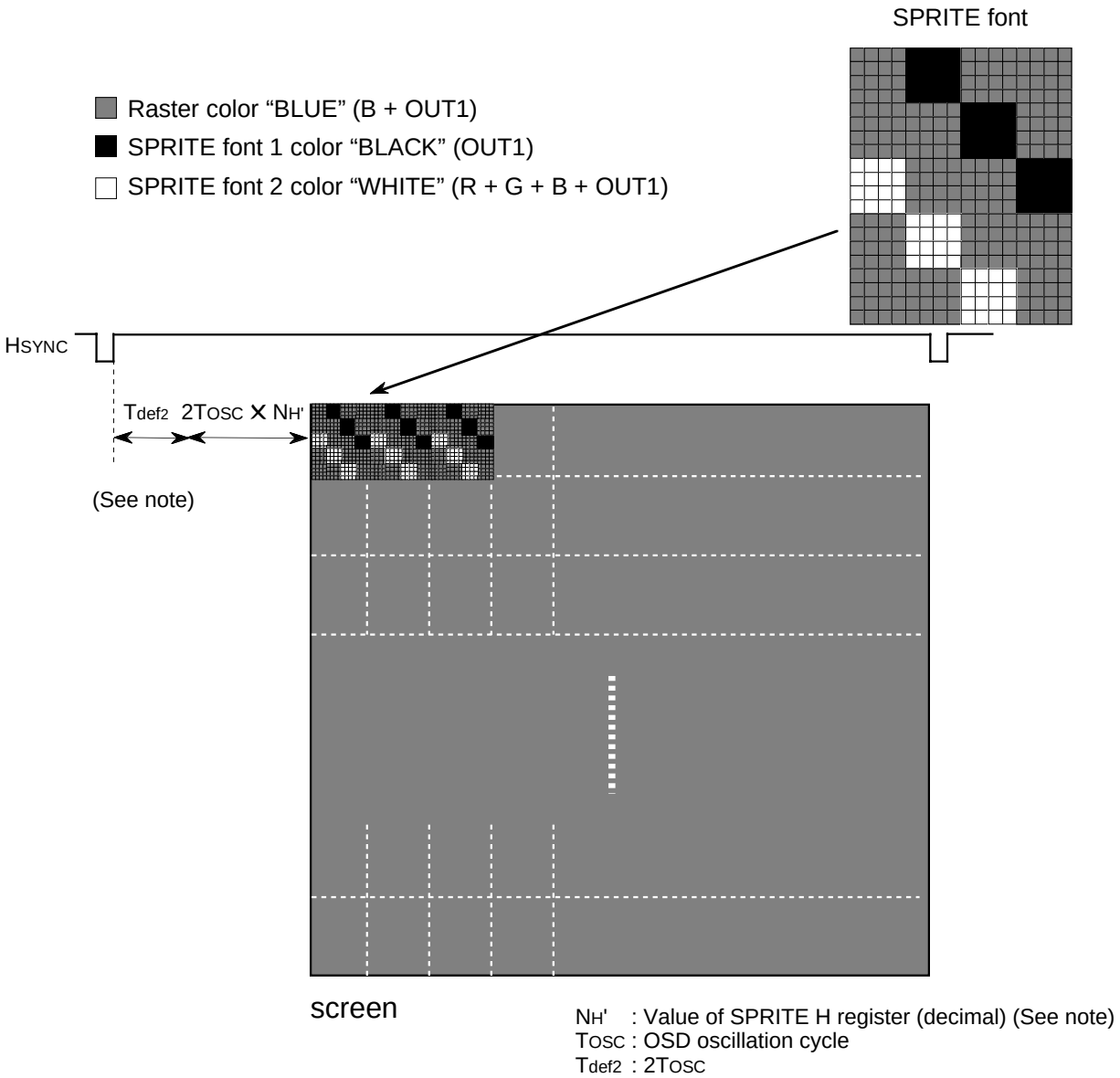


Fig. 8.10.36 Raster Flat Display Example

When setting "03$_{16}$" to SPRITE H register, it is need T_{def2} + 2T_{OSC} × 3 = 8T_{OSC} intervals from a rising edge (negative polarity) of H_{SYNC} signal to a horizontal display start position.



$N_{H'}$: Value of SPRITE H register (decimal) (See note)
T_{OSC} : OSD oscillation cycle
T_{def2} : 2T_{OSC}

Note: Do not set "0" to "2" to $N_{H'}$.

Fig. 8.10.37 Raster Patterning Display Example

8.11 SOFTWARE RUNAWAY DETECT FUNCTION

This microcomputer has a function to decode undefined instructions to detect a software runaway.

When an undefined op-code is input to the CPU as an instruction code during operation, the following processing is done.

① The CPU generates an undefined instruction decoding signal.

② The device is internally reset because of occurrence of the undefined instruction decoding signal.

③ As a result of internal reset, the same reset processing as in the case of ordinary reset operation is done, and the program restarts from the reset vector.

Note, however, that the software runaway detecting function cannot be invalid.

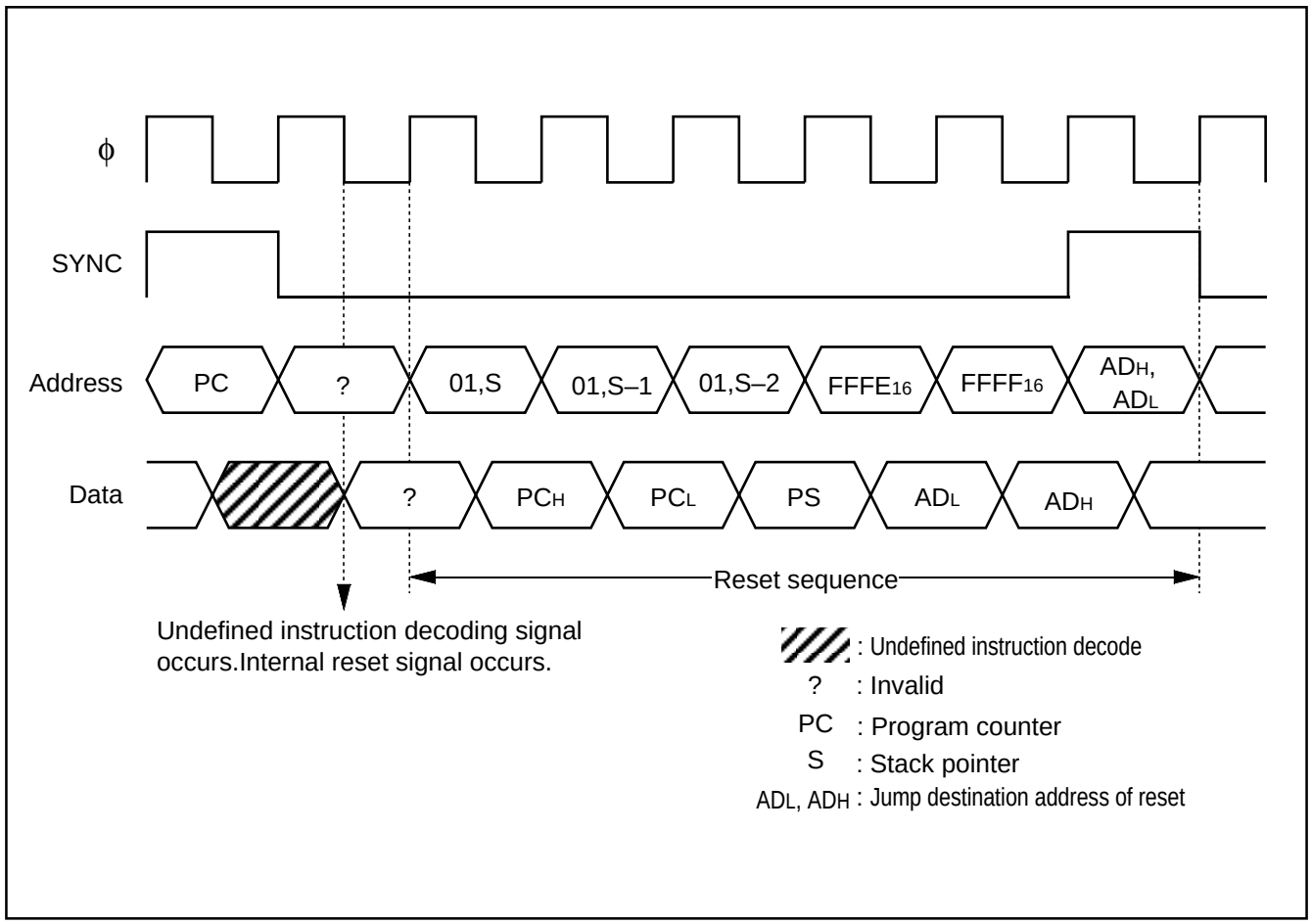


Fig.8.11.1 Sequence at Detecting Software Runaway Detection

8.12. RESET CIRCUIT

When the oscillation of a quartz-crystal oscillator or a ceramic resonator is stable and the power source voltage is 5 V ± 10 %, hold the $\overline{\text{RESET}}$ pin at LOW for 2 µs or more, then return is to HIGH. Then, as shown in Figure 8.12.2, reset is released and the program starts form the address formed by using the content of address FFFF16 as the high-order address and the content of the address FFFE16 as the low-order address. The internal state of microcomputer at reset are shown in Figures 8.2.3 to 8.2.6.

An example of the reset circuit is shown in Figure 8.12.1.

The reset input voltage must be kept 0.9 V or less until the power source voltage surpasses 4.5 V.

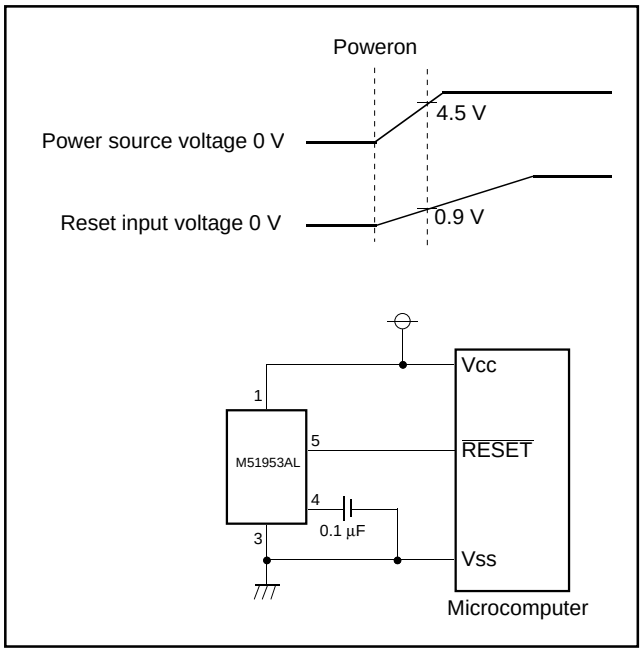
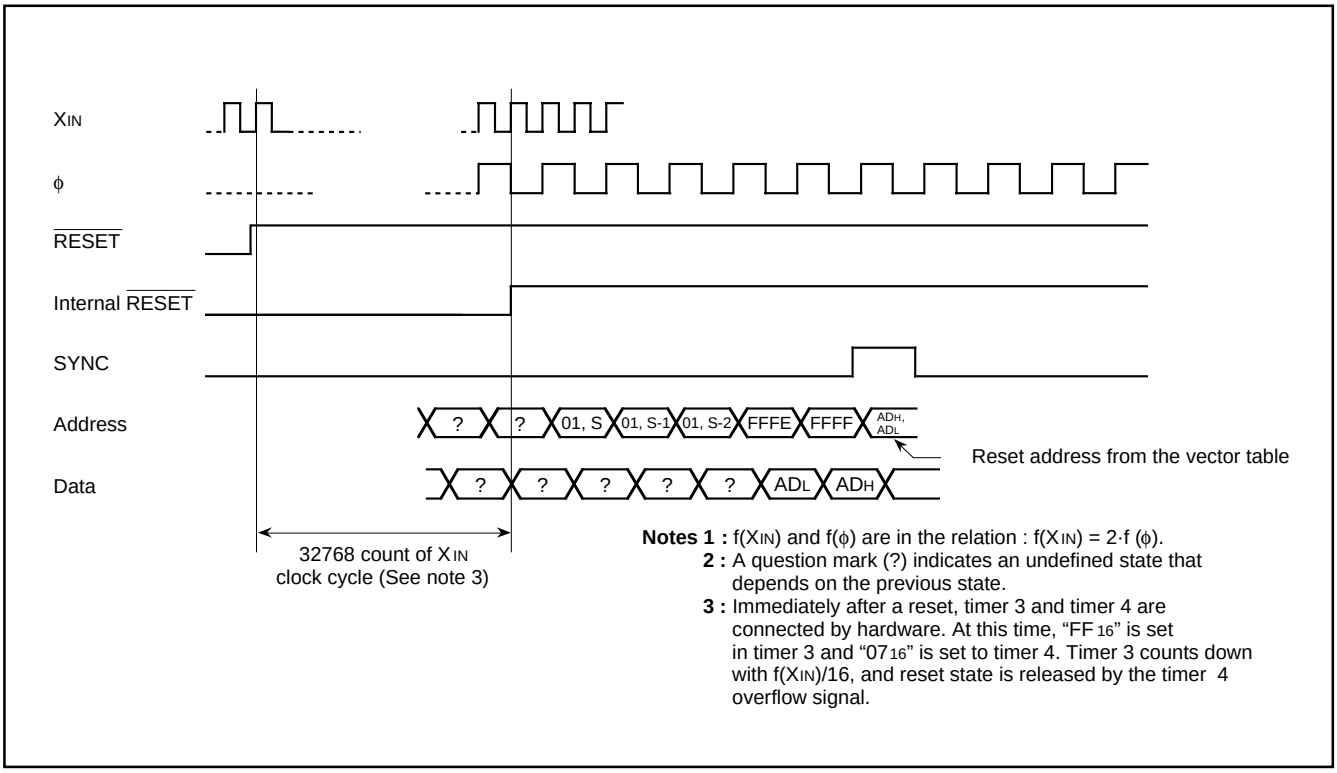


Fig.8.12.1 Example of Reset Circuit



Notes 1 : f(XIN) and f(ϕ) are in the relation : f(XIN) = 2·f (ϕ).
2 : A question mark (?) indicates an undefined state that depends on the previous state.
3 : Immediately after a reset, timer 3 and timer 4 are connected by hardware. At this time, "FF16" is set in timer 3 and "0716" is set to timer 4. Timer 3 counts down with f(XIN)/16, and reset state is released by the timer 4 overflow signal.

Fig.8.12.2 Reset Sequence

8.13 CLOCK GENERATING CIRCUIT

The built-in clock generating circuit is shown in Figure 8.13.3. When the STP instruction is executed, the internal clock ϕ stops at HIGH. At the same time, timers 3 and 4 are connected by hardware and "FF16" is set in timer 3 and "0716" is set in the timer 4. Select f(XIN)/16 as the timer 3 count source (set bit 0 of the timer mode register 2 to "0" before the execution of the STP instruction). Moreover, set the timer 3 and timer 4 interrupt enable bits to disabled ("0") before execution of the STP instruction). The oscillator restarts when external interrupt is accepted. However, the internal clock ϕ keeps its HIGH until timer 4 overflows, allowing time for oscillation stabilization when a ceramic resonator or a quartz-crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the HIGH but the oscillator continues running. This wait state is released when an interrupt is accepted (See note). Since the oscillator does not stop, the next instruction can be executed at once.

When returning from the stop or the wait state, to accept an interrupt, set the corresponding interrupt enable bit to "1" before executing the STP or the WIT instructions.

Note: In the wait mode, the following interrupts are invalid.
- VSYNC interrupt
- OSD interrupt
- Timer 2 interrupt using external clock input from TIM2 pin as count source
- Timer 3 interrupt using external clock input from TIM3 pin as count source
- Timer 4 interrupt using f(XIN)/2 as count source
- Timer 1 interrupt using f(XIN)/4096 as count source
- f(XIN)/4096 interrupt
- Multi-master I2C-BUS interface interrupt
- A-D conversion interrupt
- SPRITE interrupt

A circuit example using a ceramic resonator (or a quartz-crystal oscillator) is shown in Figure 8.13.1. Use the circuit constants in accordance with the resonator manufacture's recommended values. A circuit example with external clock input is shown in Figure 8.13.2. Input the clock to the XIN pin, and open the XOUT pin.

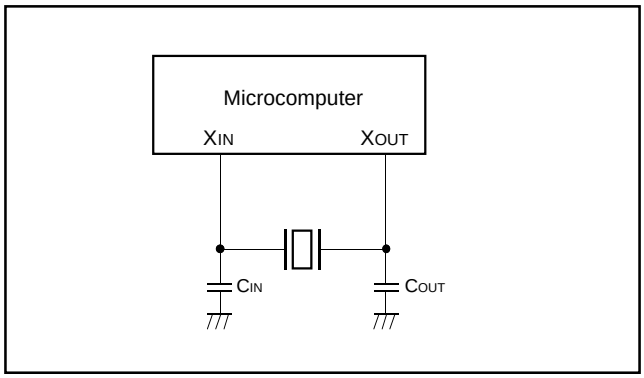


Fig.8.13.1 Ceramic Resonator Circuit Example

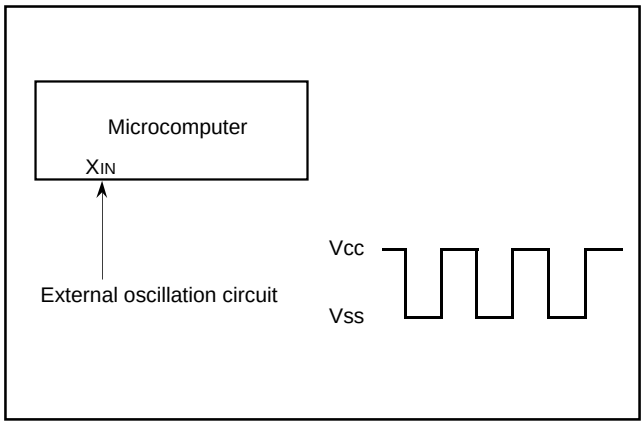


Fig.8.13.2 External Clock Input Circuit Example

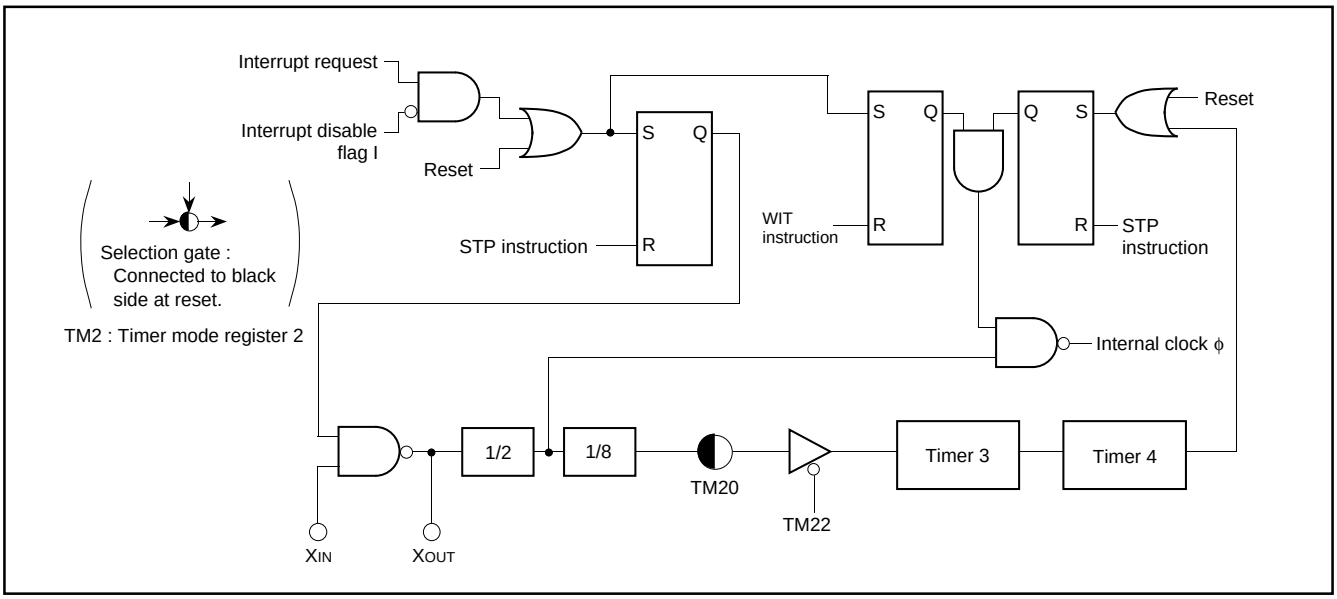


Fig.8.13.3 Clock Generating Circuit Block Diagram

8.14 DISPLAY OSCILLATION CIRCUIT

The OSD oscillation circuit has a built-in clock oscillation circuits, so that a clock for OSD can be obtained simply by connecting an LC, a ceramic resonator, or a quartz-crystal oscillator across the pins OSC1 and OSC2. Which of the sub-clock or the OSD oscillation circuit is selected by setting bits 0 and 1 of the interrupt input polarity register (address $00CD_{16}$).

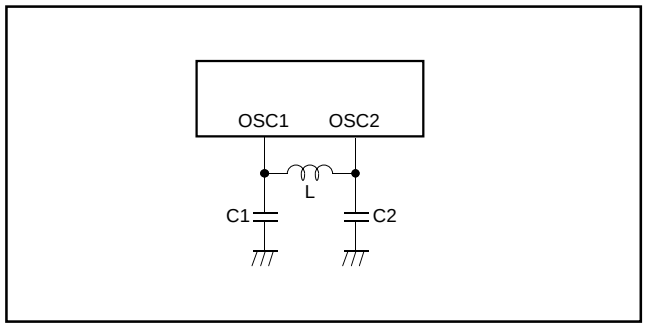
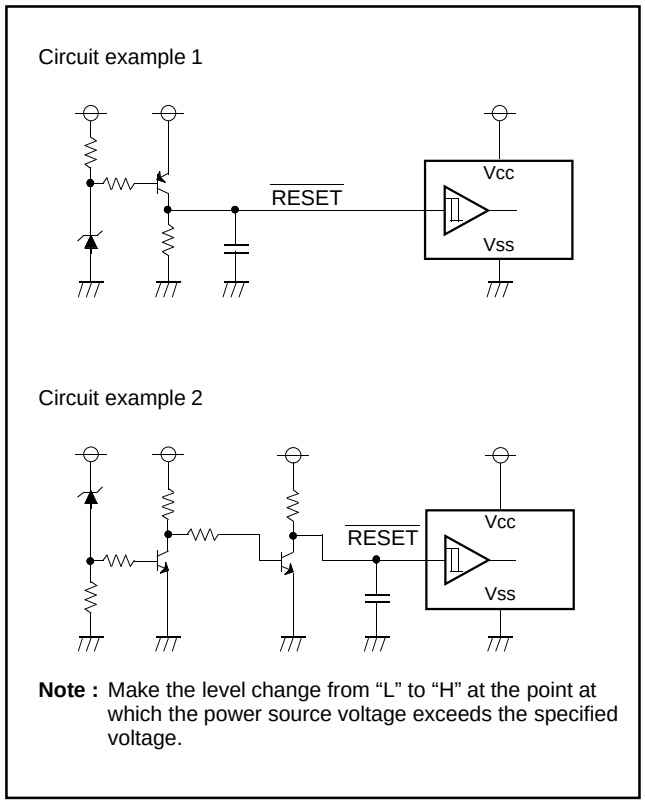


Fig.8.14.1 Display Oscillation Circuit

8.15 AUTO-CLEAR CIRCUIT

When a power source is supplied, the auto-clear function will operate by connecting the following circuit to the $\overline{\text{RESET}}$ pin.



Note : Make the level change from "L" to "H" at the point at which the power source voltage exceeds the specified voltage.

Fig.8.15.1 Auto-clear Circuit Example

8.16 ADDRESSING MODE

The memory access is reinforced with 17 kinds of addressing modes. Refer to SERIES 740 <Software> User's Manual for details.

8.17 MACHINE INSTRUCTIONS

There are 71 machine instructions. Refer to SERIES 740 <Soft- ware> User's Manual for details.

9. PROGRAMMING NOTES

• The divide ratio of the timer is 1/(n+1).

- Even though the BBC and BBS instructions are executed immediately after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. At least one instruction cycle is needed (such as an NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- After the ADC and SBC instructions are executed (in the decimal mode), one instruction cycle (such as an NOP) is needed before the SEC, CLC, or CLD instruction is executed.
- An NOP instruction is needed immediately after the execution of a PLP instruction.
- In order to avoid noise and latch-up, connect a bypass capacitor (≈ 0.1µF) directly between the V_{CC} pin–V_{SS} pin, AV_{CC} pin–V_{SS} pin, and the V_{CC} pin–CNV_{SS} pin, using a thick wire.

10. ABSOLUTE MAXIMUM RATINGS

Symbol	Parametear		Conditions	Ratings	Unit
V_{CC}, AV_{CC}	Power source voltage	V_{CC}	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 6	V
V_I	Input voltage	CNV_{SS}		–0.3 to 6	V
V_I	Input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_5$, OSC1, X_{IN}, $P5_0$, $P5_1$, $\overline{RESET}$		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage	$P0_6$, $P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_2$, $P3_5$, $P5_2$–$P5_5$, X_{OUT}, OSC2		–0.3 to V_{CC} + 0.3	V
V_O	Output voltage	$P0_0$–$P0_5$		–0.3 to 13	V
I_{OH}	Circuit current	$P5_2$–$P5_5$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$, $P3_5$		0 to 1 (See note 1)	mA
I_{OL1}	Circuit current	$P5_2$–$P5_5$, $P0_6$, $P0_7$, $P1_0$, $P1_5$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_2$, $P3_5$		0 to 2 (See note 2)	mA
I_{OL2}	Circuit current	$P1_1$–$P1_4$		0 to 6 (See note 2)	mA
I_{OL3}	Circuit current	$P0_0$–$P0_5$		0 to 1 (See note 2)	mA
I_{OL4}	Circuit current	$P2_4$, $P2_7$		0 to 10 (See note 3)	mA
P_d	Power dissipation		T_a = 25 °C	550	mW
T_{opr}	Operating temperature			–10 to 70	°C
T_{stg}	Storage temperature			–40 to 125	°C

11. RECOMMENDED OPERATING CONDITIONS (T_a = –10 °C to 70 °C, V_{CC} = 5 V ± 10 %, unless otherwise noted)

Symbol	Parameter			Limits			Unit
				Min.	Typ.	Max.	
V_{CC}	Power source voltage (See note 4), During CPU, OSD, data slicer operation			4.5	5.0	5.5	V
V_{SS}	Power source voltage			0	0	0	V
V_{IH1}	HIGH input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_5$, S_{IN}, S_{CLK}, $P5_0$, $P5_1$, $\overline{RESET}$, X_{IN}, OSC1, TIM2, TIM3, INT1–INT3		0.8V_{CC}		V_{CC}	V
V_{IH2}	HIGH input voltage	SCL1, SCL2, SDA1, SDA2		0.7V_{CC}		V_{CC}	V
V_{IL1}	LOW input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_5$		0		0.4 V_{CC}	V
V_{IL2}	LOW input voltage	SCL1, SCL2, SDA1, SDA2		0		0.3 V_{CC}	V
V_{IL3}	LOW input voltage (See note 6)	$P5_0$, $P5_1$, $\overline{RESET}$, TIM2, TIM3, INT1–INT3, X_{IN}, OSC1, S_{IN}, S_{CLK}		0		0.2 V_{CC}	V
I_{OH}	HIGH average output current (See note 1)	$P5_2$–$P5_5$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$, $P3_5$				1	mA
I_{OL1}	LOW average output current (See note 2)	$P5_2$–$P5_5$, $P0_6$, $P0_7$, $P1_0$, $P1_5$–$P1_7$, $P3_0$–$P3_2$, $P3_5$				2	mA
I_{OL2}	LOW average output current (See note 2)	$P1_1$–$P1_4$				6	mA
I_{OL3}	LOW average output current (See note 2)	$P0_0$–$P0_5$				1	mA
I_{OL4}	LOW average output current (See note 3)	$P2_4$–$P2_7$				10	mA
f(X_{IN})	Oscillation frequency (for CPU operation) (See note 5)	X_{IN}		7.9	8.0	8.1	MHz
fosc	Oscillation frequency (for OSD)	OSC1	RC oscillating mode	5.0	8.0	9.0	MHz
			LC oscillating mode	5.0	8.0	17.0	
			Ceramic oscillating mode	7.9	8.0	8.1	
f_{hs1}	Input frequency	TIM2, TIM3				100	kHz
f_{hs2}	Input frequency	S_{CLK}				1	MHz
f_{hs3}	Input frequency	SCL1, SCL2				400	MHz

12. ELECTRIC CHARACTERISTICS (V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, f(X_{IN}) = 8 MHz, T_a = –10 °C to 70 °C, unless otherwise noted)

Symbol	Parameter		Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit	Test circuit
I_{CC}	Power source current	System operation	V_{CC} = 5.5 V, f(X_{IN}) = 8 MHz	OSD OFF		20	40	mA	1
				OSD ON		30	60		
		Stop mode	V_{CC} = 5.5 V, f(X_{IN}) = 0				300	mA	
V_{OH}	HIGH output voltage	$P5_2$–$P5_5$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$, $P3_5$	V_{CC} = 4.5 V, I_{OH} = –0.5 mA		2.4			V	2
V_{OL}	LOW output voltage	$P5_2$–$P5_5$, $P0_0$–$P0_7$, $P1_0$, $P1_5$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_2$, $P3_5$	V_{CC} = 4.5 V, I_{OL} = 0.5 mA				0.4	V	
	LOW output voltage	$P2_4$–$P2_7$	V_{CC} = 4.5 V, I_{OL} = 10.0 mA				3.0		
	LOW output voltage	$P1_1$–$P1_4$	V_{CC} = 4.5 V	I_{OL} = 3 mA			0.4		
				I_{OL} = 6 mA			0.6		
V_{T+} – V_{T-}	Hysteresis (See note 6)	$\overline{RESET}$, $P5_0$, $P5_1$, TIM2, TIM3, INT1–INT3, SCL1, SCL2, SDA1, SDA2, S_{IN}, S_{CLK}	V_{CC} = 5.0 V			0.5	1.3	V	3
I_{IZH}	HIGH input leak current	$\overline{RESET}$, $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_5$, $P5_0$, $P5_1$	V_{CC} = 5.5 V, V_I = 5.5 V				5	µA	4
I_{IZL}	LOW input leak current	$\overline{RESET}$, $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_5$, $P5_0$, $P5_1$	V_{CC} = 5.5 V, V_I = 0 V				5	µA	
I_{OZH}	HIGH input leak current	$P0_0$–$P0_5$	V_{CC} = 5.5 V, V_I = 12 V				10	µA	5
R_{BS}	I^2C-BUS·BUS switch connection resistor (between SCL1 and SCL2, SDA1 and SDA2)		V_{CC} = 4.5 V				130	Ω	6

Notes 1: The total current that flows out of the IC must be 20 mA or less.

2: The total input current to IC (I_{OL1} + I_{OL2} + I_{OL3}) must be 30 mA or less.

3: The total average input current for ports $P2_4$–$P2_7$ to IC must be 20 mA or less.

4: Connect 0.1 µF or more capacitor externally between the power source pins V_{CC}–V_{SS} so as to reduce power source noise. Also connect 0.1 µF or more capacitor externally between the pins V_{CC}–CNV_{SS}.

5: Use a quartz-crystal oscillator or a ceramic resonator for the CPU oscillation circuit. When using the data slicer, use 8 MHz.

6: $P0_6$, $P0_7$, $P1_5$, $P2_3$, $P2_4$ have the hysteresis when these pins are used as interrupt input pins or timer input pins. $P1_1$–$P1_4$ have the hysteresis when these pins are used as multi-master I^2C-BUS interface ports. $P2_0$–$P2_2$ have the hysteresis when these pins are used as serial I/O pins.

7: Pin names in each parameter is described as below.

(1) Dedicated pins: dedicated pin names.

(2) Duble-/triple-function ports

- When the same limits: I/O port name.
- When the limits of functins except ports are different from I/O port limits: function pin name.

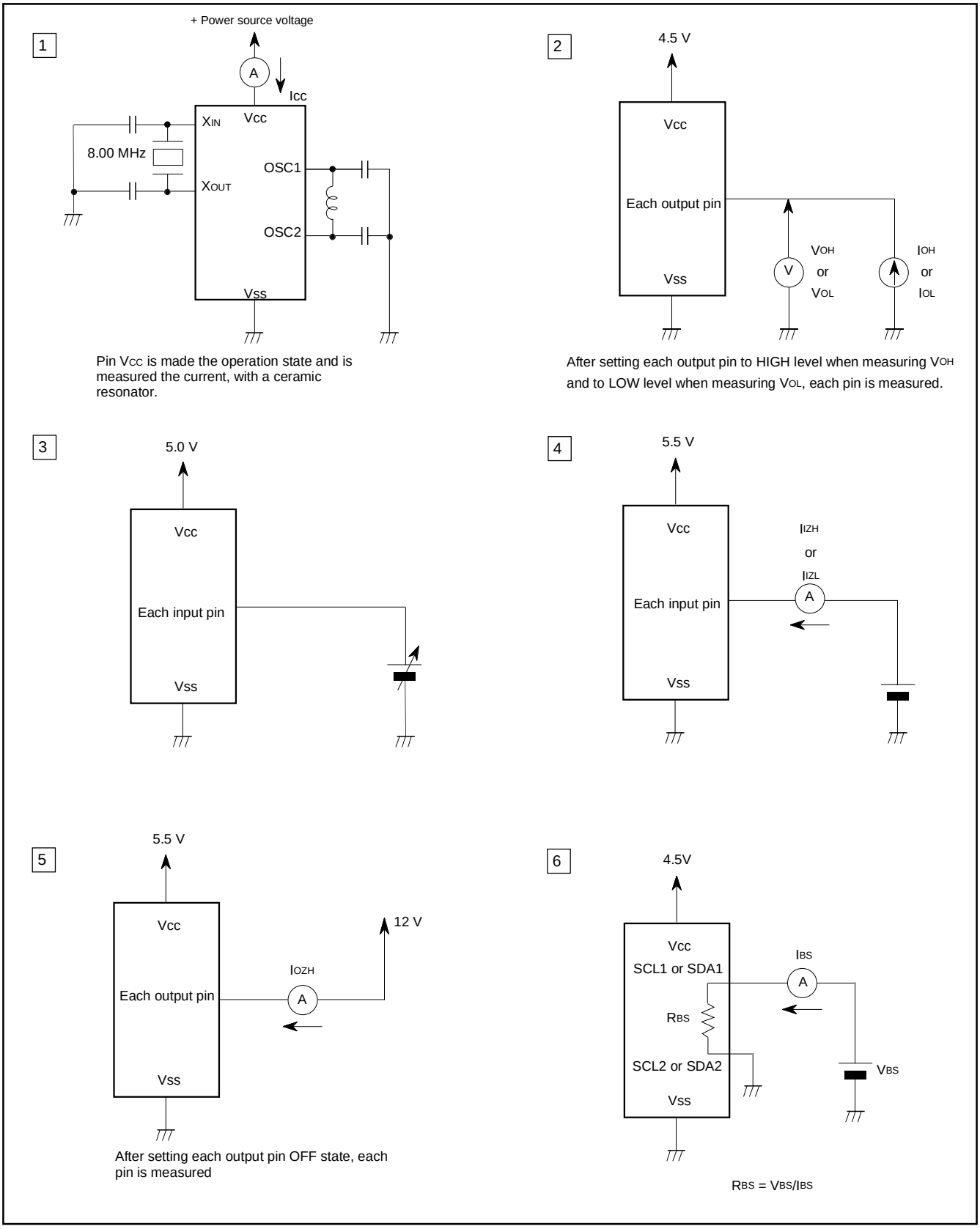


Fig.12.1 Measure Circuits

13. A-D CONVERTER CHARACTERISTICS

(V_{CC} = 5 V ± 10 %, V_{SS} = 0 V, f(X_{IN}) = 8 MHz, T_a = –10 °C to 70 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	bits
—	Absolute accuracy (excludig guantization error)	Vcc = 5 V			±2.5	LSB
T_{CONV}	Conversion time		12.25		12.5	µs
R_{LADDER}	Ladder resistor			25		kΩ
V_{IA}	Analog input voltage		0		V_{REF}	V

14. MULTI-MASTER I²C-BUS BUS LINE CHARACTERISTICS

Symbol	Parameter	Standard clock mode		High-speed clock mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		µs
$t_{HD;STA}$	Hold time for START condition	4.0		0.6		µs
t_{LOW}	LOW period of SCL clock	4.7		1.3		µs
t_R	Rising time of both SCL and SDA signals		1000	20+0.1C_b	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	µs
t_{HIGH}	HIGH period of SCL clock	4.0		0.6		µs
t_F	Falling time of both SCL and SDA signals		300	20+0.1C_b	300	ns
$t_{SU;DAT}$	Data set-up time	250		100		ns
$t_{SU;STA}$	Set-up time for repeated START condition	4.7		0.6		µs
$t_{SU;STO}$	Set-up time for STOP condition	4.0		0.6		µs

Note: C_b = total capacitance of 1 bus line

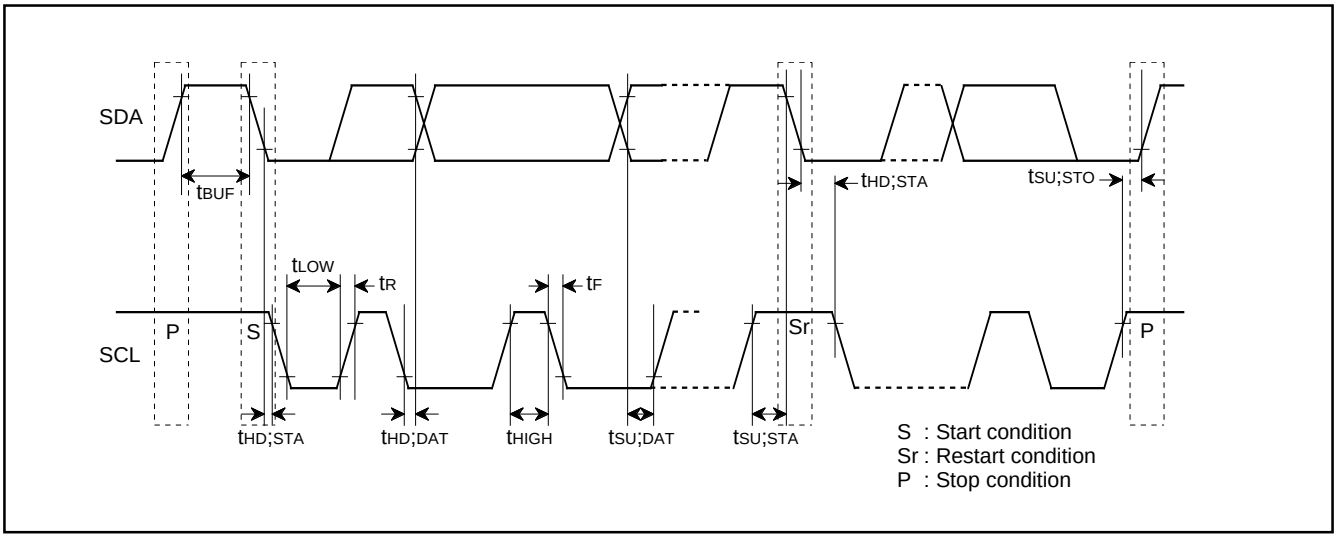


Fig.14.1 Definition Diagram of Timing on Multi-master I²C-BUS

15. PROM PROGRAMMING METHOD

The built-in PROM of the One Time PROM version (blank) and the built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter.

Product	Name of Programming Adapter
M37225ECSP	PCA7408

The PROM of the One Time PROM version (blank) is not tested or screened in the assembly process nor any following processes. To ensure proper operation after programming, the procedure shown in Figure 15.1 is recommended to verify programming.

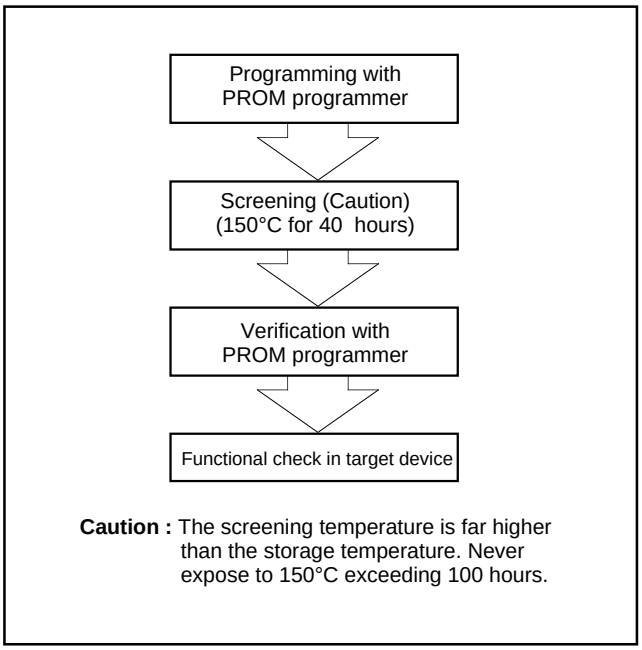


Fig. 15.1 Programming and Testing of One Time PROM Version

16. DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

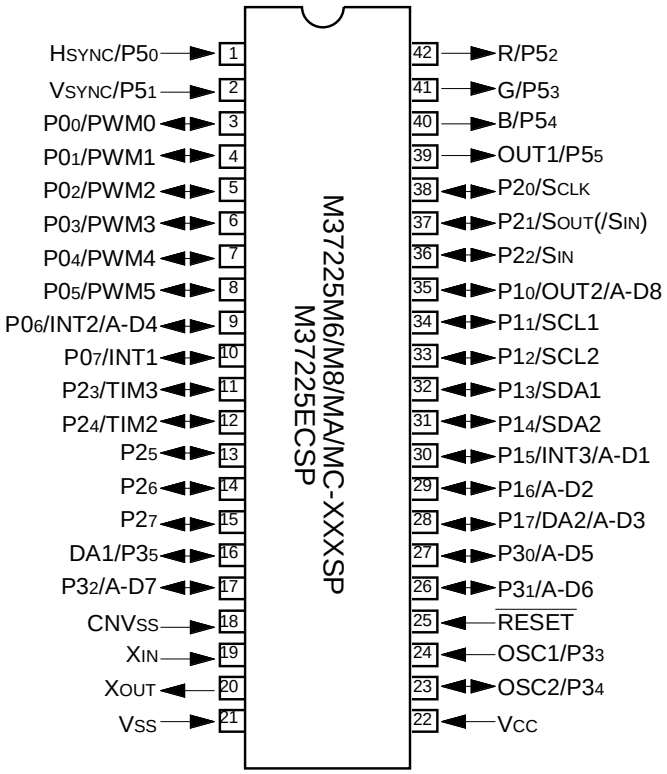
- Mask ROM Order Confirmation Form
- Mark Specification Form
- Data to be written to ROM, in EPROM form (32-pin DIP Type 27C101, three identical copies) or FDK

17. ONE TIME PROM VERSION M37225ECSP MARKING

XXXXXX is lot number

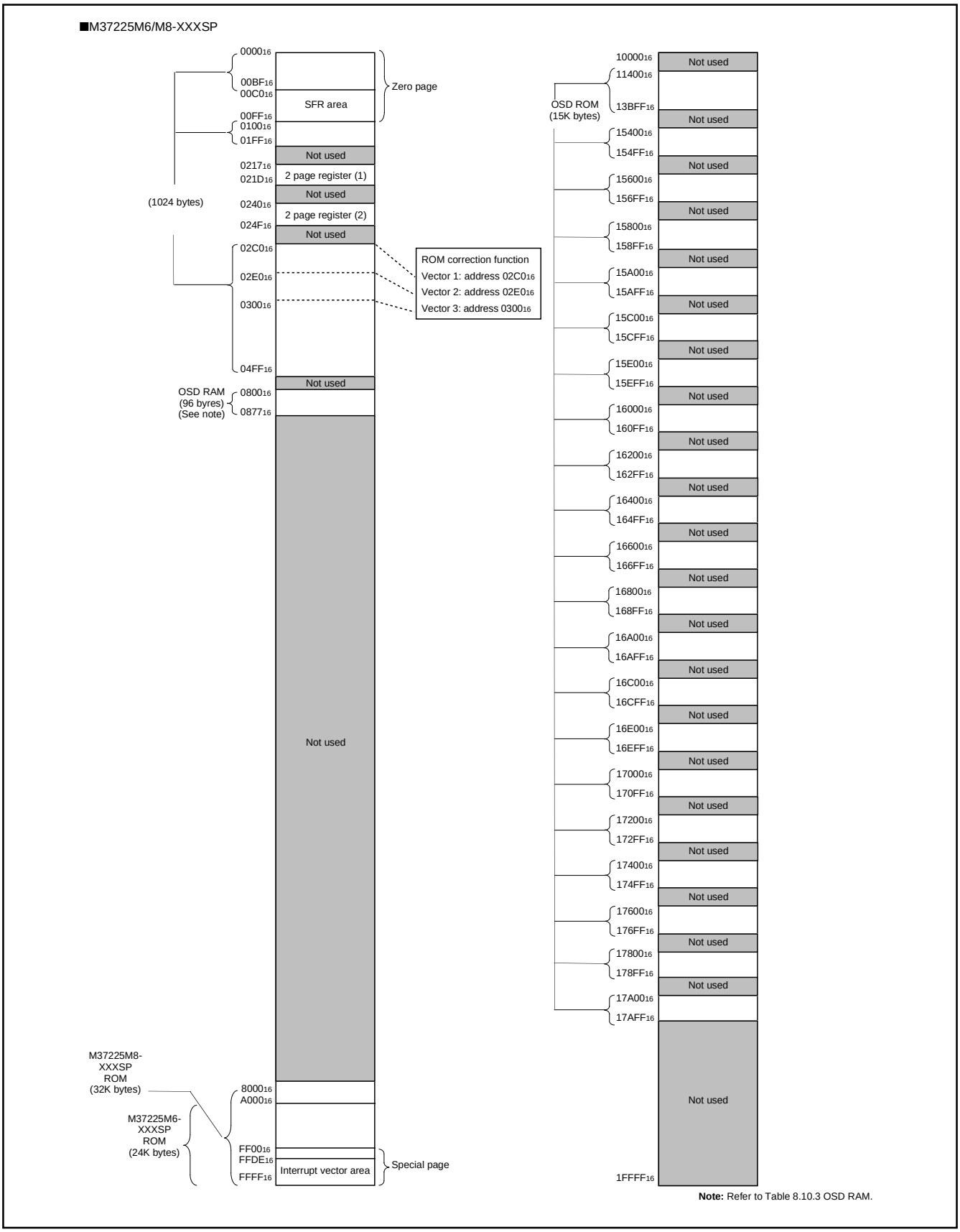
18. APPENDIX

Pin Configuration (TOP VIEW)



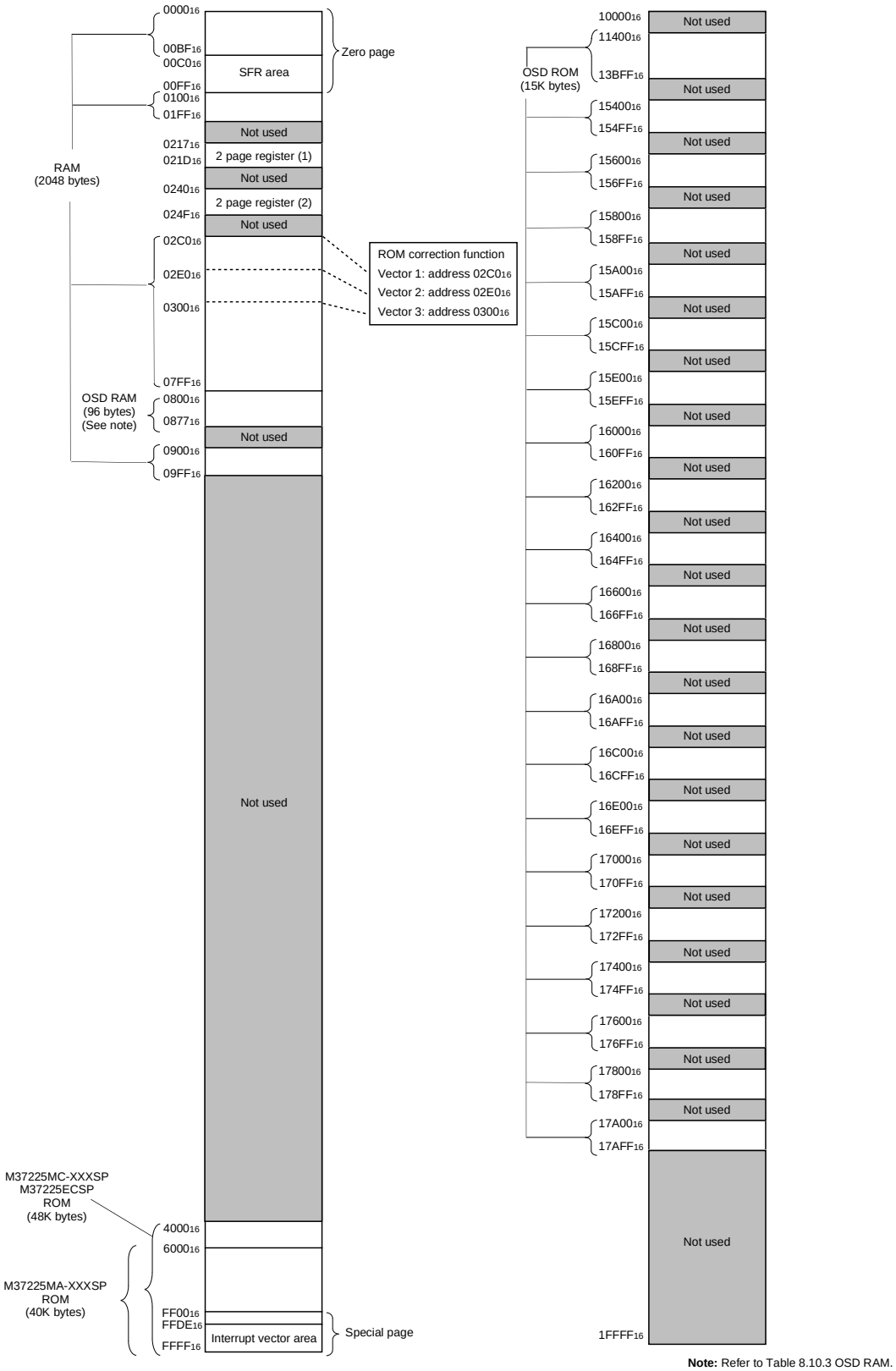
Outline 42P4B

Memory Map



Note: Refer to Table 8.10.3 OSD RAM.

■M37225MA/MC-XXXSP, M37225ECSP



Note: Refer to Table 8.10.3 OSD RAM.

Memory Map of Special Function Register (SFR)

■ SFR area (addresses $C0_{16}$ to DF_{16})

< Bit allocation >

: } Function bit

Name :

: No function bit

0 : Fix to this bit to "0" (do not write to "1")

1 : Fix to this bit to "1" (do not write to "0")

< State immediately after reset >

0 : "0" immediately after reset

1 : "1" immediately after reset

? : Indeterminate immediately after reset

Address	Register	Bit allocation b7							b0	State immediately after reset b7							b0
$C0_{16}$	Port P0 (P0)									?							
$C1_{16}$	Port P0 direction register (D0)									00_{16}							
$C2_{16}$	Port P1 (P1)									?							
$C3_{16}$	Port P1 direction register (D1)									00_{16}							
$C4_{16}$	Port P2 (P2)									?							
$C5_{16}$	Port P2 direction register (D2)									00_{16}							
$C6_{16}$	Port P3 (P3)			P35	P34IN	P33IN	P32	P31	P30	?							
$C7_{16}$	Port P3 direction register (D3)	P31S	P30S	P35D			P32D	P31D	P30D	0	0	0	?	?	0	0	0
$C8_{16}$										?							
$C9_{16}$	Port P35 output mode control register (P3S)	0	0	P35S						0	0	0	0	?	?	?	?
CA_{16}	Port P5 (P5)			P55 OUT	P54 OUT	P53 OUT	P52 OUT	P51 IN	P50 IN	0	0	?	?	?	?	?	?
CB_{16}	OSD port control register (PF)	0	OUT2 SEL	P55 SEL	P54 SEL	P53 SEL	P52 SEL	0	0	00_{16}							
CC_{16}	Test register					1	1			0	0	0	0	1	1	?	?
CD_{16}	Interrupt input polarity register (IP)	0	0	POL3	POL2	POL1	0	OCG1	OCG0	00_{16}							
CE_{16}	DA1-H register (DA1-H)									?							
CF_{16}	DA1-L register (DA1-L)									0	0	?	?	?	?	?	?
$D0_{16}$	PWM0 register (PWM0)									?							
$D1_{16}$	PWM1 register (PWM1)									?							
$D2_{16}$	PWM2 register (PWM2)									?							
$D3_{16}$	PWM3 register (PWM3)									?							
$D4_{16}$	PWM4 register (PWM4)									?							
$D5_{16}$	PWM output control register 1 (PW)	PW7	PW6	PW5	PW4	PW3	PW2	PW1	PW0	00_{16}							
$D6_{16}$	PWM output control register 2 (PN)	0	0	PN5	PN4	PN3	PN2	0	0	00_{16}							
$D7_{16}$	I^2C data shift register (S0)	D7	D6	D5	D4	D3	D2	D1	D0	?							
$D8_{16}$	I^2C address register (S0D)	SAD6	SAD5	SAD4	SAD3	SAD2	SAD1	SAD0	RBW	00_{16}							
$D9_{16}$	I^2C status register (S1)	MST	TRX	BB	PIN	AL	AAS	AD0	LRB	0	0	0	1	0	0	0	?
DA_{16}	I^2C control register (S1D)	BSEL1	BSEL0	10BIT SAD	ALS	ESO	BC2	BC1	BC0	00_{16}							
DB_{16}	I^2C clock control register (S2)	ACK	ACK BIT	FAST MODE	CCR4	CCR3	CCR2	CCR1	CCR0	00_{16}							
DC_{16}	Serial I/O mode register (SM)		SM6	SM5	0	SM3	SM2	SM1	SM0	00_{16}							
DD_{16}	Serial I/O register (SIO)									?							
DE_{16}	AD conversion register (AD)									?							
DF_{16}	AD control register (ADCON)	0		0	ADVREF	ADSTR	ADIN2	ADIN1	ADIN0	08_{16}							

■ SFR area (addresses $E0_{16}$ to FF_{16})

< Bit allocation >

: Function bit

Name :

: No function bit

0 : Fix to this bit to “0” (do not write to “1”)

1 : Fix to this bit to “1” (do not write to “0”)

< State immediately after reset >

0 : “0” immediately after reset

1 : “1” immediately after reset

? : Indeterminate immediately after reset

Address	Register	Bit allocation b7							b0	State immediately after reset b7							b0
$E0_{16}$	Block H register (BHP)			BHP5	BHP4	BHP3	BHP2	BHP1	BHP0	00_{16}							
$E1_{16}$	Block 1V register (B1VP)	B1VP7	B1VP6	B1VP5	B1VP4	B1VP3	B1VP2	B1VP1	B1VP0	?							
$E2_{16}$	Block 2V register (B2VP)	B2VP7	B2VP6	B2VP5	B2VP4	B2VP3	B2VP2	B2VP1	B2VP0	?							
$E3_{16}$	SPRITE control register (SC)	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00_{16}							
$E4_{16}$	SPRITE H register (SHP)	SHP7	SHP6	SHP5	SHP4	SHP3	SHP2	SHP1	SHP0	00_{16}							
$E5_{16}$	SPRITE V register (SVP)	SVP7	SVP6	SVP5	SVP4	SVP3	SVP2	SVP1	SVP0	?							
$E6_{16}$	Color register 1 (CO1)		CO16	CO15	CO14	CO13	CO12	CO11	CO10	0	?	?	?	?	?	?	?
$E7_{16}$	Color register 2 (CO2)		CO26	CO25	CO24	CO23	CO22	CO21	CO20	0	?	?	?	?	?	?	?
$E8_{16}$	Color register 3 (CO3)		CO36	CO35	CO34	CO33	CO32	CO31	CO30	0	?	?	?	?	?	?	?
$E9_{16}$	Color register 4 (CO4)		CO46	CO45	CO44	CO43	CO42	CO41	CO40	0	?	?	?	?	?	?	?
EA_{16}	OSD control register (OC)	OC7	OC6	OC5	OC4	OC3	OC2	OC1	OC0	00_{16}							
EB_{16}	OSD I/O polarity control register (OPC)	OPC7	OPC6	OPC5	OPC4	OPC3	OPC2	OPC1	OPC0	00_{16}							
EC_{16}	Color register 5 (CO5)		CO56	CO55	CO54	CO53	CO52	CO51	CO50	0	?	?	?	?	?	?	?
ED_{16}	Color register 6 (CO6)		CO66	CO65	CO64	CO63	CO62	CO61	CO60	0	?	?	?	?	?	?	?
EE_{16}	Color register 7 (CO7)		CO76	CO75	CO74	CO73	CO72	CO71	CO70	0	?	?	?	?	?	?	?
EF_{16}	Color register 8 (CO8)		CO86	CO85	CO84	CO83	CO82	CO81	CO80	0	?	?	?	?	?	?	?
$F0_{16}$	Timer 1 (T1)									FF_{16}							
$F1_{16}$	Timer 2 (T2)									07_{16}							
$F2_{16}$	Timer 3 (T3)									FF_{16}							
$F3_{16}$	Timer 4 (T4)									07_{16}							
$F4_{16}$	Timer mode register 1 (TM1)			TM15	TM14	TM13	TM12	TM11	TM10	00_{16}							
$F5_{16}$	Timer mode register 2 (TM2)			TM25	TM24	TM23	TM22	TM21	TM20	00_{16}							
$F6_{16}$	PWM5 register (PWM5)									?							
$F7_{16}$	Test register	00_{16}								?							
$F8_{16}$	Test register	00_{16}								?							
$F9_{16}$	Block 1 control register (B1C)				B1C4	B1C3	B1C2	B1C1	B1C0	0	0	0	?	?	?	?	?
FA_{16}	Block 2 control register (B2C)				B2C4	B2C3	B2C2	B2C1	B2C0	0	0	0	?	?	?	?	?
FB_{16}	CPU mode register (CM)	0	0	1	1	1	CM2	0	0	$3C_{16}$							
FC_{16}	Interrupt request register 1 (IREQ1)	IT3R	IICR	VSCR	OSDR	TM4R	TM3R	TM2R	TM1R	00_{16}							
FD_{16}	Interrupt request register 2 (IREQ2)	0	ADR		MSR	SPR	S1R	IT2R	IT1R	00_{16}							
FE_{16}	Interrupt control register 1 (ICON1)	IT3E	IICE	VSCE	OSDE	TM4E	TM3E	TM2E	TM1E	00_{16}							
FF_{16}	Interrupt control register 2 (ICON2)		ADE	0	MSE	SPE	S1E	IT2E	IT1E	00_{16}							

■ 2 page register area (addresses 210_{16} to $21F_{16}$, 240_{16} to $24F_{16}$)

< Bit allocation >

: } Function bit
Name :

: No function bit

0 : Fix to this bit to "0" (do not write to "1")

1 : Fix to this bit to "1" (do not write to "0")

< State immediately after reset >

0 : "0" immediately after reset

1 : "1" immediately after reset

? : Indeterminate immediately after reset

Address	Register	Bit allocation b7 b0	State immediately after reset b7 b0
210_{16}			?
211_{16}			?
212_{16}			?
213_{16}			?
214_{16}			?
215_{16}			?
216_{16}			?
217_{16}	ROM correction address 1 (high-order)		00_{16}
218_{16}	ROM correction address 1 (low-order)		00_{16}
219_{16}	ROM correction address 2 (high-order)		00_{16}
$21A_{16}$	ROM correction address 2 (low-order)		00_{16}
$21B_{16}$	ROM correction enable register (RCR)	0 0 0 0 0 RCR2 RCR1 RCR0	00_{16}
$21C_{16}$	ROM correction address 3 (high-order)		00_{16}
$21D_{16}$	ROM correction address 3 (low-order)		00_{16}
$21E_{16}$			?
$21F_{16}$			?
240_{16}	Left border control register (LBR)	LBR6 LBR5 LBR4 LBR3 LBR2 LBR1 LBR0	00_{16}
241_{16}	Right border control register (RBR)	RBR6 RBR5 RBR4 RBR3 RBR2 RBR1 RBR0	00_{16}
242_{16}			?
243_{16}			?
244_{16}			?
245_{16}	Top border control register (TBR)	TBR7 TBR6 TBR5 TBR4 TBR3 TBR2 TBR1 TBR0	?
246_{16}	Bottom border control register (BBR)	BBR7 BBR6 BBR5 BBR4 BBR3 BBR2 BBR1 BBR0	?
247_{16}	Test register	00_{16}	00_{16}
248_{16}			?
249_{16}			?
$24A_{16}$			?
$24B_{16}$			?
$24C_{16}$			?
$24D_{16}$			?
$24E_{16}$	DA2-H register (DA2H)		?
$24F_{16}$	DA2-L register (DA2L)		0 0 ? ? ? ? ? ?

Internal State of Processor Status Register and Program Counter at Reset

< Bit allocation >

: Function bit

Name :

: No function bit

0 : Fix to this bit to “0” (do not write to “1”)

1 : Fix to this bit to “1” (do not write to “0”)

< State immediately after reset >

0 : “0” immediately after reset

1 : “1” immediately after reset

? : Indeterminate immediately after reset

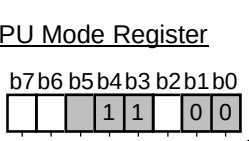
Register	Bit allocation								State immediately after reset							
	b7							b0	b7							b0
Processor status register (PS)	N	V	T	B	D	I	Z	C	?	?	?	?	?	1	?	?
Program counter (PCH)									Contents of address FFFF16							
Program counter (PCL)									Contents of address FFFE16							

Structure of Register

The figure of each register structure describes its functions, contents at reset, and attributes as follows:

<Example>

CPU Mode Register



Bit position **Bit attributes** (Note 2)

Values immediately after reset release (Note 1)

CPU mode register (CPUM) (CM) [Address 00FB16]

B	Name	Functions	After re	R W
0, 1	Processor mode bits (CM0, CM1)	b1 b0 0 0: Single-chip mode 0 1: 1 0: 1 1: } Not available	0	R W
2	Stack page selection bit (See note) (CM2)	0: 0 page 1: 1 page	1	R W
3, 4	Fix these bits to “1.”		1	R W
5	Nothing is assigned. This bit is write disable bit. When this bit is read out, the value is “1.”		1	R W
6, 7	Clock switch bits (CM6, CM7)	b7 b6 0 0: f(XIN) = 8 MHz 0 1: f(XIN) = 12 MHz 1 0: f(XIN) = 16 MHz 1 1: Do not set	0	R W

: Bit in which nothing is assigned

Notes 1: Values immediately after reset release
0 ••••••••••••••••••“0” after reset release
1 ••••••••••••••••••“1” after reset release
Indeterminate•••Indeterminate after reset release

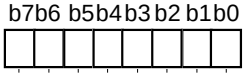
2: Bit attributes••••••The attributes of control register bits are classified into 3 types : read-only, write-only and read and write. In the figure, these attributes are represented as follows :

R••••••Read
R ••••••Read enabled
– ••••••Read disabled

W••••••Write
W ••••••Write enabled
– ••••••Write disabled
✻ ••••••“0” can be set by software, but “1” cannot be set.

Addresses 00C1$_{16}$, 00C3$_{16}$, 00C5$_{16}$

Port Pi Direction Register

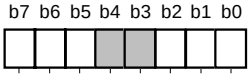


Port Pi direction register (Di) (i=0,1,2) [Addresses 00c1$_{16}$,00C3$_{16}$,00C5$_{16}$]

b	Name	Functions	After reset	R	W
0	Port Pi direction register	0 : Port Pi$_0$ input mode 1 : Port Pi$_0$ output mode	0	R	W
1		0 : Port Pi$_1$ input mode 1 : Port Pi$_1$ output mode	0	R	W
2		0 : Port Pi$_2$ input mode 1 : Port Pi$_2$ output mode	0	R	W
3		0 : Port Pi$_3$ input mode 1 : Port Pi$_3$ output mode	0	R	W
4		0 : Port Pi$_4$ input mode 1 : Port Pi$_4$ output mode	0	R	W
5		0 : Port Pi$_5$ input mode 1 : Port Pi$_5$ output mode	0	R	W
6		0 : Port Pi$_6$ input mode 1 : Port Pi$_6$ output mode	0	R	W
7		0 : Port Pi$_7$ input mode 1 : Port Pi$_7$ output mode	0	R	W

Address 00C7$_{16}$

Port P3 Direction Register



Port P3 direction register (D3) [Address 00C7$_{16}$]

B	Name	Functions	After reset	R	W
0	Port P3 direction register	0 : Port P3$_0$ input mode 1 : Port P3$_0$ output mode	0	R	W
1		0 : Port P3$_1$ input mode 1 : Port P3$_1$ output mode	0	R	W
2		0 : Port P3$_2$ input mode 1 : Port P3$_2$ output mode	0	R	W
3, 4	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are indeterminate.		indeterminate	R	—
5	Port P3 direction register	0 : Port P3$_5$ input mode 1 : Port P3$_5$ output mode	0	R	W
6	Port P3$_0$ output mode selection bit (P30S)	0 : CMOS output 1 : N-channel open-drain output	0	R	W
7	Port P3$_1$ output mode selection bit (P31S)	0 : CMOS output 1 : N-channel open-drain output	0	R	W

Address 00C9$_{16}$

Port P3$_5$ Output Mode Control Register

b7	b6	b5	b4	b3	b2	b1	b0
0	0		0				

Port P3$_5$ output mode control register (P3S) [Address 00C9$_{16}$]

B	Name	Functions	After reset	R	W
0 to 3	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are indeterminate.		Indeterminate	R	—
4	Fix this bit to "0"		0	R	W
5	Port P3$_5$ output mode selection bit (P35S)	0 : CMOS output 1 : N-channel open-drain output	0	R	W
6, 7	Fix these bits to "0"		0	R	W

Address 00CB$_{16}$

OSD Port Control Register

b7	b6	b5	b4	b3	b2	b1	b0
0						0	0

OSD port control register (PF) [Address 00CB$_{16}$]

b	Name	Functions	After reset	R	W
0, 1	Fix these bits to "0"		0	R	W
2	Port P5$_2$ output signal selection bit (P52SEL)	0 : R signal output 1 : Port P5$_2$ output	0	R	W
3	Port P5$_3$ output signal selection bit (P53SEL)	0 : G signal output 1 : Port P5$_3$ output	0	R	W
4	Port P5$_4$ output signal selection bit (P54SEL)	0 : B signal output 1 : Port P5$_4$ output	0	R	W
5	Port P5$_5$ output signal selection bit (P55SEL)	0 : OUT1 signal output 1 : Port P5$_5$ output	0	R	W
6	Port P1$_0$ output signal selection bit (OUT2SEL)	0 : Port P1$_0$ signal output 1 : OUT2 output	0	R	W
7	Fix this bit to "0"		0	R	W

Address 00CD16

Interrupt Input Polarity Register

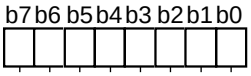
b7	b6	b5	b4	b3	b2	b1	b0
0	0				0		

Interrupt input polarity register (IP) [Address 00CD16]

b	Name	Function	After reset	R	W
0, 1	OSD clock selection bits (OCG0, OCG1)	b1 b0 Function 0 0 The clock for OSD is supplied by connecting RC or LC across the pins OSC1 and OSC2. However, it is not corresponding to the bi-scan mode. 0 1 Since the main clock is used as the clock for OSD, the oscillation frequency is limited. Because of this, the character size in width (horizonal) direction is also limited. In this case, pins OSC1 and OSC2 are also used as input ports P33 and P34 respectively. (OSD oscillation frequency = f(XIN)) 1 0 The clock for OSD is supplied by connecting LC across the pins OSC1 and OSC2. In the bi-scan mode, be sure to set this. 1 1 The clock for OSD is supplied by connecting the following across the pins OSC1 and OSC2. However, it is not corresponding to the bi-scan mode. • a ceramic resonator only for OSD and a feedback resistor • a quartz-crystal oscillator only for OSD and a feedback resistor	0	R	W
2	Fix this bit to "0."		0	R	W
3	INT1 polarity switch bit (POL1)	0 : Positive polarity 1 : Negative polarity	0	R	W
4	INT2 polarity switch bit (POL2)	0 : Positive polarity 1 : Negative polarity	0	R	W
5	INT3 polarity switch bit (POL3)	0 : Positive polarity 1 : Negative polarity	0	R	W
6, 7	Fix these bits to "0."		0	R	W

Address 00D5$_{16}$

PWM Output Control Register 1

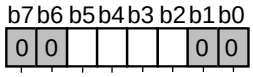


PWM output control register 1 (PW) [Address 00D5$_{16}$]

B	Name	Functions	After reset	R	W
0	DA1, DA2, PWM count source selection bit (PW0)	0 : Count source supply 1 : Count source stop	0	R	W
1	DA1 output/P3$_5$ selection bit (PW1)	0 : DA1 output 1 : P3$_5$ output	0	R	W
2	P0$_0$/PWM0 output selection bit (PW2)	0: P0$_0$ output 1: PWM0 output	0	R	W
3	P0$_1$/PWM1 output selection bit (PW3)	0: P0$_1$ output 1: PWM1 output	0	R	W
4	P0$_2$/PWM2 output selection bit (PW4)	0: P0$_2$ output 1: PWM2 output	0	R	W
5	P0$_3$/PWM3 output selection bit (PW5)	0: P0$_3$ output 1: PWM3 output	0	R	W
6	P0$_4$/PWM4 output selection bit (PW6)	0: P0$_4$ output 1: PWM4 output	0	R	W
7	P0$_5$/PWM5 output selection bit (PW7)	0: P0$_5$ output 1: PWM5 output	0	R	W

Address 00D6$_{16}$

PWM Output Control Register 2

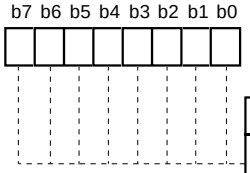


PWM output control register 2 (PN) [Address 00D6$_{16}$]

B	Name	Functions	After reset	R	W
0, 1	Fix these bits to “0.”		0	R	W
2	DA1 output polarity selection bit (PN3)	0 : Positive polarity 1 : Negative polarity	0	R	W
3	PWM output polarity selection bit (PN4)	0 : Positive polarity 1 : Negative polarity	0	R	W
4	DA2 output polarity selection bit (PN5)	0 : Output LOW 1 : Output HIGH	0	R	W
5	P1$_7$/DA2 output selection bit (PN5)	0 : P1$_7$ 1 : DA2	0	R	W
6, 7	Fix these bits to “0.”		0	R	W

Address 00D7$_{16}$

I^{2}C Data Shift Register



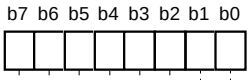
I^{2}C data shift register (S0) [Address 00D7$_{16}$]

B	Name	Functions	After reset	R	W
0 to 7	D0 to D7	This is an 8-bit shift register to store receive data and write transmit data.	Indeterminate	R	W

Note: To write data into the I^{2}C data shift register after setting the MST bit to "0" (slave mode), keep an interval of 8 machine cycles or more.

Address 00D8$_{16}$

I^{2}C Address Register

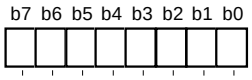


I^{2}C address register (S0D) [Address 00D8$_{16}$]

B	Name	Functions	After reset	R	W
0	$\overline{\text{Read}}$/write bit (RBW)	<Only in 10-bit addressing (in slave) mode> The last significant bit of address data is compared. 0: Wait the first byte of slave address after START condition (read state) 1: Wait the first byte of slave address after RESTART condition (write state)	0	R	—
1 to 7	Slave address (SAD0 to SAD6)	<In both modes> The address data is compared.	0	R	W

Address 00D9$_{16}$

I^{2}C Status Register



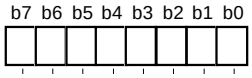
I^{2}C status register (S1) [Address 00D9$_{16}$]

B	Name	Functions	After reset	R	W
0	Last receive bit (LRB) (See note)	0 : Last bit = "0 " 1 : Last bit = "1 " (See note)	Indeterminate	R	—
1	General call detecting flag (AD0) (See note)	0 : No general call detected 1 : General call detected (See note)	0	R	—
2	Slave address comparison flag (AAS) (See note)	0 : Address mismatch 1 : Address match (See note)	0	R	—
3	Arbitration lost detecting flag (AL) (See note)	0 : Not detected 1 : Detected (See note)	0	R	—
4	I^{2}C-BUS interface interrupt request bit (PIN)	0 : Interrupt request issued 1 : No interrupt request issued	1	R	W
5	Bus busy flag (BB)	0 : Bus free 1 : Bus busy	0	R	W
6, 7	Communication mode specification bits (TRX, MST)	b7 b6 0 0 : Slave recieve mode 0 1 : Slave transmit mode 1 0 : Master recieve mode 1 1 : Master transmit mode	0	R	W

Note : These bits and flags can be read out, but cannnot be written.

Address 00DA$_{16}$

I^{2}C Control Register



I^{2}C control register (S1D) [Address 00DA$_{16}$]

B	Name	Functions	After reset	R	W
0 to 2	Bit counter (Number of transmit/recieve bits) (BC0 to BC2)	b2 b1 b0 0 0 0: 8 0 0 1: 7 0 1 0: 6 0 1 1: 5 1 0 0: 4 1 0 1: 3 1 1 0: 2 1 1 1: 1	0	R	W
3	I^{2}C-BUS interface use enable bit (ESO)	0: Disabled 1: Enabled	0	R	W
4	Data format selection bit(ALS)	0: Addressing format 1: Free data format	0	R	W
5	Addressing format selection bit (10BIT SAD)	0: 7-bit addressing format 1: 10-bit addressing format	0	R	W
6, 7	Connection control bits between I^{2}C-BUS interface and ports (BSEL0, BSEL1)	b7 b6 Connection port (See note) 0 0: None 0 1: SCL1, SDA1 1 0: SCL2, SDA2 1 1: SCL1, SDA1, SCL2, SDA2	0	R	W

Note: When using ports P11-P14 as I^{2}C-BUS interface, the output structure changes automatically from CMOS output to N-channel open-drain output.

Address 00DB16

I2C Clock Control Register

b7 b6 b5 b4 b3 b2 b1 b0

I2C clock control register (S2) [Address 00DB16]

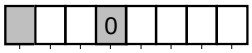
B	Name	Functions			After reset	R	W
0 to 4	SCL frequency control bits (CCR0 to CCR4)	Setup value of CCR4–CCR0	Standard clock mode	High speed clock mode	0	R	W
		00 to 02	Setup disabled	Setup disabled			
		03	Setup disabled	333			
		04	Setup disabled	250			
		05	100	400 (See note)			
		06	83.3	166			
		⋮	500/CCR value	1000/CCR value			
		1D	17.2	34.5			
		1E	16.6	33.3			
		1F	16.1	32.3			
		(at ϕ = 4 MHz, unit : kHz)					
5	SCL mode specification bit (FAST MODE)	0: Standard clock mode 1: High-speed clock mode			0	R	W
6	ACK bit (ACK BIT)	0: ACK is returned. 1: ACK is not returned.			0	R	W
7	ACK clock bit (ACK)	0: No ACK clock 1: ACK clock			0	R	W

Note: At 400 kHz in the high-speed clock mode, the duty is as below .
"0" period : "1" period = 3 : 2
In the other cases, the duty is as below.
"0" period : "1" period = 1 : 1

Address 00DC16

Serial I/O Mode Register

b7 b6 b5 b4 b3 b2 b1 b0



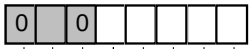
Serial I/O mode register (SM) [Address 00DC16]

B	Name	Functions	After reset	R	W
0, 1	Internal synchronous clock selection bits (SM0, SM1)	b1 b0 0 0: f(XIN)/4 0 1: f(XIN)/16 1 0: f(XIN)/32 1 1: f(XIN)/64	0	R	W
2	Synchronous clock selection bit (SM2)	0: External clock 1: Internal clock	0	R	W
3	Serial I/O port selection bit (SM3)	0: P20, P21 1: SCLK, SOUT	0	R	W
4	Fix this bit to “0.”		0	R	W
5	Transfer direction selection bit (SM5)	0: LSB first 1: MSB first	0	R	W
6	Serial input pin selection bit (SM6)	0: Input signal from SIN pin. 1: Input signal from SOUT pin.	0	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—

Address 00DF16

A-D Control Register

b7 b6 b5 b4 b3 b2 b1 b0



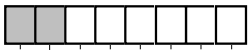
A-D control register (ADCON) [Address 00DF16]

B	Name	Functions	After reset	R	W
0 to 2	Analog input pin selection bits (ADIN0 to ADIN2)	b2 b1 b0 0 0 0 : A-D1 0 0 1 : A-D2 0 1 0 : A-D3 0 1 1 : A-D4 1 0 0 : A-D5 1 0 1 : A-D6 1 1 0 : A-D7 1 1 1 : A-D8	0	R	W
3	A-D conversion completion bit (ADSTR)	0: Conversion in progress 1: Convertion completed	1	R	W
4	VCC connection selection bit (ADVREF)	0: OFF 1: ON	0	R	W
5	Fix this bit to “0.”		0	R	W
6	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is indeterminate.		Indeterminate	R	—
7	Fix this bit to “0.”		0	R	W

Address $00E0_{16}$

Block H Register

b7 b6 b5 b4 b3 b2 b1 b0



Horizontal position register (HP) [Address $00E0_{16}$]

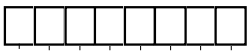
B	Name	Functions	After reset	R	W
0 to 5	Control bits of horizontal display start positions (BHP0 to BHP5) (See note 1)	Horizontal display start positions = T_{def1} + 4T_{OSC} × n (n: setting value, T_{def1}: 31T_{OSC}, T_{OSC}: OSD oscillation cycle)	0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are "0."		0	R	—

Note: The setting value synchronizes with the V_{SYNC}.

Addresses $00E1_{16}$ and $00E2_{16}$

Block i V Register

b7 b6 b5 b4 b3 b2 b1 b0



Block i V register (BiVP) (i = 1, 2) [Addresses $00E1_{16}$ and $00E2_{16}$]

B	Name	Functions	After reset	R	W
0 to 7	Control bits of vertical display start positions (BiVP0 to BiVP7) (See note 1)	Vertical display start positions = H_{def} + H × n (n: setting value, H_{def}: 17H, H: H_{SYNC})	Indeterminate	R	W

Note: Set values except "00_{16}" to BiVP.

Address 00E3$_{16}$

SPRITE Control Register

b7 b6 b5 b4 b3 b2 b1 b0

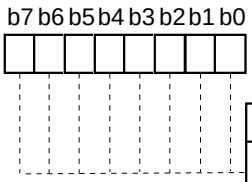
SPRITE control register (SC) [Address 00E3$_{16}$]

B	Name	Functions	After reset	R	W
0, 1	SPRITE font 1 color register specification bit (SC0, SC1)	SC1 SC0 0 0: Color register 1 0 1: Color register 2 1 0: Color register 3 1 1: Color register 4	0	R	W
2, 3	SPRITE font 2 color register specification bit (SC2, SC3)	SC3 SC2 0 0: Color register 1 0 1: Color register 2 1 0: Color register 3 1 1: Color register 4	0	R	W
4, 5	SPRITE font selection bit (SC4, SC5)	SC5 SC4 Character code: SPRITE1 / SPRITE2 0 0 F8$_{16}$ / F9$_{16}$ 0 1 FA$_{16}$ / FB$_{16}$ 1 0 FC$_{16}$ / FD$_{16}$ 1 1 FE$_{16}$ / FF$_{16}$	0	R	W
6, 7	SPRITE/raster patterning control bit (SC6, SC7) (See note)	SC7 SC6 0 0: Display OFF 0 1: Do not set 1 0: SPRITE display 1 1: Raster patterning display	0	R	W

Note : This bit is valid when bit 0 of the OSD control register to "1."

Address $00E4_{16}$

SPRITE H Register



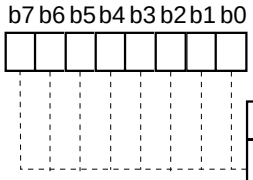
SPRITE H register (SHP) [Address $00E4_{16}$]

B	Name	Functions	After reset	R	W
0 to 7	Horizontal display start position control bits of SPRITE OSD (SHP0 to SHP7)	Horizontal display start position = T_{def2} + 2T_{OSC} × n (n: setting value, T_{def2}: 2T_{OSC}, T_{OSC}: OSD oscillation cycle)	0	R	W

Notes 1: Set values except "00_{16}" to "02_{16}" to SHP.
2: When selecting raster patterning display, setting value is synchronized with V_{SYNC} signal; when selecting SPRITE display, it is not synchronized.

Address $00E5_{16}$

SPRITE V Register



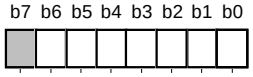
SPRITE V register (SVP) [Address $00E5_{16}$]

B	Name	Functions	After reset	R	W
0 to 7	Horizontal display start position control bits of SPRITE OSD (SVP0 to SVP7) (See note 1)	Horizontal display start position = H_{def} + H × n (n: setting value, H_{def}: 17H, H: H_{SYNC})	Indeterminate	R	W

Note: Set values except "00_{16}" to the SVP.

Addresses 00E6$_{16}$ to 00E9$_{16}$ and 00EC$_{16}$ to 00EF$_{16}$

Color Register i



Color register i (CO1 to CO8) (i=1 to 8) [Addresses 00E6$_{16}$ to 00E9$_{16}$, 00EC$_{16}$ to 00EF$_{16}$]

B	Name	Functions	After reset	R	W
0	R signal output selection bit (COi0)	0: No output 1: Output	Indeterminate	R	W
1	G signal output selection bit (COi1)	0: No output 1: Output	Indeterminate	R	W
2	B signal output selection bit (COi2)	0: No output 1: Output	Indeterminate	R	W
3	R signal output (background) selection bit (COi3)	0: No output 1: Output	Indeterminate	R	W
4	G signal output (background) selection bit (COi4)	0: No output 1: Output	Indeterminate	R	W
5	B signal output (background) selection bit (COi5)	0: No output 1: Output	Indeterminate	R	W
6	OUT1 output control bit (COi6)	0: Character output 1: Blank output	Indeterminate	R	W
7	Nothing is assined. This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—

Address 00EA16

OSD Control Register

b7 b6 b5 b4 b3 b2 b1 b0

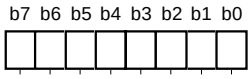
OSD control register (OC) [Address 00EA16]

B	Name	Functions	After reset	R	W
0	OSD control bit (OC0) (See note 1)	0 : All-blocks display OFF 1 : All-blocks display ON	0	R	W
1	Border type selection bit (OC1)	0 : All bordered 1 : Shadow bordered (See note 2)	0	R	W
2, 3	Window horizontal position minute adjustment bit (OC2, OC3)	b3 b2 (See notes 3 and 4) 0 0 : Standard 0 1 : Standard + 1TOSC 1 0 : Standard + 2TOSC 1 1 : Standard + 3TOSC	0	R	W
4	Window control bit (OC4)	0 : Window OFF 1 : Window ON	0	R	W
5	Scan mode selection bit (OC5)	0 : Normal scan mode 1 : Bi-scan mode (See note 5)	0	R	W
6	Raster color OUT1 control bit (OC6)	0 : No output 1 : Output	0	R	W
7	Raster color OUT2 control bit (OC7)	0 : No output 1 : Output	0	R	W

Notes 1 : Even this bit is switched during display, the display screen remains unchanged until a rising (falling) of the next VSYNC.
2 : Shadow border is output at right and bottom side of the font.
3 : TOSC = OSD oscillation cycle
4 : These bits are vallid for both left border and right border (for detail, refer to “(8) Window Function.”)
5 : When setting to bi-scan mode, connect LC between pins OSC1 and OSC2.

Address 00EB16

OSD I/O Polarity Register



OSD I/O polarity register (OPC) [Address 00EB16]

B	Name	Functions	After re	R	W
0	HSYNC input polarity switch bit (OPC0)	0 : Positive polarity input 1 : Negative polarity input	0	R	W
1	VSYNC input polarity switch bit (OPC1)	0 : Positive polarity input 1 : Negative polarity input	0	R	W
2	R/G/B output polarity switch bit (OPC2)	0 : Positive polarity output 1 : Negative polarity output	0	R	W
3	OUT1 output polarity switch bit (OPC3)	0 : Positive polarity output 1 : Negative polarity output	0	R	W
4	OUT2 output polarity switch bit (OPC4)	0 : Positive polarity output 1 : Negative polarity output	0	R	W
5	Raster color R control bit (OPC5)	0 : No output 1 : Output	0	R	W
6	Raster color G control bit (OPC6)	0 : No output 1 : Output	0	R	W
7	Raster color B control bit (OPC7)	0 : No output 1 : Output	0	R	W

Address 00F4$_{16}$

Timer Mode Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Timer mode register 1 (TM1) [Address 00F4$_{16}$]

B	Name	Functions	After reset	R	W
0	Timer 1 count source selection bit 1 (TM10)	0: f(XIN)/16 1: f(XIN)/4096	0	R	W
1	Timer 2 count source selection bit 1 (TM11)	0: Interrupt clock source 1: External clock from TIM2 pin	0	R	W
2	Timer 1 count stop bit (TM12)	0: Count start 1: Count stop	0	R	W
3	Timer 2 count stop bit (TM13)	0: Count start 1: Count stop	0	R	W
4	Timer 2 internal count source selection bit 2 (TM14)	0: f(XIN)/16 1: Timer 1 overflow	0	R	W
5	<At execution of STP instruction> Timers 3 and 4 auto set disable bit (TM15)	0: Auto set enabled 1: Auto set disabled	0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Address 00F5$_{16}$

Timer Mode Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Timer mode register 2 (TM2) [Address 00F5$_{16}$]

B	Name	Functions	After reset	R	W
0	Timer 3 count source selection bit (TM20)	0 : f(XIN)/16 1 : External clock source	0	R	W
1	Timer 4 internal interrupt count source selection bit (TM21)	0 : Timer 3 overflow signal 1 : f(XIN)/16	0	R	W
2	Timer 3 count stop bit (TM22)	0: Count start 1: Count stop	0	R	W
3	Timer 4 count stop bit (TM23)	0: Count start 1: Count stop	0	R	W
4	Timer 4 count source selection bit (TM24)	0: Internal clock source 1: f(XIN)/2	0	R	W
5	Timer 3 external count source selection bit (TM25)	0: TIM3 pin input 1: HSYNC pin input	0	R	W
6, 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Addresses 00F9$_{16}$ and 00FA$_{16}$

Block i Control Register

b7 b6 b5 b4 b3 b2 b1 b0

Block i control register (BiC) (i = 1, 2) [Addresses 00F9$_{16}$, 00FA$_{16}$]

B	Name	Functions	After reset	R	W
0 to 2	Display mode selection bits (BiC0 to BiC2)	b2 b1 b0 — Display mode × 0 0 — Display OFF 0 0 1 — OSD mode (no border) 0 1 0 — BUTTON mode (no border) 1 0 1 — OSD mode (border) 1 1 0 — BUTTON mode (border)	Indeterminate	R	W
3, 4	Dot size selection bit (BiC3, BiC4)	b4 b3 — Dot size 0 0 — 1TOSC × 1H 0 1 — Do not set 1 0 — 2TOSC × 2H 1 1 — 3TOSC × 3H	Indeterminate	R	W
5 to 7	Nothing is assigned. These bits are write disable bits. When these bits are read out, the values are “0.”		0	R	—

Notes 1 : TOSC = OSD oscillation cycle
2 : H = HSYNC

Address 00FB$_{16}$

CPU Mode Register

b7 b6 b5 b4 b3 b2 b1 b0

0 0 1 1 1 0 0

CPU mode register (CM) [Address 00FB$_{16}$]

B	Name	Functions	After reset	R	W
0, 1	Processor mode bits (CM0, CM1)	b1 b0 0 0: Single-chip mode 0 1: } Not available 1 0: } 1 1: }	0	R	W
2	Stack page selection bit (CM2) (See note)	0: 0 page 1: 1 page	1	R	W
3 to 5	Fix these bits to “1.”		1	R	W
6, 7	Fix these bits to “0.”		0	R	W

Note: This bit is set to “1” after the reset release.

Address 00FC16

Interrupt Request Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 1 (IREQ1) [Address 00FC16]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt request bit (TM1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
1	Timer 2 interrupt request bit (TM2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
2	Timer 3 interrupt request bit (TM3R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
3	Timer 4 interrupt request bit (TM4R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
4	OSD interrupt request bit (OSDR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
5	VSYNC interrupt request bit (VSCR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
6	Multi-master I2C-BUS interface interrupt request bit (IICR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
7	INT3 external interrupt request bit (IT3R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻

✻: "0" can be set by software, but "1" cannot be set.

Address 00FD16

Interrupt Request Register 2

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt request register 2 (IREQ2) [Address 00FD16]

B	Name	Functions	After reset	R	W
0	INT1 external interrupt request bit (IT1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
1	INT2 external interrupt request bit (IT2R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
2	Serial I/O interrupt request bit (S1R)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
3	SPRITE OSD interrupt request bit (SPR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
4	f(XIN)/4096 interrupt request bit (MSR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
5	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is "0."		0	R	—
6	A-D conversion interrupt request bit (ADR)	0 : No interrupt request issued 1 : Interrupt request issued	0	R	✻
7	Fix this bit to "0."		0	R	W

✻: "0" can be set by software, but "1" cannot be set.

Addresses 00FE16

Interrupt Control Register 1

b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 1 (ICON1) [Address 00FE16]

B	Name	Functions	After reset	R	W
0	Timer 1 interrupt enable bit (TM1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	Timer 2 interrupt enable bit (TM2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Timer 3 interrupt enable bit (TM3E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3	Timer 4 interrupt enable bit (TM4E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
4	OSD interrupt enable bit (OSDE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
5	VSYNC interrupt enable bit (VSCE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
6	Multi-master I2C-BUS interface interrupt enable bit (IICE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
7	INT3 external interrupt enable bit (IT3E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W

Address 00FF16

Interrupt Control Register 2

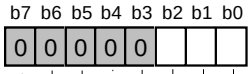
b7 b6 b5 b4 b3 b2 b1 b0

Interrupt control register 2 (ICON2) [Address 00FF16]

B	Name	Functions	After reset	R	W
0	INT1 external interrupt enable bit (IT1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
1	INT2 external interrupt enable bit (IT2E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
2	Serial I/O interrupt enable bit (S1E)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
3	SPRITE OSD interrupt enable bit (SPE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
4	f(XIN)/4096 interrupt enable bit (MSE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
5	Fix this bit to “0.”		0	R	W
6	A-D conversion interrupt enable bit (ADE)	0 : Interrupt disabled 1 : Interrupt enabled	0	R	W
7	Nothing is assigned. This bit is a write disable bit. When this bit is read out, the value is “0.”		0	R	—

Address 021B16

ROM Correction Enable Register

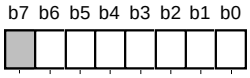


ROM correction enable register (RCR) [Address 021B16]

B	Name	Functions	After reset	R	W
0	Vector 1 enable bit (RCR0)	0: Disabled 1: Enabled	0	R	W
1	Vector 2 enable bit (RCR1)	0: Disabled 1: Enabled	0	R	W
2	Vector 3 enable bit (RCR2)	0: Disabled 1: Enabled	0	R	W
3 to 7	Fix these bits to "0."		0	R	W

Address 024016

Left Border Control Register



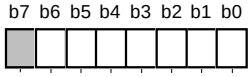
Left border control register (LBR) [Address 024016]

B	Name	Functions	After reset	R	W
0 to 6	Control bits of left border (LBR0 to LBR6)	Left border position = T_{def4} + 4TOSC × n + 1TOSC × WH (n: setting value, T_{def4}: 4TOSC, TOSC: OSD oscillation cycle, WH: value (0 to 3) of window horizontal position minute adjustment bit)	0	R	W
7	Nothing is assigned. This bit is write disable bit. When this bit is read out, the value is indeterminate.		0	R	—

Note: Set values fit for LBR ≤ RBR.

Address 024116

Right Border Control Register



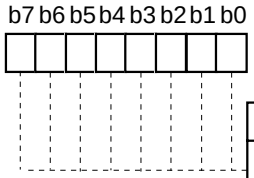
Right border control register (RBR) [Address 024116]

B	Name	Functions	After reset	R	W
0 to 6	Control bits of left border (RBR0 to RBR6)	Right border position = T_{def4} + 4TOSC × n + 1TOSC × WH (n: setting value, T_{def4}: 4TOSC, TOSC: OSD oscillation cycle, WH: value (0 to 3) of window horizontal position minute adjustment bit)	0	R	W
7	Nothing is assigned. This bit is write disable bit. When this bit is read out, the value is indeterminate.		0	R	—

Note: Set values fit for LBR ≤ RBR.

Address 0245$_{16}$

Top Border Control Register



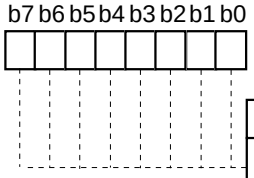
Top border control register (TBR) [Address 0245$_{16}$]

B	Name	Functions	After reset	R	W
0 to 7	Control bits of top border (TBR0 to TBR7)	Top border position = H_{def} + H × n (n: setting value, H_{def}: 17H, H: H_{SYNC})	Indeterminate	R	W

Notes 1: Set values except "00$_{16}$" to TBR.
2: Set values fit for TBR ≤ BBR.

Address 0246$_{16}$

Bottom Border Control Register



Bottom border control register (BBR) [Address 0246$_{16}$]

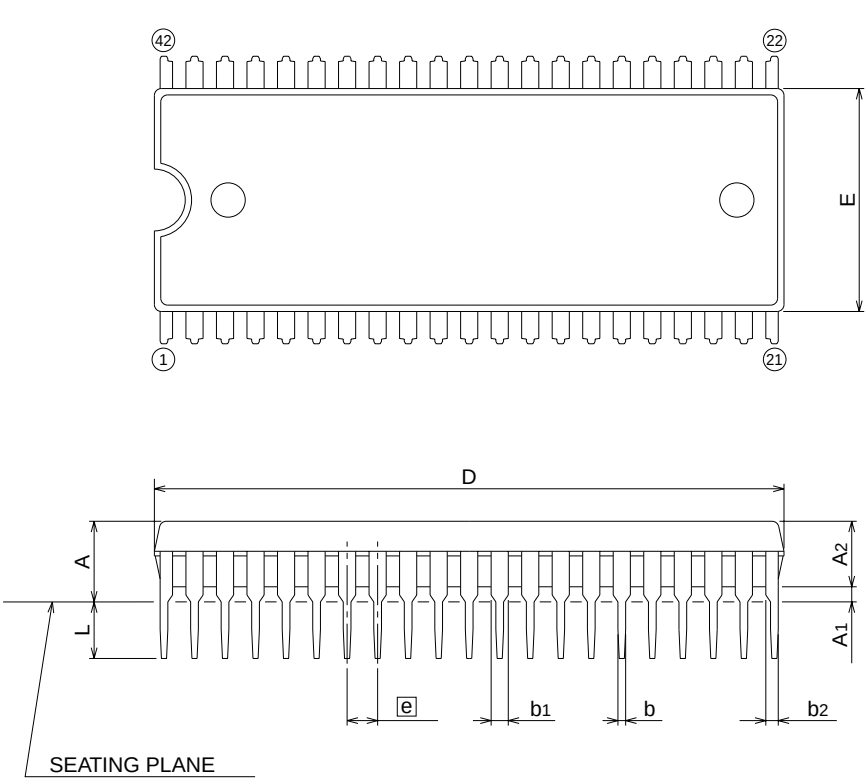
B	Name	Functions	After reset	R	W
0 to 7	Control bits of bottom border (BBR0 to BBR7)	Bottom border position = H_{def} + H × n (n: setting value, H_{def}: 17H, H: H_{SYNC})	Indeterminate	R	W

Notes 1: Set values except "00$_{16}$" to BBR.
2: Set values fit for TBR ≤ BBR.

19. PACKAGE OUTLINE

42P4B (MMP) **Plastic 42pin 600mil SDIP**

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP42-P-600-1.78	–	4.1	Alloy 42/Cu Alloy



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	5.5
A_1	0.51	–	–
A_2	–	3.8	–
b	0.35	0.45	0.55
b_1	0.9	1.0	1.3
b_2	0.63	0.73	1.03
c	0.22	0.27	0.34
D	36.5	36.7	36.9
E	12.85	13.0	13.15
e	–	1.778	–
e1	–	15.24	–
L	3.0	–	–
θ	0°	–	15°

Rev.	Date	Description	
		Page	Summary
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