PRELIMINARY

M37260M6-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for ON-SCREEN DISPLAY

DESCRIPTION

The M37260M6-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 52-pin shrink plastic molded DIP. This single-chip microcomputer is useful for the high-tech on-screen display system for TVs.

In addition to their simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

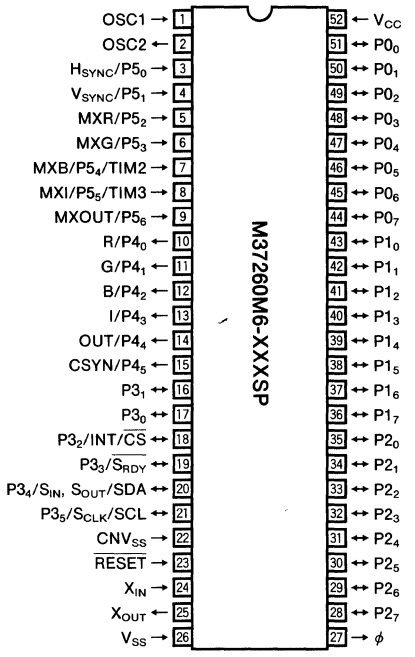
FEATURES

- Number of basic instructions 69
- Memory size ROM ..... 24576 bytes
  RAM ..... 320 bytes
  CRT ROM ..... 20480 bytes
  CRT RAM ..... 280 bytes
- Instruction execution time
  ..... 0.5μs (minimum instructions at 8MHz frequency)
- Single power supply ..... 5V±10%
- Power dissipation
  (normal operation mode at 4MHz frequency)
  ..... 110mW (V_{CC}=5.5V, CRT display)
- Subroutine nesting ..... 96 levels (Max.)
- Interrupt ..... 11 types, 11 vectors
- 8-bit timer 4
- Programmable I/O ports
  (Ports P0, P1, P2, P3) 30
- Output port (Port P4) 6
- Input port (Port P5) 7
- Serial I/O (maximum 64-bit) 1
- CRT display function
  Display characters ..... 40 characters×3 lines
  (25 lines max.)
  Dot structure ..... 12×20 dots or 16×20 dots
  Character types ..... 510 types
  Character size ..... 30 types
  (minimum dot width is 1/2 scanning line)
  Color types ..... Max 16 types (R, G, B, I)
  Character unit/blank of line unit/raster can be specified
  Display layout
  Horizontal ..... 256 levels
  Vertical ..... 1024 levels

APPLICATION

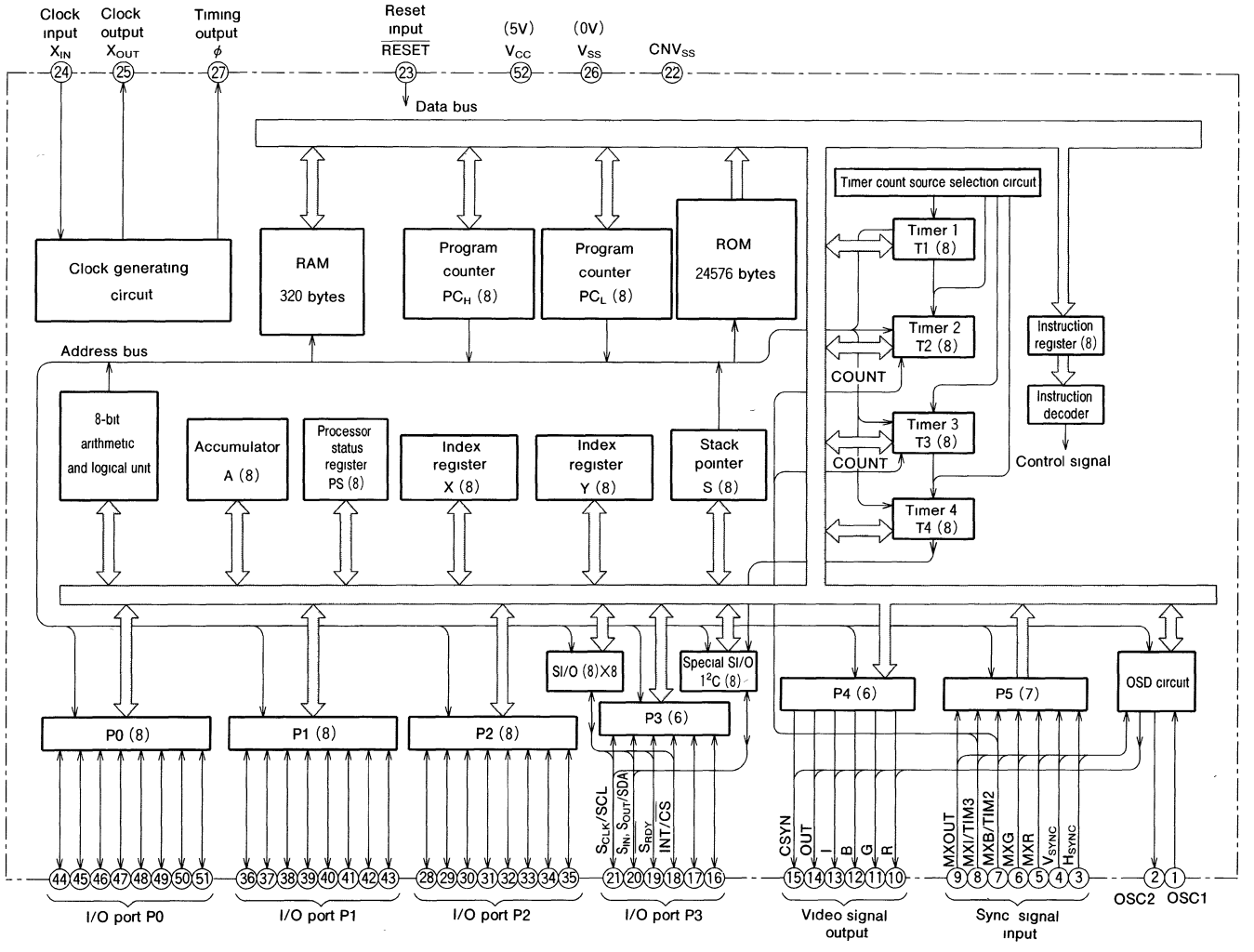
TV

PIN CONFIGURATION (TOP VIEW)



Outline 52P4B

M37260M6-XXXSP BLOCK DIAGRAM



MITSUBISHI ELECTRIC

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for ON-SCREEN DISPLAY

FUNCTIONS OF M37260M6-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			0.5μs (minimum instructions, at 8MHz frequency)
Clock frequency			8MHz (maximum)
Memory size	ROM		24576 bytes
	RAM		320 bytes
	CRT ROM		20480 bytes
	CRT RAM		280 bytes
Input/Output ports	P0, P1, P2	I/O	8-bit×3 (CMOS output)
	$P3_0$, $P3_1$	I/O	2-bit×1 (CMOS output)
	$P3_2$—$P3_5$	I/O	4-bit×1 (can be used as serial I/O pins and external interrupt pin) (N-channel open drain output)
	P4	Output	6-bit×1 (can be used as R, G, B, I, OUT, and CSYN pins) (CMOS output)
	P5	Input	7-bit×1 (can be used as H_{SYNC}, V_{SYNC}, MXR, MXG, MXB, MXI, and MXOUT pins)
Serial I/O			64-bit (maximum)×1, Special serial I/O (8-bit)×1
Timers			8-bit timer×4
Subroutine nesting			96 levels (maximum)
Interrupt			One external interrupt, eight internal interrupts, one software interrupt
CRT display function	Display characters		40 characters×3 lines (maximum 25 lines in program)
	Dot structure		12×20 dots or 16×20 dots
	Characters types		510 types
	Character size		30 types (mimimum dot width is 1/2 scanning line)
	Color types		Max. 16 types (R, G, B, I)
	Display layout		Holizontal 256 levels, Vertical 1024 levels
Clock generating circuit			Two built-in circuits (externally connected ceramic or quartz crystal oscillator)
Supply voltage			5V±10%
Power dissipation	at CRT display ON		110mW (clock frequency X_{IN}=4MHz, V_{CC}=5.5V, Typ.)
	at CRT display OFF		55mW (clock frequency X_{IN}=4MHz, V_{CC}=5.5V, Typ.)
	at stop mode		1.65mW (maximum)
Memory expansion			Possible
Operating temperature range			−10 to 70℃
Device structure			CMOS silicon gate process
Package			52-pin shrink plastic molded DIP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}
CNV_{SS}	CNV_{SS}		This is connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is a timing output pin
$P0_0$—$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with direction register allowing each I/O bit to be individually programmed as input or output At reset, this port is set to input mode The output structure is CMOS output
$P1_0$—$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0
$P2_0$—$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0
$P3_0$—$P3_5$	I/O port P3	I/O	Port P3 is a 6-bit I/O port and has basically the same functions as port P0, but the output structure of $P3_0$ and $P3_1$ is CMOS output and the output structure of $P3_2$—$P3_5$ is N-channel open drain $P3_2$ is in common with external interrupt input pin INT When serial I/O is used, $P3_2$, $P3_3$, $P3_4$, and $P3_5$ work as $\overline{CS}$, $\overline{S_{RDY}}$, S_{IN}/S_{OUT}, and S_{CLK} pins, respectively. When special serial I/O is used, $P3_4$ and $P3_5$ work as SDA and SCL pins, respectively.
OSC1	Clock input for CRT display	Input	There are I/O pins of the clock generating circuit for the CRT display function
OSC2	Clock output for CRT display	Output	
H_{SYNC}	H_{SYNC} input	Input	This is a horizontal synchronizing signal input for CRT display This pin is in common with input Port $P5_0$
V_{SYNC}	V_{SYNC} input	Input	This is a vertical synchronizing signal input for CRT display. This pin is in common with input Port $P5_1$
MXR, MXG, MXB, MXI, MXOUT	Video signal input for mixing	Input	These are video signal input pins. MXR, MXG, MXB, MXI, and MXOUT are in common with $P5_2$, $P5_3$, $P5_4$, $P5_5$, and $P5_6$ Also $P5_4$ and $P5_5$ are in common with external clock input pins TIM2 and TIM3
R, G, B, I, OUT	Video signal output	Output	This is a 5-bit output pin for CRT display The output structure is CMOS output R, G, B, I, and OUT are in common with $P4_0$, $P4_1$, $P4_2$, $P4_3$, and $P4_4$
CSYN	Composite sync signal output	Output	This is a composite sync signal output pin, and in common with output port $P4_5$

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The M37260 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions are not provided.

The WIT instruction can be used.

The STP instruction can be used.

CPU Mode Register

The CPU mode register is allocated to address $00FB_{16}$. Bits 0 and 1 of this register are processor mode bits. This register also has a stack page selection bit.

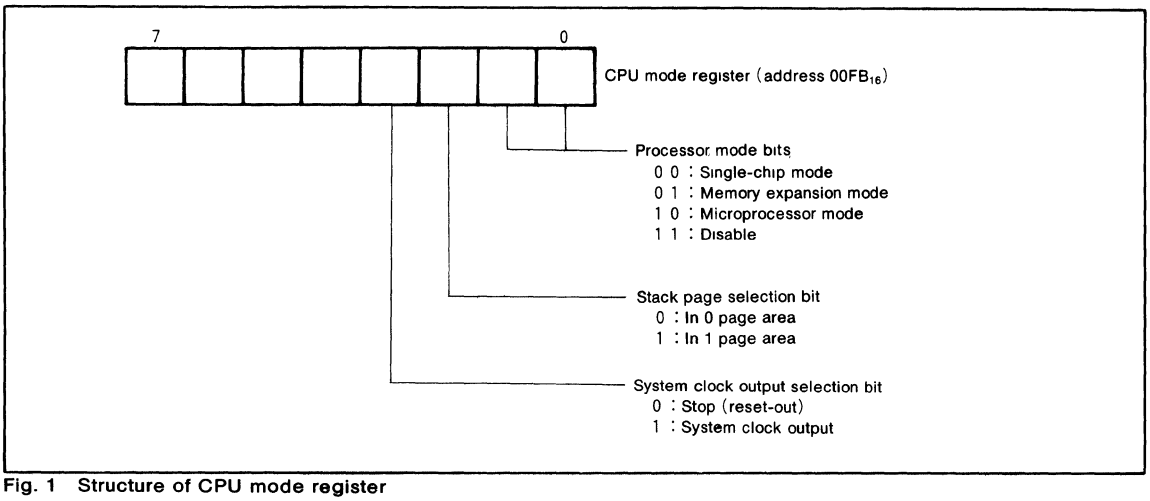


Fig. 1 Structure of CPU mode register

MEMORY

• Special Function Register (SFR) Area

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• RAM

RAM is used for data storage as well as a stack area.

• ROM

ROM is used for storing user programs as well as the interrupt vector area.

• RAM for display

RAM for display is used for specifing the character codes and colors to display.

• ROM for display

ROM for display is used for storing character data.

• Interrupt Vector Area

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• Zero Page

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

• Special Page

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

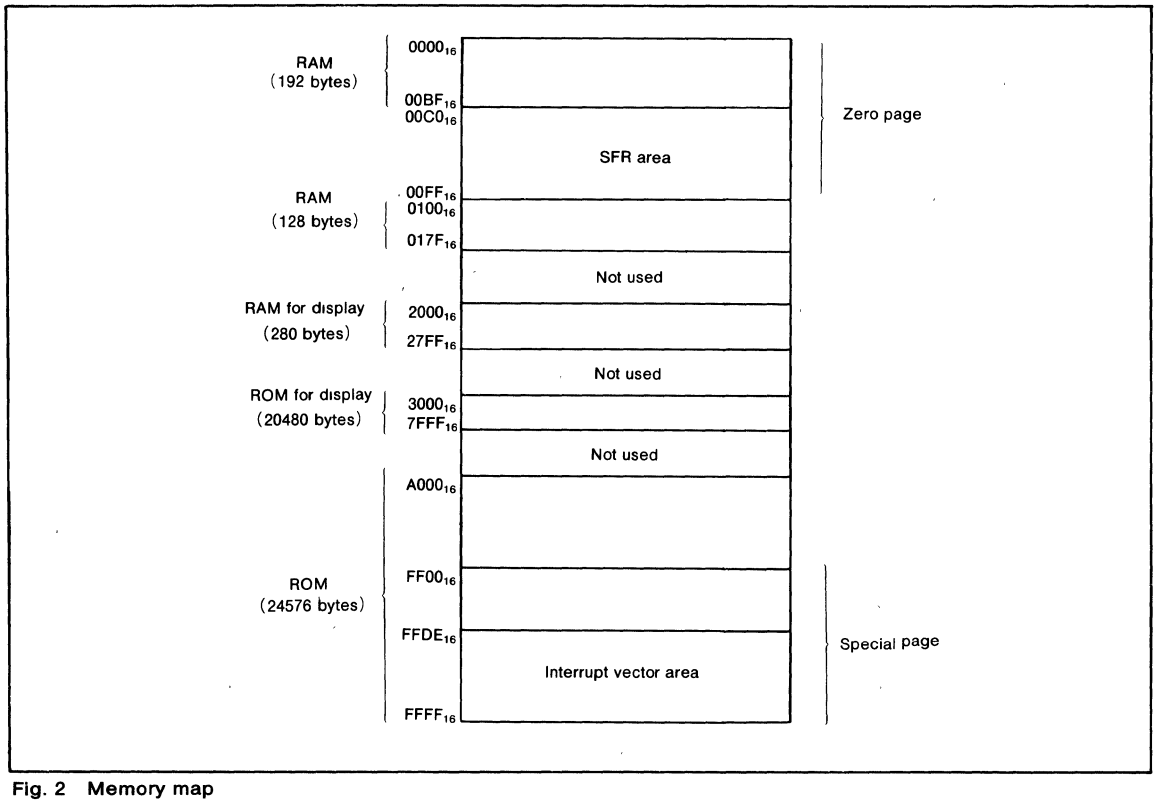


Fig. 2 Memory map

$00C0_{16}$	Port P0
$00C1_{16}$	Port P0 direction register
$00C2_{16}$	Port P1
$00C3_{16}$	Port P1 direction register
$00C4_{16}$	Port P2
$00C5_{16}$	Port P2 direction register
$00C6_{16}$	Port P3
$00C7_{16}$	Port P3 direction register
$00C8_{16}$	Port P4
$00C9_{16}$	Port P4 mode register
$00CA_{16}$	Port P5
$00CB_{16}$	
$00CC_{16}$	
$00CD_{16}$	Serial I/O mode register 1
$00CE_{16}$	Serial I/O mode register 2
$00CF_{16}$	Serial I/O register 0
$00D0_{16}$	Serial I/O register 1
$00D1_{16}$	Serial I/O register 2
$00D2_{16}$	Serial I/O register 3
$00D3_{16}$	Serial I/O register 4
$00D4_{16}$	Serial I/O register 5
$00D5_{16}$	Serial I/O register 6
$00D6_{16}$	Serial I/O register 7
$00D7_{16}$	Character size register 1 (block 1)
$00D8_{16}$	Character size register 2 (block 2)
$00D9_{16}$	Character size register 3 (block 3)
$00DA_{16}$	Blank control register 1 (block 1)
$00DB_{16}$	Blank control register 2 (block 2)
$00DC_{16}$	Blank control register 3 (block 3)
$00DD_{16}$	Block 1 interrupt occurrence position control register
$00DE_{16}$	Block 2 interrupt occurrence position control register
$00DF_{16}$	Block 3 interrupt occurrence position control register

$00E0_{16}$	Horizontal position register
$00E1_{16}$	Vertical position register 1 (block 1)
$00E2_{16}$	Vertical position register 2 (block 2)
$00E3_{16}$	Vertical position register 3 (block 3)
$00E4_{16}$	Vertical position register 4 (block 1 to 3)
$00E5_{16}$	Mixing circuit control register
$00E6_{16}$	
$00E7_{16}$	
$00E8_{16}$	CRT input polarity register
$00E9_{16}$	Sync. generater control register
$00EA_{16}$	CRT control register
$00EB_{16}$	Display block counter
$00EC_{16}$	CRT output polarity register
$00ED_{16}$	Wipe mode register
$00EE_{16}$	Wipe start register
$00EF_{16}$	
$00F0_{16}$	Timer 1
$00F1_{16}$	Timer 2
$00F2_{16}$	Timer 3
$00F3_{16}$	Timer 4
$00F4_{16}$	Timer 12 mode register
$00F5_{16}$	Timer 34 mode register
$00F6_{16}$	Special serial I/O register
$00F7_{16}$	Special mode register 1
$00F8_{16}$	Special mode register 2
$00F9_{16}$	
$00FA_{16}$	
$00FB_{16}$	CPU mode register
$00FC_{16}$	Interrupt request register 1
$00FD_{16}$	Interrupt request register 2
$00FE_{16}$	Interrupt control register 1
$00FF_{16}$	Interrupt control register 2

Fig. 3 SFR (Special Function Register) memory map

INTERRUPTS

Interrupts can be caused by 10 different events consisting of two external, seven internal, and one software events.

Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed, interrupt disable flag I is set, and the program jumps to the address specified in the vector table. The interrupt request bit is cleared automatically. The reset and BRK instruction interrupt can never be disabled. Other interrupts are disabled when the interrupt disable flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figure 4 shows the structure of the interrupt request registers 1 and 2 and interrupt control registers 1 and 2.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt disable flag is "0". The interrupt request bit can be reset with a program, but not set. The interrupt enable bit can be set and reset with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 5 shows interrupts control.

Interrupt Causes

(1) V_{SYNC} and CRT interrupts

The V_{SYNC} interrupt is an interrupt request synchronized with the vertical synchronization signal.

The CRT interrupt is generated after character block display to the CRT is completed.

(2) INT interrupt

With an external interrupt input, the system detects that the level of a pin changes from "L" to "H" or from "H" to "L", and generates an interrupt request. The input active edge can be selected by bit 5 of the CRT input active edge register (address $00E8_{16}$) : when this bit is "0", a change from "L" to "H" is detected; when it is "1", a change from "H" to "L" is detected. Note that all bits are cleared to "0" at reset.

(3) Timer 1, 2, 3 and 4 interrupts

An interrupt is generated by an overflow of timer 1, 2, 3, or 4.

(4) Serial I/O interrupt

This is an interrupt request from the clock-synchronized serial I/O function.

Note that serial I/O or special serial I/O is selected by bit 3 of the serial I/O mode register 2 (address $00CE_{16}$).

(5) 1 ms interrupt

This interrupt is generated regularly with a 1024μs period. When the X_{IN} clock is 4MHz, set bits 7 and 4 of the sync generator control register to "0". When the X_{IN} clock is 8MHz, set bit 7 of the sync generator control register to "0" and bit 4 to "1".

(6) BRK instruction interrupt

This interrupt has the lowest priority of all software interrupts. It does not have a corresponding interrupt enable bit, and it is not affected by the interrupt disable flag (non-maskable).

Table 1. Interrupt vector address and priority.

Event	Priority	Vector addresses	Remarks
$\overline{\text{RESET}}$	1	$FFFF_{16}$, $FFFE_{16}$	Non-maskable
CRT interrupt	2	$FFFD_{16}$, $FFFC_{16}$	
INT interrupt	3	$FFFB_{16}$, $FFFA_{16}$	External interrupt
Serial I/O interrupt	4	$FFF9_{16}$, $FFF8_{16}$	
1 ms interrupt	5	$FFF7_{16}$, $FFF6_{16}$	
Timer 4 interrupt	6	$FFF5_{16}$, $FFF4_{16}$	
V_{SYNC} interrupt	7	$FFF3_{16}$, $FFF2_{16}$	External interrupt
Timer 3 interrupt	8	$FFF1_{16}$, $FFF0_{16}$	
Timer 2 interrupt	9	$FFEF_{16}$, $FFEE_{16}$	
Timer 1 interrupt	10	$FFED_{16}$, $FFEC_{16}$	
BRK instruction interrupt	11	$FFDF_{16}$, $FFDE_{16}$	Non-maskable software interrupt

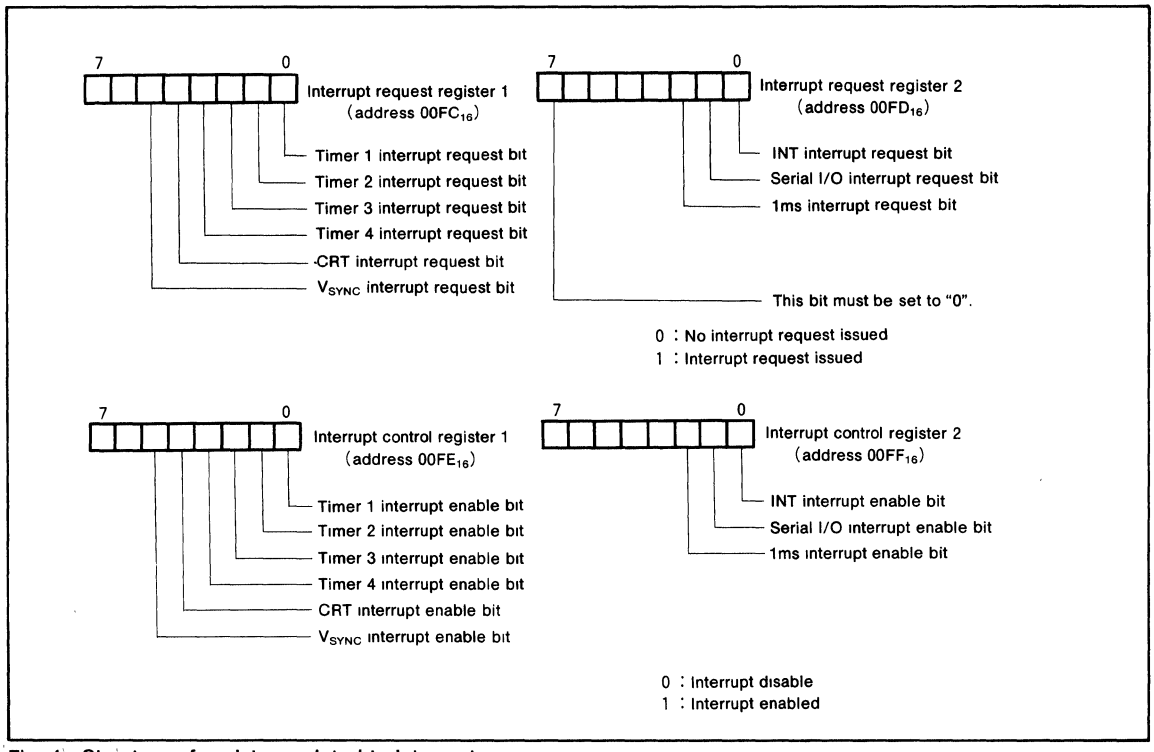


Fig. 4 Structure of registers related to interrupt

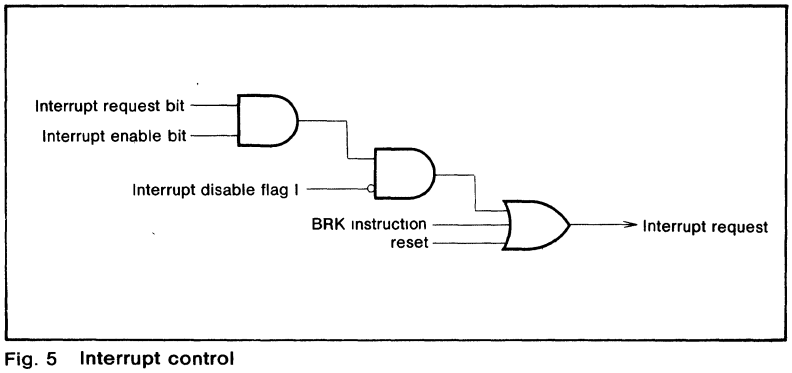


Fig. 5 Interrupt control

TIMER

The M37260M6-XXXSP has four timers; timer 1, timer 2, timer 3 and timer 4. All of timers are 8-bit structure and have 8-bit latches.

A block diagram of timer 1 through 4 is shown in Figure 7.

All of the timers are down count timers and their division ratio are $1/(n+1)$, where n is the contents of timer latch. The same value is set to timer by writing the count value to the latch (addresses $00F0_{16}$ to $00F3_{16}$: timer 1 to timer 4) When a timer reaches "00_{16}" and the next count pulse is input to a timer, a value which is the contents of the reload latch are loaded into the timer. The timer interrupt request bit is set at the next count pulse after the timer reaches "00_{16}".

The contents of each timer is shown in following.

(1) Timer 1

Either $f(X_{IN})$ divided by 16 or a 1024μs clock can be selected as the count source of timer 1.

(When the X_{IN} clock is 4MHz, set bits 7 and 4 of the sync generator control register (address $00E9_{16}$) to "0". When the X_{IN} clock is 8MHz, set bit 7 of the sync generator control register to "0" and bit 4 to "1".) When bit 0 of the timer 12 mode register (address $00F4_{16}$) is "0", $f(X_{IN})$ divided by 16 is selected; when it is "1", the 1024μs clock is selected.

Timer 1 interrupt request is occurred with timer 1 overflow

(2) Timer 2

$f(X_{IN})$ divided by 16, timer 1 overflow signal, or an external clock input from $P5_4$/MXB/TIM2 pin can be selected as the count source of timer 2 by specifying bit 4 and 1 of the timer 12 mode register (address $00F4_{16}$).

Timer 2 interrupt request is occurred with timer 2 overflow.

(3) Timer 3

Either $f(X_{IN})$ divided by 16 or an external clock input from $P5_5$/MXI/TIM3 pin can be selected as the count source of timer 3 by specifying bit 0 of the timer 34 mode register (address $00F5_{16}$).

Timer 3 interrupt request is occurred with timer 3 overflow.

(4) Timer 4

$f(X_{IN})$ divided by 16, $f(X_{IN})$ divided by 2, or timer 3 overflow signal can be selected as the count source of timer 4 by specifying bit 4 and 1 of the timer 34 mode register (address $00F5_{16}$).

Timer 4 interrupt request is occurred with timer 4 overflow. And the timer 4 overflow signal can be used as the clock source of special serial I/O.

At reset or an STP instruction is executed, timer 3 and timer 4 are connected automatically, and the value "FF_{16}" is set to timer 3, and the value "07_{16}" is set to timer 4

$f(X_{IN})$ divided by 16 is selected as count source of timer 3.

When the internal reset is removed or stop mode is removed, the internal clock is connected by timer 6 overflow at above state. In this reason, the program starts with stable clock.

The timer related registers structure is shown in Figure 6.

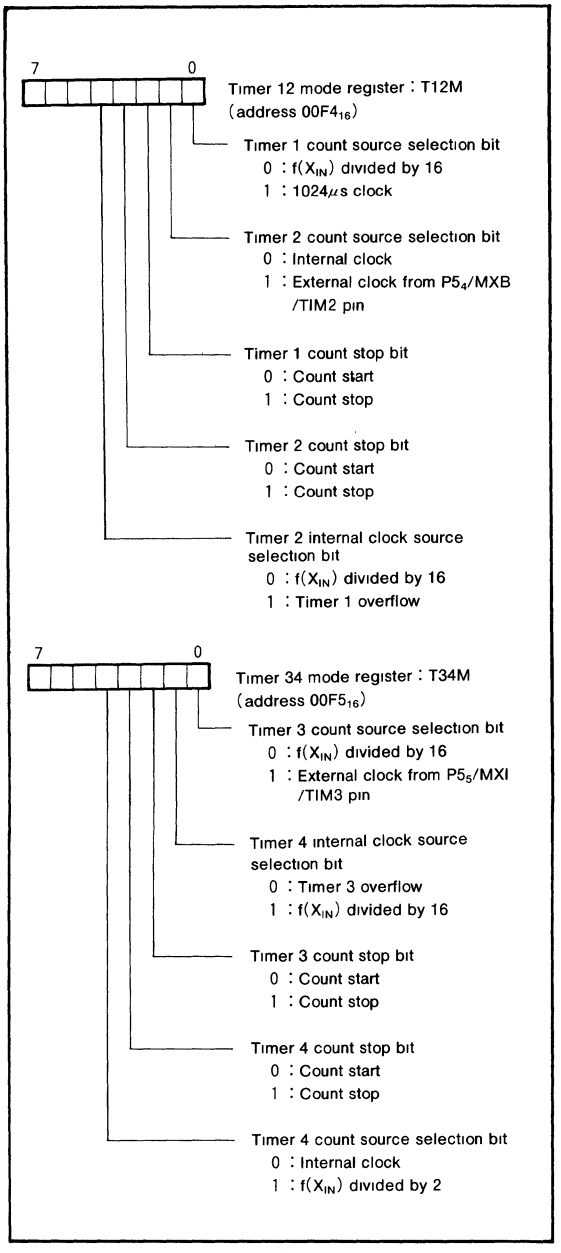
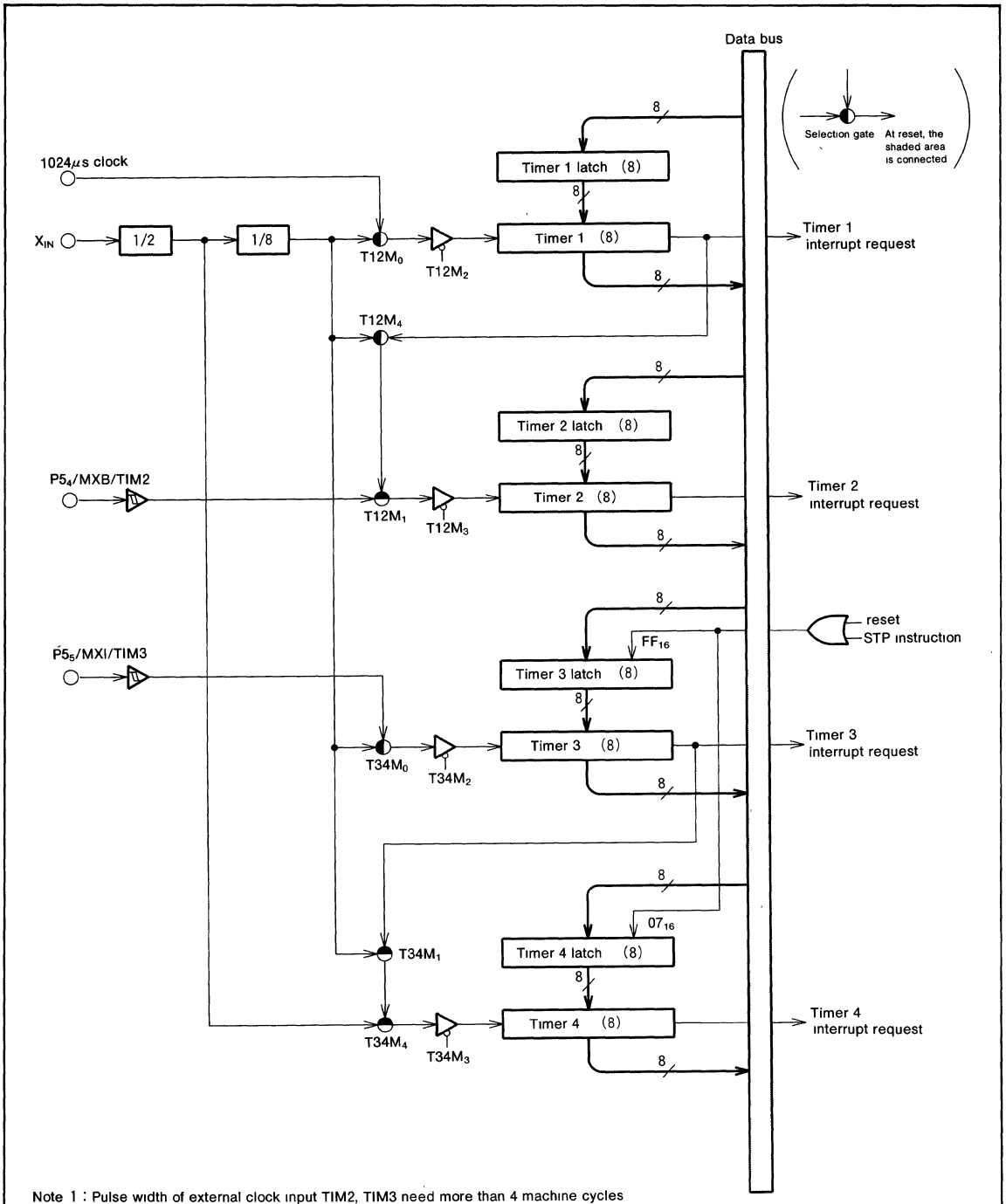


Fig. 6 Structure of timer 12 mode register and timer 34 mode register



Note 1 : Pulse width of external clock input TIM2, TIM3 need more than 4 machine cycles

2 : When the external clock source is selected, timer 2 and timer 3 are counted by the rising edge of input signal

Fig. 7 Block diagram of timer 1, timer 2, timer 3 and timer 4

SERIAL I/O

The M37260M6-XXXSP has a built-in serial I/O function that can either transmit or receive up to 64-bits of serial data in clock-synchronized form. The serial I/O function can transfer up to 64 bits of data in 8-bit units according to the setting of the serial I/O shift register.

A block diagram of the serial I/O function is shown in Fig. 8. The serial I/O receive enabled signal pin ($\overline{S_{RDY}}$), synchronization clock I/O pin (S_{CLK}), and data I/O pins (S_{OUT} and S_{IN}) also function as the P3 port.

Bit 2 of the serial I/O mode register 1 (address $00CD_{16}$) selects whether the synchronizaion clock is supplied internally or externally (from the S_{CLK} pin) and, if the internal clock is selected, bits 1 and 0 select whether $f(X_{IN})$ is divided by 8, 16, 32, or 64. Bits4 and 3 select whether port P3 is used for serial I/O. Bits 2, 1, and 0 of the serial I/O mode register 2 select the count of the transfer clock at which the serial I/O interrupt request is generated The operation of the serial I/O function is described below.

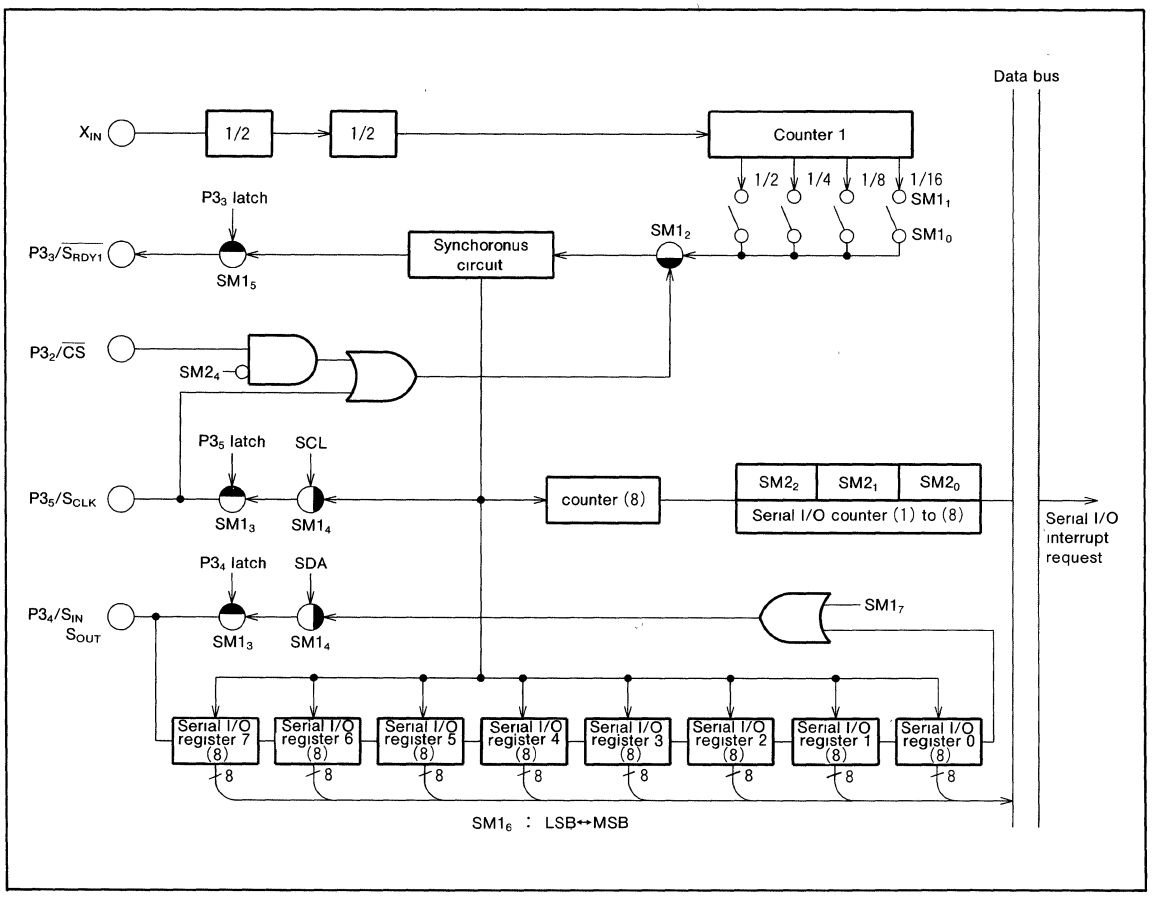


Fig. 8 Block diagram of serial I/O

If the serial I/O register 0 (address $00CF_{16}$) is written to, the $\overline{S_{RDY}}$ signal is at "H" during the write cycle; it then goes "L" when the write cycle ends to indicate reception enabled status. If the serial I/O register's transfer clock goes "L" even once, the $\overline{S_{RDY}}$ signal goes "H". During the write cycle to the serial I/O register 0, the value set in the serial I/O mode register 2 is set in the serial I/O counter, and the serial I/O register's transfer clock is forced to "H". After the write cycle ends, the data in each register is shifted one bit in sequence from serial I/O register 0 to serial I/O register 1, serial I/O register 2, serial I/O register 3, serial I/O register 4, serial I/O register5, serial I/O register 6, to serial I/O register 7, until it is finally output from the S_{OUT} pin, each time the transfer clock changes from "H" to "L". Bit 6 of the serial I/O mode register selects whether transfer is from the lowest bit of each serial I/O register, or from the highest bit.

During reception, data is fetched from the S_{IN} pin each time the transfer clock changes from "L" to "H" and, at the same time, the data in each register is shifted one bit in sequence from serial I/O register 7 to serial I/O register 6, serial I/O register 5, serial I/O register 4, serial I/O register 3, serial I/O register 2, serial I/O register 1, to serial I/O register 0.

If the transfer clock is the count value set in the serial I/O mode register 2, when the serial I/O counter reaches "0", the transfer clock stops at "H" and the corresponding interrupt request bit is set.

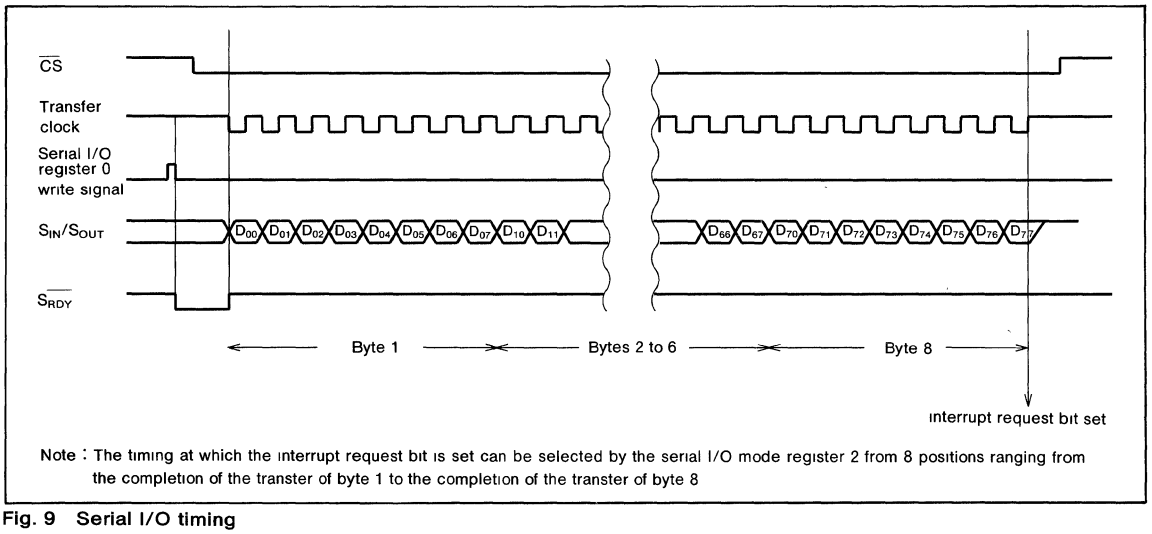
If an external clock is selected as the clock source, it must be controlled externally because the transfer clock does not stop, even when the interrupt request bit is set. Use a clock of no more that 1MHz with a duty cycle of 50% as the external clock.

Serial I/O timing is shown in Fig. 9. If an external clock is used for the transfer, the external clock must be "H" when the serial I/O counter is initialized. If the internal clock is switched to an external clock, make sure that it is switched while no transfer is in progress, and make sure that the serial I/O counter is initialized after the switch.

A connection example for transferring data from one M37260M6-XXXSP to another is shown in Fig. 10. If $P3_2$ is used as the $\overline{CS}$ pin, set the $P3_2$ direction register to input ("0") and set bit 4 of the serial I/O mode register 2 to "0". This setting ensures that the transfer clock is fixed at "H" when the $P3_2$ input signal is "H", and data is not shifted. If the $P3_2$ input signal goes "L", data will be shifted according to the clock input from the $P3_5/S_{CLK}$ pin. Note that if bit 4 of the serial I/O mode register 2 is set to "1", the data will be shifted according to the clock input from the $P3_5/S_{CLK}$ pin, regardless of the $P3_2$ input signal.

Note 1 : When writing programs, remember that the serial I/O counter will also be set by using bit manipulation instructions such as SEB and CLB to write to the serial I/O register 0.

2 : When writing data to serial I/O registers 0 to 7, make sure that serial I/O register 0 is the last one written to.



Note : The timing at which the interrupt request bit is set can be selected by the serial I/O mode register 2 from 8 positions ranging from the completion of the transfer of byte 1 to the completion of the transfer of byte 8

Fig. 9 Serial I/O timing

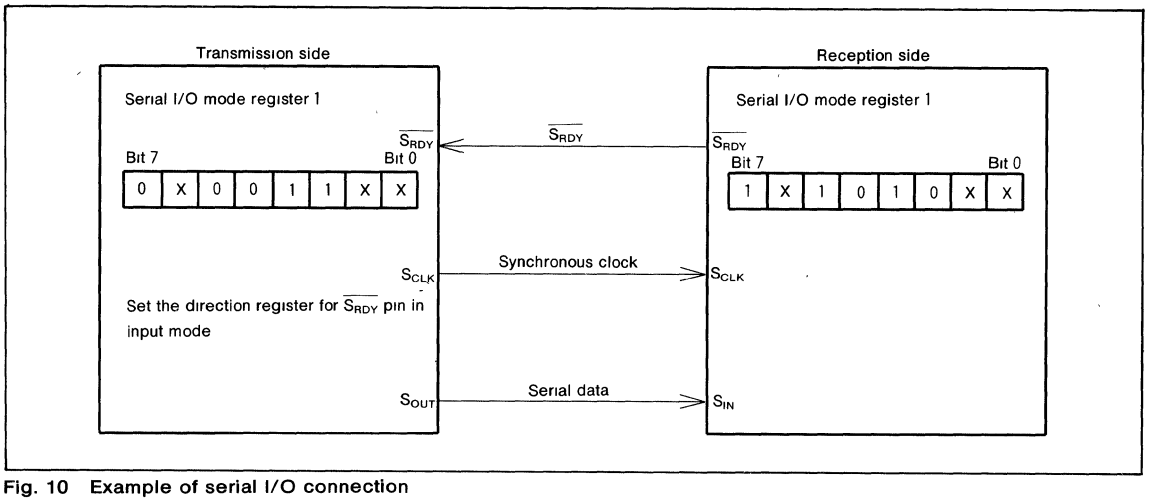


Fig. 10 Example of serial I/O connection

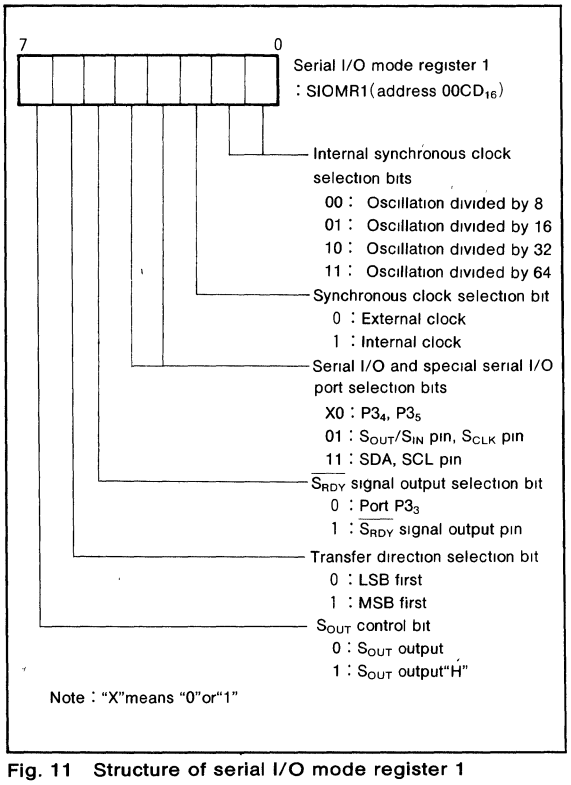


Fig. 11 Structure of serial I/O mode register 1

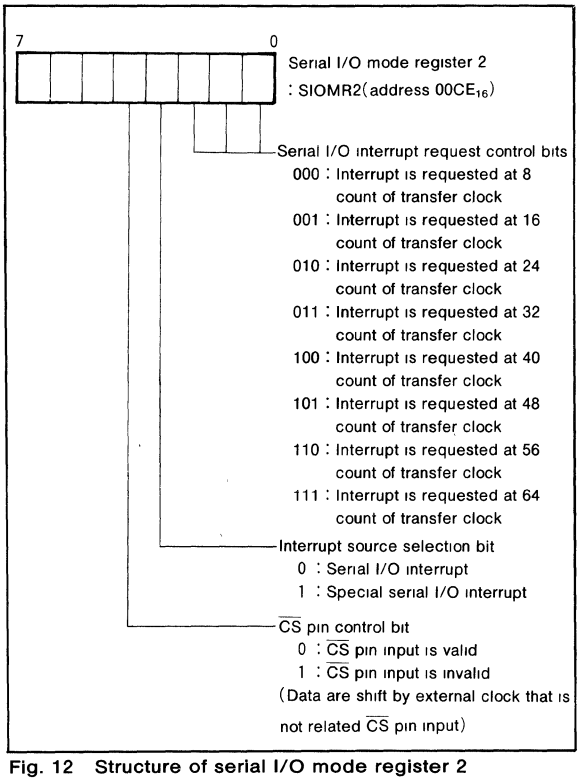


Fig. 12 Structure of serial I/O mode register 2

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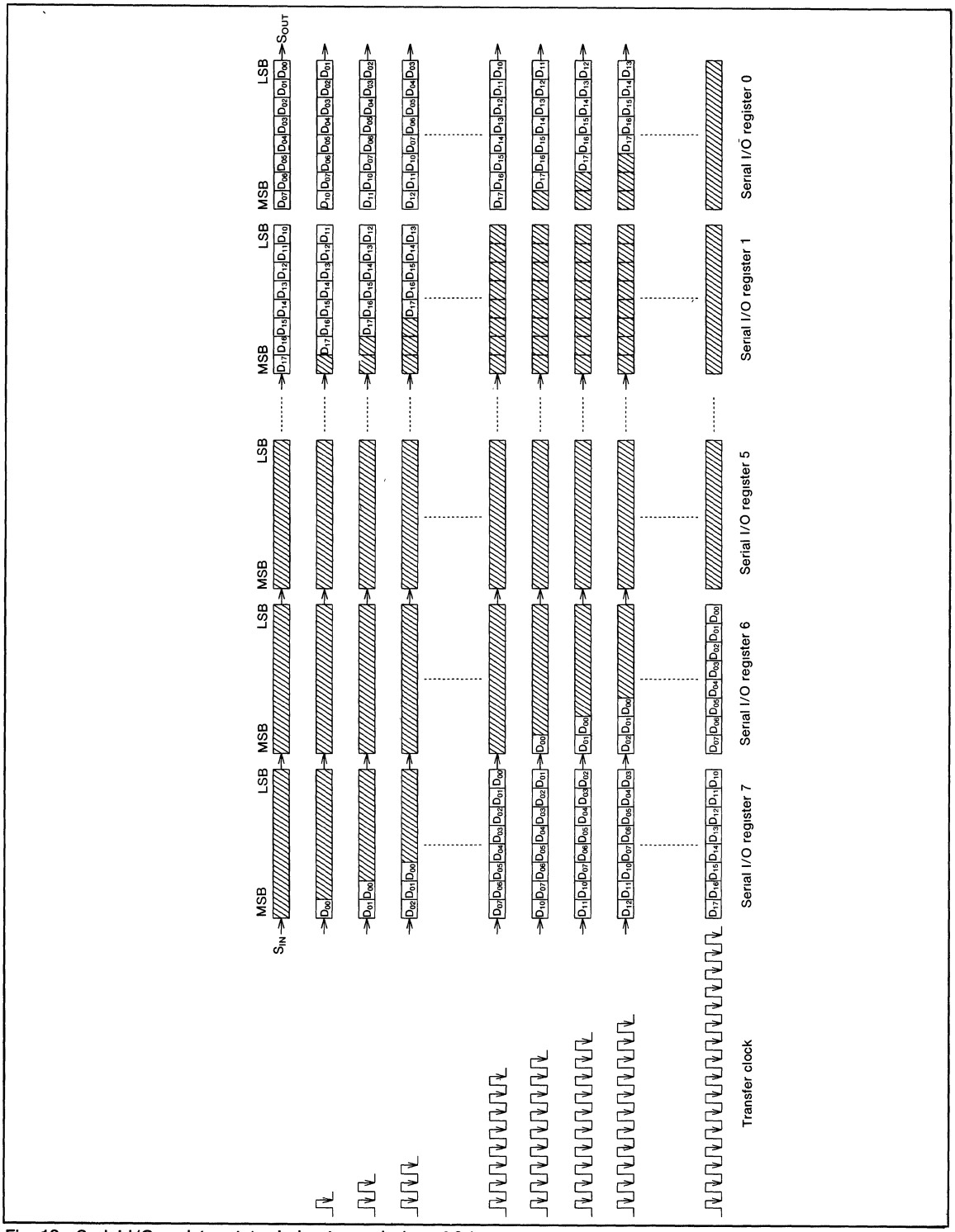

Fig. 13 Serial I/O register state during transmission of 2-byte date

Fig. 14 Serial I/O register state during reception of 2-byte date

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SPECIAL MODE (I^2C BUS MODE*)

M37260M6-XXXSP has a special serial I/O circuit that can be reception or transmission of serial data in conformity with I^2C (Inter IC) bus format.

I^2C bus is a two line directional serial bus developed by Philips to transfer and control data among internal ICs of a machinery.

M37260M6-XXXSP's special serial I/O is not included the clock synchronisation function and the arbitration detectable function at multimaster.

Operations of master transmission and master reception with special serial I/O explained in the following:

(1) Master transmission

① To generate an interrupt at the end of transmission, set bit 3 of serial I/O mode register 2 (address $00CE_{16}$) to "1" so as to special serial I/O interrupt is selected.

② Then set bit 1 of interrupt control register 2 (address $00FF_{16}$) to "1" so as to special serial I/O interrupt is enabled. Clear the interrupt disable flag I to "0" by using the CLI instruction.

③ The output signals of master transmission SDA and SCL are output from ports $P3_4$ and $P3_5$. Set all bits (bits 4 and 5) corresponding to $P3_4$ and $P3_5$ of the port P3 register (address $00C6_{16}$) and the port P3 direction register (address $00C7_{16}$) to "1".

④ Set the transmission clock. The transmission clock uses the overflow signal of timer 4. Set appropriate value in timer 4 and timer 34 mode register. (For instance, if $f(X_{IN})/2$ is selected as the clock source of timer 4 and 9 is set in timer 4 when $f(X_{IN})$ is 4MHz, the master transmission clock frequency is 100kHz.)

⑤ Set contents of the special mode register 2 (address $00F8_{16}$). (Usually, the vaule is "03_{16}".)

⑥ Set the bits 3 and 4 of serial I/O mode register 1 (address $00CD_{16}$) so as the port $P3_4$ and $P3_5$ is specified to SDA and SCL. After that set the special mode register 1 (address $00F7_{16}$). Figure 18 shows the structure of special mode registers 1 and 2.
Initial setting is completed by the above procedure.

⑦ Clear bits 0 and 1 of special mode register 2 (to "0") to make both SDA and SCL output to "L". This is for arbitration. Immediately after this, write data to be transmitted in the special serial I/O register (address $00F6_{16}$). The start signal has been completed.
The hardware automatically sends out data of 9-clock cycle. The 9th clock is for ACK reception and the output level becomes "H" at this clock. If other master outputs the start signal to transmit data simultaneously with this 9th clock, it is not detected as an arbitration-lost.
When the ACK bit has been transmitted, bit 1 of the interrupt request register 2 is set to "1" (issue of interrupt request), notifying the end of data transmission.

⑧ To transmit data successively, write data to be sent to the special serial I/O register, and set the interrupt enabled state again. By repeating this procedure, unlimited number of bytes can be transmitted.

⑨ To terminate data transfer, clear bits 0 and 1 of the special mode register 2 to "0".

⑩ Set bit 1 clock SCL to "1".

⑪ Then set bit 0 data SDA to "1". This procedure transmits the stop signal.
Figure 16 shows master transmission timing explained above. (the numbers in this figure are correspond to above explained numbers.)

(2) Master reception

Master reception is carried out in the interrupt routine after data is transferred by master transmission. For master transmission and interrupt thereafter, see the preceding section (1) Master transmission (the process until ⑦ in Figure 16.)

In the interrupt routine, set master reception ACK provided (22_{16}) in the special mode register 1 (address $00F7_{16}$), and write "FF_{16}" in the special serial I/O register (address $00F6_{16}$). This sets data line SDA to "H" and to perform 8-clock master reception. Then, a clock of "L" is transmitted to data line SDA for ACK receiving. In the ACK provided mode, the above ACK is automatically sent out.

Repeat the above receiving operation for a necessary number of times. Then return to the master transmission mode and transmit the stop signal by the same procedure for the master transmission (the process from ⑨ to ⑪ in Figure 16.)

Figure 17 shows master reception timing.

* : Purchase of Mitsubishi Electric Corporation's I^2C components converys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

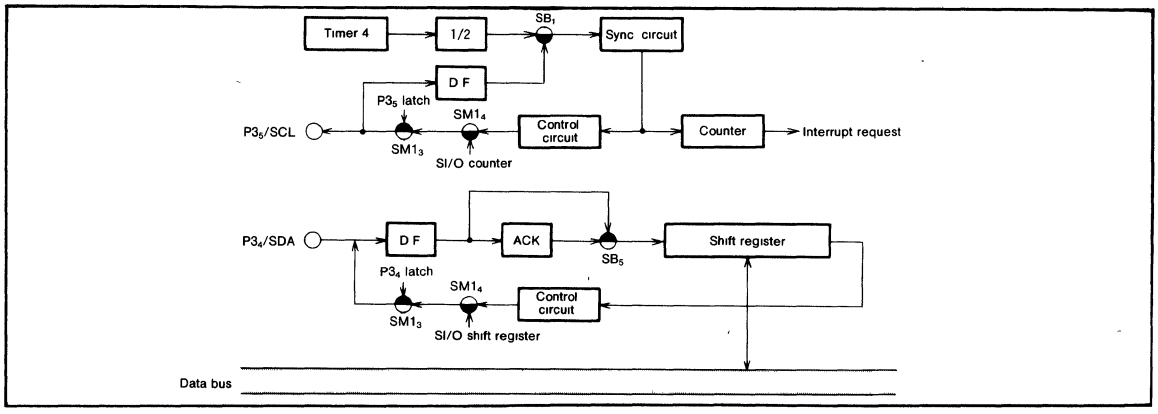

Fig. 15 Block diagram of special serial I/O

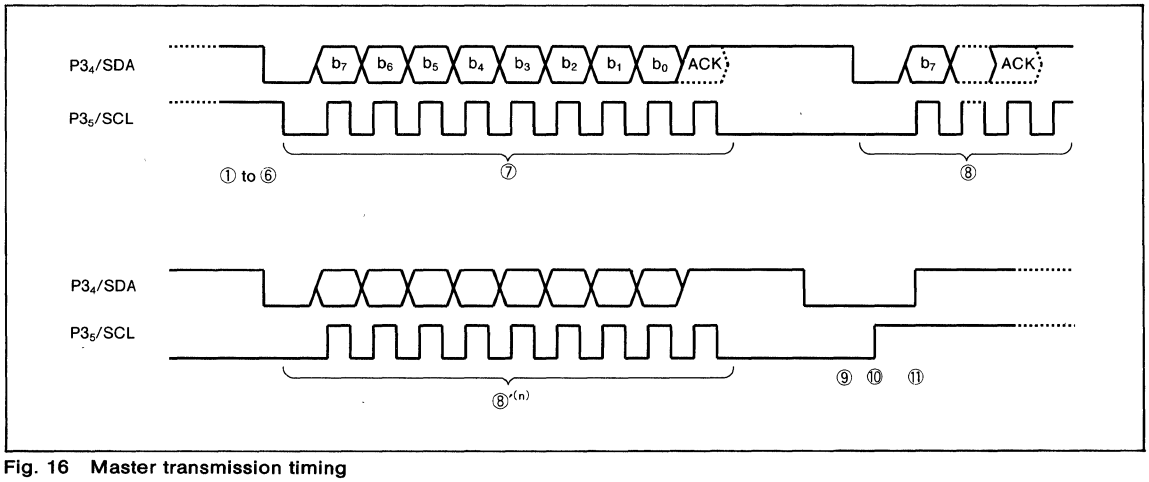

Fig. 16 Master transmission timing

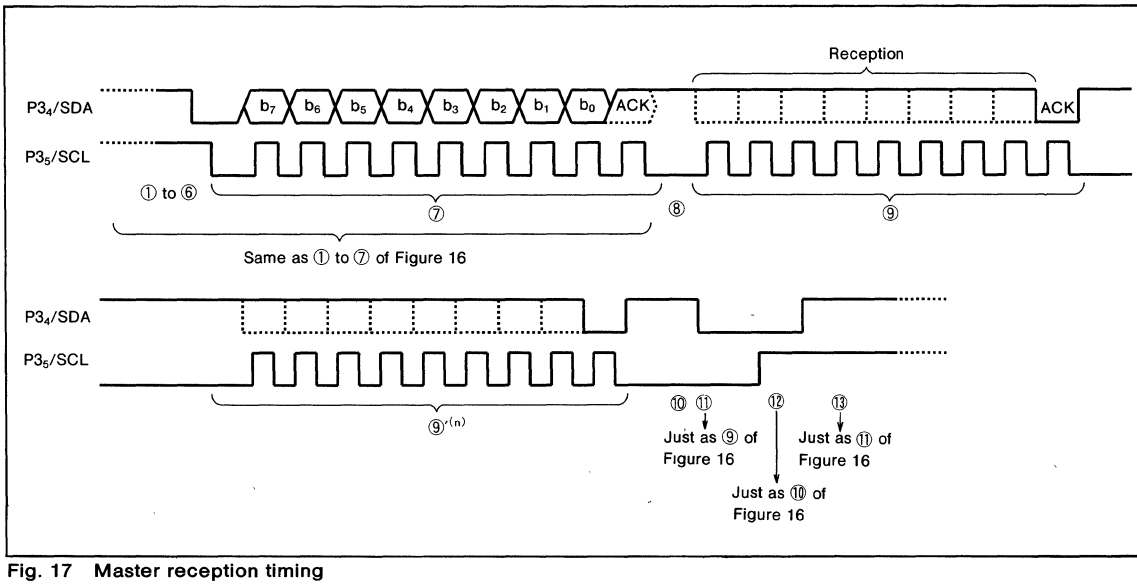

Fig. 17 Master reception timing

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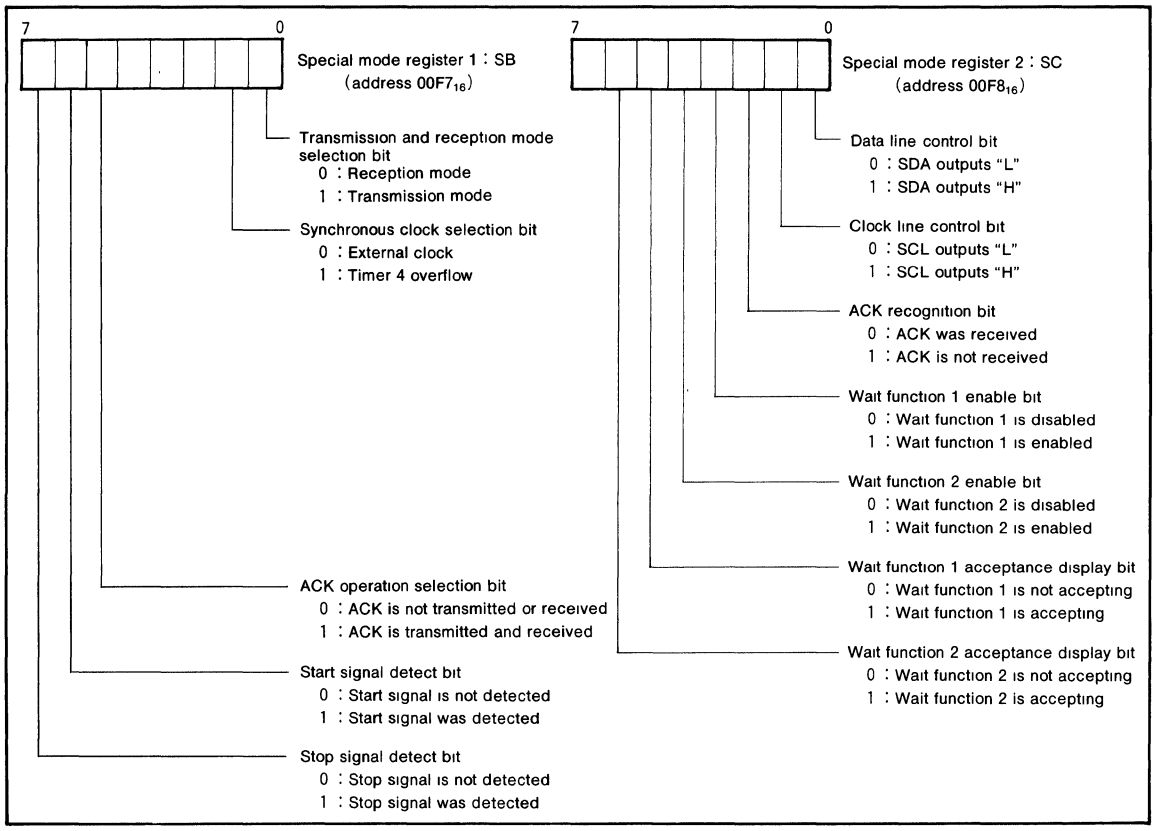


Fig. 18 Structure of special mode registers 1 and 2

(3) Wait functions

Wait function 1 holds the SCL line at "L" after the 8th clock falls in special mode. Wait function 2 holds the SCL line at "L" after the 9th clock falls in the same way.

When one of the wait functions operates, the internal counter that counts the clock must be reset after bit 3 or 4 of the special mode register 2 is set to "1", to enable the corresponding wait function 1 or 2 to operate, Reset the internal counter by writing data to the special serial I/O register (address 00F6$_{16}$), or by setting the START signal detection bit to "1". Reset the internal counter for each byte before data transfer.

The wait functions can be released by setting the corresponding bit 5 or 6 of the special mode register 2 to "1".

Note 1 : Clear the START signal detection bit (bit 6) and the STOP signal detection bit (bit 7) of the special mode register 1 by writing "1" to bit 6 or bit 7.

2 : If the special serial I/O function is operating, change the value of bit 4 of the sync generator control register (address 00E9$_{16}$) to suit the frequency of the system clock (X_{IN}).

CRT DISPLAY FUNCTIONS

Table 2 outlines the CRT display functions of the M37260M6-XXXSP. The M37260M6-XXXSP incorporates a 40 columns×3 lines CRT display control circuit. CRT display is controlled by the CRT display control register.

Up to 510 kinds of characters can be displayed, and colors can be specified for each character. A combination of up to 16 colors can be obtained by using each output signal (R, G, B, and I).

Table 2. Outline of CRT display functions

Item		Efficiency
Display characters		40 characters×3 lines (maximum 25 lines)
Character configuration		12×20 or 16×20 dots
Kinds of character		510 kinds
Character size		30 kinds
Color	Kinds of color	16 (maximum)
	Coloring unit	Character
Extension display		Possible (multiple lines)

Characters are displayed in a 12×20 or 16×20 dots configuration to obtain smooth character patterns. (See Figure 19)

The following shows the procedure how to display characters on the CRT screen.

① Write the display character code to the display RAM.
② Write the color code to the display RAM.
③ Specify the vertical position and character size by using the vertical position register and the character size register.
④ Specify the horizontal position by using the horizontal position register.
⑤ Write the display enable bit to the designated block display flag of the CRT control register. When this is done, the CRT starts operation according to the input of the V_{SYNC} signal.

The CRT display circuit has an extended display mode. This mode allows multiple lines (more than 4 lines) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Figure 20 shows a block diagram of the CRT display control circuit. Figure 21 shows the structure of the CRT display control register.

And the mixing circuit is built-in that can be output the signal mixed external color signals with internal color signals, so that the CRT display can be controlled by the 2-chip constructed system.

The sync generator that generates the synchronous signal can be output each synchronous signal as NTSC or PAL with/without interlacing.

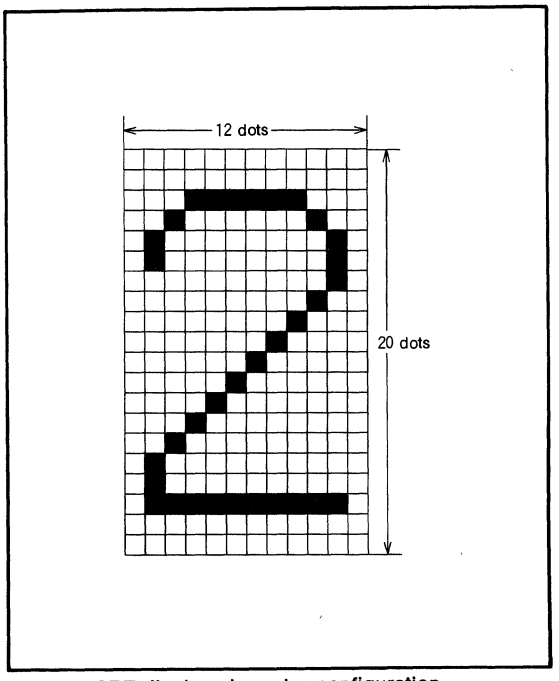


Fig. 19 CRT display character configuration

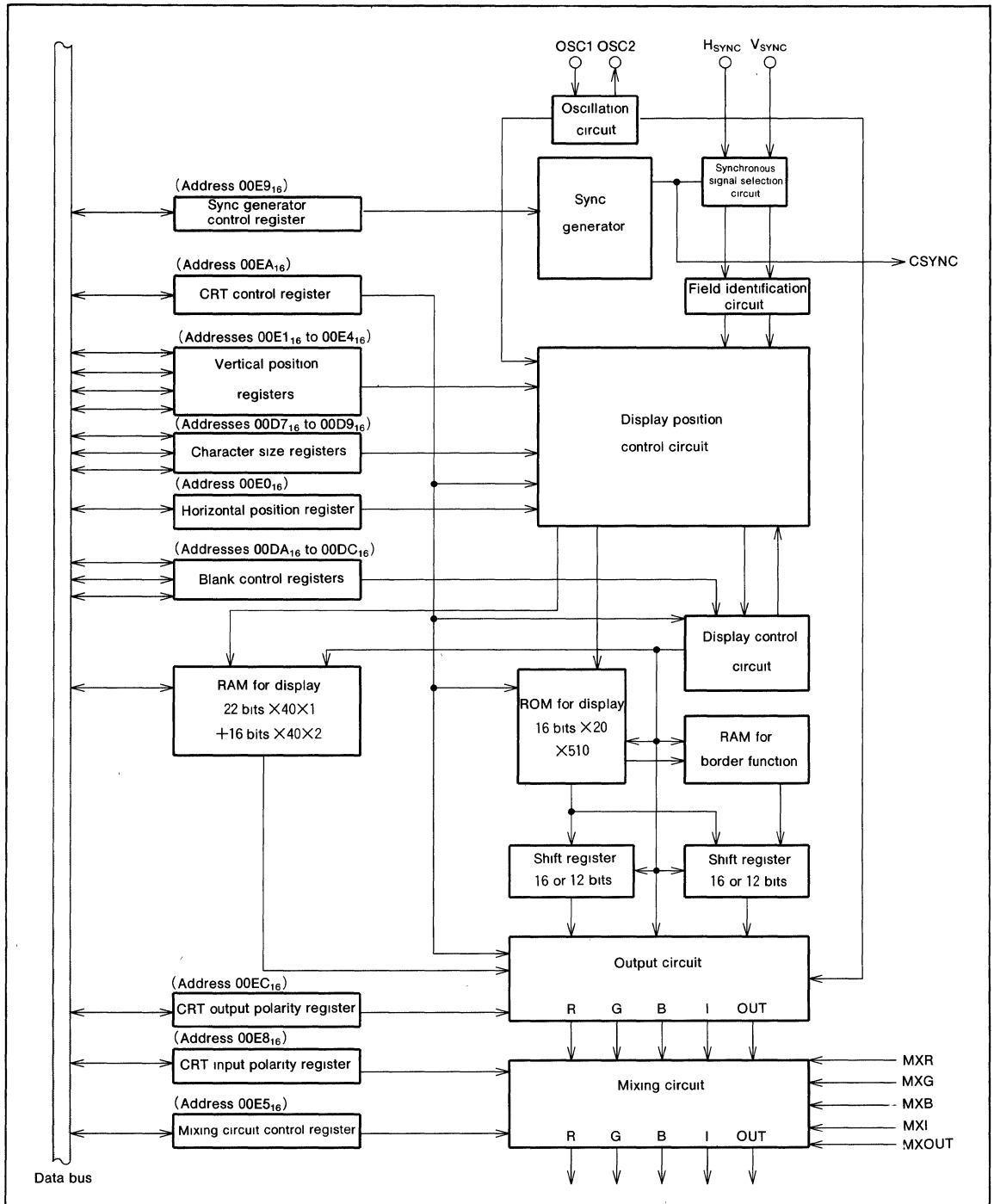


Fig. 20 CRT display control circuit block diagram

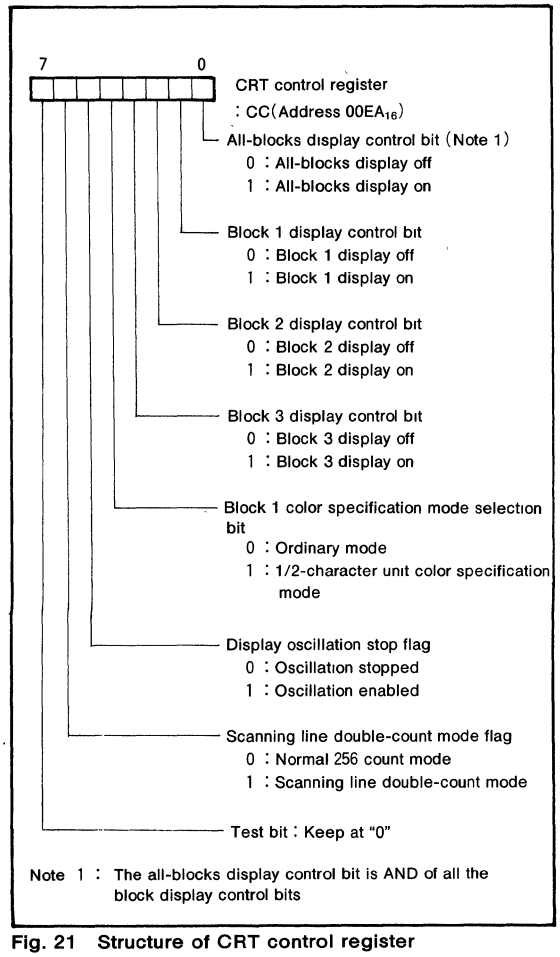


Fig. 21 Structure of CRT control register

(1) Display Position

Character display position is specified in units called blocks. There are three blocks—block 1 to block 3—and each block can hold up to 40 characters (for details, see the previous section (3) Display Memory.)

The display position of each block can be set horizontally and vertically by software.

Horizontal positions can be selected for all blocks in common from 256-steps in 4Tc units (Where Tc : display oscillation period).

Vertical display positions can be selected for each block from 1024-steps in single scanning line units.

If a display start position is superimposed on another block ((b) in Figure 23), the block with the smallest number (1 to 3) is displayed.

If the display position of a block comes while another block is displayed ((c) in Figure 23), the second block is displayed.

Vertical positions for each block can be set in 1024 steps (where each step is one scanning line) as values 00_{16} to FF_{16} in vertical position registers 1 to 3 (addresses $00E1_{16}$ to $00E3_{16}$) and values 00_{16} to $3F_{16}$ in bits 0 to 5 of vertical position register 4. The structures of the vertical position registers are shown in Figure 22.

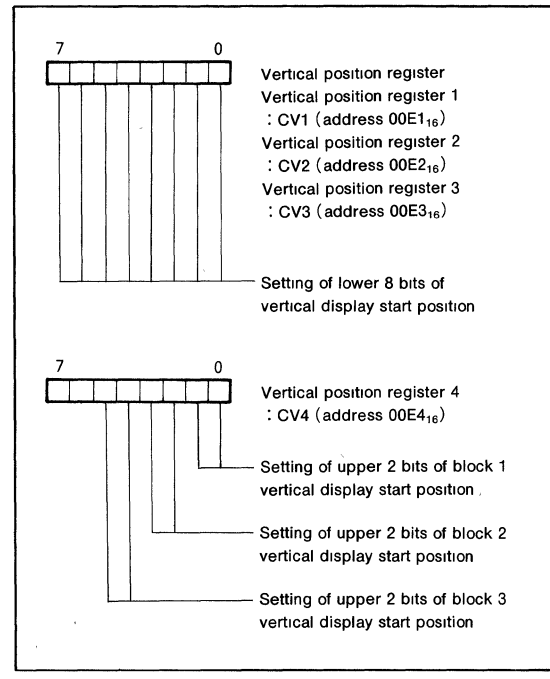
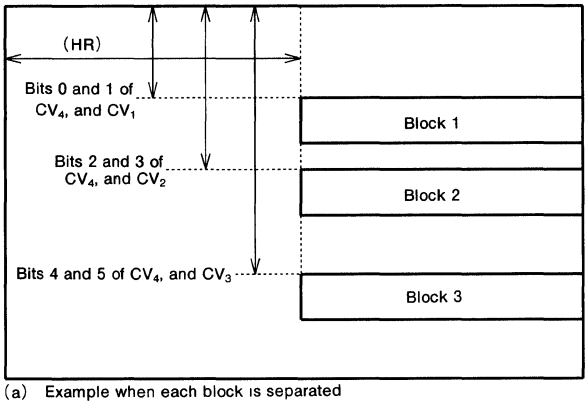
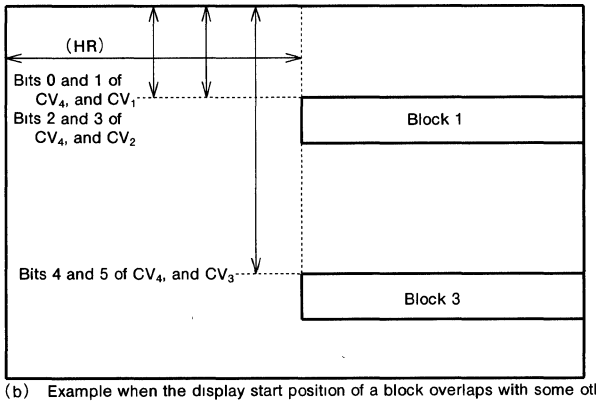


Fig. 22 Structure of vertical position registers

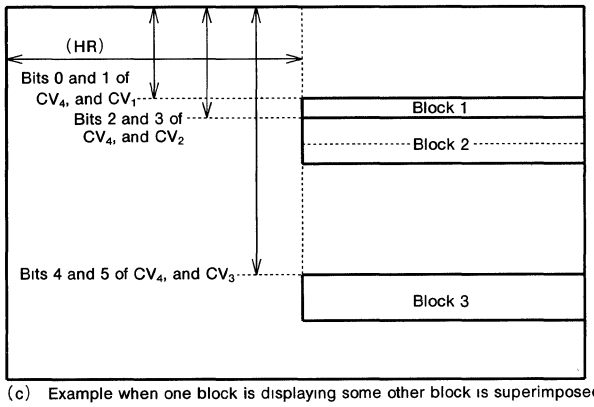
The horizontal position is common to all blocks, and can be set in 256 steps (where one step is $4T_C$, T_C being the display oscillation period) as values 00_{16} to FF_{16} in the horizontal position register (address $00E0_{16}$). The structure of the horizontal position register is shown in Figure 24.



(a) Example when each block is separated



(b) Example when the display start position of a block overlaps with some other block



(c) Example when one block is displaying some other block is superimposed

Fig. 23 Display position and value of vertical position registers CVx (x : 1 to 4)

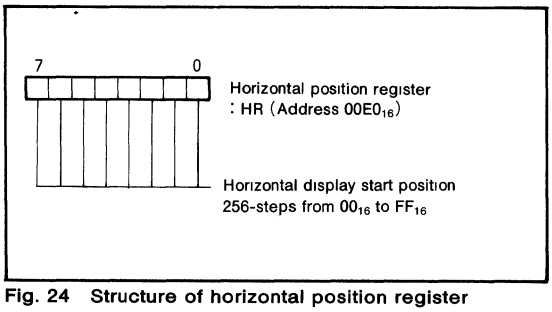


Fig. 24 Structure of horizontal position register

(2) Character Size

The size of characters to be displayed can be selected from 30 types, by combining 5 vertical types and 6 horizontal types in block units. Set the size with the character size registers (addresses 00D7$_{16}$ to 00D9$_{16}$). Either of two character font configurations, 12 dots wide×20 dots high or 16 dots wide×20 dots high, can be selected for each block. The configuration of the character ROM font is shown in Figure 26.

The display start position in the horizontal direction is the same, regardless of changes in character size, but it does differ if the character font configuration is changed. The display start position in the horizontal direction for 16 dots wide×20 dots high characters is 4T_C to the right of that for 12 dots wide×20 dots high characters.

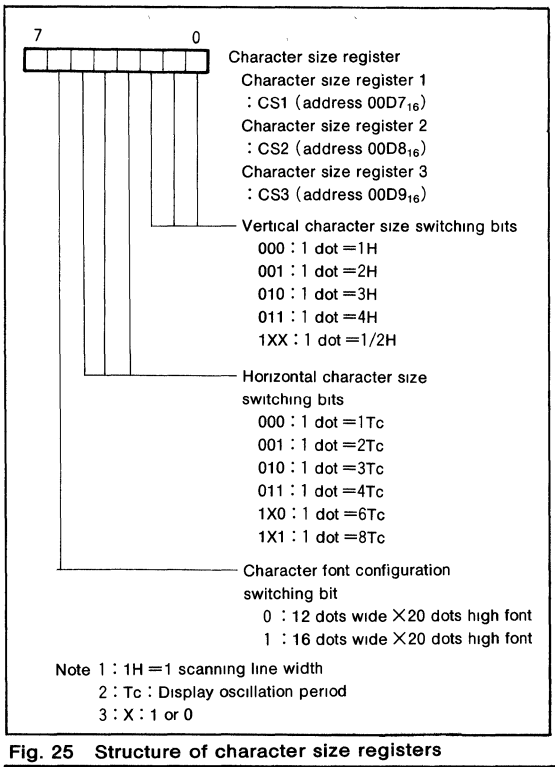


Fig. 25 Structure of character size registers

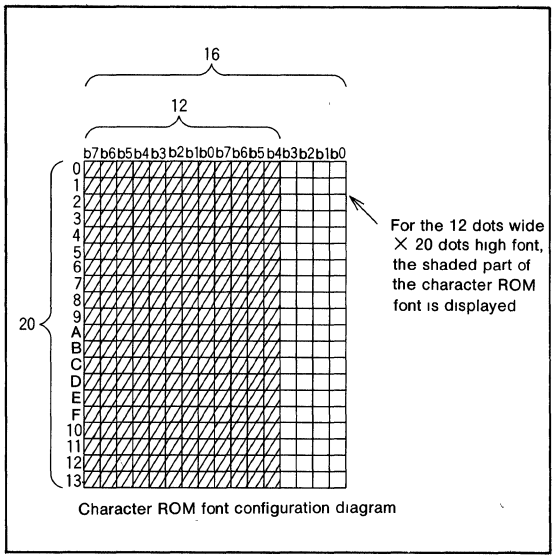


Fig. 26 Character ROM font for 12 dots wide × 20 dots high font

The 1 dot=1/2 scanning line display function differentiates between odd-numbered and even-numbered fields from differences in the waveform in the synchronization signals used by the interlace method, and displays one character font for both fields. Bit 6 of the sync generator control register (address $00E9_{16}$) controls the active edge of the field identification flag, and the character font divided for each field can be selected.
The field identification flag can also be read out from bit 6 of the display block counter (address $00EB_{16}$).

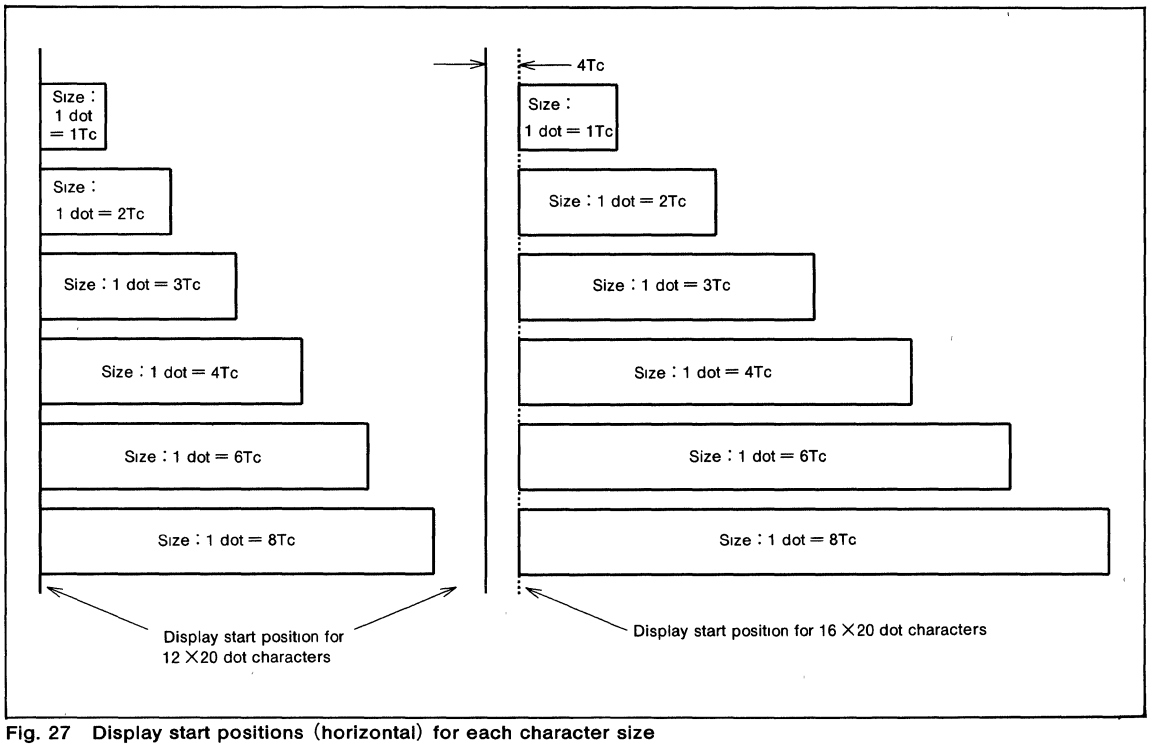


Fig. 27 Display start positions (horizontal) for each character size

The description below assumes that field identification is based on the case where the active edges of both the horizontal and vertical synchronization signals are negative.
Each field is identified as either odd or even by the hardware detecting the positions of the falling edges of the horizontal and vertical synchronization signals, and comparing them. Therefore, to ensure correct field identification, make sure that the two synchronization signals are input in accordance with the identification criteria given below.
Since the field identification is based on the system clock (X_{IN}), make sure that the value of bit 4 of the sync generator control register (address $00E9_{16}$) is changed in accordance with the frequency of the system clock.

Even-numbered field : The vertical synchronization signal falls within 2μs before or after the fall of the horizontal synchronization signal.

Odd-numbered field : The vertical synchronization signal falls within 2μs before or after a point 1/2 a cycle after the fall of the horizontal synchronization signal.

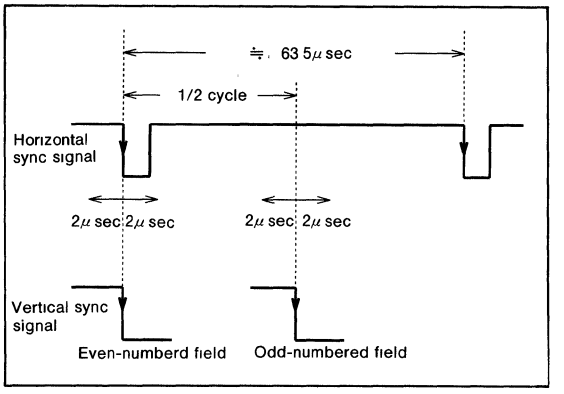
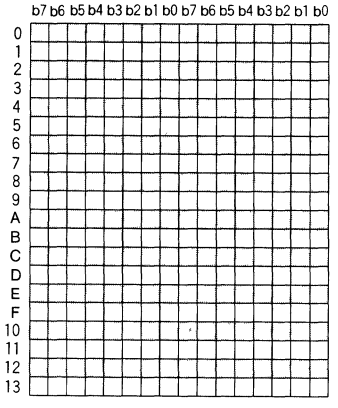


Fig. 28 Identification criteria for field identification

Field	Sync signal (Example : negative edge input)	Field identification flag active edge bit (bit 6 of the sync generator control register)	Field identification flag bit (bit 6 of the display block counter)	Display font
Odd-numbered field	Horizontal sync signal / Vertical sync signal	0	1	□ part
		1	0	□ part
Even-numbered field	Horizontal sync signal / Vertical sync signal	0	0	□ part
		1	1	□ part



Character ROM font configuration

Example : When the field identification flag active edge bit is 0, odd-numbered fields display the □ font and even-numbered fields display the □ font, Bit 6 of the display block counter can be read as the field identification flag : it is "1" for an odd-numbered field, "0" for an even-numbered field

Note : The field identification flag changes at the fall of the vertical sync signal (negative edge input)

Fig. 29 Relationships between field identification flag and display font

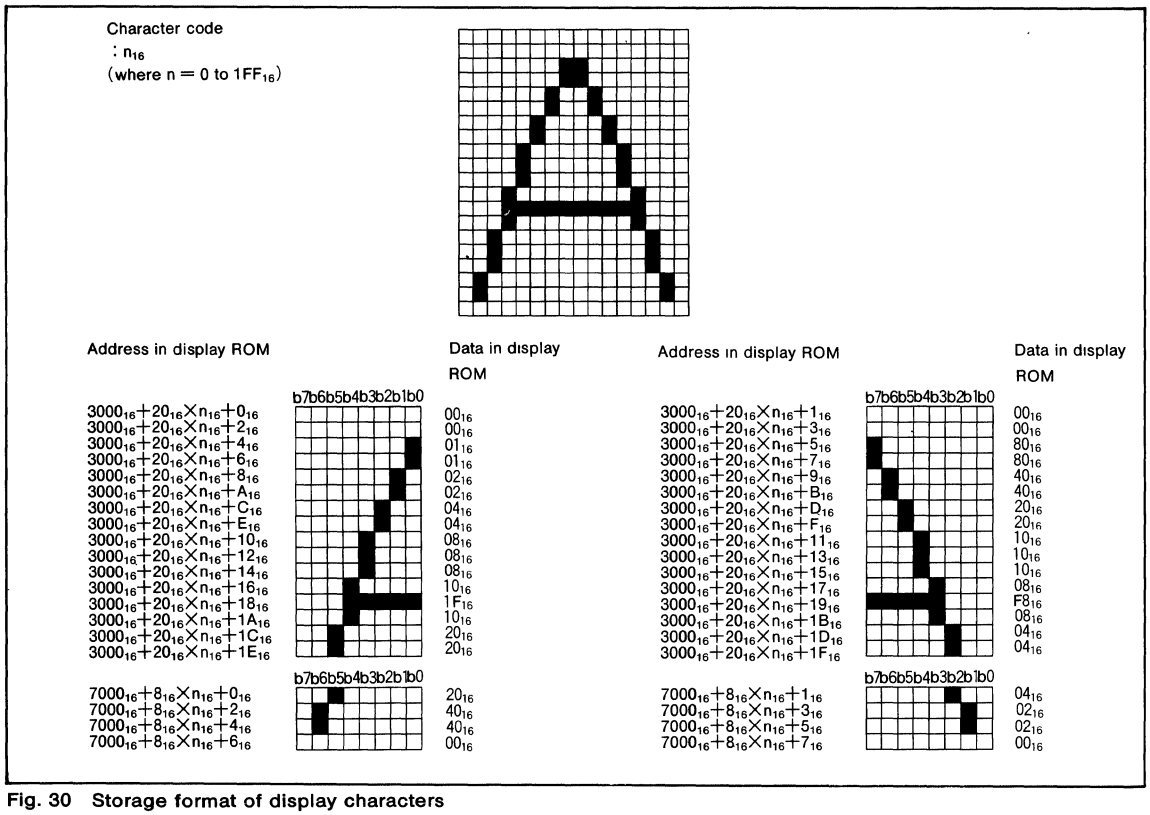


Fig. 30 Storage format of display characters

(3) Display Memory

There are two types of display memory: CRT display ROM (addresses 3000_{16} to $7FFF_{16}$) which contains previously stored (masked) character dot data, and display RAM (addresses 2000_{16} to $27FF_{16}$) which specifies characters and colors to be displayed. These memory types are described below.

① CRT display ROM (addresses 3000_{16} to $7FFF_{16}$)

The CRT display ROM contains dot pattern data for display characters. To display these stored characters in operation, specify character codes (code determined based on addresses in CRT display ROM) that are specific to those characters, by writing them to the CRT display RAM.

Since the CRT display ROM has contains 20K bytes and the data for one character takes up 40 bytes, 512 characters can be stored. However, a two-character space is required for test purposes, so in practice 510 characters can be stored for display.

Within the CRT display ROM area, data for part of each character that is [upper 16 dots high] × [left-hand 8 dots wide] is stored at addresses $300X_{16}$ to $3FFX_{16}$ (where X = 0, 2, 4, 6, 8, A, C, E), data for part of each character that is [upper 16 dots high] × [right-hand 8 dots wide] is stored at $300Y_{16}$ to $3FFY_{16}$ (where Y=1, 3, 5, 7, 9, B, D, F), data for part of each character that is [lower 4 dots high] × [left-hand 8 dots wide] is stored at addresses $700M_{16}$ to $7FFM_{16}$ (where M=0, 2, 4, 6, 8, A, C, E), and data for part of each character that is [lower 4 dots high] × [right-hand 8 dots wide] is stored at $700N_{16}$ to $7FFN_{16}$ (where N=1, 3, 5, 7, 9, B, D, F), as shown in Figure 30.

Table 3. Character Code Chart (Partially abbreviated)

Character code	Character data storage address			
	Left-hand 8 dots		Right-hand 8 dots	
	Upper 16 dots	Lower 4 dots	Upper 16 dots	Lower 4 dots
000_{16}	3000_{16}	7000_{16}	3001_{16}	7001_{16}
	3002_{16}	7002_{16}	3003_{16}	7003_{16}
	3004_{16}	7004_{16}	3005_{16}	7005_{16}
	3006_{16}	7006_{16}	3007_{16}	7007_{16}
	3008_{16}		3009_{16}	
	$300A_{16}$		$300B_{16}$	
	$300C_{16}$		$300D_{16}$	
	$300E_{16}$		$300F_{16}$	
	3010_{16}		3011_{16}	
	3012_{16}		3013_{16}	
	3014_{16}		3015_{16}	
	3016_{16}		3017_{16}	
	3018_{16}		3019_{16}	
	$301A_{16}$		$301B_{16}$	
	$301C_{16}$		$301D_{16}$	
	$301E_{16}$		$301F_{16}$	
001_{16}	3020_{16}	7008_{16}	3021_{16}	7009_{16}
	3022_{16}	$700A_{16}$	3023_{16}	$700B_{16}$
	3024_{16}	$700C_{16}$	3025_{16}	$700D_{16}$
	3026_{16}	$700E_{16}$	3027_{16}	$700F_{16}$
	3028_{16}		3029_{16}	
	$302A_{16}$		$302B_{16}$	
	$302C_{16}$		$302D_{16}$	
	$302E_{16}$		$302F_{16}$	
	3030_{16}		3031_{16}	
	3032_{16}		3033_{16}	
	3034_{16}		3035_{16}	
	3036_{16}		3037_{16}	
	3038_{16}		3039_{16}	
	$303A_{16}$		$303B_{16}$	
	$303C_{16}$		$303D_{16}$	
	$303E_{16}$		$303F_{16}$	
⋮	⋮	⋮	⋮	⋮
$1FF_{16}$	$6FE0_{16}$	$7FF8_{16}$	$6FE1_{16}$	$7FF9_{16}$
	$6FE2_{16}$	$7FFA_{16}$	$6FE3_{16}$	$7FFB_{16}$
	$6FE4_{16}$	$7FFC_{16}$	$6FE5_{16}$	$7FFD_{16}$
	$6FE6_{16}$	$7FFE_{16}$	$6FE7_{16}$	$7FFF_{16}$
	$6FE8_{16}$		$6FE9_{16}$	
	$6FEA_{16}$		$6FEB_{16}$	
	$6FEC_{16}$		$6FED_{16}$	
	$6FEE_{16}$		$6FEF_{16}$	
	$6FF0_{16}$		$6FF1_{16}$	
	$6FF2_{16}$		$6FF3_{16}$	
	$6FF4_{16}$		$6FF5_{16}$	
	$6FF6_{16}$		$6FF7_{16}$	
	$6FF8_{16}$		$6FF9_{16}$	
	$6FFA_{16}$		$6FFB_{16}$	
	$6FFC_{16}$		$6FFD_{16}$	
	$6FFE_{16}$		$6FFF_{16}$	

Each character code used when specifying display characters is defined as n_{16} (where n = 0 to 1FF), and is determined based on the address in CRT display ROM that contains the data for that character (see the storage format of display character shown in Fig. 30). The character codes are listed in Table 3.

② CRT display RAM (addresses 2000_{16} to $27FF_{16}$)

The CRT display RAM is allocated at addresses 2000_{16} to $27FF_{16}$, and is divided into a display character code specification part and a display color code specififcation part for each block. The contents of this area are shown in Table 4.

For example, to display one character at the first character position (the left edge) of block 1, write the character code to bit 6 of address $20C0_{16}$ and to address 2000_{16}, and write the color code to the lowermost 6 bits (bits 0 to 5) of address $20C0_{16}$. For details of the color codes, see section (4) Color codes. The structure of the CRT display RAM is shown in Fig. 31.

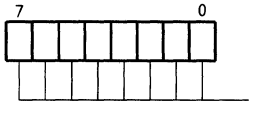
When generating a mask for the M37260M6-XXXSP, note that the character patterns of Table 6 and Table 7 must be written to the specified addresses as a test character pattern.

Table 4. CRT display RAM description

Block	Display position (from left side)	Character code specification		Color code specification	1/2 character unit color code specification
		High-order 1 bit	Low-order 8 bit		
Block 1	1st character	$20C0_{16}$	2000_{16}	$20C0_{16}$	2180_{16}
	2nd character	$20C1_{16}$	2001_{16}	$20C1_{16}$	2181_{16}
	3rd character	$20C2_{16}$	2002_{16}	$20C2_{16}$	2182_{16}
	⋮	⋮	⋮	⋮	⋮
	38th character	$20E5_{16}$	2025_{16}	$20E5_{16}$	$21A5_{16}$
	39th character	$20E6_{16}$	2026_{16}	$20E6_{16}$	$21A6_{16}$
	40th character	$20E7_{16}$	2027_{16}	$20E7_{16}$	$21A7_{16}$
Not used		$20E8_{16}$ to $20FF_{16}$	2028_{16} to $203F_{16}$	$20E8_{16}$ to $20FF_{16}$	
Block 2	1st character	2100_{16}	2040_{16}	2100_{16}	
	2nd character	2101_{16}	2041_{16}	2101_{16}	
	3rd character	2102_{16}	2042_{16}	2102_{16}	
	⋮	⋮	⋮	⋮	
	38th character	2125_{16}	2065_{16}	2125_{16}	
	39th character	2126_{16}	2066_{16}	2126_{16}	
	40th character	2127_{16}	2067_{16}	2127_{16}	
Not used		2128_{16} to $213F_{16}$	2068_{16} to $207F_{16}$	2128_{16} to $213F_{16}$	
Block 3	1st character	2140_{16}	2080_{16}	2140_{16}	
	2nd character	2141_{16}	2081_{16}	2141_{16}	
	3rd character	2142_{16}	2082_{16}	2142_{16}	
	⋮	⋮	⋮	⋮	
	38th character	2165_{16}	$20A5_{16}$	2165_{16}	
	39th character	2166_{16}	$20A6_{16}$	2166_{16}	
	40th character	2167_{16}	$20A7_{16}$	2167_{16}	
Not used		2168_{16} to $217F_{16}$	$20A8_{16}$ to $20BF_{16}$	2168_{16} to $217F_{16}$	

Block 1
[Character specification]

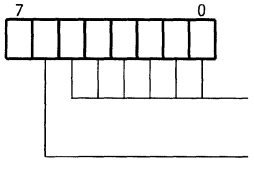
1st column : 2000_{16}
to
40th column : 2027_{16}



Low-order 8 bits of character code

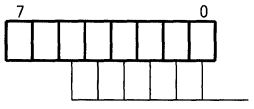
[Color and character specification]

1st column : $20C0_{16}$
to
40th column : $20E7_{16}$



Color code specification in the normal mode or former 1/2 color code specification in the 1/2-character unit color specification mode
High-order 1 bit of character code

1st column : 2180_{16}
to
40th column : $21A7_{16}$

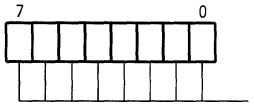


Latter 1/2 color code specification in the 1/2-character unit color specification mode

Block 2 and 3
[Character specification]

1st column : 2040_{16}
to
40th column : 2067_{16}

(Addresses 2080_{16} to $20A7_{16}$ in the case of block 3)

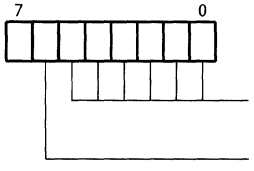


Low-order 8 bits of character code

[Color and character specification]

1st column : 2100_{16}
to
40th column : 2127_{16}

(Addresses 2140_{16} to 2167_{16} in the case of block 3)



Color code specification

High-order 1 bit of character code

Fig. 31 Structure of CRT display RAM

③ Block overwriting function of display memory

Character codes or color codes for 40 characters can be written for each block in a batch by overwriting data at a specific address.

The addresses for block overwriting, the addresses in display memory overwritten by these addresses, and the contents of these addresses are listed in Table 5.

Table 5. Block overwriting of display memory

Address for block overwriting	Addresses in overwritten display memory	Memory contents
2200_{16}	2000_{16} to 2027_{16}	Block 1 character code
2201_{16}	2040_{16} to 2067_{16}	Block 2 character code
2202_{16}	2080_{16} to $20A7_{16}$	Block 3 character code
2203_{16}	$20C0_{16}$ to $20E7_{16}$	Block 1 color code
2204_{16}	2100_{16} to 2127_{16}	Block 2 color code
2205_{16}	2140_{16} to 2167_{16}	Block 3 color code
2206_{16}	2180_{16} to $21A7_{16}$	Block 1 color code 2

Note : After a write instruction is executed for a block overwriting address, wait at least 60 machine cycles before issuing a read or write instruction from the CPU for a block overwriting address or for display memory.

④ Notes on display RAM data access

If the display RAM is accessed (data read or write, block write) from the CPU during OSD display, make sure that the display RAM for each block is accessed after it has been confirmed that the block has been displayed, by an event such as a CRT interrupt.

RAM data can be destroyed if the display RAM for a block that is currently being displayed is accessed.

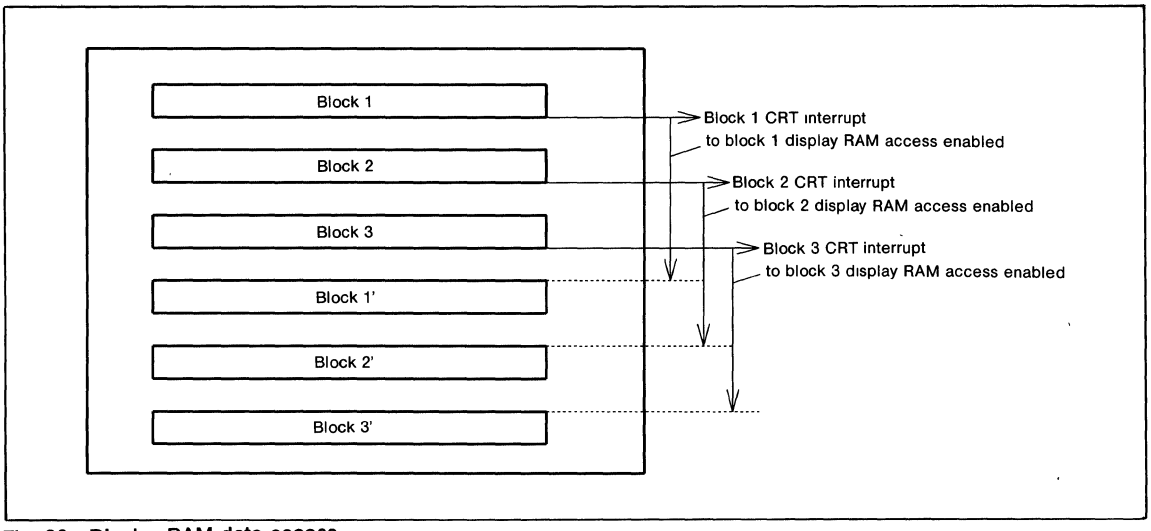


Fig. 32 Display RAM date access

Table 6. Test character pattern 1 settings

Address	Data	Address	Data
$6FE0_{16}$	00_{16}	$6FF0_{16}$	00_{16}
$6FE1_{16}$	00_{16}	$6FF1_{16}$	00_{16}
$6FE2_{16}$	00_{16}	$6FF2_{16}$	00_{16}
$6FE3_{16}$	00_{16}	$6FF3_{16}$	00_{16}
$6FE4_{16}$	00_{16}	$6FF4_{16}$	00_{16}
$6FE5_{16}$	00_{16}	$6FF5_{16}$	00_{16}
$6FE6_{16}$	00_{16}	$6FF6_{16}$	00_{16}
$6FE7_{16}$	00_{16}	$6FF7_{16}$	00_{16}
$6FE8_{16}$	00_{16}	$6FF8_{16}$	00_{16}
$6FE9_{16}$	00_{16}	$6FF9_{16}$	00_{16}
$6FEA_{16}$	00_{16}	$6FFA_{16}$	00_{16}
$6FEB_{16}$	00_{16}	$6FFB_{16}$	00_{16}
$6FEC_{16}$	00_{16}	$6FFC_{16}$	00_{16}
$6FED_{16}$	00_{16}	$6FFD_{16}$	00_{16}
$6FEE_{16}$	00_{16}	$6FFE_{16}$	00_{16}
$6FEF_{16}$	00_{16}	$6FFF_{16}$	00_{16}
$7FF8_{16}$	00_{16}	$7FFC_{16}$	00_{16}
$7FF9_{16}$	00_{16}	$7FFD_{16}$	00_{16}
$7FFA_{16}$	00_{16}	$7FFE_{16}$	00_{16}
$7FFB_{16}$	00_{16}	$7FFF_{16}$	00_{16}

Table 7. Test character pattern 2 settings

Address	Data	Address	Data
$6FC0_{16}$	88_{16}	$6FD0_{16}$	22_{16}
$6FC1_{16}$	11_{16}	$6FD1_{16}$	22_{16}
$6FC2_{16}$	00_{16}	$6FD2_{16}$	00_{16}
$6FC3_{16}$	00_{16}	$6FD3_{16}$	00_{16}
$6FC4_{16}$	00_{16}	$6FD4_{16}$	00_{16}
$6FC5_{16}$	00_{16}	$6FD5_{16}$	00_{16}
$6FC6_{16}$	00_{16}	$6FD6_{16}$	00_{16}
$6FC7_{16}$	00_{16}	$6FD7_{16}$	00_{16}
$6FC8_{16}$	44_{16}	$6FD8_{16}$	11_{16}
$6FC9_{16}$	44_{16}	$6FD9_{16}$	11_{16}
$6FCA_{16}$	00_{16}	$6FDA_{16}$	00_{16}
$6FCB_{16}$	00_{16}	$6FDB_{16}$	00_{16}
$6FCC_{16}$	00_{16}	$6FDC_{16}$	00_{16}
$6FCD_{16}$	00_{16}	$6FDD_{16}$	00_{16}
$6FCE_{16}$	00_{16}	$6FDE_{16}$	00_{16}
$6FCF_{16}$	00_{16}	$6FDF_{16}$	00_{16}
$7FF0_{16}$	08_{16}	$7FF4_{16}$	00_{16}
$7FF1_{16}$	88_{16}	$7FF5_{16}$	00_{16}
$7FF2_{16}$	00_{16}	$7FF6_{16}$	80_{16}
$7FF3_{16}$	00_{16}	$7FF7_{16}$	11_{16}

(4) Color Codes

The color each display character can be specified by specifying the four color outputs (R, G, B, and I) with the CRT display RAM. A color code can be specified for each character, and 2^4=16 colors can be set.

The R, G, B, and I outputs are set by bits 0 to 3 of the color code, character or blank output is set by bit 4, and character output or blank output is specified by bit 5. The structure of the color code is shown in Figure 33.

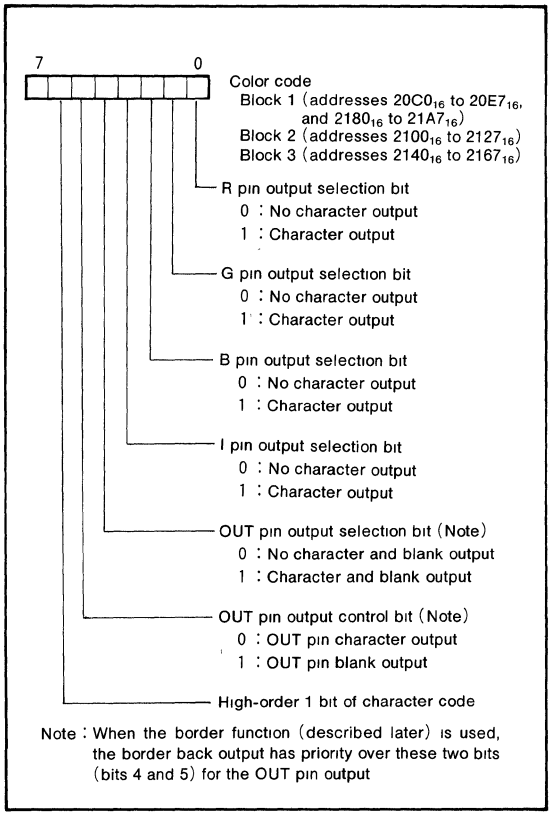


Fig. 33 Structure of color code

(5) 1/2-Character Unit Color Specification Mode

Colors can be specified in 1/2-characters units for the characters of block 1 alone, by setting bit 4 of the CRT control register (address $00EA_{16}$). In 1/2-character unit color specification mode, each half of a display character in block 1 is displayed as follows:

- Left-hand half : The color of the color code specified by bits 0 to 5 of color code specification addresses $20C0_{16}$ to $20E7_{16}$ in the CRT display RAM.
- Right-hand half : The color of the color code specified by bits 0 to 5 of color code specification addresses 2180_{16} to $21A7_{16}$ in the CRT display RAM.

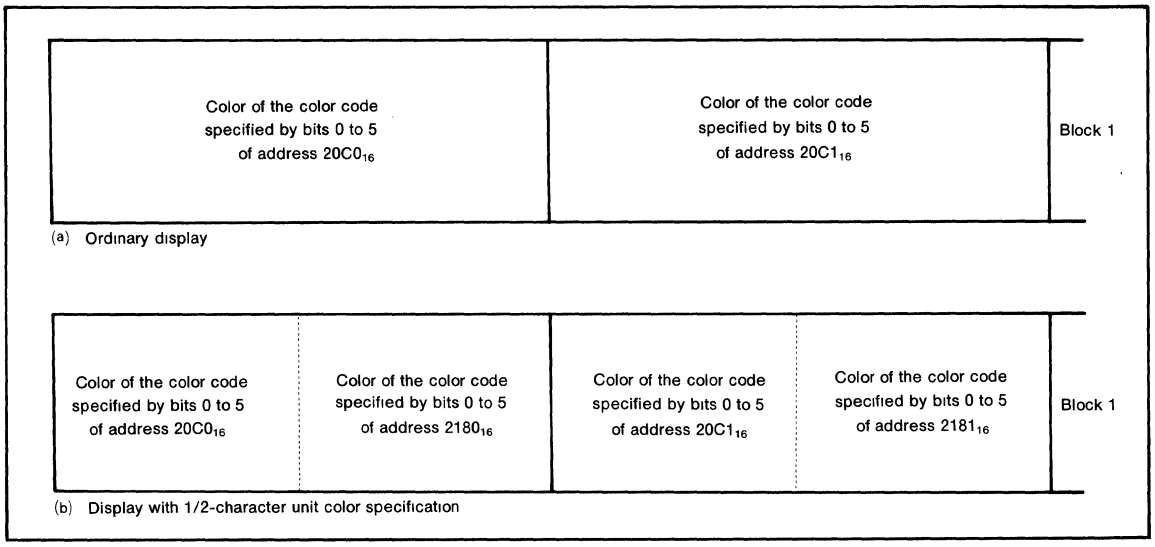


Fig. 34 Correspondence between ordinary color specification and 1/2-character unit color specification mode

(6) Multiline Display

The M37260M6-XXXSP can ordinarily display three lines of characters, in three blocks with different vertical positions. In addition, up to 25 lines can be displayed by using CRT interrupts and the display block counter.

A CRT interrupt is a function that generates an interrupt for each block at the point at which the display of any desired number of dots has been completed. In other words, when a scanning line reaches the point of the display position (specified by the vertical and horizontal position registers) of a certain block, the character display of that block starts, and an interrupt is issued at the point at which the number of dots set by the interrupt position control register is exceeded.

If the lateral character size has been set to 1 dot = 1/2 scanning line width, the CRT interrupt position can be set to 10 steps in 1 block/2 dot units; for all other scanning line widths it can be set to 20 steps in 1 block/1 dot units.

The display block counter counts the number of times the display of a block has been completed, and its contents are incremented by 1 each time the display of one block is completed.

To provide multiline display, enable CRT interrupts by clearing the interrupt disable flag to "0" and setting the CRT interrupt enable bit (bit 4 at address $00FE_{16}$) to "1". The processing within the CRT interrupt processing routine is as follows.

①Read the value of the display block counter.
②The value of ① enables identification of a block whose display has completed (whether a CRT interrupt generation cause has occurred).
③Read the interrupt position control register.
④The value of ③ enables identification of the number of dots at which the CRT interrupt is to occur.
⑤Write the display character code, color code, and display position of that block into the character code, color code (CRT display RAM contents), and vertical display position (contents of vertical position register) to be displayed next.

The structure of the display block counter is shown in Figure 35.

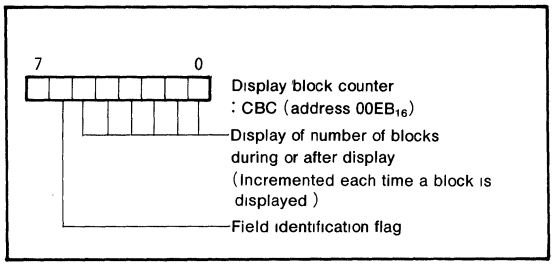


Fig. 35 Structure of display block counter

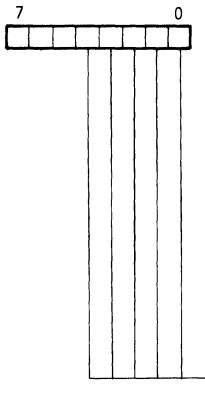


Fig. 36 Structure of interrupt position control register

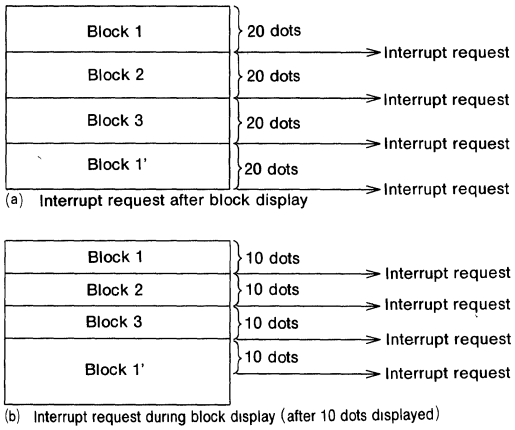


Fig. 37 Timing of CRT interrupts

(a) When lateral character size is not 1 dot =1/2 scanning line width

Interrupt occurrence position control register					Timing of interrupt request generation
b4	b3	b2	b1	b0	
0	0	0	0	0	Interrupt after completion of 1-dot display
0	0	0	0	1	Interrupt after completion of 2-dot display
0	0	0	1	0	Interrupt after completion of 3-dot display
0	0	0	1	1	Interrupt after completion of 4-dot display
		:			:
		:			:
1	0	0	1	1	Interrupt after completion of 20-dot display
		:			} Interrupts disabled (no interrupt requests)
		:			
1	1	1	1	1	

(b) When lateral character size is 1 dot =1/2 scanning line width

Interrupt occurrence position control register					Timing of interrupt request generation			
b4	b3	b2	b1	b0		Odd-numbered field	Even-numbered field	
0	0	0	0	×		1	2	
0	0	0	1	×		3	4	
0	0	1	0	×	Interrupt after	5	6	dot
0	0	1	1	×	completion of	7	8	display
		:		×		:	:	
		:		×		:	:	
1	0	0	1	×		19	20	
		:		×	} Interrupts disabled (no interrupt requests)			
		:		×				
1	1	1	1	×				

Fig. 38 Timing of interrupt request generation with respect to values in interrupt position control register

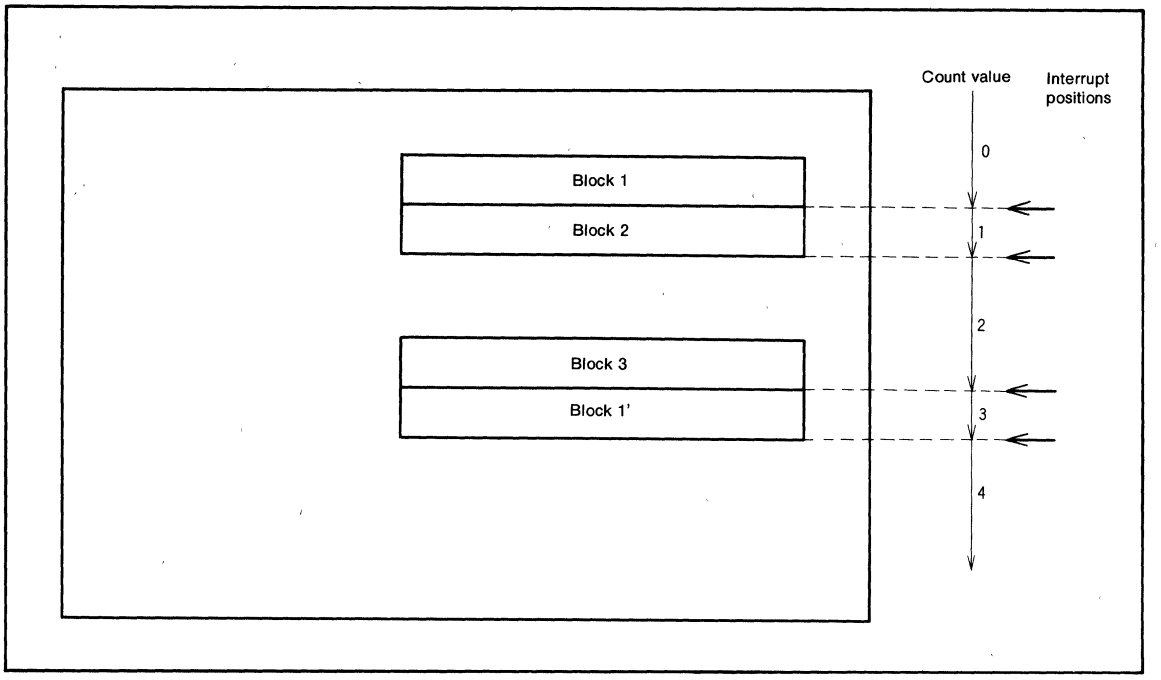


Fig. 39 Timing of CRT interrupts and values in display block counter

(7) Scanning Line Double-Count Mode

Scanning line double-count mode enables an increase in character size in the vertical direction to twice the normal size, and it can also double the display start position of the characters in the vertical direction by double-counting scanning lines. In other words, the vertical position register sets either a normal mode in which one step is one scanning line, or a scanning line double-count mode is which one step is two scanning lines.

Scanning line double-count mode can be specified by setting bit 6 of the CRT control register (address $00EA_{16}$) to "1".

Since this mode functions in screen units, a change in mode while a screen is being displayed is not validated until the next screen is displayed.

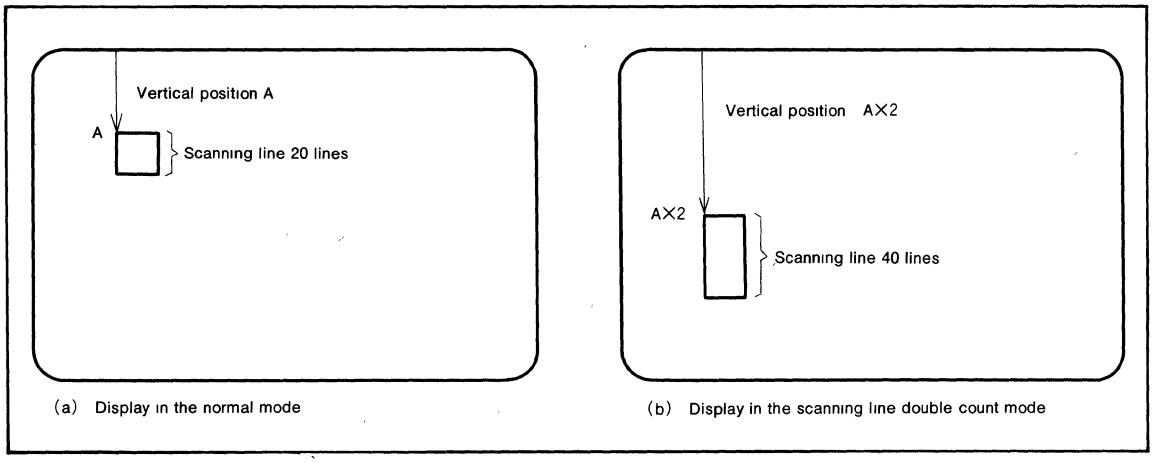


Fig. 40 Corresponding between normal mode display and scanning line double-count mode display

(8) Border Function

A one clock (one dot) border can be drawn around each character displayed, in both the horizontal and vertical directions.

This border is output from the OUT pin. In this case, bits 4 and 5 in the color code (the OUT pin output contents) are ignored, and the border output is output from the OUT pin.

The border can be set in block units by the blank control registers (addresses $00DA_{16}$ to $00DC_{16}$). The relationship between the settings of the blank control registers and the border function are listed in Table 8, and the structure of the blank control registers is shown in Fig. 42.

Table 8. Corresponding between the blank control register value and border function

Blank control register		Function	Output example
BLn1	BLn0		
X	0	Normal	R, G, B, I output OUT output
0	1	Border including character	R, G, B, I output OUT output
1	1	Border excluding character	R, G, B, I output OUT output

X : 1 or 0

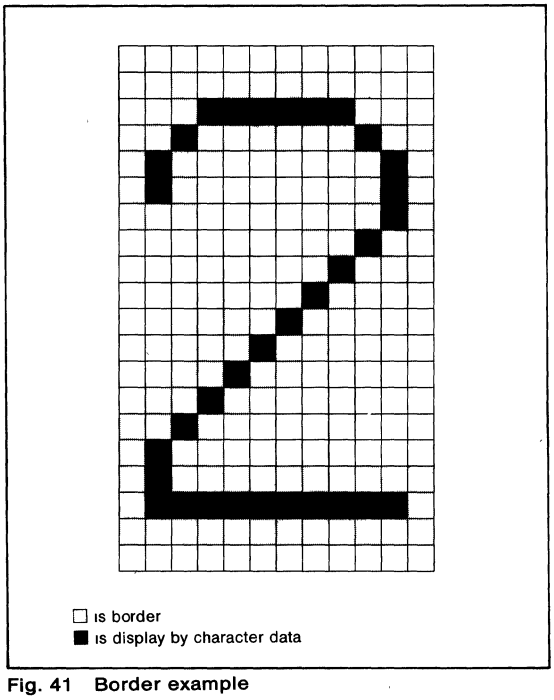


Fig. 41 Border example

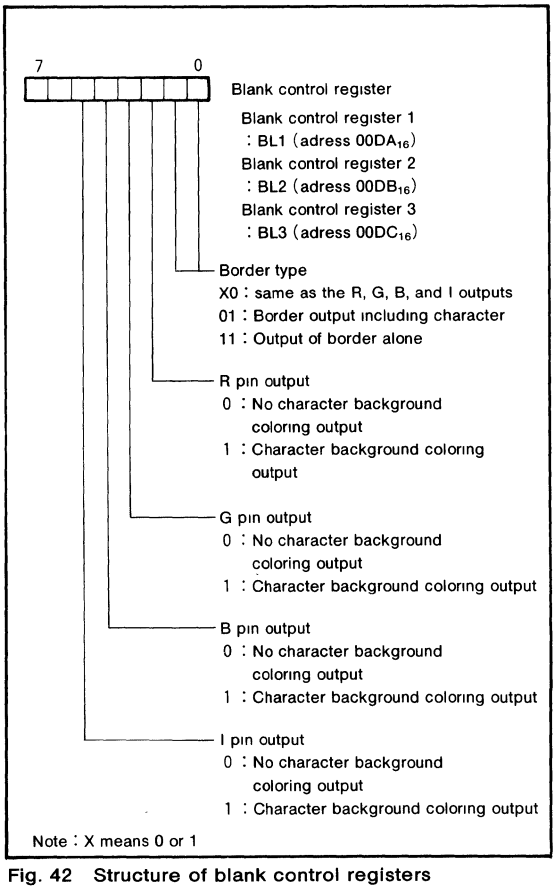
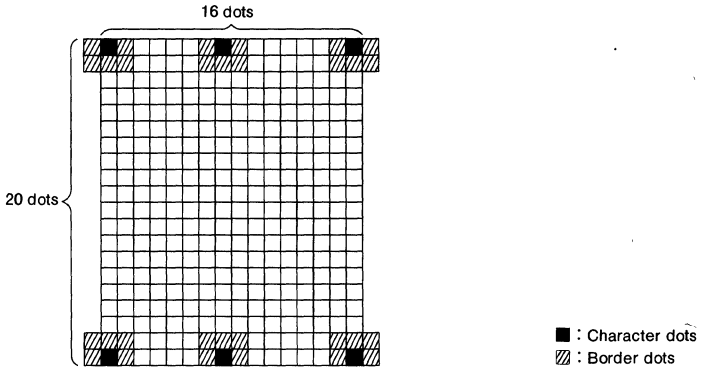


Fig. 42 Structure of blank control registers

(a) When vertical character size is not 1 dot = 1/2 scanning line width, borders avobe the uppermost dots and borders below the lowermost dots of the character font are not displayed



(b) When vertical character size is 1 dot = 1/2 scanning line width, borders avobe and below the uppermost dots and borders below the lowermost dots of the character font are not displayed

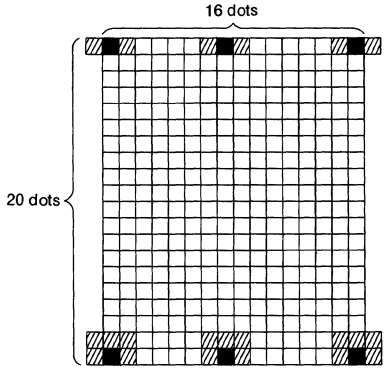


Fig. 43 Notice of border function

(9) Character Background Color Function

The character background of the 16×20 or 12×20 area of a character (the blank part), excluding the character part itself, or character border part can be colored. The background color can be selected from 16 colors set by bits 2, 3, 4, and 5 of the blank control register. Since a background color can be set for each block, up to 15 background colors can be set for a screen when multi-line display is used.

Six character display types with background colors can be selected by combining bits 4 and 5 of the display memory color code with bits 0 and 1 of the blank control register.

Table 9. Display types

Display memory color code		Blank control register		OUT signal background coloring signal	Example of output signal	Example of character
BL2	BL1	BLn1	BLn0			
×	0	×	0	No OUT signal No background coloring signal	R, G, B, and I for character OUT R, G, B, and I for background	
0	1	×	0	OUT signal same as R, G, B, and I No background coloring signal	R, G, B, and I for character OUT R, G, B, and I for background	
×	×	0	1	Border including character Border coloring signal	R, G, B, and I for character OUT R, G, B, and I for background	
×	×	1	1	Border-only output Border coloring signal	R, G, B, and I for character OUT R, G, B, and I for background	
1	1	1	0	Blank output Background coloring (Note 1)	R, G, B, and I for character OUT R, G, B, and I for background	
1	1	0	0	Blank output Background coloring with border (Note 1, 2)	R, G, B, and I for character OUT R, G, B, and I for background	

Note 1 : If there are no character R, G, B, and I outputs, the background R, G, B, and I signals become the same as the OUT output
2 : When the characters (① and③ in Figure 44) have the dots which are displayed adjoining a character (② in Figure 44) whose display type is the background coloring with border, the border of the adjoined characters (① and ③ in Figure 44), bear no relation to the display type; are displayed in the background area (② in Figure 44)

n : 1 to 3
× : 0 or 1

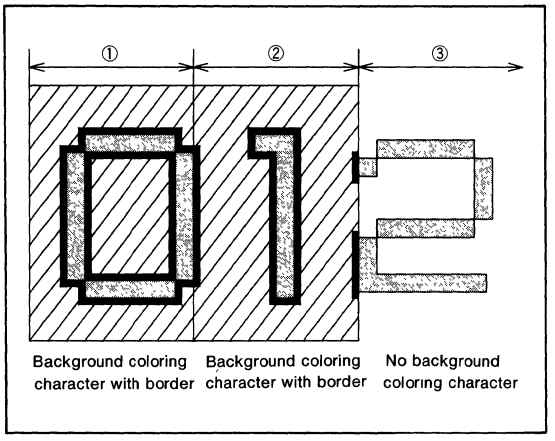


Fig. 44 Notice of character background color function

(10) Mixing Function

Color signals (MXR, MXG, MXB, MXI, and MXOUT) input from outside and color signals (R, G, B, I, and OUT) generated internally can be ORed and output as a mixed signal.

The mixing control register (address $00E5_{16}$) can be used to turn on and off the mixing of the external and internal color signals, and also to specify which of the two signals has priority when they are combined.

The I pin can be switched to output an overlapped signal indicating the parts of the external color signals (MXR, MXG, MXB, MXI, and MXOUT) and internal color signals (R, G, B, I, and OUT) that are overlapped.

The MXB and MXI pins can also be used as external input pins for timer 2 and timer 3.

Examples of displays generated with an internal color signal for the letter "I" and an external color signal for the letter "O" are shown in Figure 46.

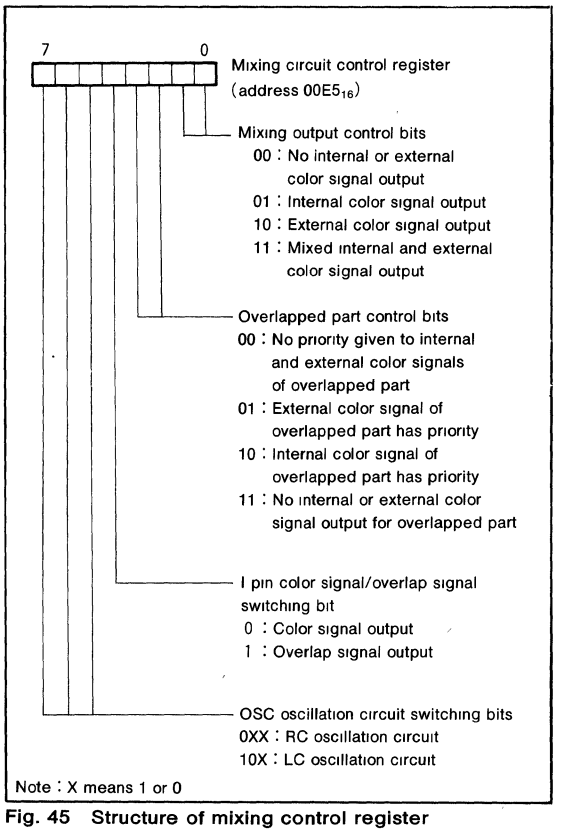


Fig. 45 Structure of mixing control register

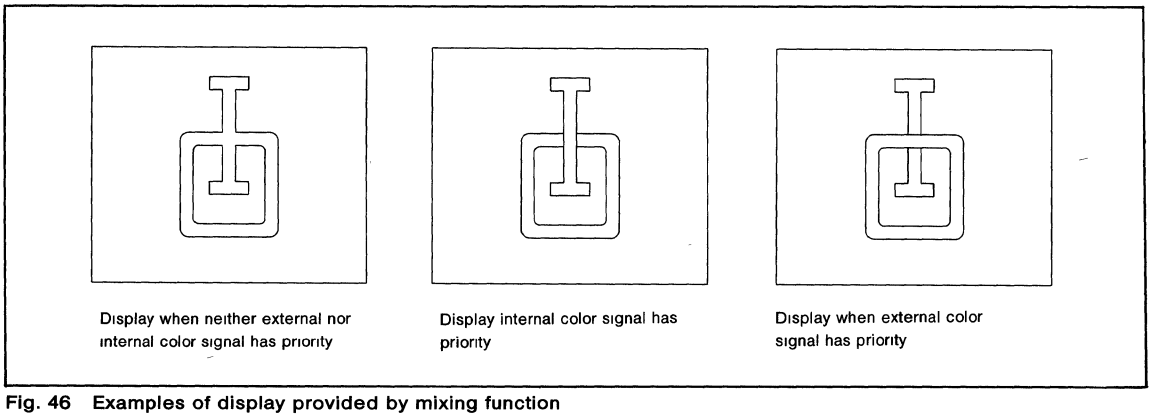


Fig. 46 Examples of display provided by mixing function

(11) CRT Output Pin Control

The CRT output pins R, G, B, I, and OUT and the sync-generator output pin CSYN can also function as ports $P4_0$, $P4_1$, $P4_2$, $P4_3$, $P4_4$, and $P4_5$. Clear the corresponding bit of the port P4 mode register (address $00C9_{16}$) to "0" to specify that pin as CRT output pin, or set it to "1" to specify it as an ordinary port P4 pin.

The input active edges of the H_{SYNC}, V_{SYNC}, MXR, MXG, MXB, MXI, and MXOUT signals can be specified with the bits of the CRT input polarity register (address $00E8_{16}$), and the output active edges of the R, G, B, I, and OUT signals can be specified with the bits of the CRT output polarity register (address $00EC_{16}$). Clear a bit to "0" to specify positive active edge; set it to "1" to specify negative active edge. The structure of the CRT output polarity register is shown in Fig. 48 and that of the CRT input polarity register is shown in Fig. 49.

(12) Raster Coloring Function

An entire screen (raster) can be colored by setting the upper 5 bits of the CRT output polarity register. Since each of the R, G, B, and I pins can be switched to raster coloring output, 16 raster colors can be obtained.

If the OUT pin has been set to raster coloring output, a raster coloring signal is always output during the horizontal scanning period. This setting is necessary for erasing a background TV image.

If the R, G, B, and I pins have been set to raster coloring output, a raster coloring signal is output during the horizontal scanning period whenever there is no other color character output. This ensures that character colors do not mix with the raster color.

An example in which a magenta letter "I" and a red letter "O" are displayed with blue raster coloring is shown in Fig. 47.

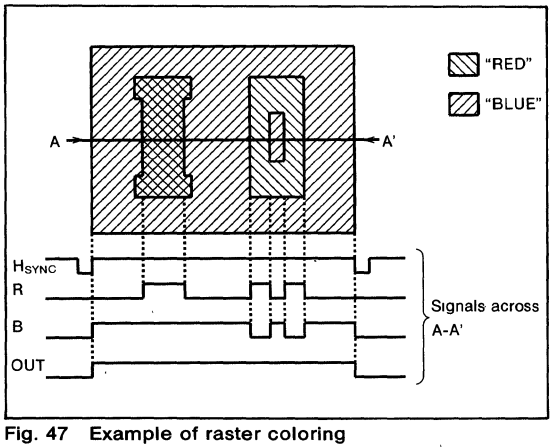


Fig. 47 Example of raster coloring

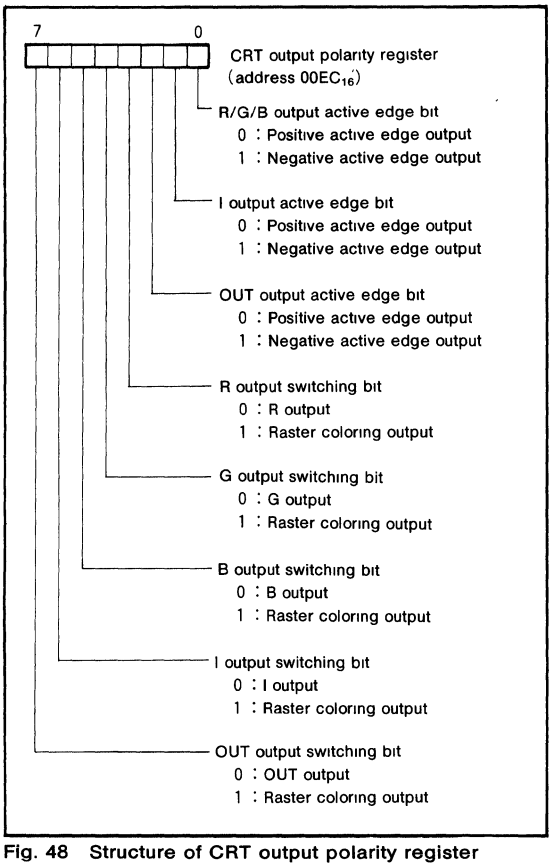


Fig. 48 Structure of CRT output polarity register

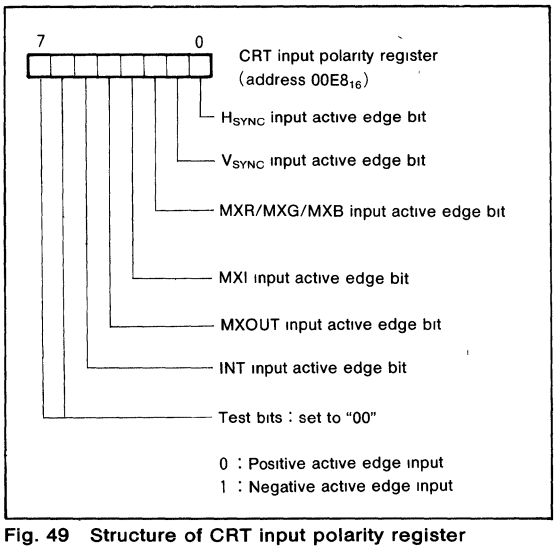


Fig. 49 Structure of CRT input polarity register

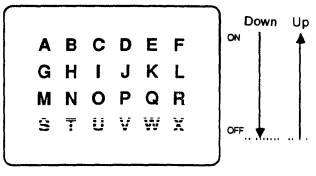
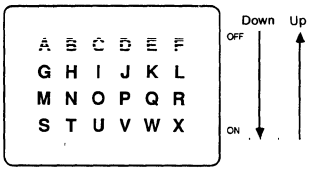
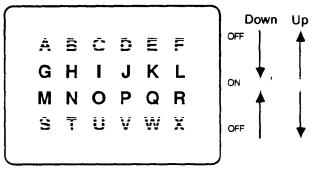
(13) Wipe Function

① Wipe mode

The M37260M6-XXXSP allows the display area to be gradually expanded or shrunk in the vertically direction in units of 1H (H: H_{SYNC} signal). There are three modes for this wipe method. Each mode has Down and UP modes, providing a total of six modes.

Table 10 shows the contents of each wipe mode.

Table 10. Wipe operation in each mode and the values of wipe mode register

Mode		Wipe operation		Wipe mode register		
				Bit 2	Bit 1	Bit 0
1	DOWN	Appear from upper side		0	0	1
	UP	Erase from lower side		1	0	1
2	DOWN	Erase from upper side		0	1	0
	UP	Appear from lower side		1	1	0
3	DOWN	Erase from both upper and lower side		0	1	1
	UP	Appear to both upper and lower side		1	1	1

② Wipe speed

The wipe speed is determined by the vertical synchronization (V_{SYNC}) signal. For the NTSC interlace method, assuming that

V=16.7ms 262.5 H_{SYNC} signals per screen

Table 11. Wipe speed (NTSC method with interlacing, H=262.5)

Wipe resolution	Wipe speed (in all picture)
1 H unit	16.7 (ms) ×262.5÷ 1 ≒ 4 (s)
2 H unit	16.7 (ms) ×262.5÷ 2 ≒ 2 (s)
4 H unit	16.7 (ms) ×262.5÷ 4 ≒ 1 (s)

The wipe speed is shown in Table 11.

Wipe resolution varies with each wipe mode. In mode 1 and 2, one of three resolutions (1H, 2H, 4H) can be selected. In mode 3, wipe is done in units of 4H alone.

Table 12. Wipe mode and wipe resolution

Mode	Wipe resolution	Wipe speed
Mode 1 Mode 2	1 H Unit	about 4 second
	2 H Unit	about 2 second
	4 H Unit	about 1 second
Mode 3	4 H Unit	about 1 second

Table 13. Relationship between wipe speed and wipe resolution

Wipe resolution	Wipe speed (full screen)		
	NTSC method	PAL method	Bi-scan method (525H/flame)
1H (2H) unit	about 4 second	about 6 second	about 4 second
2H (4H) unit	about 2 second	about 3 second	about 2 second
4H (8H) unit	about 1 second	about 1.5 second	about 1 second

Note : Values in parentheses refer to resolutions for bi-scan method.
To perform a wipe with the bi-scan method, set bit 6 of the CRT control register to "1"

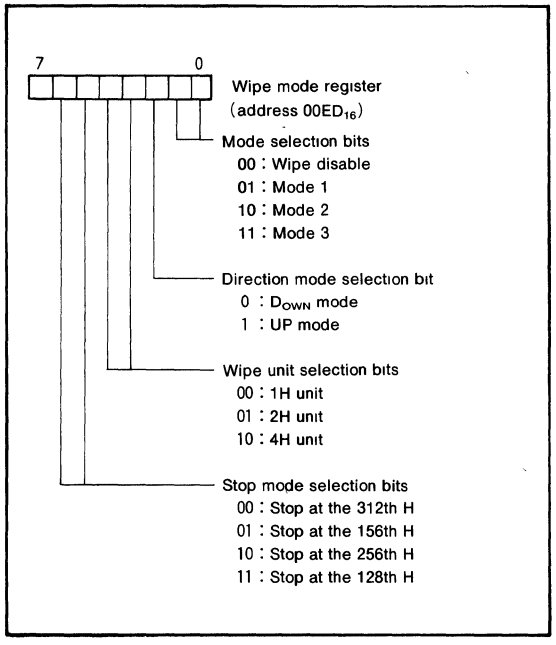


Fig. 50 Structure of wipe mode register

SYNC GENERATOR

The sync generator can output a total of six synchronization signals : NTSC method with interlacing, without interlacing, or bi-scan, and PAL method with interlacing, without interlacing, or bi-scan. Since the synchronization signal is output from the CSYN/$P4_5$ pin, set bit 5 of the port P4 mode register to "0".

Activate the sync generator by clearing bit 7 of the sync generator control register to "0" and setting bit 4 to match the X_{IN} clock frequency.

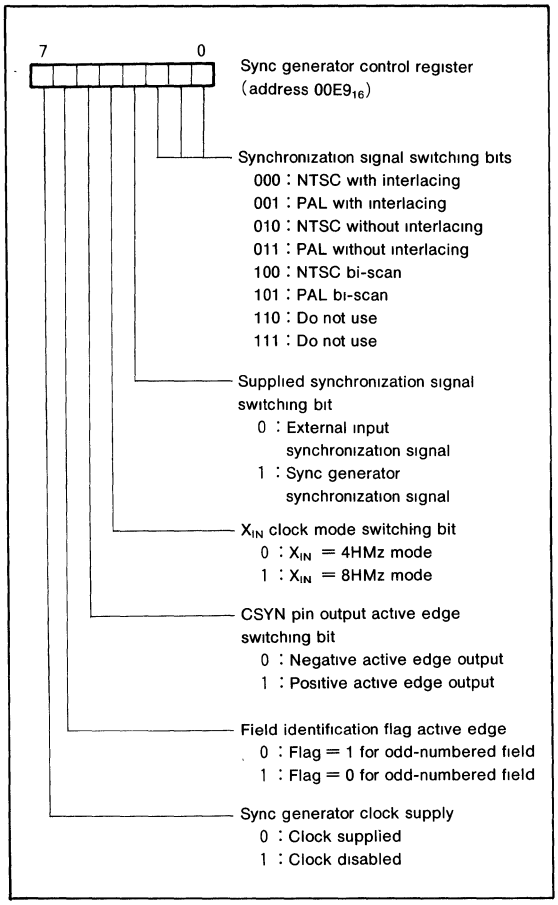


Fig. 51 Structure of sync generator control register

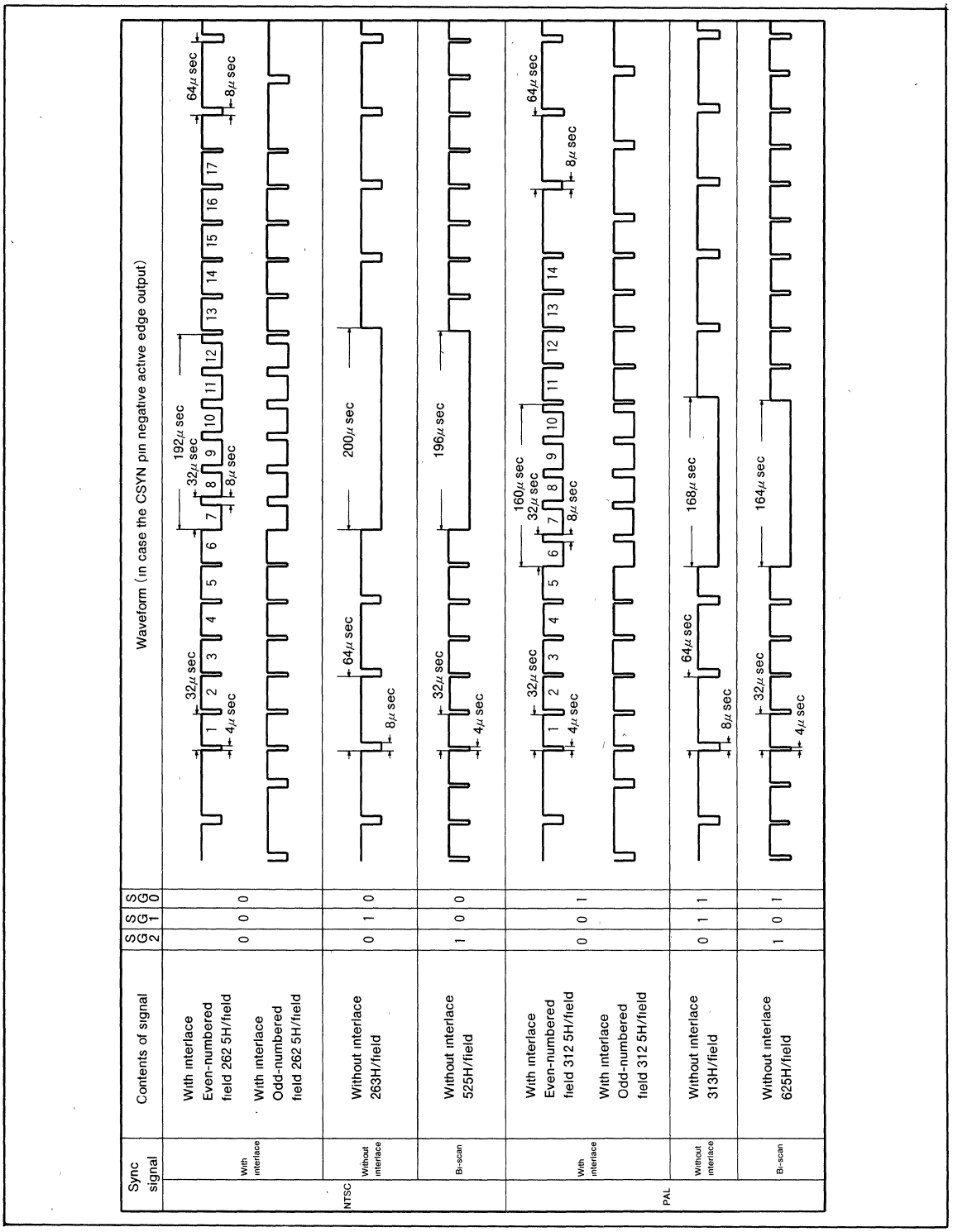
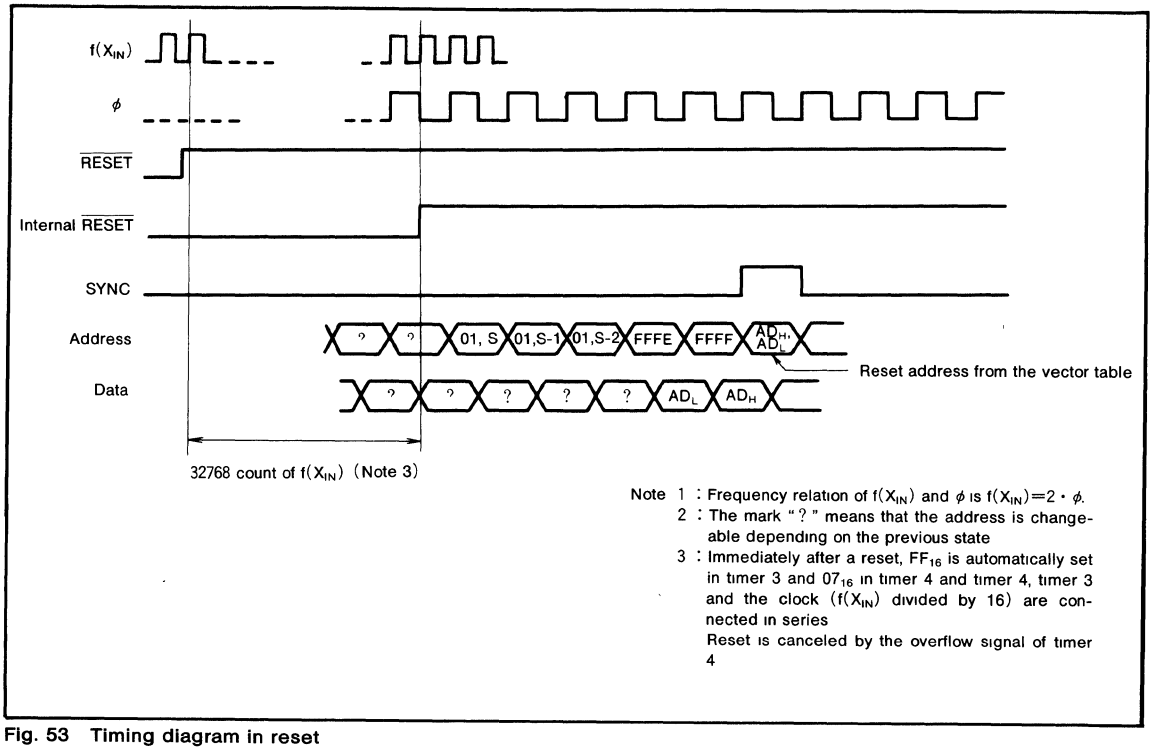


Fig. 52 Relation between the synchronization signals of sync generator and output waveform

RESET CIRCUIT

The M37260M6-XXXSP is reset according to the sequence shown in Figure 53. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for no less than 2μs while the power voltage is 5V$\pm$10% and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 54.

An example of the reset circuit is shown in Figure 55. The reset input voltage must be kept below 0.6V until the supply voltage surpasses 4.5V.



Note 1 : Frequency relation of $f(X_{IN})$ and ϕ is $f(X_{IN})=2 \cdot \phi$.
2 : The mark "?" means that the address is changeable depending on the previous state
3 : Immediately after a reset, FF_{16} is automatically set in timer 3 and 07_{16} in timer 4 and timer 4, timer 3 and the clock ($f(X_{IN})$ divided by 16) are connected in series
Reset is canceled by the overflow signal of timer 4

Fig. 53 Timing diagram in reset

		Address	Contents of register
(1)	Port P0 direction register	$00C1_{16}$	00_{16}
(2)	Port P1 direction register	$00C3_{16}$	00_{16}
(3)	Port P2 direction register	$00C5_{16}$	00_{16}
(4)	Port P3 direction register	$00C7_{16}$	X X 0 0 0 0 0 0
(5)	Port P4 mode register	$00C9_{16}$	00_{16}
(6)	Serial I/O mode register 1	$00CD_{16}$	00_{16}
(7)	Serial I/O mode register 2	$00CE_{16}$	X X X 0 0 0 0 0
(8)	Character size register 1	$00D7_{16}$	X
(9)	Character size register 2	$00D8_{16}$	X
(10)	Character size register 3	$00D9_{16}$	X
(11)	Blank control register 1	$00DA_{16}$	X X
(12)	Blank control register 2	$00DB_{16}$	X X
(13)	Blank control register 3	$00DC_{16}$	X X
(14)	Block 1 interrupt occurrence position control register	$00DD_{16}$	X X X
(15)	Block 2 interrupt occurrence position control register	$00DE_{16}$	X X X
(16)	Block 3 interrupt occurrence position control register	$00DF_{16}$	X X X
(17)	Horizontal position register	$00E0_{16}$	00_{16}
(18)	Vertical position register 4	$00E4_{16}$	X X
(19)	Mixing circuit control register	$00E5_{16}$	00_{16}
(20)	CRT input polarity register	$00E8_{16}$	00_{16}
(21)	Sync generator control register	$00E9_{16}$	00_{16}
(22)	CRT control register	$00EA_{16}$	00_{16}
(23)	Display block counter	$00EB_{16}$	X 0 0 0 0 0 0 0
(24)	CRT output polarity register	$00EC_{16}$	00_{16}
(25)	Wipe mode register	$00ED_{16}$	X 0 0 0 0 0 0 0
(26)	Timer 1	$00F0_{16}$	FF_{16}
(27)	Timer 2	$00F1_{16}$	07_{16}
(28)	Timer 3	$00F2_{16}$	FF_{16}
(29)	Timer 4	$00F3_{16}$	07_{16}
(30)	Timer 12 mode register	$00F4_{16}$	X X X 0 0 0 0 0
(31)	Timer 34 mode register	$00F5_{16}$	X X X 0 0 0 0 0
(32)	Special mode register 1	$00F7_{16}$	0 0 0 X X X 0 0
(33)	Special mode register 2	$00F8_{16}$	X 0 0 0 0 0 0 0
(34)	CPU mode register	$00FB_{16}$	1 1 1 0 1 1 0 0
(35)	Interrupt request register 1	$00FC_{16}$	X X 0 0 0 0 0 0
(36)	Interrupt request register 2	$00FD_{16}$	X X X X X 0 0 0
(37)	Interrupt control register 1	$00FE_{16}$	X X 0 0 0 0 0 0
(38)	Interrupt control register 2	$00FF_{16}$	X X X X X 0 0 0
(39)	Processor status register		1
(40)	Program counter	PC_H	Contents of address $FFFF_{16}$
		PC_L	Contents of address $FFFE_{16}$

Note : Since the contents of both registers other than those listed above and the RAM are undefined at reset, it is necessary to set initial values
At reset, "0" is read from the bits marked X

Fig. 54 Internal state of microcomputer at reset

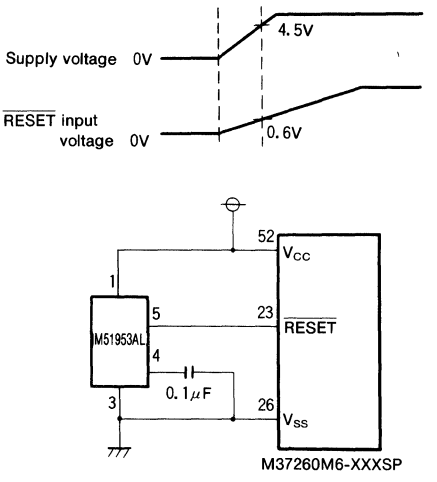


Fig. 55 Example of reset circuit

MITSUBISHI ELECTRIC

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS output.

As shown in the memory map (Figure 3), port P0 can be accessed at zero page memory address $00C0_{16}$.

Port P0 has a direction register (address $00C1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor mode bits (bit 0 and bit 1 at address $00FB_{16}$), three different modes can be selected; single-chip mode, memory expansion mode and microprocessor mode.

In these modes it functions as address (A_7 to A_0) output port (excluding single-chip mode) For more details, refer the processor mode information.

(2) Port P1

In single-chip mode, port P1 has the same function as port P0. In other modes, it functions as address (A_{15} to A_8) output port.

For more details, refer the processor mode information.

(3) Port P2

In single-chip mode, port P2 has the same function as port P0. In other modes, it functions as data (D_7 to D_0) input/output port. For more details, refer the processor modes information.

(4) Port P3

Port P3 is a 6-bit I/O port with function similar to port P0, but the output structure of $P3_0$, $P3_1$ is CMOS output, and $P3_2$-$P3_5$ is N-channel open drain.

$P3_2$ is in common with the external input pin INT and the serial I/O input pin $\overline{CS}$.

When a serial I/O function is selected, $P3_3$ to $P3_5$ work as $\overline{S_{RDY}}$, S_{IN}/S_{OUT}, and S_{CLK} pins.

When a special serial I/O function is selected, $P3_4$ and $P3_5$ work as SDA and SCL pins.

In microprocessor mode or memory expansion mode, $P3_0$ and $P3_1$ work R/$\overline{W}$ output pin and SYNC output pin.

(5) OSC1, OSC2 pins

Clock input/output pins for CRT display function.

(6) H_{SYNC}, V_{SYNC} pins

H_{SYNC} is a horizontal synchronizing signal input pin for CRT display.

V_{SYNC} is a vertical synchronizing signal input pin for CRT display.

(7) R, G, B, I, OUT pins

This is a 5-bit output pin for CRT display and in common with $P4_0$-$P4_4$.

(8) CSYN pin

CSYN pin outputs the composite sync signal by the sync generator.

CSYN pin is in common with $P4_5$.

(9) MXR, MXG, MXB, MXI, MXOUT pins

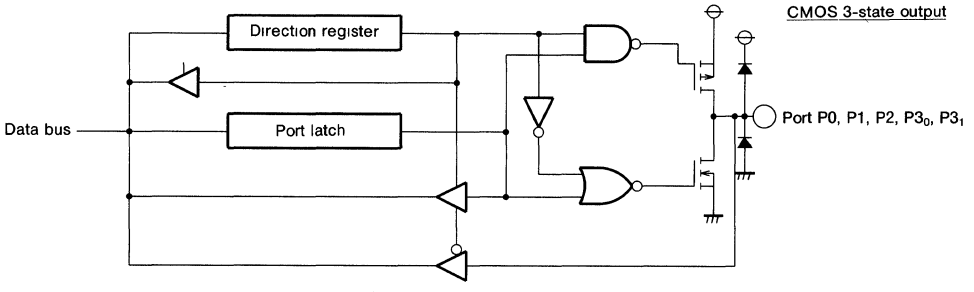
These are video signal input pins for mixing function.

MXR, MXG, MXB, MXI, and MXOUT are in common with the input port $P5_2$, $P5_3$, $P5_4$, $P5_5$, $P5_6$. MXB and MXI are also in common with the external clock input pins TIM2 and TIM3.

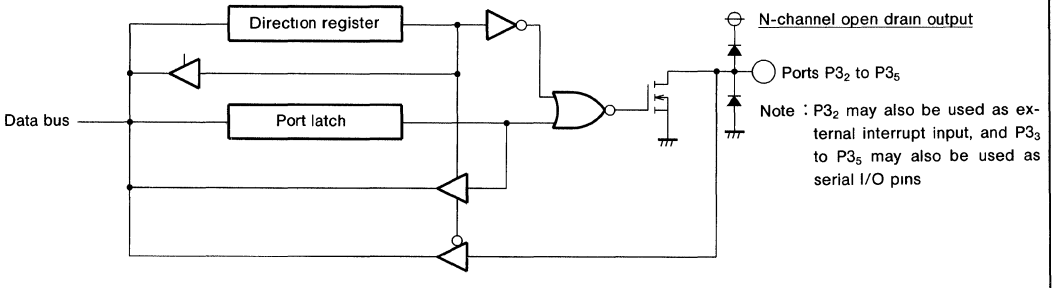
(10) ϕ pin

The internal system clock (1/2 the frequency of the oscillator connected between the X_{IN} and X_{OUT} pins) is output from this pin. If an STP or WIT instruction is executed, output stops after going "H".

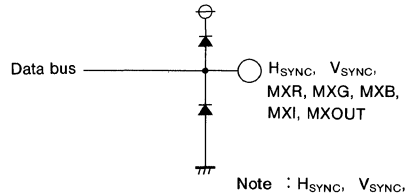
Port P0, P1, P2, $P3_0$, $P3_1$



Ports $P3_2$ to $P3_5$



H_{SYNC}, V_{SYNC}, MXR, MXG, MXB, MXI, MXOUT



ϕ, R, G, B, I, OUT, CSYN

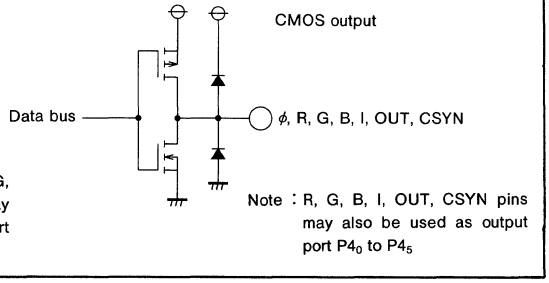


Fig. 56 Ports P0 to P3, H_{SYNC}, V_{SYNC}, MXR, MXG, MXB, MXI, MXOUT, ϕ, R, G, B, I, OUT and CSYN pin block diagram

PROCESSOR MODE

By changing the contents of the processor mode bits (bits 0 and 1 at address $00FB_{16}$), three different operation modes can be selected; single-chip mode, memory expansion mode, and microprocessor mode.

In the memory expansion mode and the microprocessor mode , ports P0 to P3 can be used as address, and data input/output pins.

Figure 60 shows the functions of ports P0 to P3.

The memory map for the single-chip mode is shown in Figure 2 and for other modes, in Figure 57.

By connecting CNV_{SS} to V_{SS}, all three modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microprocessor mode.

The three different modes are explained as follows:

(1) Single-chip mode [00]
The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0-P3 will work as I/O ports.

(2) Memory expansion mode [01]
The microcomputer will be placed in the memory expansion mode after connecting CNV_{SS} to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.
In this mode, port P0 and port P1 are as a system address bus and its I/O pin function is lost.
Port P2 becomes the data bus of D_7 to D_0 (including instruction code) and loses its I/O port function. Port $P3_0$ and $P3_1$ works as R/$\overline{W}$ output pin and SYNC output pin.

(3) Microprocessor mode [10]
The microcomputer will be placed in the microprocessor mode after connecting CNV_{SS} to V_{CC} and initiating a reset or connecting CNV_{SS} to V_{SS} and processor mode bits are set to "10". In this mode, the internal ROM is inhibited so the external memory is required
Other functions are same as the memory expansion mode. The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 14.

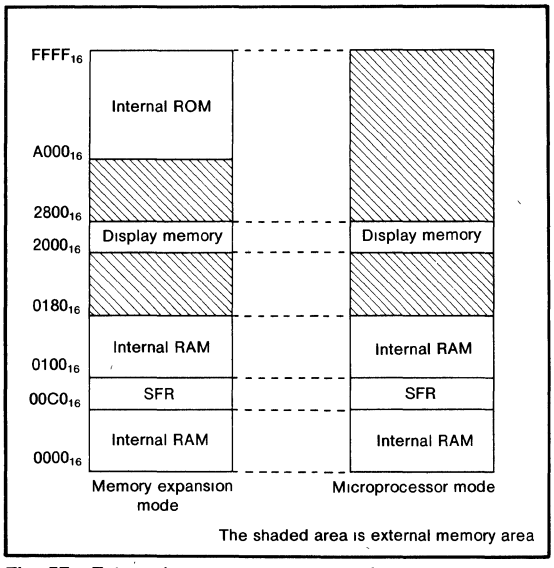


Fig. 57 External memory area at each processor mode

Note 1 : Use the M37260M6-XXXSP in the microprocessor mode or the memory expansion mode only at program development.
The standard is assured only in the single-chip mode.
2 : The display ROM cannot be placed on the external memory area.

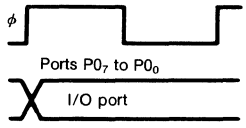
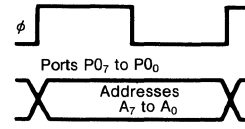
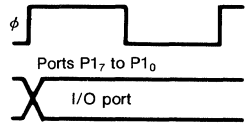
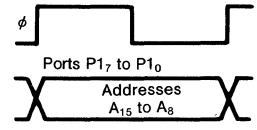
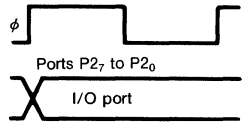
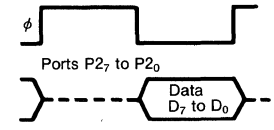
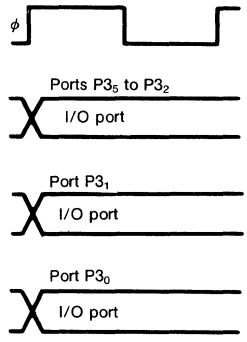
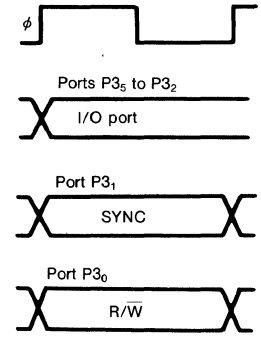
Port \ Mode	Single-chip mode	Memory expansion mode	Microprocessor mode
CM_1	0	0	1
CM_0	0	1	0
Port P0			Same as left
Port P1			Same as left
Port P2			Same as left
Port P3			Same as left

Fig. 58 Processor mode and function of ports P0 to P3 (CM_1, CM_0 : bit 1 and bit 0 of CPU mode register)

Table 14. Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expansion mode • Microprocessor mode	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V_{CC}	• Microprocessor mode	The microprocessor mode is set by the reset

Data-set timing of CPU mode register

The value of bit 0 and bit 1 in the CPU mode register is set at the second rising edge of the SYNC signal after the writing instruction is executed.
However the value of bit 2 and bit 3 is set at the first rising edge of the SYNC signal, just as in the other registers.

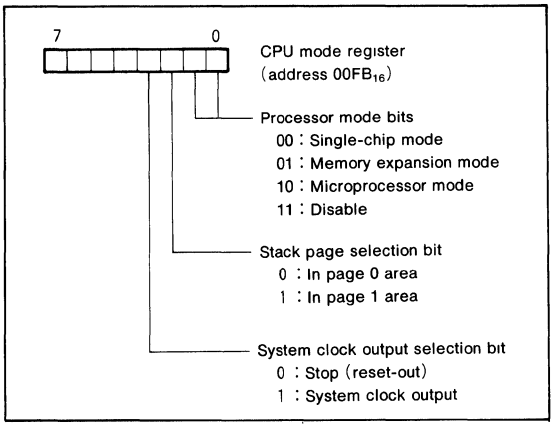


Fig. 59 Structure of CPU mode register

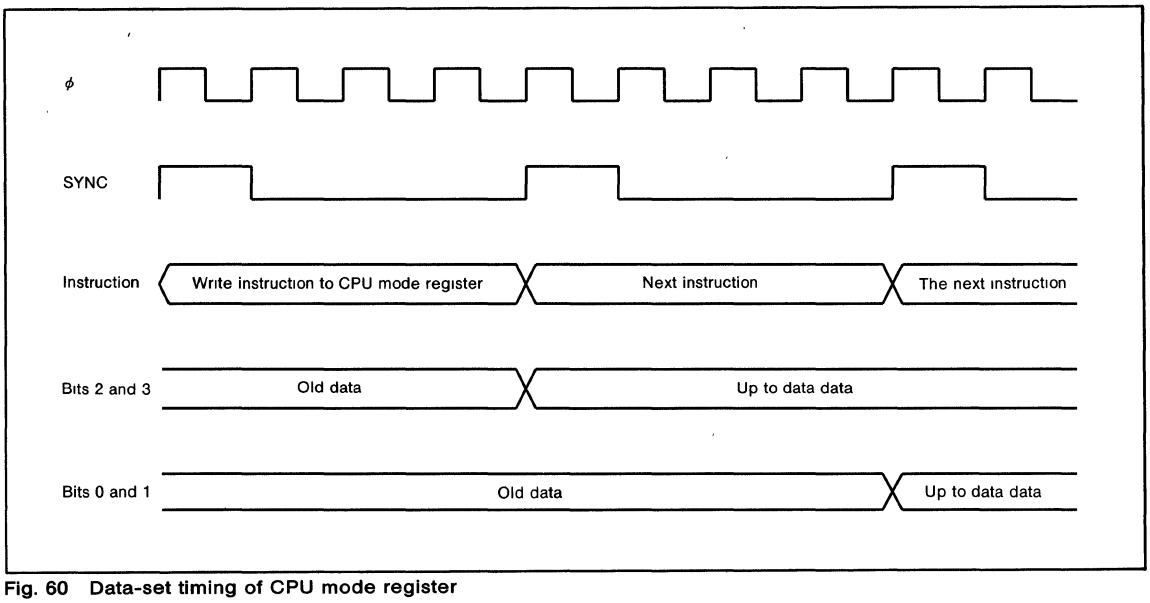


Fig. 60 Data-set timing of CPU mode register

Table 15. The value of CPU mode register at reset

CNV_{SS} pin	b7			CPU mode register				b0
V_{SS}	1	1	1	0	1	1	0	0
V_{CC}	1	1	1	0	1	1	1	0

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 63.

When an STP instruction is executed, the internal clock ϕ stops oscillating at "H" level. At the same time, timer 3 and timer 4 are connected automatically and FF_{16} is set in the timer 3, 01_{16} is set in the timer 4, and timer 3 count source is forced to $f(X_{IN})$ divided by 16. This connection is cleared when an external interrupt is accepted or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the internal clock ϕ keeps its "H" level until timer 4 overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 61.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock usage is shown in Figure 62 X_{IN} is the input, and X_{OUT} is open.

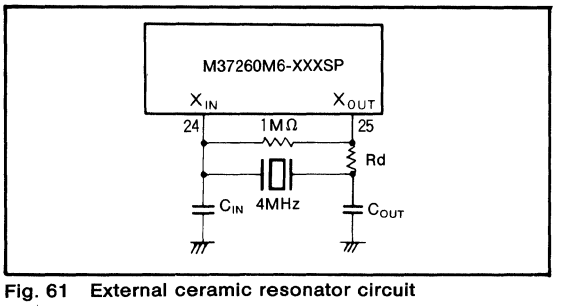


Fig. 61 External ceramic resonator circuit

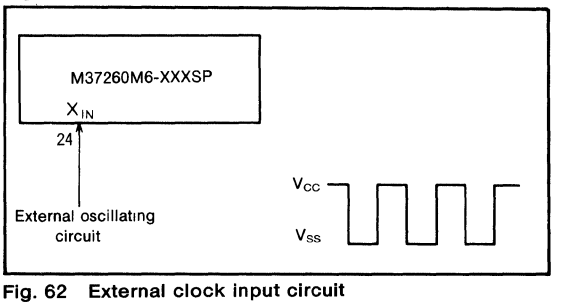


Fig. 62 External clock input circuit

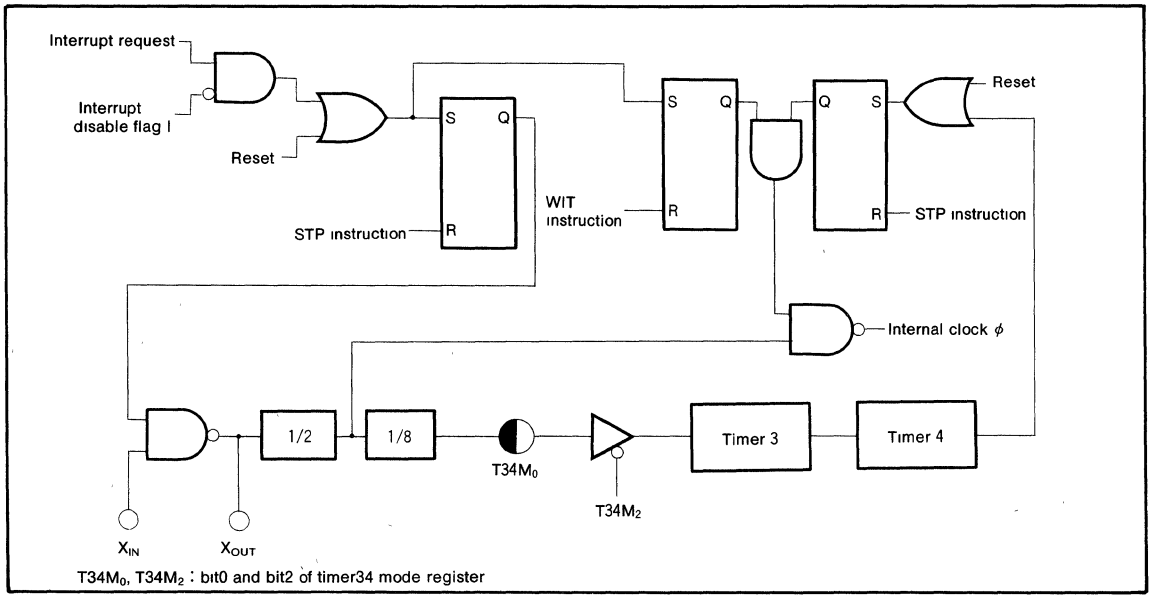


Fig. 63 Block diagram of clock generating circuit

DISPLAY OSCILLATION CIRCUIT

The CRT display clock oscillation circuit has built-in RC and LC oscillation circuits, so that a clock can be obtained simply by connecting an RC or LC circuit between the OSC1 and OSC2 pins.

Select the RC or LC oscillation circuit by setting bits 6 and 7 of the mixing control register (see the structure of the mixing control register in Figure 45).

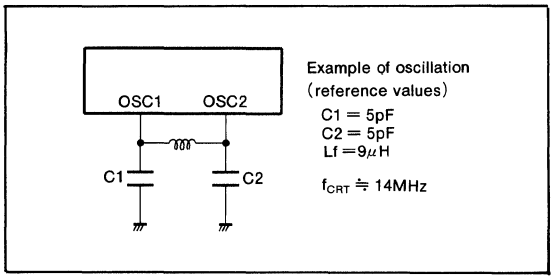
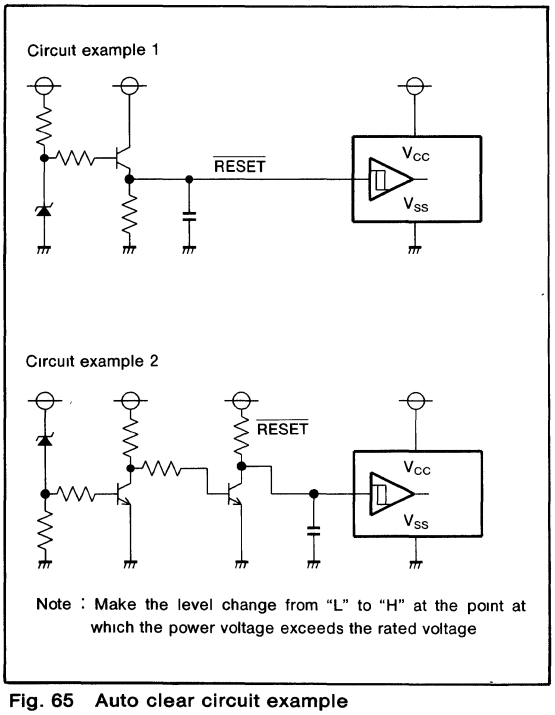


Fig. 64 Display oscillation circuit

AUTO CLAER CIRCUIT

When power is supplied, the auto-clear function can be performed by connecting the following circuit to reset pin.



Note : Make the level change from "L" to "H" at the point at which the power voltage exceeds the rated voltage

Fig. 65 Auto clear circuit example

PROGRAMMING NOTES

(1) The frequency ratio of the timer is 1/(n+1).
(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instruction are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as an NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
(3) After the ADC and SBC instructions are executed (indecimal mode), one instruction cycle (such as an NOP) is needed before the SEC, CLC, or CLD instructions are executed.
(4) An NOP instruction must be used after the execution of a PLP insturction.
(5) In order to avoid noise and latch-up, connect a bypass capacitor ($\approx 0.1\mu F$) directly between the V_{CC} pin and V_{SS} pin using a heavy wire.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

(1) mask ROM order confirmation from
(2) mark specification from
(3) ROM data ····· EPROM 3 sets

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "off" state	−0.3 to 6	V
V_I	Input voltage CNV_{SS}		−0.3 to 6	V
V_I	Input voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_5$, MXR, MXG, MXB, MXI, MXOUT, H_{SYNC}, V_{SYNC}, $\overline{RESET}$		−0.3 to V_{CC}+0.3	V
V_O	Output voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_5$, R, G, B, I, OUT, CSYN, X_{OUT}, OSC2		−0.3 to V_{CC}+0.3	V
I_{OH}	Circuit current R, G, B, I, OUT, CSYN, $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$, $P3_1$		0 to 1(Note 1)	mA
I_{OL1}	Circuit current R, G, B, I, OUT, CSYN, $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_5$		0 to 2(Note 2)	mA
P_d	Power dissipation	T_a=25℃	550	mW
Topr	Operating temperature		−10 to 70	℃
Tstg	Storage temperature		−40 to 125	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−10 to 70℃, V_{CC}=5V±10% unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage(Note 3) During the CPU and CRT operation	4.5	5.0	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{IH}	"H" input voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_3$, H_{SYNC}, V_{SYNC}, MXR, MXG, MXB, MXI, MXOUT, $\overline{RESET}$, X_{IN}, OSC1	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P3_4$, $P3_5$	0.7V_{CC}		V_{CC}	V
V_{IL1}	"L" input voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$, $P3_1$, $P3_3$, MXR, MXG, MXOUT	0		0.4V_{CC}	V
V_{IL2}	"L" input voltage $P3_2$, $P3_4$, $P3_5$, H_{SYNC}, V_{SYNC}, $\overline{RESET}$, X_{IN}, OSC1, MXB, MXI	0		0.2V_{CC}	V
I_{OH}	"H" average output current (Note 1) R, G, B, I, OUT, CSYN, $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$, $P3_1$			1	mA
I_{OL}	"L" average output current (Note 2) R, G, B, I, OUT, CSYN, $P0_0$−$P0_7$, $P1_0$−$P1_7$ $P2_0$−$P2_7$, $P3_0$−$P3_5$			2	mA
f_{CPU}	Oscillating frequency (for CPU operation)(Note 4)	3.6	4.0	8.1	MHz
f_{CRT}	Oscillating frequency (for CRT display)	12.0	14.0	16.0	MHz
fhs	Input frequency INT, TIM2, TIM3, SCL			100	kHz
fhs	Input frequency S_{CLK}			1	MHz

Note 1 : The total current that flows out of the IC should be 20mA (max)
2 : The total current shold be 30mA (max)
3 : Apply 0.022μF or greater capacitance externally between the V_{CC}−V_{SS} power supply pins so as to reduce power source noise
Also apply 0.068μF or greater capacitance externally between the V_{CC}−CNV_{SS} pins
4 : Use a quartz crystal oscillator or a ceramic resonator for the CPU oscillation circuit

ELECTRIC CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, f(X_{IN}) =4MHz, T_a=−10 to 70℃ unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ	Max	
I_{CC}	Supply current	V_{CC}=5.5V, f(X_{IN})=4MHz CRT OFF		10	20	mA
		V_{CC}=5.5V, f(X_{IN})=4MHz CRT ON		20	50	mA
		At stop mode			300	μA
V_{OH}	"H" output voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$, $P3_1$, R, G, B, I, OUT, CSYN	V_{CC}=4.5V I_{OH}=−0.5mA	2.4			V
V_{OL}	"L" output voltage $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_3$, R, G, B, I, OUT, CSYN	V_{CC}=4.5V I_{OL}=0.5mA			0.4	V
	"L" output voltage $P3_4$, $P3_5$	V_{CC}=4.5V I_{OL}=3mA			0.4	V
V_{T+}−V_{T-}	Hysteresis $\overline{RESET}$	V_{CC}=5.0V		0.5	0.7	V
	Hysteresis (Note 1) H_{SYNC}, V_{SYNC}, $P3_2$, $P3_4$, $P3_5$, MXB, MXI	V_{CC}=5.0V		0.5	1.3	V
I_{OZH}	"H" input leak current $\overline{RESET}$, $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_5$, H_{SYNC}, V_{SYNC}, MXR, MXG, MXB, MXI, MXOUT	V_{CC}=5.5V V_O=5.5V			5	μA
I_{OZL}	"L" input leak current $\overline{RESET}$, $P0_0$−$P0_7$, $P1_0$−$P1_7$, $P2_0$−$P2_7$, $P3_0$−$P3_5$, H_{SYNC}, V_{SYNC}, MXR, MXG, MXB, MXI, MXOUT	V_{CC}=5.5V V_O=0V			5	μA

Note 1. $P3_2$, MXB, MXI have the hysteresis when these pins are used as interrupt input pins or timer input pins.
$P3_4$, $P3_5$ have the hysteresis when these pins are used as serial I/O and special serial I/O ports.