M37409PSS

PIGGYBACK for M37409M2-XXXSP

DESCRIPTION

The M37409PSS is an EPROM mounted-type microcomputer which utilizes CMOS technology, and is designed for developing programs for single-chip 8-bit microcomputers the M37409M2-XXXSP. It is housed in a piggyback-type 52-pin shrink DIP.

There is a 28-pin socket on the package for the M5L2764K or the M5L27128K EPROM.

The M37409PSS simplifies the development of programs for the M37409M2-XXXSP, and is excellent for making prototypes.

Therefore the M37409PSS can be used for the development of programs for the M37409M2-XXXSP.

FEATURES

- Differences with the M37409M2-XXXSP are:

(1) ROMless, EPROM is attached externally.

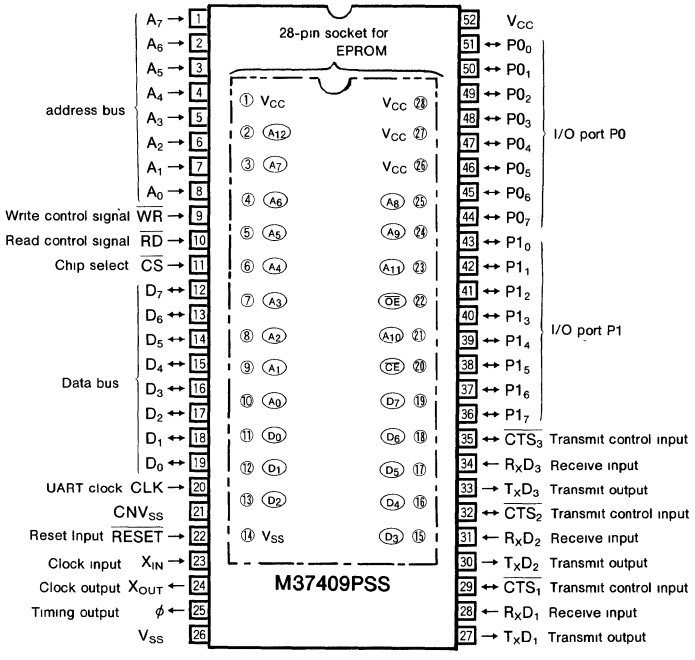
(2) Suitable EPROM is the M5L2764K or the M5L27128K.

APPLICATION

Development of programs for the following systems;

- Office automation equipment

PIN CONFIGURATION (TOP VIEW)



Outline 52S1M

The symbol "○" indicates sockets for EPROM

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±5% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions.) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional register allowing each I/O bit to be individually programmed as input or output. This port is connected to the system bus only, and can not be accessesd from the local bus At reset this port becomes input mode. The output structure is CMOS output
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same function as port P0 This port is connected to the local bus and can be used as only input port from the system bus. The output structure is CMOS output.
T_XD_1~ T_XD_3	UART transfer output	Output	These are UART transfer data output pins
R_XD_1~ R_XD_3	UART receive input	Input	These are UART receive data input pins
$\overline{CTS_1}$~ $\overline{CTS_3}$	UART transfer control input	I/O	These are UART transfer control signal input pins and can be used as I/O port which have basically same function as port P1
CLK	UART clock input	Input	This port is an external clock input pin for baud rate
A_0~A_7	Address input	Input	This port is input for system address
D_0~D_7	Data input/output	I/O	This port is input or output the system data
$\overline{CS}$	Chip select	Input	System data can be read or written by inputting "L" to this port
$\overline{RD}$	Read control input	Input	Memory or register data specified by A_0~A_7 is read from D_0~D_7 by inputting "L" to this port
$\overline{WR}$	Write control input	Input	Data input from D_0~D_7 is written to memory or register specified by A_0~A_7 by inputting "L" to this port
(A_0)~(A_{12})	Output port A	Output	These are for addresses to an EPROM mounted on the package.
(D_0)~(D_7)	Input port D	Input	These are for input data from an EPROM mounted on the package

EXPLANATION OF FUNCTION BLOCK OPERATION

The differences between the M37409PSS and the M37409M2-XXXSP are noted below. The following explanations apply to the M37409PSS. Specification variations for other chips are noted accordingly.

MEMORY

The M37409PSS is mounted an EPROM instead of an external ROM.

The address of an EPROM is $0800_{16} \sim 1FFF_{16}$, and this memory size is 6144 bytes. Other than these, the M37409PSS has the same function as the M37409M2-XXXSP.

PRECATION FOR USE

(1) In case of the M5L2764K EPROM use the following areas (refer to Figure 1).

- For use the M37409M2-XXXSP, usable ROM area is $1000_{16} \sim 1FFF_{16}$.

M5L2764K ..... addresses $1000_{16} \sim 1FFF_{16}$

M5L27128K ..... addresses $3000_{16} \sim 3FFF_{16}$

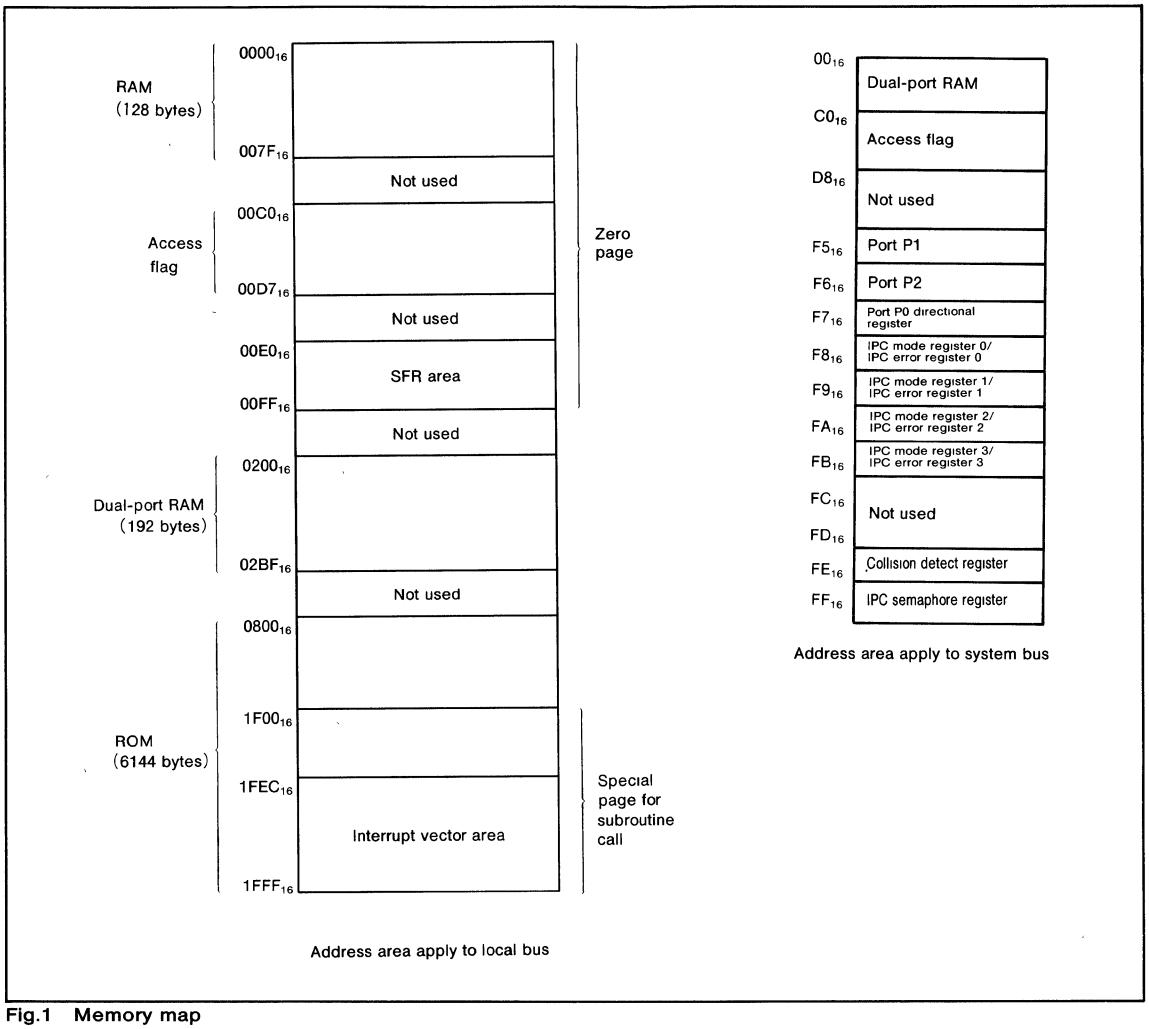


Fig.1 Memory map

$00E0_{16}$	Port P1	$00F0_{16}$	IPC mode register 0
$00E1_{16}$	Port P1 directional register	$00F1_{16}$	IPC mode register 1
$00E2_{16}$	Dual-port RAM direction specify register	$00F2_{16}$	IPC mode register 2
$00E3_{16}$		$00F3_{16}$	IPC mode register 3
$00E4_{16}$	UART1 receive/transfer buffer register	$00F4_{16}$	IPC error register 0
$00E5_{16}$	UART1 status register/UART1 mode register	$00F5_{16}$	IPC error register 1
$00E6_{16}$	UART1 control register	$00F6_{16}$	IPC error register 2
$00E7_{16}$	UART1 divider for baud rate generate	$00F7_{16}$	IPC error register 3
$00E8_{16}$	UART2 receive/transfer buffer register	$00F8_{16}$	
$00E9_{16}$	UART2 status register/UART2 mode register	$00F9_{16}$	IPC semaphore register
$00EA_{16}$	UART2 control register	$00FA_{16}$	Collision detect register
$00EB_{16}$	UART2 divider for baud rate generate	$00FB_{16}$	Interrupt enable register
$00EC_{16}$	UART3 receive/transfer buffer register	$00FC_{16}$	Interrupt request register
$00ED_{16}$	UART3 status register/UART3 mode register	$00FD_{16}$	Prescaler X
$00EE_{16}$	UART3 control register	$00FE_{16}$	Timer X
$00EF_{16}$	UART3 divider for baud rate generate	$00FF_{16}$	Timer control register

Fig. 2 SFR (Special Function Register) memory map

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors cut-off	−0.3∼7	V
V_I	Input voltage X_{IN}, $\overline{RESET}$, D_0∼D_7		−0.3∼7	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, D_0∼D_7, A_0∼A_7, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, CLK, R_XD_1∼R_XD_3, $\overline{CTS_1}$∼$\overline{CTS_3}$		−0.3∼V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3∼13	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, X_{OUT}, ϕ, D_0∼D_7, T_XD_1∼T_XD_3, $\overline{CTS_1}$∼$\overline{CTS_3}$, A_0∼A_{13}		−0.3∼V_{CC}+0.3	V
P_d	Power dissipation	T_a=25℃	1000	mW
T_{opr}	Operating temperature		−10∼70	℃
T_{stg}	Storage temperature		−40∼125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±5%, T_a=−10∼70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage X_{IN}, $\overline{RESET}$, CLK, $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, R_XD_1∼R_XD_3, $\overline{CTS_1}$∼$\overline{CTS_3}$	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage A_0∼A_7, D_0∼D_7, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$	2		V_{CC}+0.3	V
V_{IH}	"H" input voltage D_0∼D_7	0.45V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, CLK, R_XD_1∼R_XD_3, $\overline{CTS_1}$∼$\overline{CTS_3}$	−0.3		0.2V_{CC}	V
V_{IL}	"L" input voltage A_0∼A_7, D_0∼D_7, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$	−0.3		0.8	V
V_{IL}	"L" input voltage $\overline{RESET}$	−0.3		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	−0.3		0.16V_{CC}	V
V_{IL}	"L" output voltage D_0∼D_7	0		0.15V_{CC}	V
I_{OH}	"H" output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, ϕ, T_XD_1∼T_XD_3, $\overline{CTS_1}$∼$\overline{CTS_3}$			−10	mA
I_{OH}	"H" output current D_0∼D_7			−1.0	mA
I_{OL}	"L" output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, ϕ, T_XD_1∼T_XD_3, $\overline{CTS_1}$∼$\overline{CTS_3}$			10	mA
I_{OL}	"L" output current D_0∼D_7			−1.6	mA

Note 1 : Average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms
2 : Total of "L" output current I_{OL}, of ports P0, P1, T_XD_1∼T_XD_3 and $\overline{CTS_1}$∼$\overline{CTS_3}$ is −50mA max
Total of "H" output current I_{OH}, of port P0, P1, T_XD_1∼T_XD_3 and $\overline{CTS_1}$∼$\overline{CTS_3}$ is 50mA max

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	"H" output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, ϕ, T_XD_1∼T_XD_3, $\overline{CTS_1}$∼$\overline{CTS_3}$	I_{OH}=−10mA	V_{CC}−2			V
V_{OH}	"H" output voltage D_0∼D_7	I_{OH}=−1mA	2.4			V
V_{OL}	"L" output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, ϕ, T_XD_1∼T_XD_3, $\overline{CTS_1}$∼$\overline{CTS_3}$	I_{OL}=10mA			2	V
V_{OL}	"L" output voltage D_0∼D_7	I_{OL}=1.6mA			0.4	V
I_I	Input leak current A_0∼A_7, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, CLK	V_{SS}≦V_I≦V_{CC}	−5		5	μA
I_I	Input leak current $\overline{RESET}$, X_{IN}	V_{SS}≦V_I≦7V	−5		5	μA
I_{OZ}	Tri-state leak current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, D_0∼D_7, $\overline{CTS_1}$∼$\overline{CTS_3}$	V_{SS}+0.5≦V_O≦V_{CC}−0.5V	−5		5	μA
V_{T+}−V_{T-}	Hysteresis $\overline{RESET}$, CLK, R_XD_1∼R_XD_3, $\overline{CTS_1}$∼$\overline{CTS_3}$			0.6		V