M37412E5-XXXFP

PROM VERSION of M37412M4-XXXFP

DESCRIPTION

The M37412E5-XXXFP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 72-pin plastic QFP. The features of this chip are similar to those of the M37412M4-XXXFP except that this chip has a 10240 bytes PROM built in. This single-chip microcomputer is useful for home electrical appliances and consumer appliance controllers.

In addition to its simple instruction sets, the PROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming. Since general purpose PROM writers can be used for the built-in PROM, this chip is suitable for small quantity production runs.

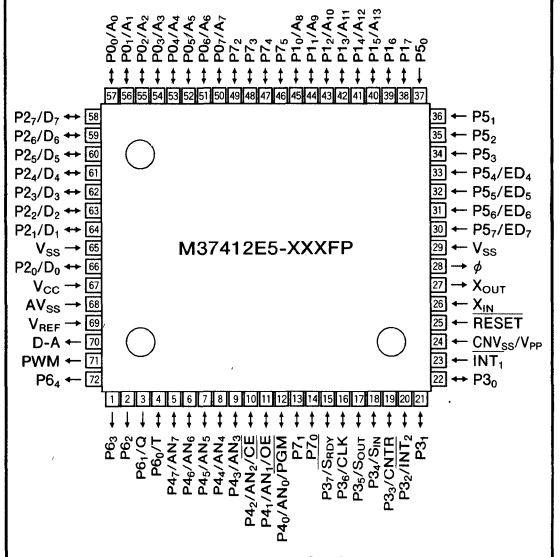
FEATURES

- Number of basic instructions 69
- Memory size PROM ..... 10240 bytes
  RAM ..... 160 bytes
- Instruction execution time
  ..... 2μs (minimum instructions at 4MHz frequency)
- Single power supply ..... 5V±5%
- Power dissipation
  normal operation mode (at 4MHz frequency) 15mW
- Subroutine nesting ..... 80 levels (Max.)
- Interrupt ..... 7 types, 5 vectors
- 8-bit timer 4
- Programmable I/O ports (Ports P0, P1, P2, P3, P4, P7) 46
- Input port (Port P5) 8
- Output port (Port P6) 5
- Serial I/O (8-bit) 1
- A-D converter ..... 8-bit successive approximation
- D-A converter
- 8-bit PWM function
- Watchdog timer
- PROM (equivalent to the M5L27128)
  program voltage 21V

APPLICATION

Office automation equipment
VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



Outline 72P6

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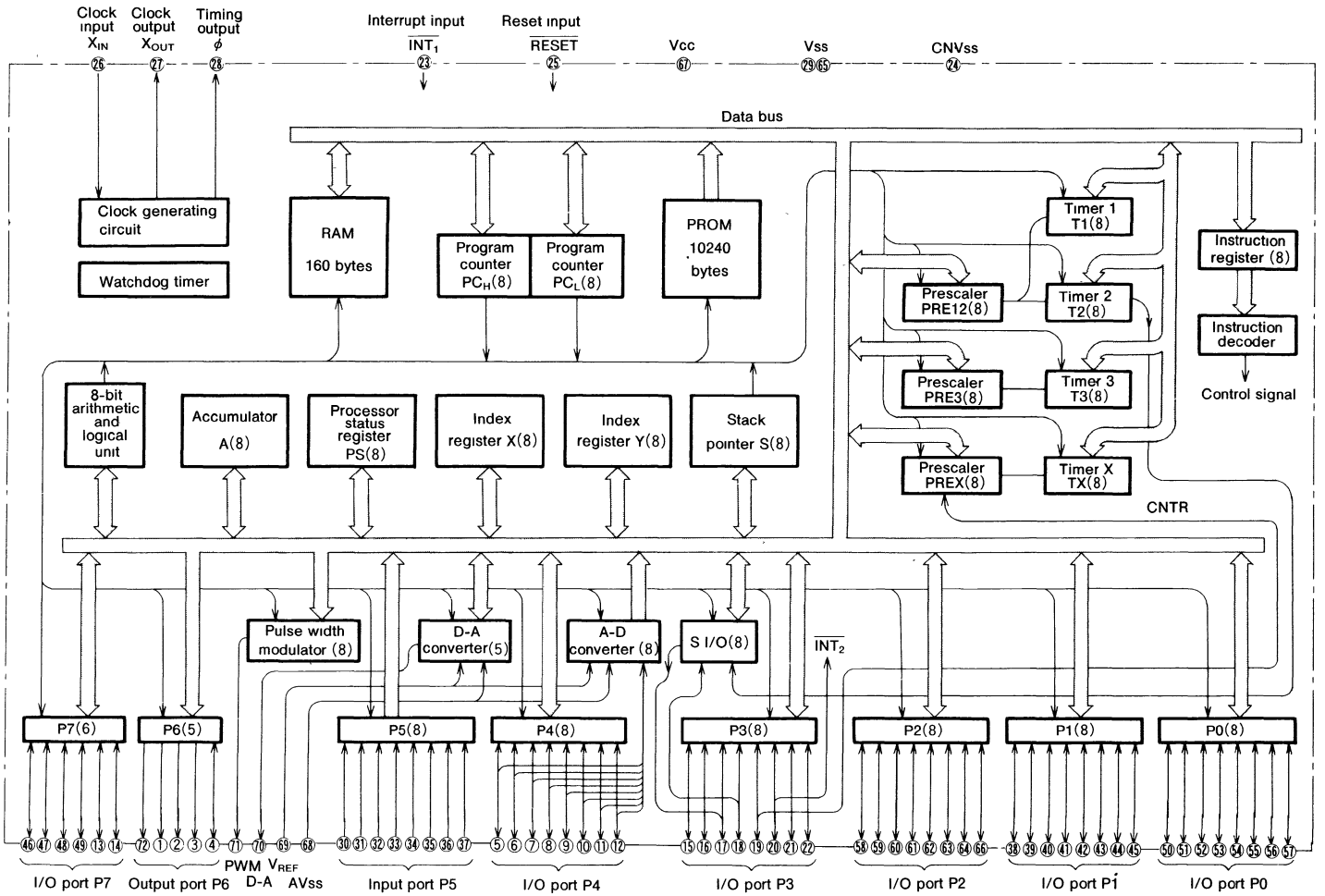
M37412E5-XXXFP BLOCK DIAGRAM



FUNCTIONS OF M37412E5-XXXFP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			2μs (minimum instructions, at 4MHz frequency)
Clock frequency			4MHz
Memory Size	PROM		10240 bytes (Note 1)
	RAM		160 bytes
Input/Output ports	$\overline{INT_1}$	Input	1-bit×1
	P0, P1, P2, P3, P4	I/O	8-bit×5 (a part of P3 is common with serial I/O, timer I/O, and interrupt input)
	P5	Input	8-bit×1
	P6	Output	5-bit×1 (a part of P6 is in common with external trigger output pin)
	P7	I/O	6-bit×1
Serial I/O			8-bit×1
Timers			8-bit prescaler×3+8-bit timer×4
A-D conversion			8-bit×1 (8 channels)
D-A conversion			5-bit×1
Pulse width modulator			8-bit×1
Watchdog timer			15-bit×1
Subroutine nesting			80 levels (max)
Interrupt			Two external interrupts, three internal timer interrupts
Clock generating circuit			built-in (ceramic or quartz crystal oscillator)
Supply voltage			5V±5%
Power dissipation			15mW (at 4MHz frequency)
Input/Output characteristics	Input/Output voltage		12V (Ports P0, P1, P3, P4, P5, P6, P7, $\overline{INT_1}$)
	Output current		5mA (Ports P0, P1, P2, P3, P4, P7)
Memory expansion			Possible
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate process
Package			72-pin plastic molded QFP

Note 1 : The PROM programing voltage is 21V (equivalent to the M5L27128)

PIN DESCRIPTION

Pin	Mode	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Single-chip /EPROM	Power supply		Supply 5V±5% to V_{CC} and 0V to V_{SS}
CNV_{SS}/ V_{PP}	Single-chip	CNV_{SS} input	Input	Connect to 0V
	EPROM	V_{PP} input		Connect to V_{PP} when programming or verifing.
$\overline{RESET}$	Single-chip	RESET input	Input	To reset, keep this input terminal low for more than 2μs (min) under normal V_{CC} conditions If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
	EPROM	RESET input		Connect to V_{SS}
X_{IN}	Single-chip /EPROM	Clock input	Input	Connect a ceramic or a quartz crystal oscillator between X_{IN} and X_{OUT} for clock oscillation. If an external clock input is used, connect the clock input to the X_{IN} pin and open the X_{OUT} pin.
X_{OUT}		Clock output	Output	
ϕ	Single-chip /EPROM	Timing output	Output	For timing output
$\overline{INT_1}$	Single-chip	Interrupt input	Input	Interrupt input INT_1.
	EPROM	Interrupt input	Input	Connect to 0V.
$P0_0$~$P0_7$	Single-chip	I/O port P0	I/O	Port P0 is an 8-bit I/O port with direction registers which can program each bit as input or output It is set to input mode at reset. The output format is N-ch open drain
	EPROM	Address input A_0~A_7	Input	P0 works as the lower 8 bit address input (A_0~A_7).
$P1_0$~$P1_7$	Single-chip	I/O port P1	I/O	Port P1 is an 8-bit I/O port which has the same function as Port P0
	EPROM	Address input A_8~A_{13}	Input	$P1_0$~$P1_4$ works as the higher 5 bit address inputs (A_8~A_{13}) Connect $P1_5$~$P1_7$ to V_{CC}
$P2_0$~$P2_7$	Single-chip	I/O port P2	I/O	Port P2 is an 8-bit I/O port which has the same function as port P0 The output format is CMOS.
	EPROM	Data input/ output D_0~D_7	I/O	Port 2 works as an 8 bit data bus (D_0~D_7)
$P3_0$~$P3_7$	Single-chip	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions port P0 When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively Also $P3_3$ and $P3_2$ work as CNTR pin and the lowest interrupt pin ($\overline{INT_2}$), respectively The output format is N-ch open drain
	EPROM	Input Port P3	Input	Connect to 0V
$P4_0$~$P4_7$	Single-chip	I/O port P4	I/O	Port P4 is an 8-bit I/O port which has the same function as port P0 Ports $P4_7$~$P4_0$ are common with Analog inputs AN_7~AN_0 The output format is N-ch open drain
	EPROM	Select mode	Input	$P4_2$, $P4_1$, $P4_0$ work as $\overline{CE}$, $\overline{OE}$ and $\overline{PGM}$ inputs, respectively Connect $P4_5$~$P4_7$ to 0V and $P4_4$ and $P4_3$ to V_{CC}
$P5_0$~$P5_7$	Single-chip	Input port	Input	Port P5 is an 8-bit input port. Ports $P5_7$~$P5_4$ have edge sence functions
	EPROM	Input port	Input	Connect to 0V

PIN DESCRIPTION (Continued)

Pin	Mode	Name	Input/ Output	Functions
$P6_0$~$P6_4$	Single-chip	Output port	Output	Port P6 is an 5-bit output port. At external trigger output mode, $P6_0$ and $P6_1$ are in common with the trigger input pin (T) and the trigger output pin (Q), respectively The output structure is N-channel open drain
	EPROM	Output port	Output	Connect to 0V
$P7_0$~$P7_5$	Single-chip	I/O port P7	I/O	Port P7 is an 6-bit I/O port which has the same function as Port P0.
	EPROM	Input port P7	Input	Connect to 0V.
AV_{SS}	Single-chip	Analog voltage input	Input	GND pin for the A-D and D-A converters.
	EPROM	Analog voltage input	Input	Connect to 0V.
V_{REF}	Single-chip	Reference voltage input	Input	Reference input for A-D and D-A converters.
	EPROM	Reference voltage input	Input	Connect to 0V
D-A	Single-chip	D-A output	Output	D-A converter output pin
	EPROM	D-A output	Output	Connect to 0V.
PWM	Single-chip	PWM output	Output	Pulse width modulation output pin (N-ch open drain format).
	EPROM	PWM output	Output	Connect to 0V

EPROM MODE

The M37412E5-XXXFP features an EPROM mode in addition to its normal modes. When the $\overline{RESET}$ signal level is low ("L"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1 gives the pin connections in the EPROM mode. When in the EPROM mode, ports P0, P1, P2, $P4_0 \sim P4_2$, and CNV_{SS} are used for the PROM (equivalent to the M5L27128). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5L27128. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 1. Pin function in EPROM mode

	M37412E5-XXXFP	M5L27128
V_{CC}	V_{CC}	V_{CC}
V_{PP}	CNV_{SS}/V_{PP}	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports P0, $P1_0 \sim P1_5$	$A_0 \sim A_{13}$
Data I/O	Port P2	$D_0 \sim D_7$
$\overline{CE}$	$P4_2/\overline{CE}$	$\overline{CE}$
$\overline{OE}$	$P4_1/\overline{OE}$	$\overline{OE}$
$\overline{PGM}$	$P4_0/\overline{PGM}$	$\overline{PGM}$

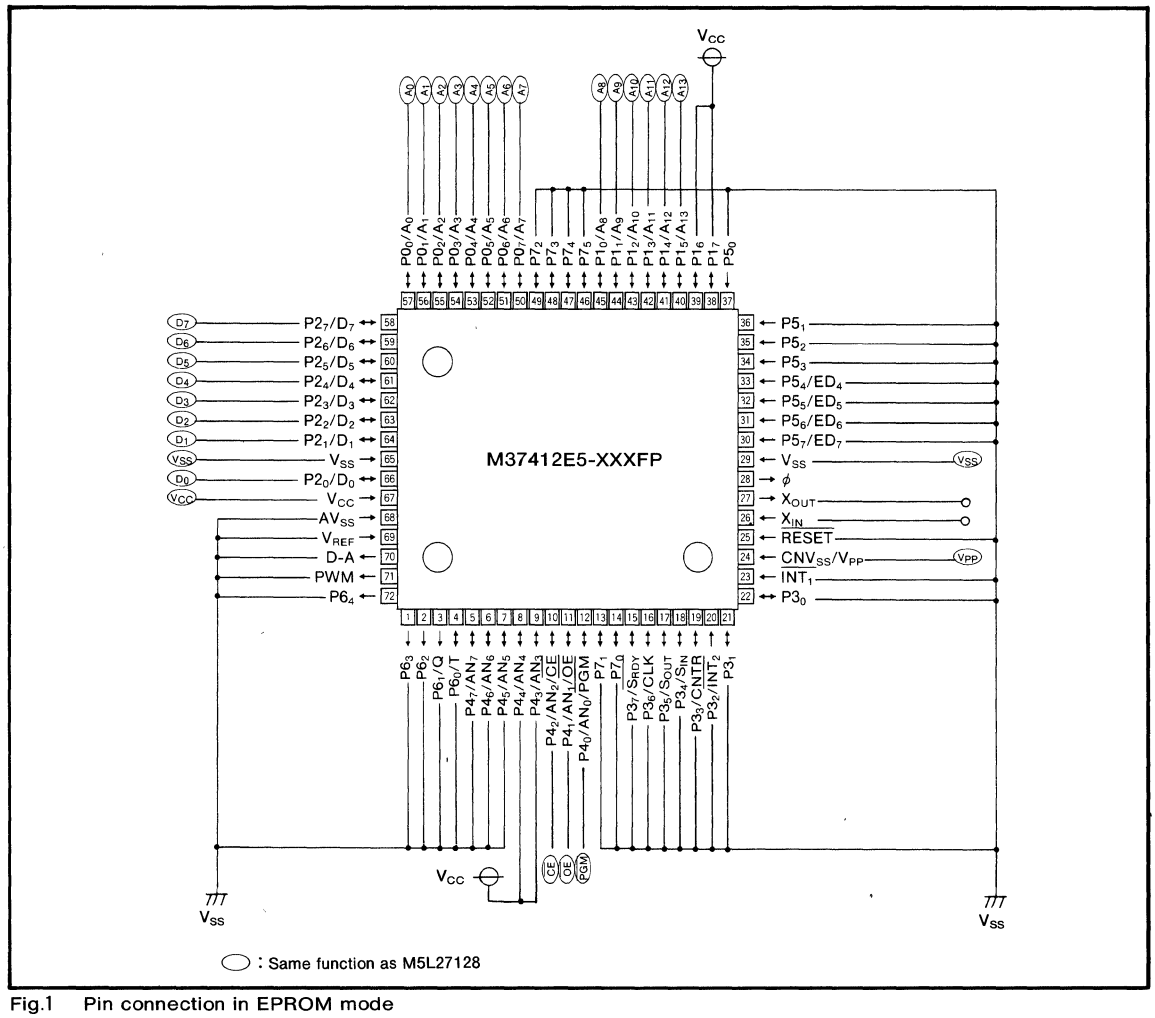


Fig.1 Pin connection in EPROM mode

PROM READING AND WRITING

Reading

To read the PROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level, and the $\overline{PGM}$ pin to a "H" level. Input the address of the data (A_0~A_{13}) to be read and the data will be output to the I/O pins D_0~D_7. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pins are in the "H" state.

Writing

To write to the PROM, set the $\overline{CE}$ pin to a "L" level and the $\overline{OE}$ pin to a "H" level. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins A_0~A_{13}, and the data to be written is input to pins D_0~D_7. Set the $\overline{PGM}$ pin to a "L" level to begin writing.

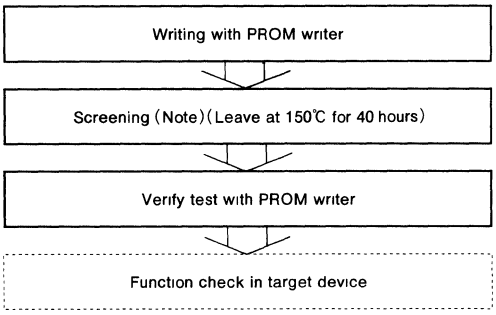
Notes on Writing

When using an PROM writer, the address range should be between 1800_{16} and $3FFF_{16}$. When data is written between addresses 0000_{16} and $3FFF_{16}$, fill addresses 0000_{16} to $17FF_{16}$ with 00_{16}.

NOTES ON HANDLING

(1) Since a high voltage (21V) is used to write data, care should be taken when turning on the EPROM writer's power.

(2) For the programmable microcomputer (shipped in blank or OTP type) . Mitsubishi does not perform PROM write test and screening in the assembly process and following process. To improve reliability after write, performing write and test according to the flow below before use is recommended.



Note : Since the screening temperature is higher than storage temperature, never expose to 150℃ exceeding 100 hours.

Table 2. I/O signal in each mode

Mode \ Pin	$\overline{CE}$(10)	$\overline{OE}$(11)	$\overline{PGM}$(12)	V_{PP}(24)	V_{CC}(67)	Data I/O (58~64, 66)
Read-out	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Output
Programming	V_{IL}	V_{IH}	Pulse(V_{IH}→V_{IL})	V_{PP}	V_{CC}	Input
Programming verify	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Output
Program disable	V_{IH}	X	X	V_{PP}	V_{CC}	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively.
2 : An X indicates either V_{IL} or V_{IH}

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} With the output transistor cut-off	−0.3~7	V
V_I	Input voltage X_{IN}		−0.3~7	V
V_I	Input voltage $P2_0$~$P2_7$, $P4_0$~$P4_7$		−0.3~V_{CC}+0.3	V
V_I	Input voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$, $P7_0$~$P7_5$, $\overline{INT_1}$		−0.3~13	V
V_I	Input voltage CNV_{SS}, $\overline{RESET}$		−0.3~13 (Note 1)	V
V_O	Output voltage $P2_0$~$P2_7$, $P4_0$~$P4_7$, X_{OUT}, ϕ, D-A		−0.3~V_{CC}+0.3	V
V_O	Output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P3_0$~$P3_7$, $P6_0$~$P6_4$, $P7_0$~$P7_5$, PWM		−0.3~13	V
P_d	Power dissipation	T_a=25℃	300	mW
T_{opr}	Operating temperature		−10~70	℃
Tstg	Storage temperature		−40~125	℃

Note 1 : In EPROM programming mode, CNV_{SS} is 22.0V

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±5%, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{SS}	Supply voltage		0		V
V_{REF}	Reference voltage	4		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, CNV_{SS}, $P6_0$, $P7_0$~$P7_5$	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $\overline{INT_1}$, CNV_{SS}, $P6_0$, $P7_0$~$P7_5$	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P7_0$~$P7_5$ (Note 2)			10	mA
$I_{OL(peak)}$	"L" peak output current $P6_0$~$P6_3$ (Note 2)			15	mA
$I_{OL(peak)}$	"L" peak output current PWM, $P6_4$ (Note 2)			5	mA
$I_{OL(avg)}$	"L" average output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P7_0$~$P7_5$ (Note 1)			5	mA
$I_{OL(avg)}$	"L" average output current $P6_0$~$P6_3$ (Note 1)			7	mA
$I_{OL(avg)}$	"L" average output current PWM, $P6_4$ (Note 1)			2.5	mA
$I_{OH(peak)}$	"H" peak output current $P2_0$~$P2_7$ (Note 2)			−10	mA
$I_{OH(avg)}$	"H" average output current $P2_0$~$P2_7$ (Note 1)			−5	mA
$f(X_{IN})$	Internal clock oscillating frequency			4	MHz

Note 1 : The average output currents $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms
2 : Do not allow the combined low-level output current of ports P0, P1, P2, P3, P4, P6, and PWM to exceed 80mA
Do not allow the combined high-level output current of port P2 to exceed 50mA
3 : "H" input voltage of ports P0, P1, P3, P5, $P6_0$, P7 and $\overline{INT_1}$ is available up to +12V

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max	
V_{OH}	"H" output voltage $P2_0$~$P2_7$	I_{OH}=−10mA	3			V
V_{OH}	"H" output voltage ϕ	I_{OH}=−2.5mA	3			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_3$, $P7_0$~$P7_5$	I_{OL}=10mA			2	V
V_{OL}	"L" output voltage $P6_4$, ϕ, PWM	I_{OL}=5mA			2	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{INT_1}$		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $P3_6$	When used as CLK input	0.3	0.8		V
$V_{T+}-V_{T-}$	Hysteresis $P3_2$	When used as $\overline{INT_2}$ input	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $P3_3$	When used as CNTR input	0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis $P6_0$	When used as T input	0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$			0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_3$, $P7_0$~$P7_5$	V_I=0V			−5	μA
I_{IL}	"L" input current $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_I=0V			−5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$, $P7_0$~$P7_5$	V_I=12V			12	μA
I_{IH}	"H" input current $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, $P2_0$~$P2_7$, $P4_0$~$P4_7$	V_I=5V			5	μA
V_{RAM}	RAM retention voltage	At clock stop	2			V
I_{CC}	Supply current	ϕ, X_{OUT}, and D-A pins opened, other pins at V_{SS}, and A-D converter in the finished condition — f(X_{IN})=4MHz Square wave		3	6	mA
		At clock stop T_a=25℃			1	μA
		At clock stop T_a=75℃			10	

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=AV_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	V_{REF}=V_{CC}			8	Bits
—	Absolute accuracy	V_{REF}=V_{CC}			±3	LSB
R_{LADDER}	Ladder resistance value	V_{REF}=V_{CC}	2		10	kΩ
t_{CONV}	Conversion time				50	μs
V_{REF}	Reference input voltage		2		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

D-A CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=AV_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	V_{REF}=V_{CC}			5	Bits
—	Error in full scale range	V_{REF}=V_{CC}			±1	%
t_{SU}	Setup time	V_{REF}=V_{CC}			3	μs
R_O	Output resistance	V_{REF}=V_{CC}			3	kΩ
V_{REF}	Reference voltage		4		V_{CC}	V

TIMING REQUIREMENTS

Single-chip mode (V_{CC}=5V±5%, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max	
$t_{su(P0D-\phi)}$	Port P0 input setup time		270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time		270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time		270			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time		270			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time		270			ns
$t_{su(P7D-\phi)}$	Port P7 input setup time		270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		20			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		20			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time		20			ns
$t_{h(\phi-P7D)}$	Port P7 input hold time		20			ns
t_C	External clock input cycle time		250			ns
t_W	External clock input pulse width		75			ns
t_r	External clock rising edge time				25	ns
t_f	External clock falling edge time				25	ns

Eva-chip mode (V_{CC}=5V±5%, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max	
$t_{su(P0D-\phi)}$	Port P0 input setup time		270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time		270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns

Memory expanding mode and microprocessor mode

(V_{CC}=5V±5%, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		30			ns

SWITCHING CHARACTERISTICS

Single-chip mode (V_{CC}=5V±5%, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig 2			230	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				230	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig 3			230	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time	Fig 2			230	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time				230	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				230	ns
$t_{d(\phi-P7Q)}$	Port P7 data output delay time				230	ns

Eva-chip mode (V_{CC}=5V±5%, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig 2			250	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				250	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig 3			300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time	Fig 2			250	ns
$t_{d(\phi-R/WF)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-P3_0Q)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-P3_0QF)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-P3_1Q)}$	Port $P3_1$ data output delay time				200	ns
$t_{d(\phi-P3_1QF)}$	Port $P3_1$ data output delay time				200	ns

Memory expanding mode and microprocessor mode

(V_{CC}=5V±5%, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ	Max	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig. 2			250	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig 3			300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time	Fig 2			250	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns

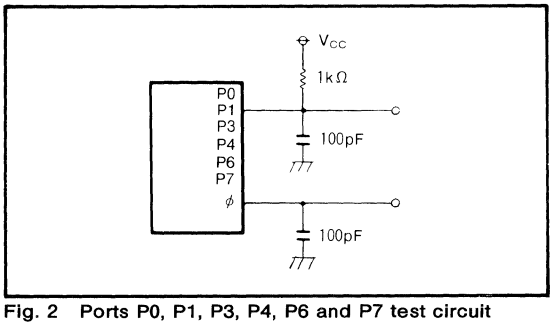


Fig. 2 Ports P0, P1, P3, P4, P6 and P7 test circuit

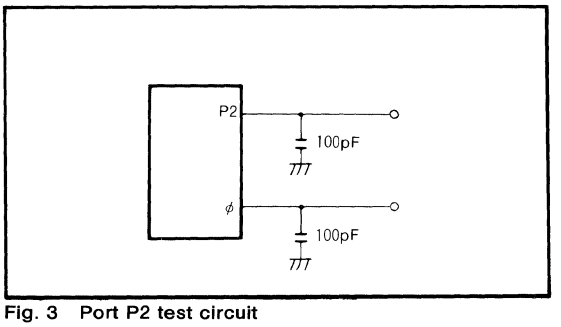
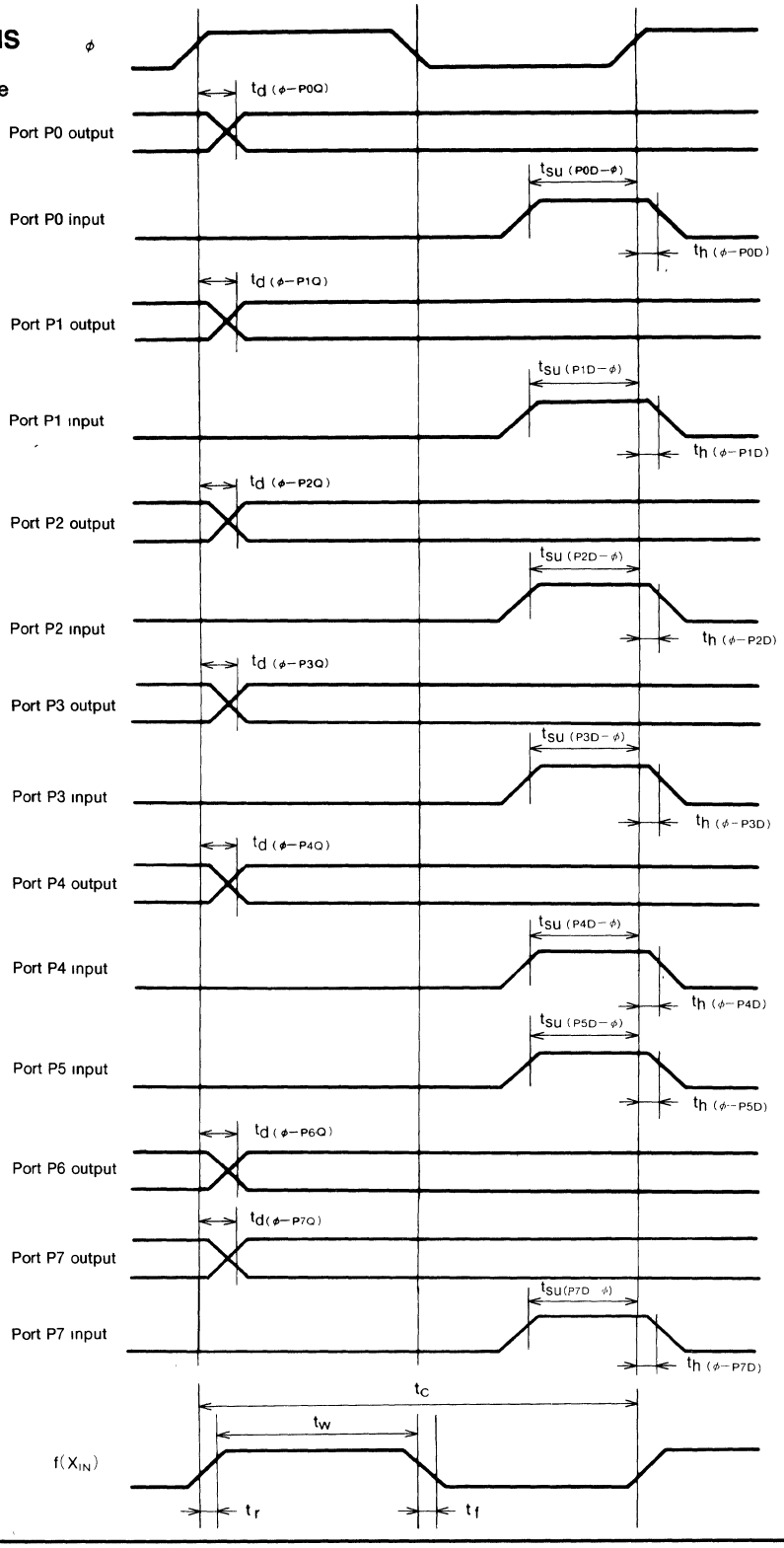


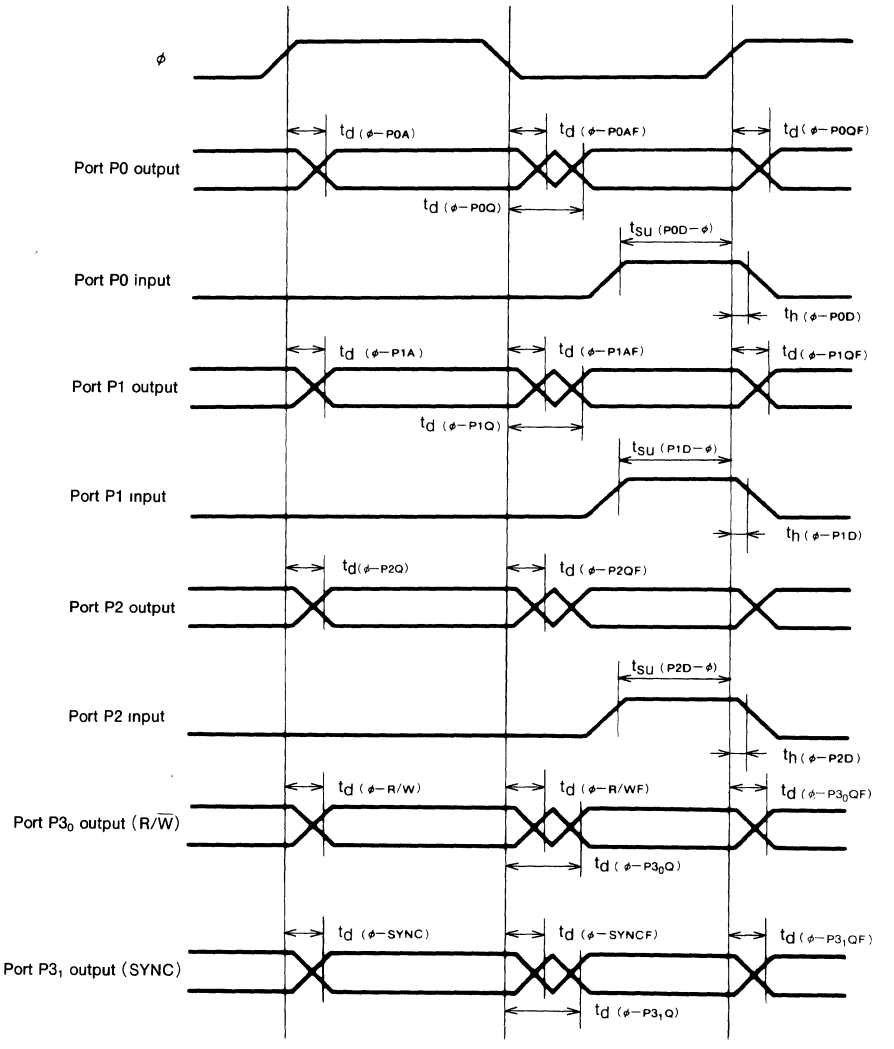
Fig. 3 Port P2 test circuit

TIMING DIAGRAMS

In single-chip mode



In eva-chip mode



In memory expanding mode and microprocessor mode