M37412M4-XXXFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37412M4-XXXFP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 72-pin plastic molded QFP.

This single-chip microcomputer is useful for household appliance and other consumer applications.

In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

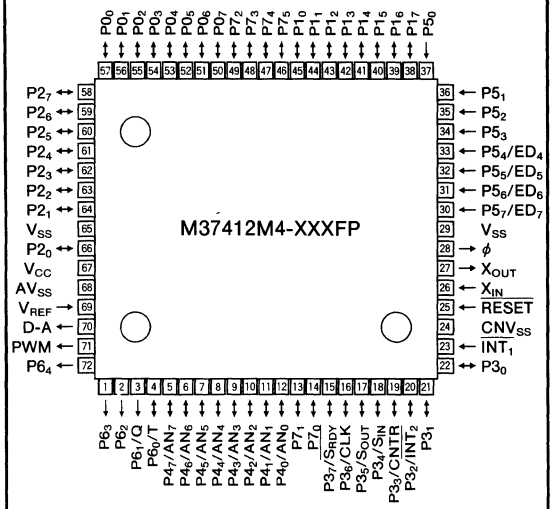
FEATURES

- Number of basic instructions 69
- Memory size ROM ..... 8192 bytes
  RAM ..... 160 bytes
- Instruction execution time
  ..... 2μs (minimum instruction, at 4MHz frequency)
- Single power supply ..... 5V$\pm$10%
- Power dissipation
  normal operation mode (at 4MHz frequency) 15mW
- Subroutine nesting ..... 80 levels (Max.)
- Interrupt ..... 7 types, 5 vectors
- 8-bit timer 4
- Programmable I/O ports (Ports P0, P1, P2, P3, P4, P7)
  46
- Input port (Port P5) 8
- Output port (Port P6) 5
- Serial I/O (8-bit) 1
- 8-bit A-D converter 1
- 5-bit D-A converter 1
- 8-bit PWM function 1
- Watchdog timer 1

APPLICATION

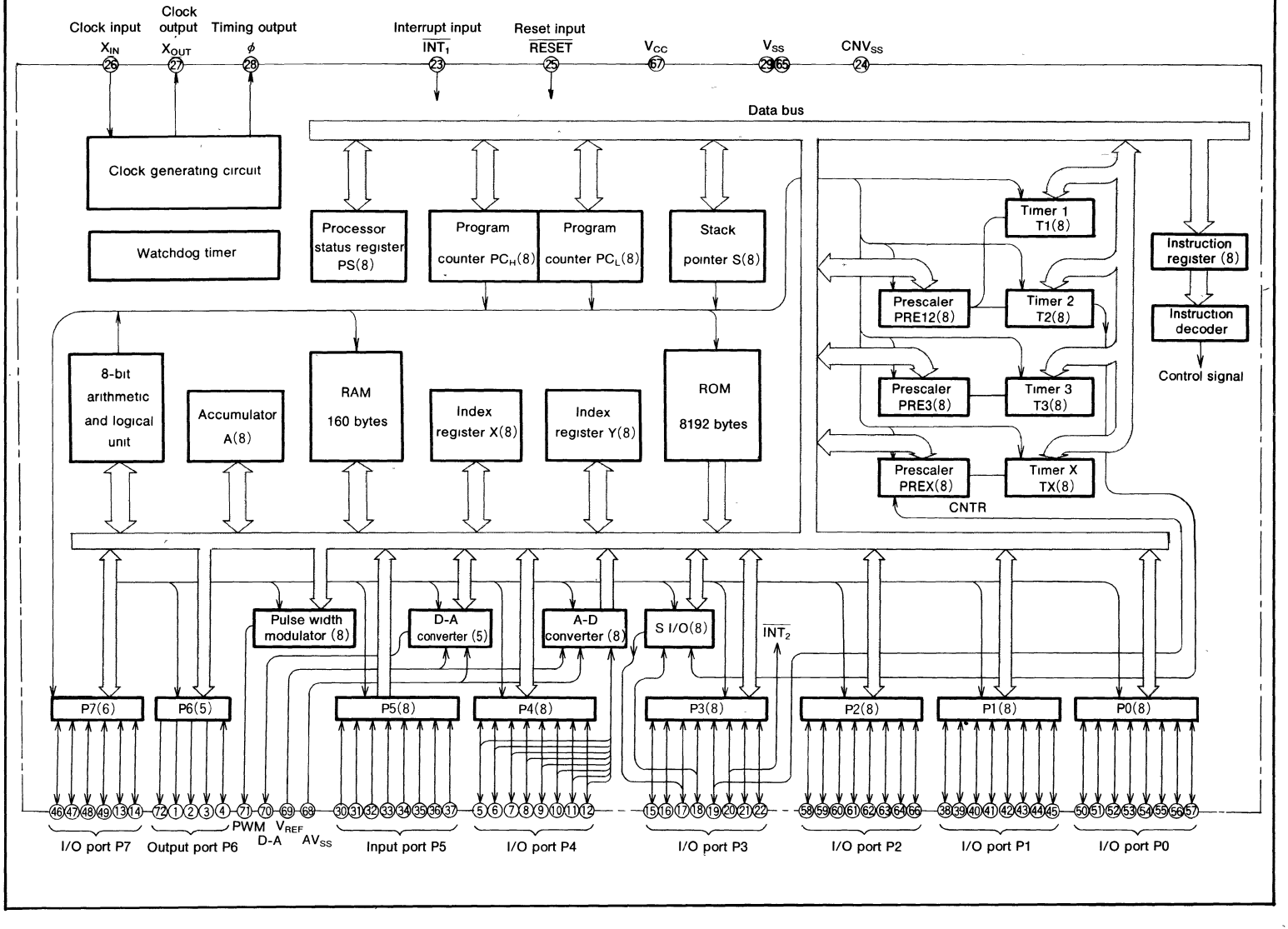
VCR, Tuner, Audio-visual equipment
Office automation equipment

PIN CONFIGURATION (TOP VIEW)



Outline 72P6

M37412M4-XXXFP BLOCK DIAGRAM



FUNCTIONS OF M37412M4-XXXFP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			2μs (minimum instructions, at 4MHz frequency)
Clock frequency			4MHz
Memory size	ROM		8192bytes
	RAM		160bytes
Input/Output ports	$\overline{INT_1}$	Input	1-bit×1
	P0, P1, P2, P3, P4	I/O	8-bit×5 (a part of P3 is common with serial I/O, timer I/O, and interrupt input)
	P5	Input	8-bit×1
	P6	Output	5-bit×1 (a part of P6 is common with external trigger output pin)
	P7	I/O	6-bit×1
Serial I/O			8-bit×1
Timers			8-bit prescaler×3+8-bit timer×4
A-D conversion			8-bit×1 (8 channels)
D-A conversion			5-bit×1
Pulse width modulator			8-bit×1
Watchdog timer			15-bit×1
Subroutine nesting			80 levels (max)
Interrupts			Two external interrupts, Three internal timer interrupts
Clock generating circuit			Built-in (ceramic or quartz crystal oscillator)
Supply voltage			5V±10%
Power dissipation			15mW (at 4MHz frequency)
Input/Output characteristics	Input/Output voltage		12V (Ports P0, P1, P3, P4, P5, P6, P7, $\overline{INT_1}$)
	Output current		5mA (Ports P0, P1, P2, P3, P4, P7)
Memory expansion			Possible
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate process
Package			72-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit To control the generation frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin
AV_{SS}	Voltage input for A-D and A-D		This is GND input pin for the A-D and D-A converters
V_{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D and D-A converters
D-A	D-A output	Output	This is output pin from the D-A converter
PWM	PWM output	Output	This is output pin from the pulse width modulator The output structure is N-channel open drain
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional register allowing each I/O bit to be individually programmed as input or output At reset, this port is set to input mode The output structure is N-channel open drain
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0 The output structure is N-channel open drain
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is CMOS output
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0 When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively. Also $P3_3$ and $P3_2$ work as CNTR pin and the lowest interrupt input pin ($\overline{INT_2}$), respectively.
$P4_0$~$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0. $P4_7$~$P4_0$ work as analog input port AN_7~AN_0 The output structure is N-channel open drain
$P5_0$~$P5_7$	Input port P5	Input	Port P5 is an 8-bit input port $P5_4$~$P5_7$ can be used as the edge sense inputs
$P6_0$~$P6_4$	Output port P6	Output	Port P6 is a 5-bit output port At external trigger output mode, $P6_0$ and $P6_1$ are in common with the trigger input pin (T) and the trigger output pin (Q), respectively The output structure is N-channel open drain
$P7_0$~$P7_5$	I/O port P7	I/O	Port P7 is a 6-bit I/O port and has basically the same functions as port P0 The output structure is N-channel open drain

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The M37412 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions are not provided.

The WIT instruction can be used.

The STP instruction can be used.

Timer Control Register

The timer control register is allocated to address $00FF_{16}$. Bits 0 and 1 of this register are processor mode bits. This register also has a stack page selection bit.

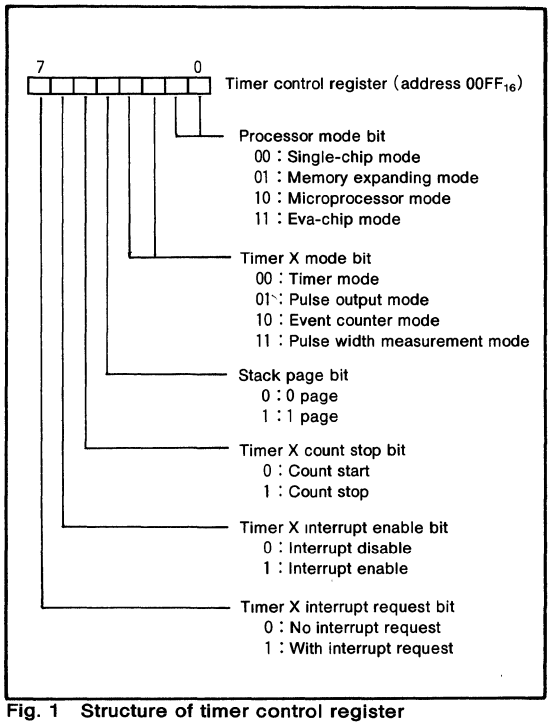


Fig. 1 Structure of timer control register

MEMORY

• Special Function Register (SFR) Area

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• RAM

RAM is used for data storage as well as a stack area.

• ROM

ROM is used for storing user programs as well as the interrupt vector area.

• Interrupt Vector Area

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• Zero Page

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

• Special Page

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

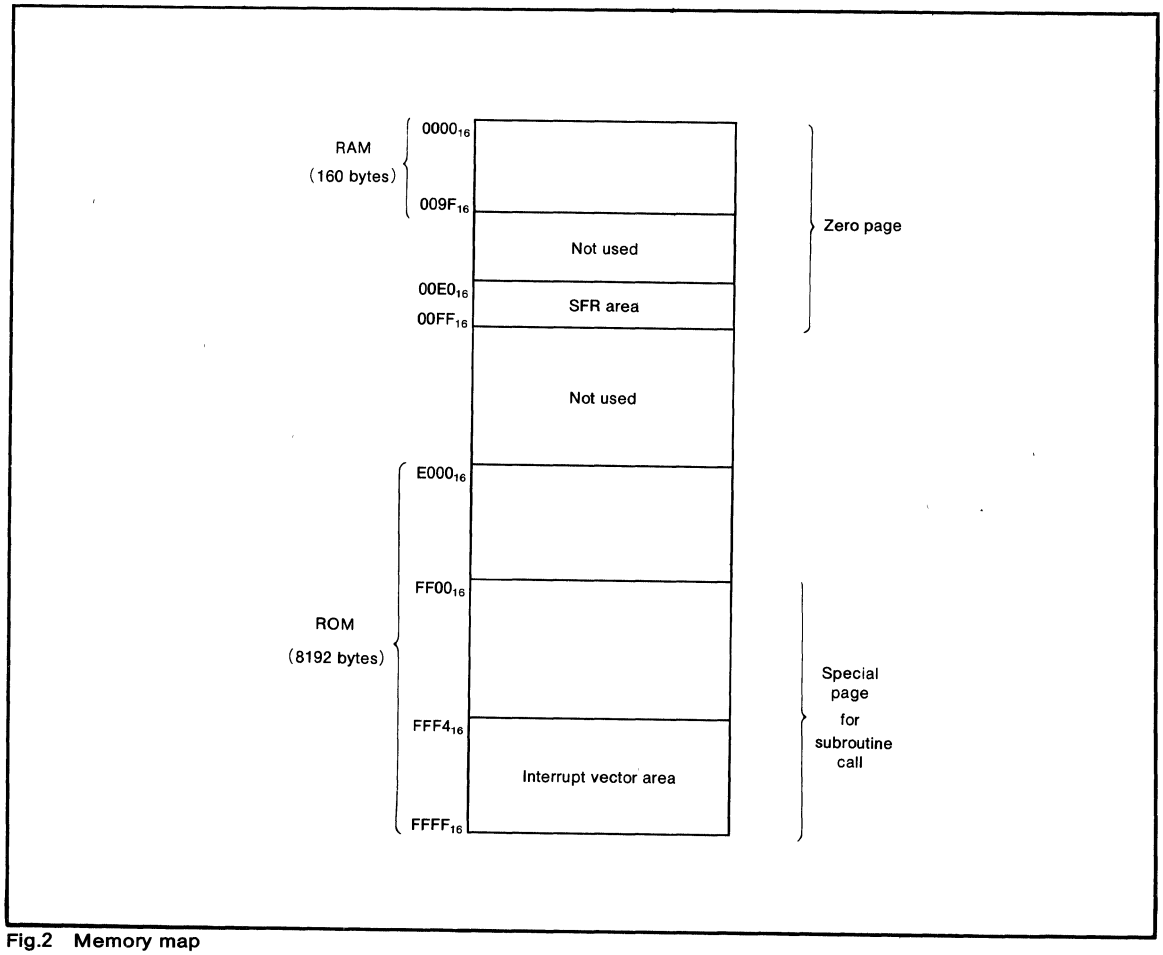


Fig.2 Memory map

$00E0_{16}$	Port P0	$00F0_{16}$	D-A conversion register
$00E1_{16}$	Port P0 directional register	$00F1_{16}$	Pulse width modulation register
$00E2_{16}$	Port P1	$00F2_{16}$	Successive approximation register
$00E3_{16}$	Port P1 directional register	$00F3_{16}$	A-D control register
$00E4_{16}$	Port P2	$00F4_{16}$	Watchdog timer
$00E5_{16}$	Port P2 directional register	$00F5_{16}$	Serial I/O mode register
$00E6_{16}$	Port P7	$00F6_{16}$	Serial I/O register
$00E7_{16}$	Port P7 directional register	$00F7_{16}$	Timer 3 prescaler
$00E8_{16}$	Port P3	$00F8_{16}$	Timer 3
$00E9_{16}$	Port P3 directional register	$00F9_{16}$	Timer 1, 2 prescaler
$00EA_{16}$	Port P4	$00FA_{16}$	Timer 1
$00EB_{16}$	Port P4 directional register	$00FB_{16}$	Timer 2
$00EC_{16}$	Port P5	$00FC_{16}$	Timer X prescaler
$00ED_{16}$	Port P5 latch	$00FD_{16}$	Timer X
$00EE_{16}$	Port P6	$00FE_{16}$	Interrupt control register
$00EF_{16}$	Special function selection register	$00FF_{16}$	Timer control register

Fig. 3 SFR (Special Function Register) memory map

INTERRUPT

The M37412M4-XXXFP can be interrupted from seven sources; $\overline{INT_1}$, timer X, timer 1, timer 2/serial I/O, or $\overline{INT_2}$/BRK instruction.

However, the $\overline{INT_2}$ pin is used with port $P3_2$ and the corresponding directional register bit should be set to "0" when $P3_2$ is used as an interrupt input pin.

The value of bit 2 of the serial I/O mode register (address $00F5_{16}$) determine whether the interrupt is from timer 2 or from serial I/O. When bit 2 is "0" the interrupt is from timer 2, and when bit 2 is "1" the interrupt is from serial I/O. Also, when the bit 2 is "1", parts of port P3 are used for serial I/O. These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same functions as the interrupts.

Table 1. Interrupt vector address and priority

Interrupt	Priority	Vector address
$\overline{RESET}$	1	$FFFF_{16}$, $FFFE_{16}$
$\overline{INT_1}$	2	$FFFD_{16}$, $FFFC_{16}$
Timer X	3	$FFFB_{16}$, $FFFA_{16}$
Timer 1	4	$FFF9_{16}$, $FFF8_{16}$
Timer 2 or serial I/O	5	$FFF7_{16}$, $FFF6_{16}$
$\overline{INT_2}$ (BRK)	6	$FFF5_{16}$, $FFF4_{16}$

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, the interrupt disable flag I is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupt are inhibited when the interrupt disable flag I is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 4. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0".

The interrupt request bits are set when the following conditions occur:

(1) When the $\overline{INT_1}$ or $\overline{INT_2}$ pins go from "H" to "L"
(2) When the contents of timer X, timer 1, timer 2 (or the serial I/O counter) go to "0"

These request bits can be reset by the program but can not be set by the program. However, the interrupt enable bit can be set and reset by the program.

Since the BRK instruction and the $\overline{INT_2}$ interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if $\overline{INT_2}$ generated the interrupt.

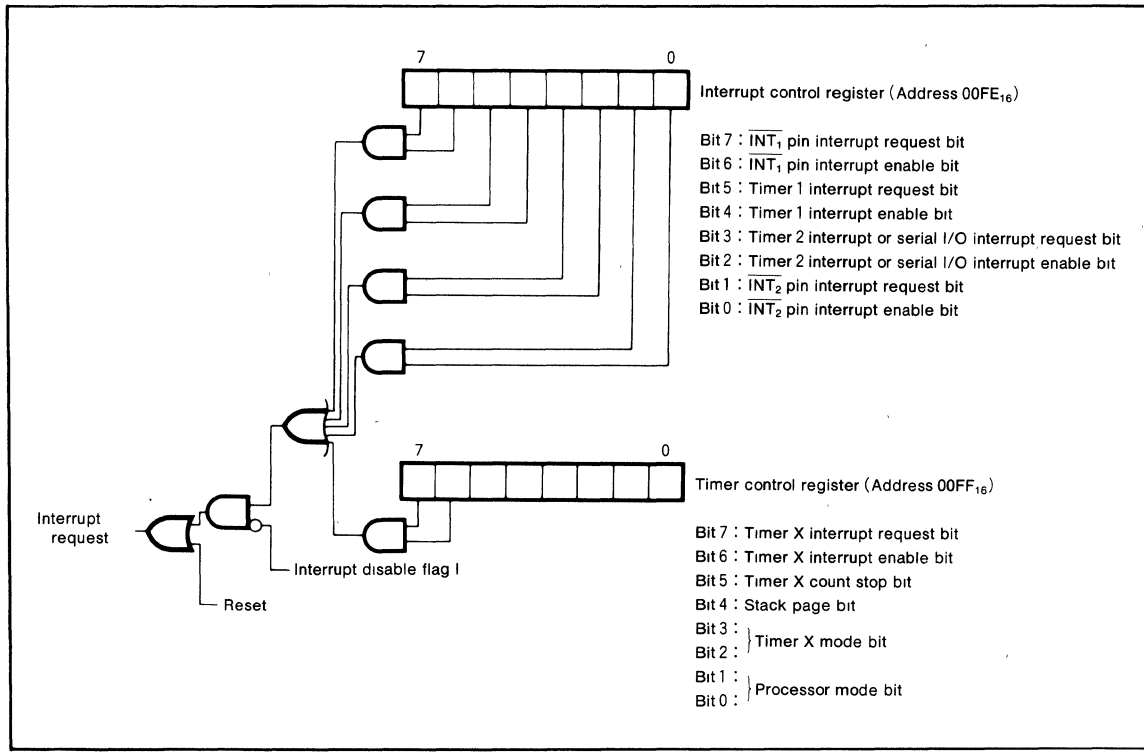


Fig. 4 Interrupt control

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TIMER

The M37412M4-XXXFP has three timers; timer X, timer 1, timer 2 and timer 3. Since P3 (in serial I/O mode) and timer 2 use some of the same architecture, they cannot be used at the same time (see serial I/O section). Timer X has four modes which can be selected by bit 2 and 3 of the timer control register. When the timer X count stop bit (bit 5) is set to "1", the timer X will stop regardless of which mode it is in. A block diagram of timer X, timer 1, timer 2 and timer 3 is shown in Figure 5.

The $P3_3$/CNTR pin cannot be used as CNTR when $P3_3$ is being used in the normal I/O mode.

Timer 1 and timer 2 share with a prescaler. This prescaler has an 8-bit programmable latch used as a frequency divider. The division ratio is defined as $1/(n+1)$, where n is the decimal contents of the prescaler latch. All four timers are down-count timers which are reloaded from the timer latch following the zero cycle of the timer (i.e. the cycle after the timer counts to zero).

The timer interrupt request bit is set to "1" during the next clock pulse after the timer reaches zero. The interrupt and timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see Interrupt section). The prescaler latch and timer latch can be loaded with any number.

The four modes of timer X as follows:

(1) Timer mode [00]
In this mode the clock is driven by the oscillator frequency divided by 16. When the timer down-counts to zero, the timer interrupt request bit is set to "1" and the contents of the timer's latch is reloaded into the timer and the counting begins again.

(2) Pulse output mode [01]
In this mode, the polarity of the CNTR signal is reversed each time the timer down-counts to zero.

(3) Event counter mode [10]
This mode operates in the same manner as the timer mode except, the clock source is input to the CNTR pin. This mode will allow an interrupt to be generated whenever a specified number of external events have been generated. The timer down-counts every rising edge of the clock source.

(4) Pulse width measurement mode [11]
This mode measures the pulse width (between lows) input to the CNTR pin. The timer, driven by the oscillator frequency divided by 16, continues counting during the low cycle of the CNTR pin. When the timer contents reaches "0", the interrupt request bit is set to "1", the timer's reload latch is reloaded and the counting resumes.

The structure of the timer control register is shown in Figure 6.

When the STP instruction is executed, or after reset, the prescaler and timer latch are set to FF_{16} and 01_{16}, respectively. Also, when the STP instruction is executed, the oscillator's frequency (divided by 16) will become the counting source, regardless of the timer X mode setting. This state will be released when the timer X interrupt request bit is set to "1", or after a reset. Timer X will then enter the mode specified by its mode bits. For more details on the STP instruction, refer to the oscillation circuit section.

The function of timer 3 is as same as that of timer 1 and timer 2, with the exception that the detection of its overflow is known by the overflow bit (bit 3 of address $00EF_{16}$). When the timer down-counts to zero, the overflow bit is set to "1" and the contents of the timer's latch is reloaded into the timer.

The reset of the overflow bit is made by;

a) hard ware reset
b) write "0" to overflow bit
c) write instruction to timer 3

The structure of special function selection register is shown in Figure 7.

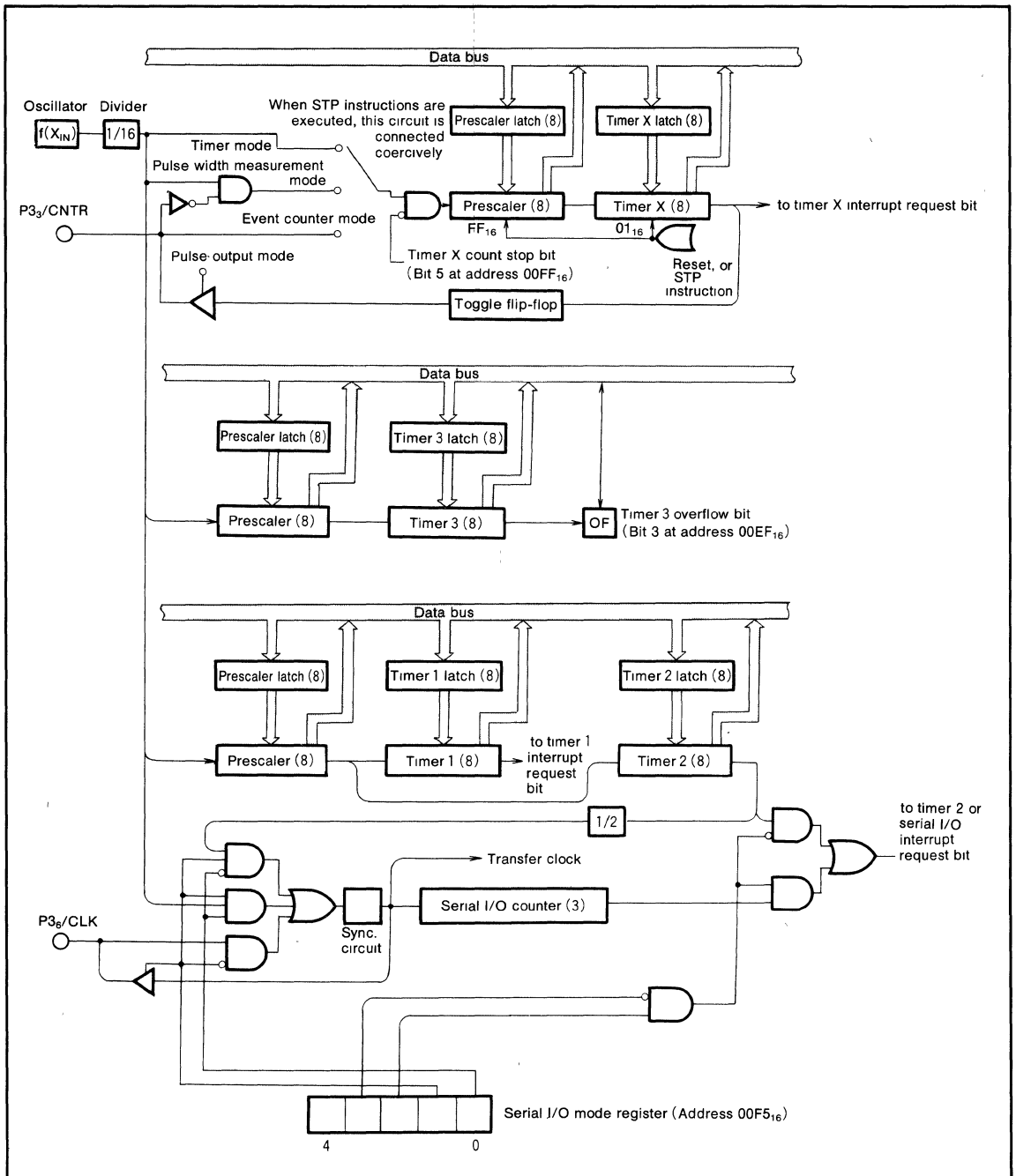

Fig.5 Block diagram of timer X, timer 1, timer 2, and timer 3

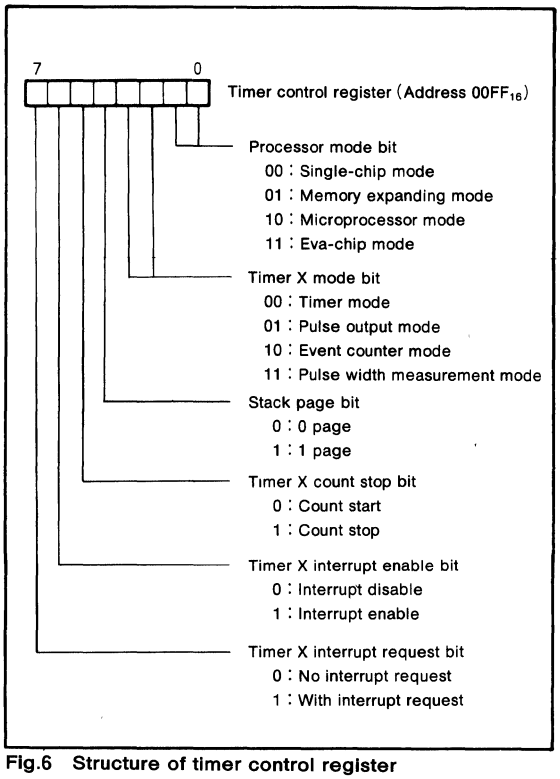

Fig.6 Structure of timer control register

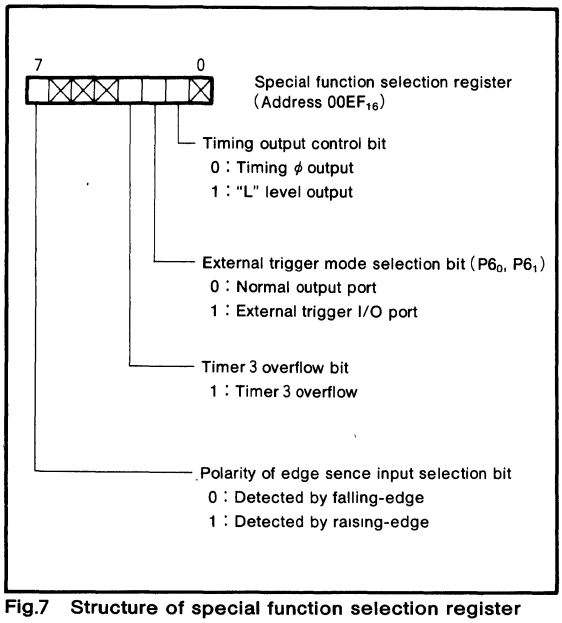

Fig.7 Structure of special function selection register

SERIAL I/O

A block diagram of the serial I/O is shown in Figure 8.

In the serial I/O mode the receive ready signal ($\overline{S_{RDY}}$), synchronous input /output clock (CLK), and the serial I/O pins (S_{OUT}, S_{IN}) are used as $P3_7$, $P3_6$, $P3_5$, and $P3_4$, respectively. The serial I/O mode register (address $00F5_{16}$) is a 5-bit register. Bits 1 and 0 of this register is used to select a synchronous clock source.

When these bits are [00] or [01], an external clock from $P3_6$ is selected. When these bits are [10], the overflow signal from timer 2, divided by two, becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], the oscillator frequency divided by 16, becomes the clock.

Bit 2 to 4 decide whether parts of P3 will be used as a serial I/O or not. When bit 3 is "0" and bit 2 is "1", $P3_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P3_6$. If an external synchronous clock is selected, the clock is input to $P3_6$ and $P3_5$ will be a serial output and $P3_4$ will be a serial input. To use $P3_4$ as a serial input, set the directional register bit which corresponds to $P3_4$ to "0". For more information on the directional register, refer to the I/O pin section.

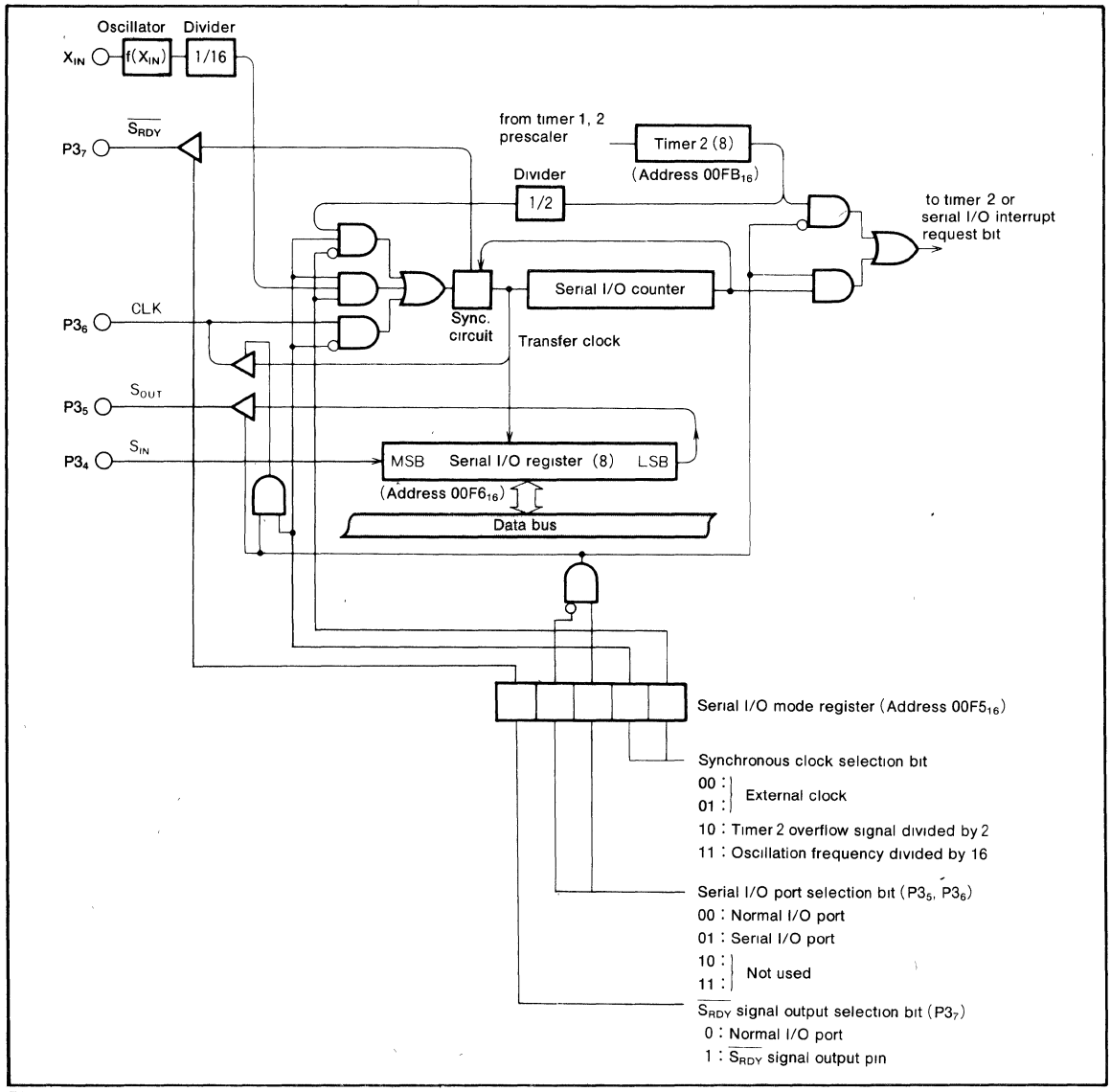

Fig.8 Block diagram of serial I/O

To use the serial I/O, bit 3 and bit 2 need to be set to "01", if they are "00" $P3_6$ will function as a normal I/O. Interrupts will be generated from the serial I/O counter instead of timer 2. Bit 4 determines if $P3_7$ is used as an output pin for the receive data ready signal (bit 4=1, $\overline{S_{RDY}}$) or used as normal I/O pin (bit 4=0). The serial I/O function is discussed below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.

Internal clock—The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register (address $00F7_{16}$). After the falling edge of the write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M37412M4-XXXFP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/C counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to $P3_5$. During the rising edge of this clock, data can be input from $P3_4$ and the data in the serial I/O register will be shifted 1 bit. Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrpt request bit will be set.

External clock—If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 500kHz at a duty cycle of 50%. The timing diagram is shown in Figure 9. An example of communication between two M37412M4-XXXFPs is shown in Figure 10.

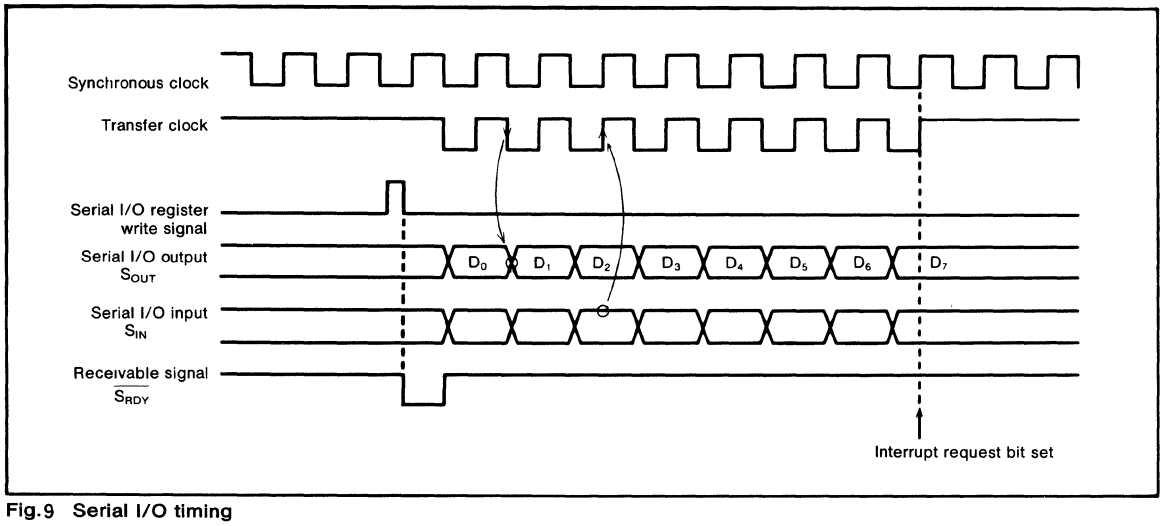

Fig.9 Serial I/O timing

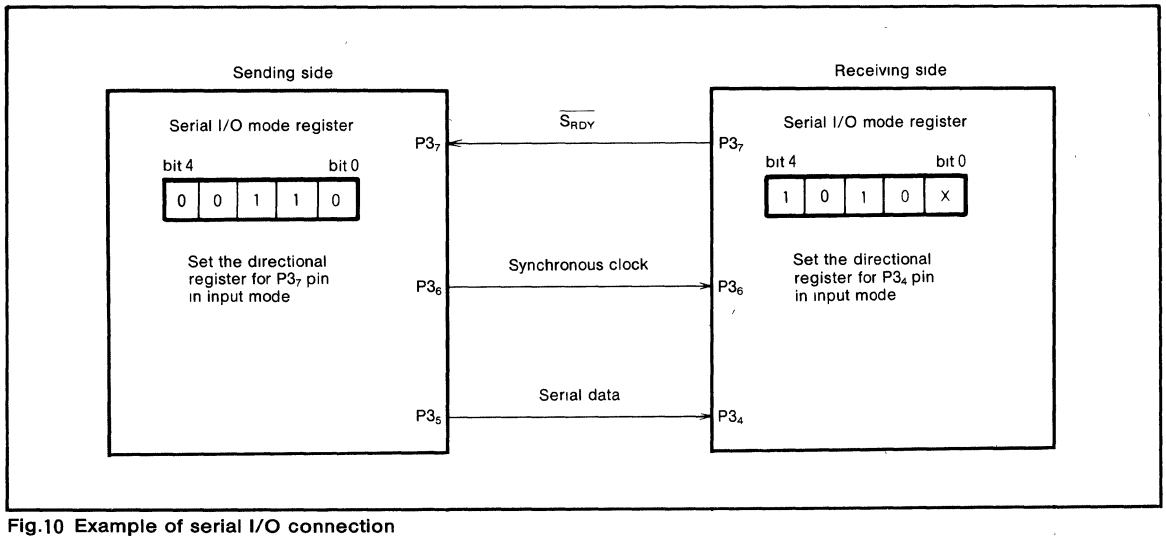

Fig.10 Example of serial I/O connection

A-D CONVERTER

An 8-bit successive approximation method of A-D conversion is employed providing a precision of ±3LSB. A block diagram of the A-D convertor is shown in Figure 11. Conversion is automatic once it is started with the program.

The six analog inputs are used in common with pins $P4_7$~$P4_0$ of port 4. Bits 2, 1 and 0 of the A-D control register (address $00F3_{16}$) are used to select which pins are used for A-D conversion. The input condition is accomplished by setting to "0" the bit in the directional register that corresponds to the pin where A-D conversion is to take place. Bit 4 of the A-D control register is the A-D conversion end bit. During A-D conversion, this bit is "0", and upon completion becomes "1". Thus, it can be ascertained whether or not A-D conversion has been completed or not by inspecting this bit. The relation between the contents of the A-D control register and the selection of input pins are shown in Figure 12.

The results of the conversion can be found be reading the contents of the successive approximation register address $00F2_{16}$ which stores the results of the conversion. The procedure for executing A-D conversion is next explained. Firstly, the pin that is to be used for the A-D conversion is selected by setting bit 1 and bit 0 of the A-D control register. Next, the successive approximation is written to upon which the A-D conversion starts. Since actual data is not written to the successive approximation, any type of may be written. Simultaneous with its being written, the A-D conversion end bit (bit 4 of address $00F3_{16}$) is cleared to "0" signifying that A-D conversion operations are being conducted. A-D conversion completes after 198 clock cycles upon which the A-D conversion end bit is set to "1" and the results of the conversion can be found in the successive approximation register. Since the comparator consists of the capacitive coupled configuration, $f(X_{IN})$ is needed larger than 1MHz during A-D conversion.

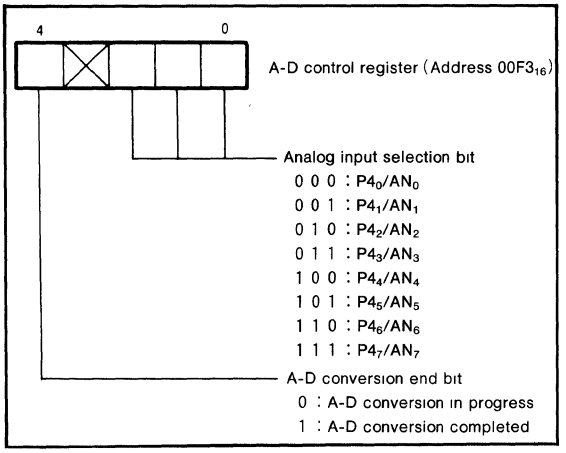

Fig.12 Structure of A-D control register

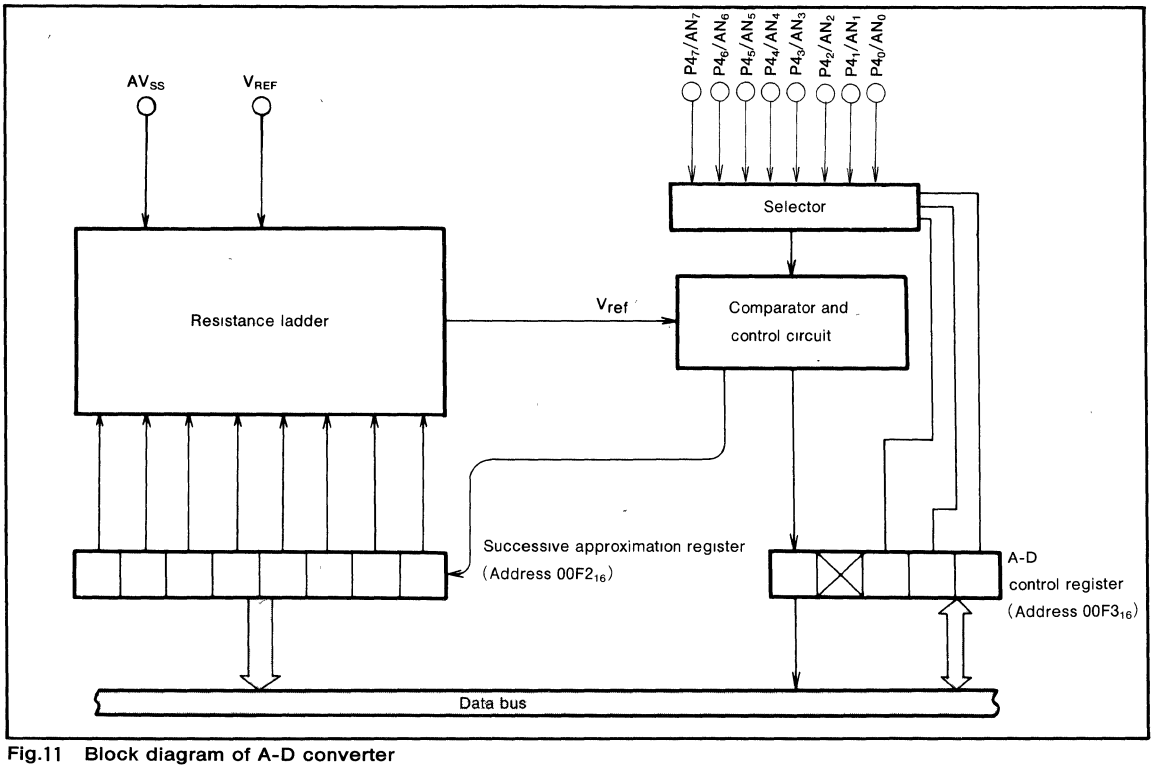

Fig.11 Block diagram of A-D converter

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D-A CONVERTER

The R-2R method is used for D-A conversion. The block diagram is shown in Figure 13 An analog voltage is output that corresponds to the contents of the D-A conversion register (address $00F0_{16}$). Ideally, the relation of the analog output voltage V and the contents (n) of the D-A conversion register is $V=V_{REF} \times n/32 (n=0 \sim 31)$.

Reset operation clears the content n of the D-A conversion register to 0_{16}.

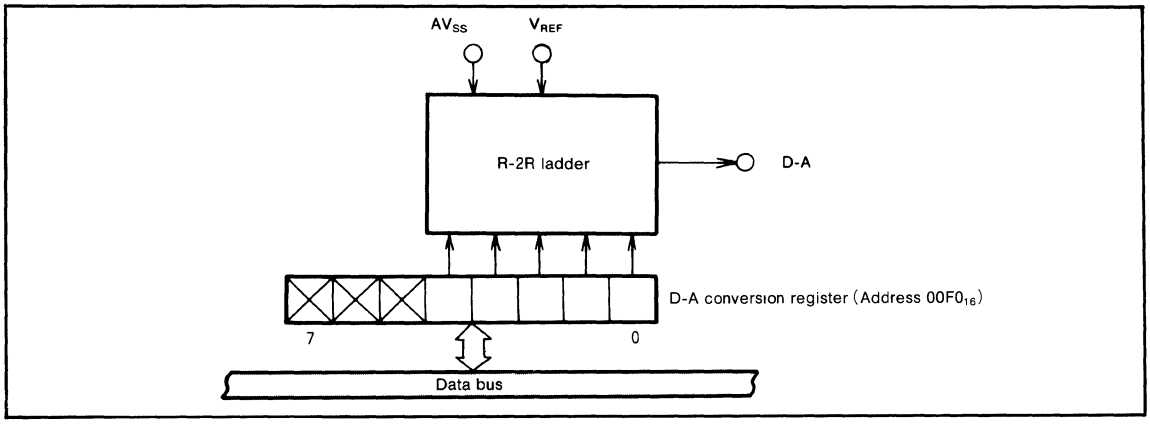

Fig.13 Block diagram of D-A converter

PULSE WIDTH MODULATOR

The pulse width modulation register (address $00F1_{16}$) is configured of an 8-bit counter. The period of repetition is 4080 clock cycles. With the content of the pulse width modulation register m, the PWM pin becomes high-level for the period of 4080 × m/255 (m=0~255). Figure 14 shows that relationship. An N-channel open drain output is used for the PWM pin.

Reset sets the content m of the pulse width modulation register to 00_{16}.

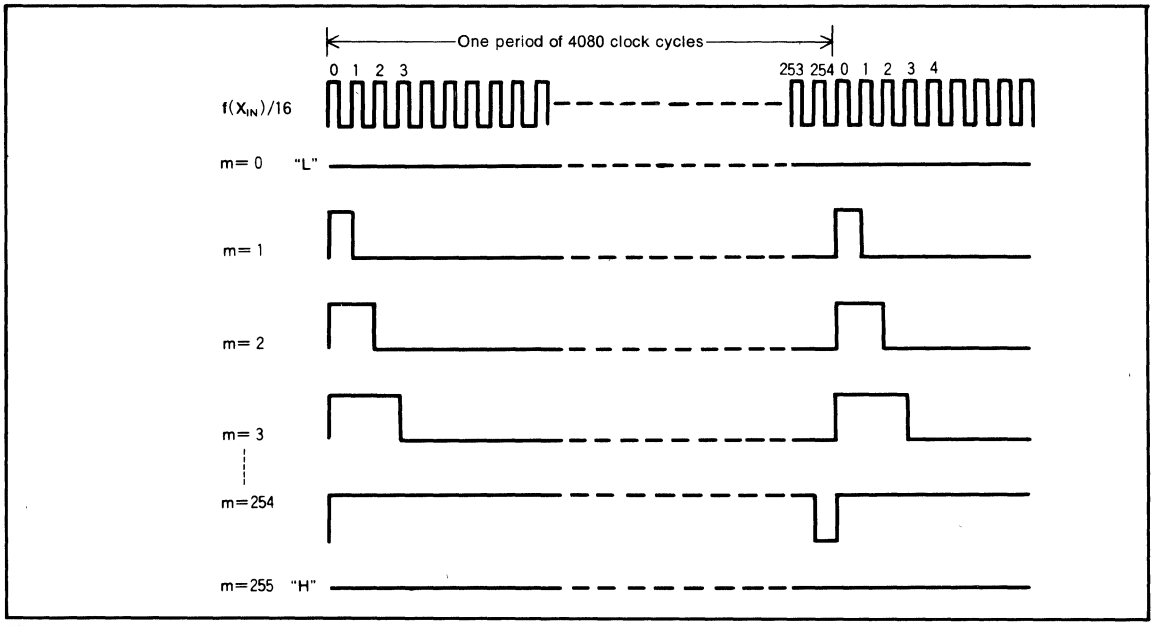

Fig.14 Relation between m and PWM output

WATCHDOG TIMER

The watchdog timer provides the means to return to a reset condition when a program runs wild and the program will not run the normal loops.

The watchdog timer (address $00F4_{16}$) is a 15-bit counter. The watchdog timer counts 1/16th the output frequency of the oscillator. The watchdog timer is set to $7FFF_{16}$ when a reset is accomplished a write operation has been made to it. As well as any of the instructions that generate a write signal, such as STA, LDM, and CLB, can be used to write data to the watchdog timer. An output of the most significant bits of the watchdog timer is input to the reset circuit. When 262144 clock cycles have been counted, the most significant bit becomes "0" and reset is carried out. When reset is carried out, the watchdog timer is set to $7FFF_{16}$ and reset is released. The program then begins again from reset vector address. Normally, the program is written so that a writing operation is made to the watchdog timer prior to the most significant bit's becoming "0". Application of a +10V to the $\overline{\text{RESET}}$ pin will disable the watchdog timer function.

Since execution of the STP instruction causes both the clock and the watchdog timer to stop, an option is offered where the STP instruciotn can be disabled.

RESET CIRCUIT

The M37412M4-XXXFP is reset according to the sequence shown in Figure 15. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFF_{16}$ as the low order address, when the $\overline{\text{RESET}}$ pin is held at "L" level for more than 2μs while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 16.

An example of the reset circuit is shown in Figure 17.

When the power on reset is used, the $\overline{\text{RESET}}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

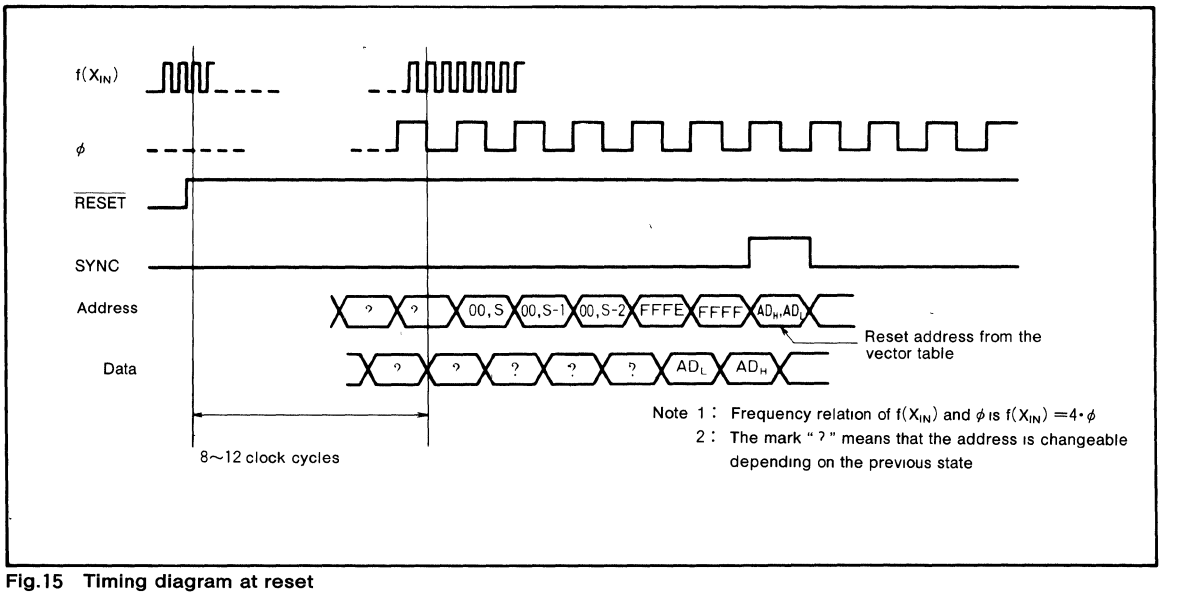

Fig.15 Timing diagram at reset

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		Address	
(1)	Port P0 directional register	(E1 16) ···	00 16
(2)	Port P1 directional register	(E3 16) ···	00 16
(3)	Port P2 directional register	(E5 16) ···	00 16
(4)	Port P7 directional register	(E6 16) ···	0 0 0 0 0 0
(5)	Port P3 directional register	(E9 16) ···	00 16
(6)	Port P4 directional register	(EB 16) ···	00 16
(7)	Port P6	(EE 16) ···	1 1 1 1 1
(8)	Special function selection register	(EF 16) ···	0 X X X 0 0 0 X
(9)	D-A conversion register	(F0 16) ···	0 0 0 0 0
(10)	Pulse width modulation register	(F1 16) ···	00 16
(11)	Watchdog timer	(F4 16) ···	7FFF 16
(12)	Serial I/O mode register	(F5 16) ···	0 0 0 0 0
(13)	Prescaler X	(FC 16) ···	FF 16
(14)	Timer X	(FD 16) ···	01 16
(15)	Interrupt control register	(FE 16) ···	00 16
(16)	Timer control register	(FF 16) ···	00 16
(17)	Interrupt disable flag on processor status register	(PS) ···	1
(18)	Program counter	(PCH) ···	Contents of address FFFF16
		(PCL) ···	Contents of address FFFE16

Fig.16 Internal state of microcomputer at reset

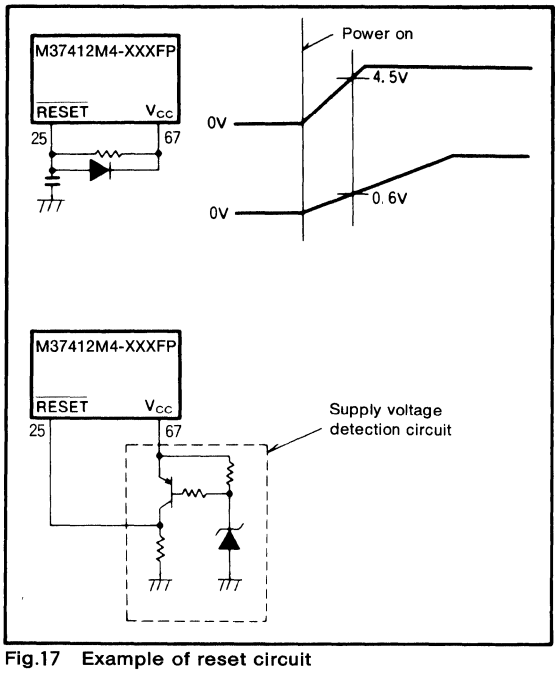


Fig.17 Example of reset circuit

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with N-channel open drain output.

As shown in the memory map (Figure 2), port P0 can be accessed at zero page memory address $00E0_{16}$. Port P0 has a directional register (address $00E1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor status register (bit 0 and bit 1 at address $00FF_{16}$), four different modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and eva-chip mode. These modes (excluding single-chip mode) have a multiplexed address output function in addition to the I/O function. For more details, see the processor mode information.

(2) Port P1
In the single-chip mode, port P1 has the same function as P0, but it has CMOS output. In the other modes, P1's functions are slightly different from P0's. For more details, see the processor mode information.

(3) Port P2
In the single-chip mode, port P2 has the same function as P0. In the other modes, P2's functions are slightly different from P0's.
For more details, see the processor mode information.

(4) Port P3
In the single-chip mode, port P3 has the same function as P0. In the other modes, P3's functions are slightly different from P0's. Port P3 can also be used as serial I/O, $\overline{INT_2}$ and I/O pins for timer X. For more details, see the processor mode information.

(5) Port P4
Port P4 has the same function as port P0 in the single-chip mode. But $P4_7$ through $P4_2$ can also be used as analog input pins AN_7 through AN_2.

(6) Port P5
Port P5 is an input port. $P5_4$ through $P5_7$ can also be used as edge sence inputs. In such a case, reading is begun from $00ED_{16}$. $00ED_{16}$ is provided with a latch which is set to "1" when the input changes from high-level to low-level.
And for $P5_7$, polarity of input edge can be selected by polarity of edge sense input selection bit (bit 7 of address $00EF_{16}$).
When this bit is set to "0", its latch is set to "1" at the input level goes to "L" from "H". When this bit is set to "1", its latch is set to "1" at the input level goes to "H" from "L". At the reset state, this bit is set to "0".
When content of polarity of edge sense input selection bit was set by program, the latch (bit 7 of address $00ED_{16}$) must be reset once.
The input pulse width must be at least 7 clock cycles wide. The latch is reset by using such instructions as LDM and CLB to write a "0" to the latch. When $00ED_{16}$ is read, the lower order 4 bits are always zero.
When port P5 is used as level sense input, read the contents of the address $00EC_{16}$.

(7) Port P6
Port P6 is a 5-bit output port. It has N-channel open drain output. $P6_0$ and $P6_1$ can be used as external trigger I/O pins, when external trigger mode selection bit (bit 2 of address $00EF_{16}$) is set to "1". In this case, $P6_0$ and $P6_1$ are trigger clock input pin and trigger output pin, respectively. Using external trigger mode, $P6_0$'s latch must be set to "1" in order to off the output transistor. In external trigger mode, the content of $P6_1$'s latch is output to pin when the rising or falling edge is input to $P6_0$ pin.
When external trigger mode selection bit is set to "0", $P6_0$ and $P6_1$ are normal output ports. At the reset state, this bit is set to "0".

(8) Port P7
Port P7 is a 6-bit I/O port. In this single-chip mode, port P7 has the same functions as port P0.
The functions of this port do not change even though the processor mode may change.

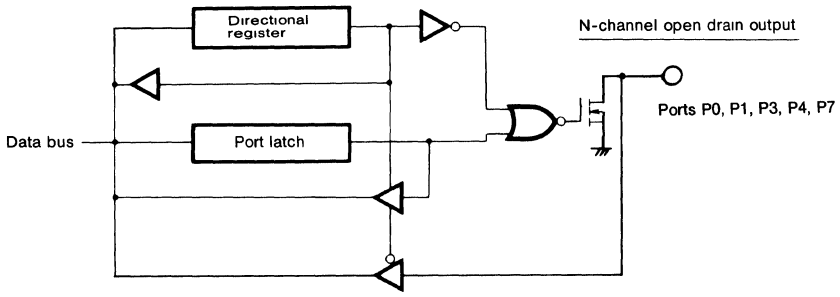
(9) Clock ϕ output pin
In normal conditions, the oscillator frequency divided by four is output as ϕ. The timing output ϕ is fixed "L" state when the timing output control bit (bit 1 of address $00EF_{16}$) is set to "1". But in this case, except the timing output is active. The timing output ϕ is output again when the timing output control bit is set to "0". At reset state this bit is set to "0".

(10) $\overline{INT_1}$ pin
The $\overline{INT_1}$ pin is an interrupt input pin. The $\overline{INT_1}$ interrupt request bit (bit 7 at address $00FE_{16}$) is set to "1" when the input level of this pin changes from "H" to "L".

(11) $\overline{INT_2}$ pin ($P3_2/\overline{INT_2}$ pin)
The $\overline{INT_2}$ pin is an interrupt input pin used with $P3_2$. To use this pin as an interrupt pin, set the corresponding bit in the directional register to input ("0"). When this signal level changes from "H" to "L", the interrupt request bit (bit 1 at address $00FE_{16}$) is set to "1".

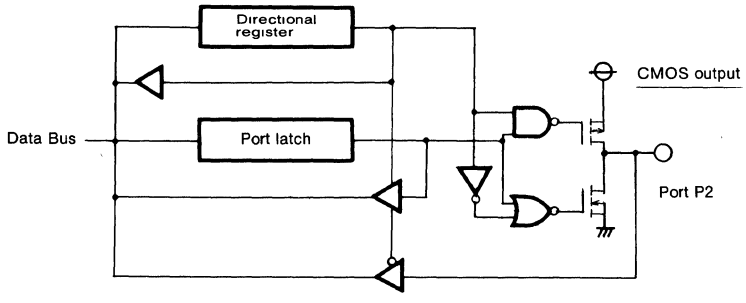
(12) CNTR pin ($P3_3$/CNTR pin)
The $P3_3$/CNTR pin is an I/O pin of timer X. To use this pin as the timer X input pin, set the corresponding directional register bit to input ("0"). In the event counter mode, CNTR becomes the input pin of the external pulse. In the pulse output mode, the CNTR output changes polarity each time the contents of timer X goes to "0". In the pulse width measurement mode, the pulse to be measured is input to this pin.

Port P0, P1, P2, P3, P4, P7

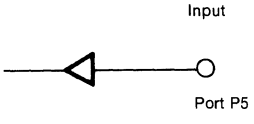


Note 1 : Port P3 can be also used as I/O pin of serial I/O, timer I/O, and interrupt input
Port P4 can be also used as analog input

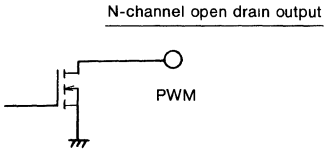
Ports P2



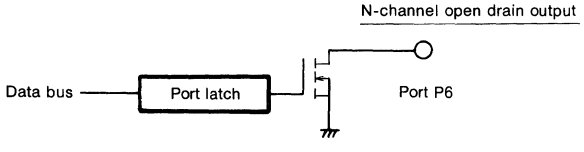
Port P5



PWM



Port P6



ϕ

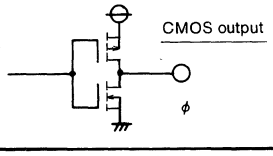


Fig.18 Block diagram of ports P0~P7 (single-chip mode), and output format of ϕ.

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address $00FF_{16}$), four different operation modes can be selected; single-chip mode, memory expanding mode, microprocessor mode and evaluation chip (eva-chip) mode. In the memory expanding mode, microprocessor mode and eva-chip mode, ports P0～P3 can be used as multiplexed I/O for address, data and control signals, as well as the normal functions of the I/O ports.

Figure 20 shows the functions of ports P0～P3.

The memory map for the single-chip mode is illustrated in Figure 2 and for other modes, in Figure 19.

By connecting CNV_{SS} to V_{SS}, all four modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode. Supplying 10V to CNV_{SS} places the microcomputer in the eva-chip mode. The four different modes are explained as follows:

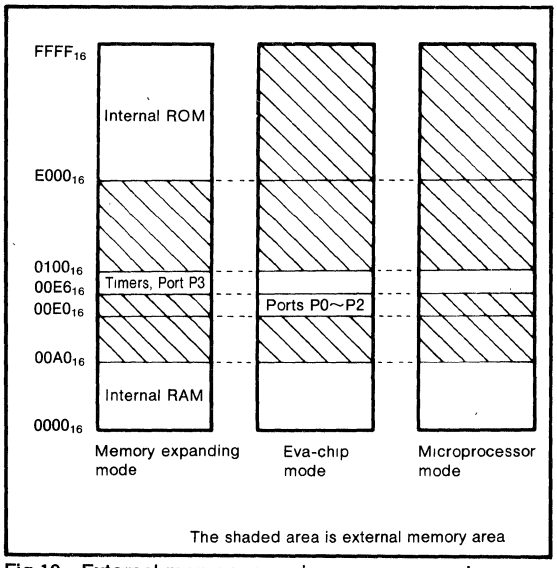


Fig.19 External memory area in processor mode

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0～P3 will work as original I/O ports.

(2) Memory expanding mode [01]

The microcomputer will be placed in the memory expanding mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

In this mode, port P0 and port P1 are as a system address bus and the original I/O pin function is lost. P2 becomes the data bus (D_7～D_0) and loses its normal I/O functions. Pins $P3_1$ and $P3_0$ output the SYNC and R/$\overline{W}$ control signals, respectively.

(3) Microprocessor mode [10]

After connecting CNV_{SS} to V_{CC} and initiating a reset, the microcomputer will automatically default to this mode. With the exceptions that the internal ROM is disabled and that external memory must be attached in this mode, this mode is the same as the memory expanding mode.

(4) Eva-chip mode [11]

When 10V is supplied to CNV_{SS} pin, the microcomputer is forced into the eva-chip mode. The main purpose of this mode is to evaluate ROM programs prior to masking them into the microcomputer's internal ROM.

In this mode, the internal ROM is inhibited so the external memory is requierd.

The lower 8 bits of address data for port P0 is output when ϕ goes to "H" state. When ϕ goes to the "L" state, P0 retains its original I/O functions.

Port P1's higher 8 bits of address data are output when ϕ goes to "H" state and as it changes back to the "L" state it retains its original I/O functions. Port P2 retains its original I/O functions while ϕ is at the "H" state, and works as a data bus of D_7～D_0 (including instruction code) while at the "L" state. Pins $P3_1$ and $P3_0$ output the SYNC and R/$\overline{W}$ control signals, respectively while ϕ is in the "H" state. When in the "L" state, $P3_1$ and $P3_0$ retain their original I/O function.

The R/$\overline{W}$ output is used to read/write from/to the outside. When this pin is in the "H" state, the CPU reads data, and when in the "L" state, the CPU writes data.

The SYNC is a synchronous signal which goes to the "H" state when it fetches the OP CODE.

The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 2.

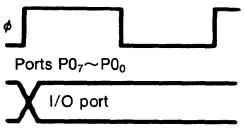
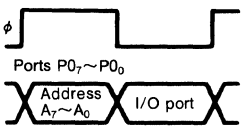
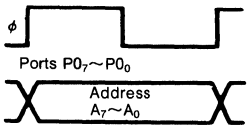
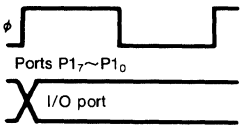
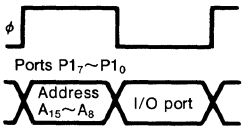
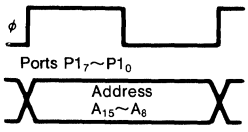
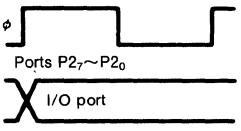
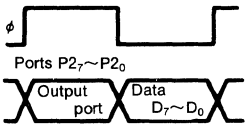
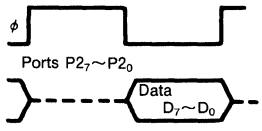
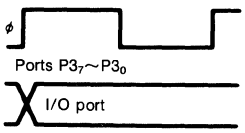
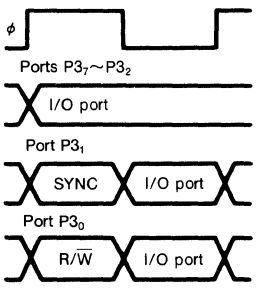
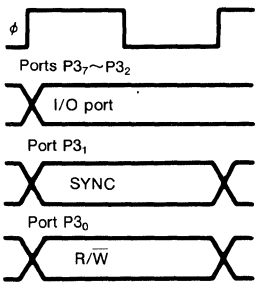
Port \ Mode	Single-chip mode	Eva-chip mode	Memory expanding mode	Microprocessor mode
CM_1	0	1	0	1
CM_0	0	1	1	0
Port P0				Same as left
Port P1				Same as left
Port P2				Same as left
Port P3				Same as left

Fig.20 Processor mode and functions of ports P0~P3

Table 2. Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expanding mode • Eva-chip mode • Microprocessor mode	The single-chip mode is set by the reset All modes can be selected by changing the processor mode bit with the program
V_{CC}	• Eva-chip mode • Microprocessor mode	The microprocessor mode is set by the reset Eva-chip mode can be also selected by changing the processor mode bit with the program.
10V	• Eva-chip mode	Eva-chip mode only.

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 23.

When the STP instruction is executed, the oscillation of internal clock ϕ is stopped in the "H" state.

Also, the prescaler X and timer X are loaded with FF_{16} and 01_{16}, respectively. The oscillator (dividing by 16) is then connected to the prescaler input. This connection is cleared when timer X overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the internal clock ϕ keeps its "H" level until timer X overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 21.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock usage is shown in Figure 22. X_{IN} is the input, and X_{OUT} is open.

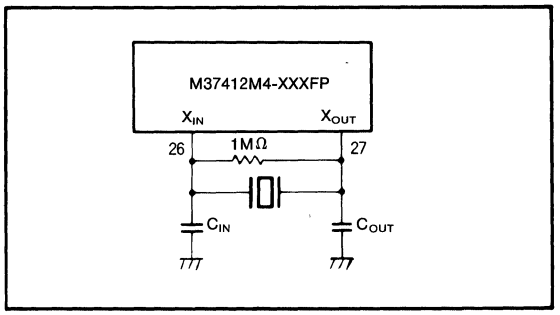


Fig.21 External ceramic resonator circuit

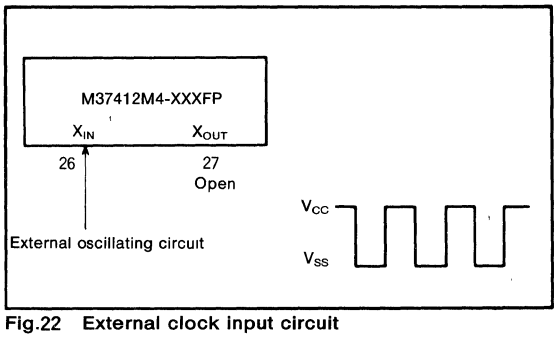


Fig.22 External clock input circuit

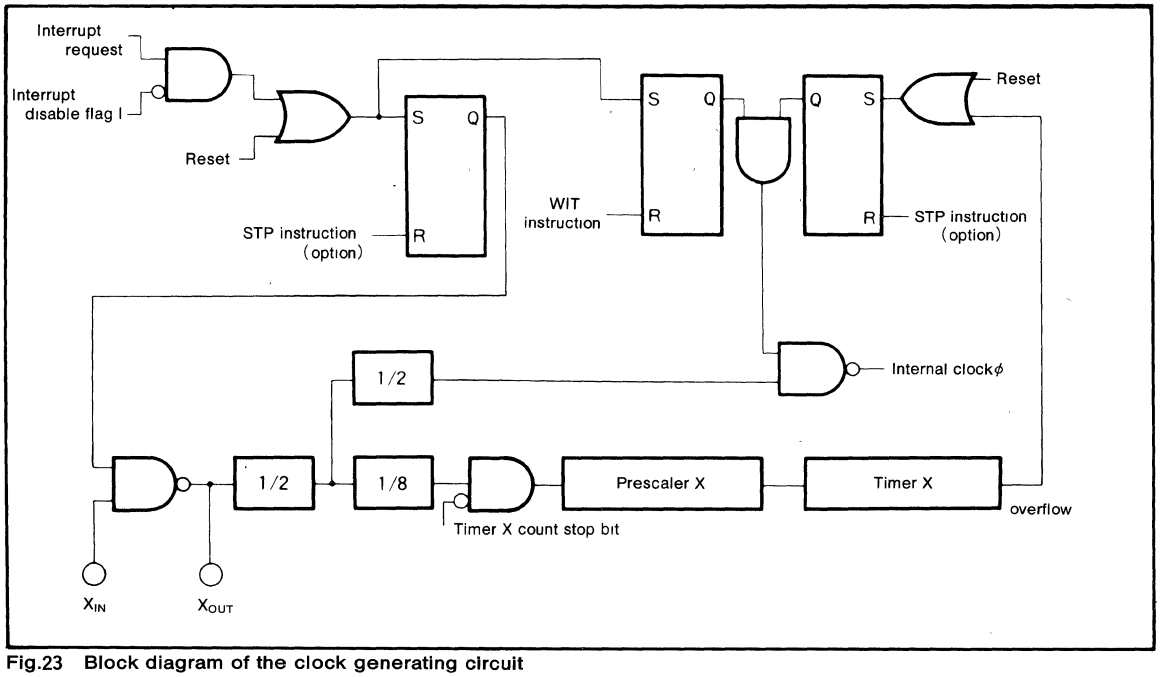


Fig.23 Block diagram of the clock generating circuit

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PROGRAMMING NOTES

(1) The frequency ratio of the timer and the prescaler is 1/(n+1).
(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
(3) Reading the timer and prescaler must be avoided while the input to the prescaler is changing.
(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
(5) A NOP instruction must be used after the execution of a PLP instruction.
(6) Since the comparator consists of the capacitive coupled configuration, f(X_{IN}) is needed larger than 1MHz during A-D conversion. And during A-D conversion, don't use STP or WIT instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

(1) mask ROM confirmation form
(2) mark specification form
(3) ROM data ..... EPROM 3sets

Write the following option on the mask ROM confirmation form

• STP instruction option

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors cut-off	−0.3∼7	V
V_I	Input voltage X_{IN}		−0.3∼7	V
V_I	Input voltage $P2_0$∼$P2_7$, $P4_0$∼$P4_7$		−0.3∼V_{CC}+0.3	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$, $P7_0$∼$P7_5$, $\overline{INT_1}$		−0.3∼13	V
V_I	Input voltage CNV_{SS}, $\overline{RESET}$		−0.3∼13	V
V_O	Output voltage $P2_0$∼$P2_7$, $P4_0$∼$P4_7$, X_{OUT}, ϕ, D-A		−0.3∼V_{CC}+0.3	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$∼$P3_7$, $P6_0$∼$P6_3$, $P7_0$∼$P7_5$, PWM		−0.3∼13	V
P_d	Power dissipation	T_a=25℃	300	mW
T_{opr}	Operating temperature		−10∼70	℃
T_{stg}	Storage temperature		−40∼125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=−10∼70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{REF}	Reference voltage	4		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, CNV_{SS}, $P6_0$, $P7_0$∼$P7_5$	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $\overline{INT_1}$, CNV_{SS}, $P6_0$, $P7_0$∼$P7_5$	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P7_0$∼$P7_5$ (Note 2)			10	mA
$I_{OL(peak)}$	"L" peak output current $P6_0$∼$P6_3$ (Note 2)			15	mA
$I_{OL(peak)}$	"L" peak output current PWM (Note 2)			5	mA
$I_{OL(avg)}$	"L" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P7_0$∼$P7_5$ (Note 1)			5	mA
$I_{OL(avg)}$	"L" average output current $P6_0$∼$P6_3$ (Note 1)			7	mA
$I_{OL(avg)}$	"L" average output current PWM (Note 1)			2.5	mA
$I_{OH(peak)}$	"H" peak output current $P2_0$∼$P2_7$ (Note 2)			−10	mA
$I_{OH(avg)}$	"H" average output current $P2_0$∼$P2_7$ (Note 1)			−5	mA
$f(X_{IN})$	Internal clock oscillating frequency			4	MHz

Note 1 : Average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms.
2 : Total of "L" output current I_{OL}, of ports P0, P1, P2, P3, P4, P6, P7 and PWM is 80mA max.
Total of "H" output current I_{OH}, of port P2 is 50mA max.
3 : "H" input voltage of ports P0, P1, P3, $P4_0$∼$P4_3$, P5, $P6_0$, P7 and $\overline{INT_1}$ is available up to +12V

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{OH}	"H" output voltage $P2_0$~$P2_7$	I_{OH}=−10mA		3			V
V_{OH}	"H" output voltage ϕ	I_{OH}=−2.5mA		3			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_3$, $P7_0$~$P7_5$	I_{OL}=10mA				2	V
V_{OL}	"L" output voltage ϕ, PWM, $P6_4$	I_{OL}=5mA				2	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{INT_1}$			0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $P3_6$	When used as CLK input		0.3	0.8		V
$V_{T+}-V_{T-}$	Hysteresis $P3_2$	When used as $\overline{INT_2}$ input		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $P3_3$	When used as CNTR input		0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis $P6_0$	When used as T input		0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$				0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}			0.1		0.5	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$, $P7_0$~$P7_5$, PWM	V_I=0V				−5	μA
I_{IL}	"L" input current $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_I=0V				−5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, $P5_0$~$P5_7$, $P6_0$, $P7_0$~$P7_5$, PWM	V_I=12V				12	μA
I_{IH}	"H" input current $\overline{INT_1}$, $\overline{RESET}$, X_{IN}, $P2_0$~$P2_7$, $P4_0$~$P4_7$	V_I=5V				5	μA
V_{RAM}	RAM retention voltage	At clock stop		2			V
I_{CC}	Supply current	ϕ, X_{OUT}, and D-A pins opened, other pins at V_{SS}, and A-D converter in the finished condition	f(X_{IN})=4MHz Square wave		3	6	mA
			At clock stop T_a=25℃			1	μA
			At clock stop T_a=75℃			10	μA

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=AV_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
—	Resolution	V_{REF}=V_{CC}			8	Bits
—	Absolute accuracy	V_{REF}=V_{CC}			±3	LSB
R_{LADDER}	Ladder resistance value	V_{REF}=V_{CC}	2		10	kΩ
t_{CONV}	Conversion time				50	μs
V_{REF}	Reference input voltage		2		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

D-A CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=AV_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
—	Resolution	V_{REF}=V_{CC}			5	Bits
—	Error in full scale range	V_{REF}=V_{CC}			±1	%
t_{SU}	Setup time	V_{REF}=V_{CC}			3	μs
R_O	Output resistance	V_{REF}=V_{CC}			3	kΩ
V_{REF}	Reference voltage		4		V_{CC}	V

TIMING REQUIREMENTS

Single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time	270			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time	270			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time	270			ns
$t_{su(P7D-\phi)}$	Port P7 input setup time	270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time	20			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time	20			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time	20			ns
$t_{h(\phi-P7D)}$	Port P7 input hold time	20			ns
t_C	External clock input cycle time	250			ns
t_W	External clock input pulse width	75			ns
t_r	External clock rising edge time			25	ns
t_f	External clock falling edge time			25	ns

Eva-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ.	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	270			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time	270			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time	20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time	20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	20			ns

Memory expanding mode and microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ.	Max.	
$t_{su(P2D-\phi)}$	Port P2 input setup time	270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time	30			ns

SWITCHING CHARACTERISTICS

Single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig 24			230	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				230	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig.25			230	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time	Fig 24			230	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time				230	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				230	ns
$t_{d(\phi-P7Q)}$	Port P7 data output delay time				230	ns

Eva-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig 24			250	ns
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				250	ns
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				200	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig.25			300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time	Fig 24			250	ns
$t_{d(\phi-R/WF)}$	R/$\overline{W}$ signal output delay time				250	ns
$t_{d(\phi-P3_0Q)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-P3_0QF)}$	Port $P3_0$ data output delay time				200	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				250	ns
$t_{d(\phi-P3_1Q)}$	Port $P3_1$ data output delay time				200	ns
$t_{d(\phi-P3_1QF)}$	Port $P3_1$ data output delay time				200	ns

Memory expanding mode and microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig 24			250	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time	Fig 25			300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-R/W)}$	R/$\overline{W}$ signal output delay time	Fig 24			250	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns

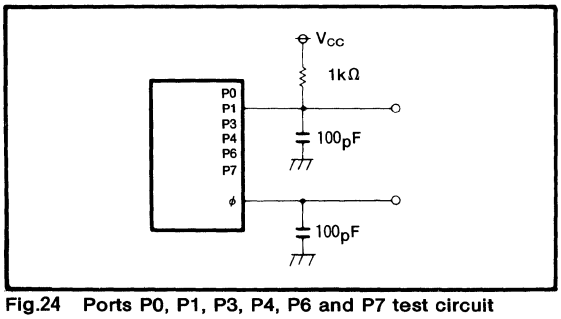


Fig.24 Ports P0, P1, P3, P4, P6 and P7 test circuit

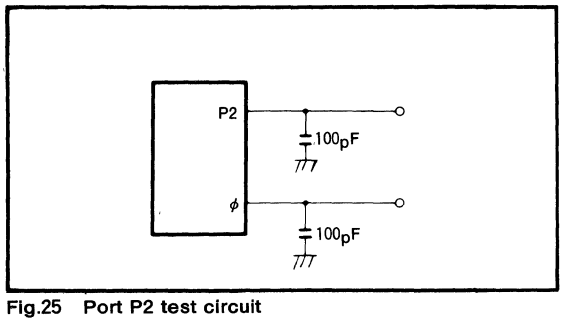
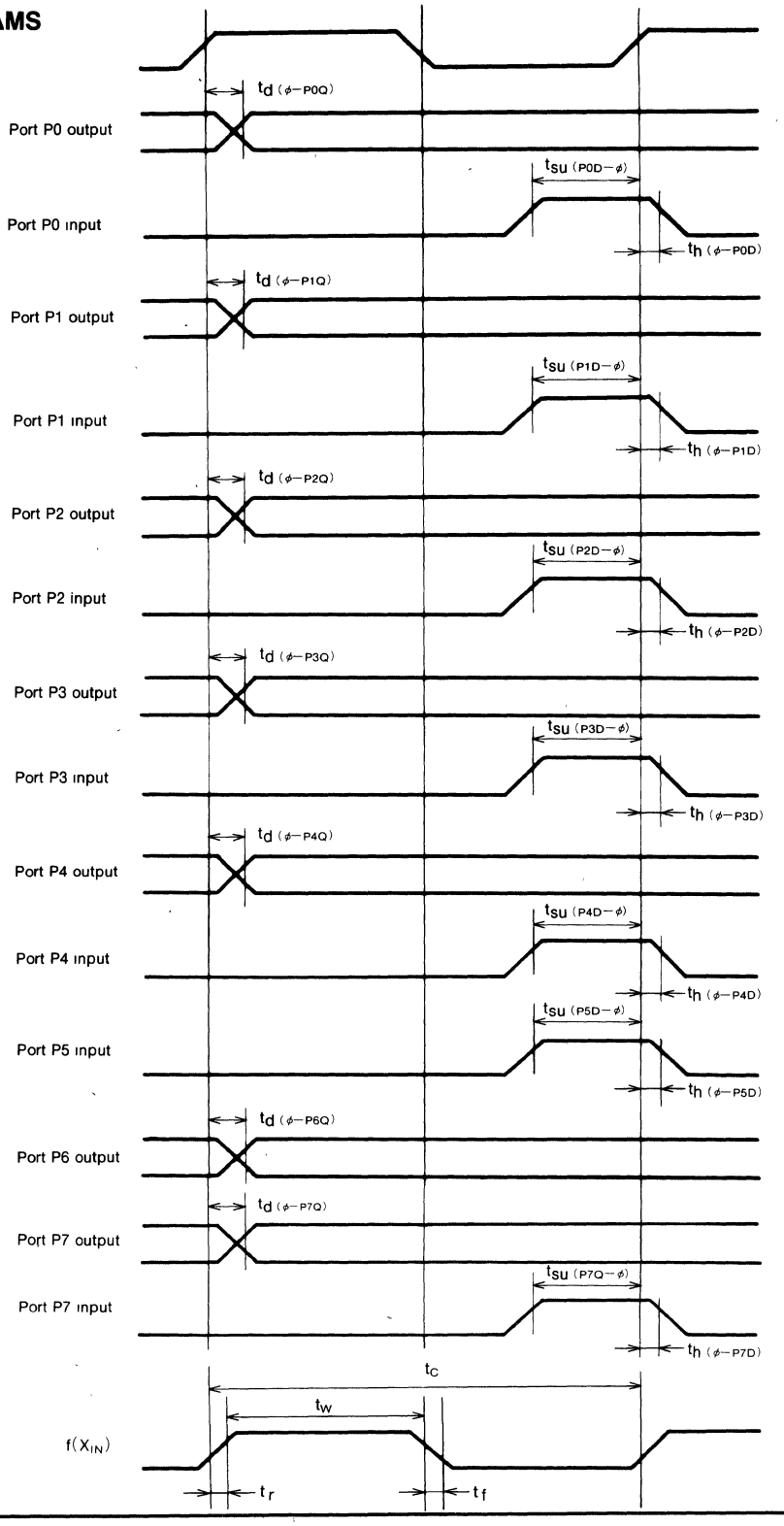


Fig.25 Port P2 test circuit

TIMING DIAGRAMS

In single-chip mode



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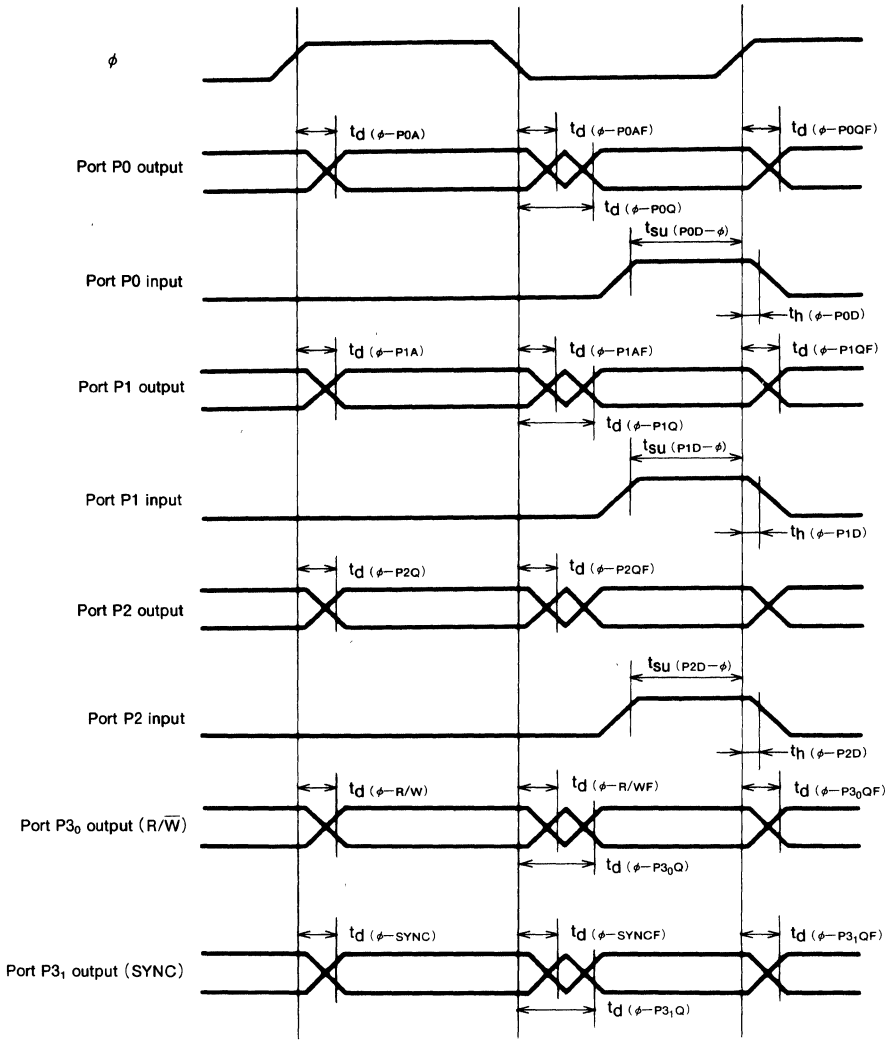
In eva-chip mode



In memory expanding mode and microprocessor mode