M37413M4HXXXFP
M37413M6HXXXFP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37413M4HXXXFP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 80-pin plastic molded QFP. This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction set, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M37413M4HXXXFP and the M37413M6HXXXFP are noted below. The following explanations apply to the M37413M4HXXXFP.

Specification variations for other chips are noted accordingly.

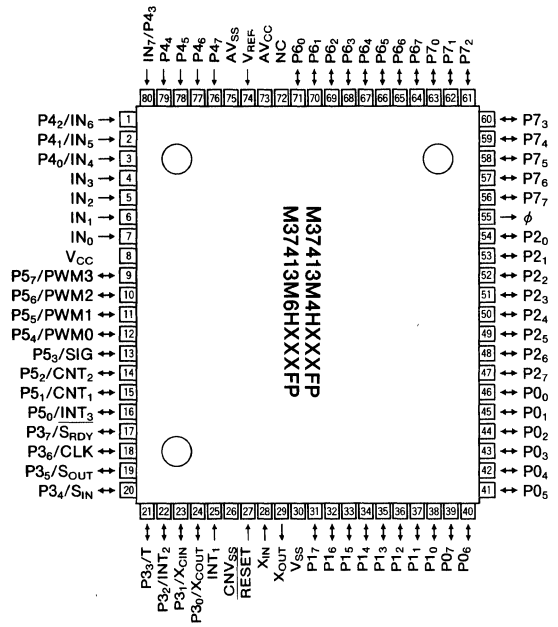
The M37413M4HXXXFP has the same functions as the M37413M4-XXXFP except for the method of writing to interrupt request distinguish registers.

Type name	ROM size
M37413M4HXXXFP	8192 bytes
M37413M6HXXXFP	12288 bytes

FEATURES

- Number of basic instructions 69
- Memory size ROM ... 8192 bytes (M37413M4HXXXFP)
  12288 bytes (M37413M6HXXXFP)
  RAM ..... 256 bytes
- Instruction execution time
  (minimum instructions at 8MHz frequency)
  at high-speed mode 1μs
  at normal mode 4μs
- Single power supply
  high-speed mode (at 8MHz frequency)
  ..... 4.5~5.5V
  normal mode (at 8MHz frequency)
  high-speed mode (at 2MHz frequency)
  ..... 2.5~5.5V
- Power dissipation
  high-speed mode (at 8MHz frequency)
  ..... 30mW (V_{CC}=5V, Typ.)
  low-speed mode (at 32kHz frequency for clock function) ..... 54μW (V_{CC}=3V, Typ.)
- RAM retention voltage (stop mode)
  ..... 2.0V≦V_{RAM}≦5.5V
- Subroutine nesting ..... 96levels (Max.)
- Interrupt 10types, 5vectors
- 8-bit timer ..... 4 (3 when used as serial I/O)
- 16-bit timer 1
- Programmable I/O ports
  (Ports P0, P1, P2, P3, P5, P6, P7) 56
- Input port (Port P4) 8
- Serial I/O (8-bit) 1
- A-D converter 8-bit, 8channel
- Two clock generating circuits
  (One is for main clock, the other is for clock function)

PIN CONFIGURATION (TOP VIEW)



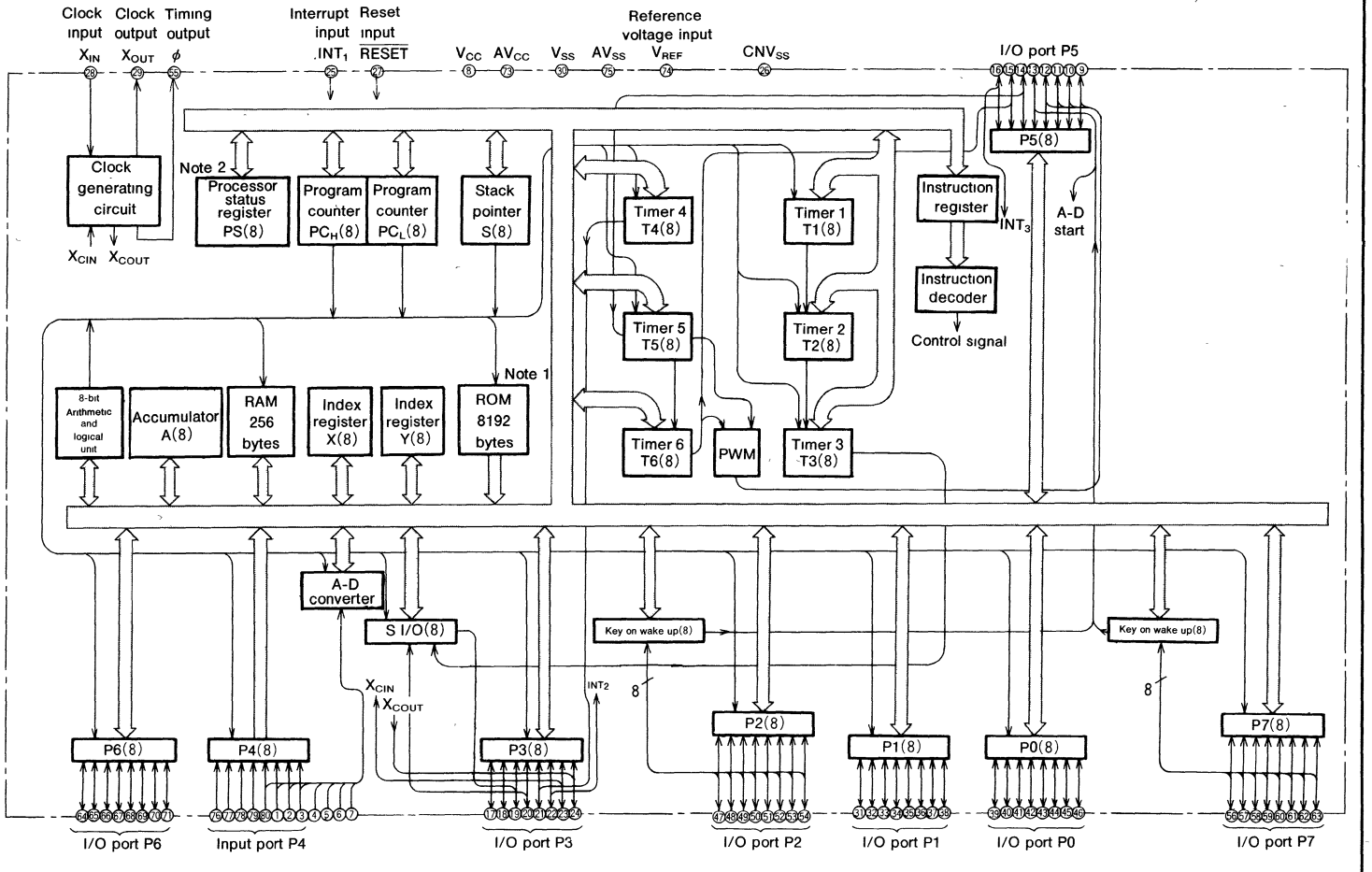
Outline 80P6S

NC : No connection

APPLICATION

Audio-visual equipment, VCR, Tuner, Office automation equipment, Camera, Communications apparatus, Cordless telephone.

M37413M4HXXXFP BLOCK DIAGRAM



Note 1 : 12288 bytes for M37413M6HXXXFP

2 : PC_H uses 6 bits only

FUNCTIONS OF M37413M4HXXXFP, M37413M6HXXXFP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			1μs (minimum instructions, at 8MHz frequency)
Clock frequency			8MHz
Memory size	M37413M4HXXXFP	ROM	8192bytes
		RAM	256bytes
	M37413M6HXXXFP	ROM	12288bytes
		RAM	256bytes
Input/Output port	P0, P2, P7	I/O	8-bit×3 (CMOS output, Pull-up option)
	P1, P3, P5, P6	I/O	8-bit×4 (N-channel open drain output, Pull-up option)
	P4	Input	8-bit×1 (Pull-up option)
Serial I/O			8-bit×1
Timers			8-bit timer×4
			16-bit timer×1
Subroutine nesting			96 (max.)
Interrupt			4 external interrupts, 5 internal interrupts, 1 software interrupt
Clock generating circuit			Two built-in circuits (ceramic or quartz crystal oscillator)
Operating temperature range			−20~75℃
Device structure			CMOS silicon gate
Package			80-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}
CNV_{SS}	CNV_{SS}		This is connect to V_{SS}
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 16μs (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open
X_{OUT}	Clock output	Output	
INT_1	Interrupt input	Input	This is the highest order interrupt input pin
AV_{CC}	Voltage input for A-D		This is power supply input pin for the A-D converter
AV_{SS}	Voltage input for A-D		This is GND input pin for the A-D converters. Connect to V_{SS}
V_{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D converter
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output At reset, this port is set to input mode The output structure is CMOS output Pull-up option of this port is valid only in input mode
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is N-ch open drain Pull-up option of this port is valid only in input mode
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0 and also works as the key on wake up function with mask option Pull-up option of this port is valid only in input mode
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P1 When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively Also $P3_3$, $P3_2$, $P3_1$, and $P3_0$ work as timer 4 overflow signal divided by 2 output pin (T), INT_2 pin, X_{CIN} and X_{COUT} pins, respectively Pull-up option of this port is valid in both input and output modes
$P4_0$~$P4_7$	Input port P4	Input	Port P4 is an 4-bit input port $P4_0$~$P4_3$ are in common with IN_4~IN_7 Pull-up option can be used when this port is used as a input port
$P5_0$~$P5_7$	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same function as P1. $P5_0$, $P5_1$, $P5_2$ and $P5_3$ are in common with INT_3, timer 3 input, timer 5 input and A-D trigger input respectively $P5_4$~$P5_7$ are also in common with PWM0~PWM3 Pull-up option of this port is valid in both input and output modes.
$P6_0$~$P6_7$	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same functions as port P1 Pull-up option of this port is valid in both input and output modes
$P7_0$~$P7_7$	I/O port P7	I/O	Port P7 is an 8-bit I/O port and has basically the same functions as port P2 Pull-up option of this port is valid only in input mode

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The M37413 microcomputers use the standard MELPS 740 instruction set For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions are not provided.

The WIT instruction can be used.

The STP instruction can be used.

MEMORY

• Special Function Register (SFR) Area

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• RAM

RAM is used for data storage as well as a stack area.

• ROM

ROM is used for storing user programs as well as the interrupt vector area.

• Interrupt Vector Area

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• Zero Page

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

• Special Page

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

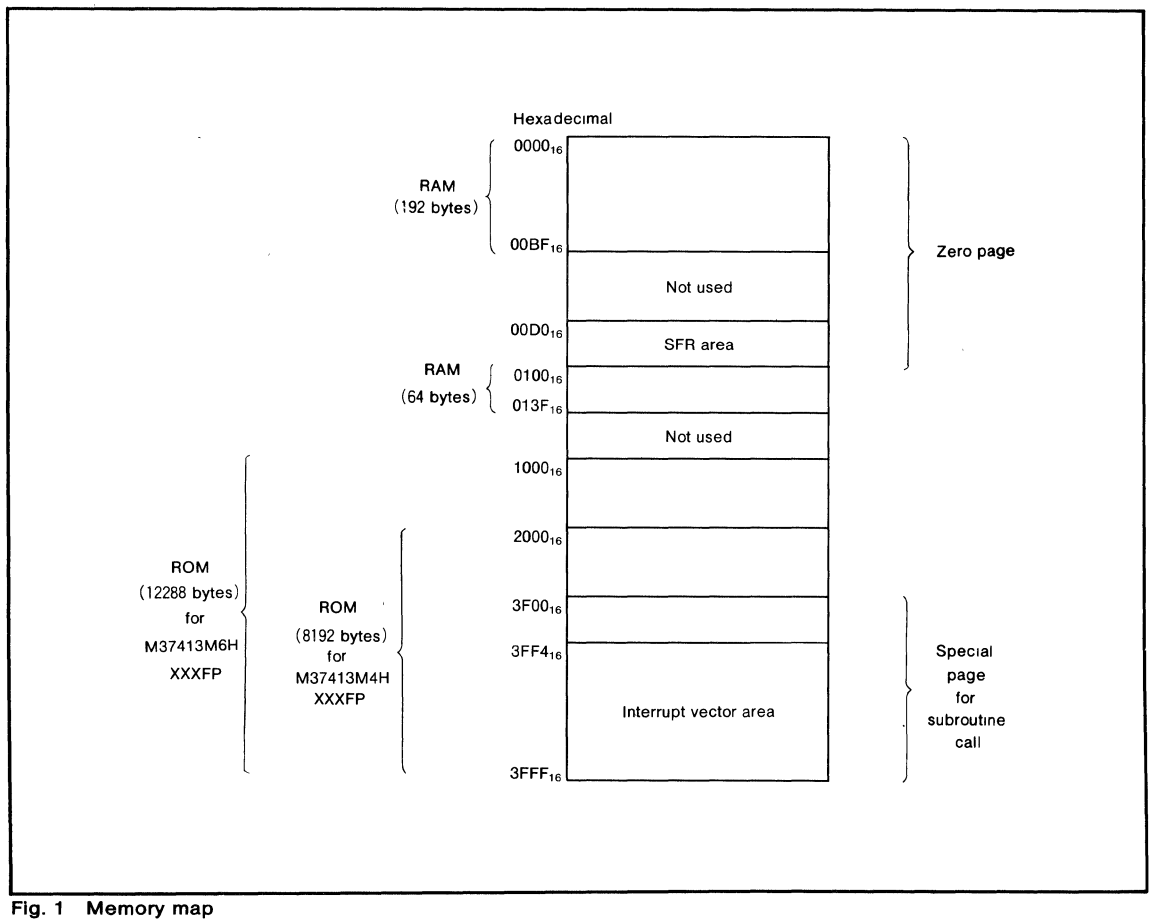


Fig. 1 Memory map

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$00D0_{16}$	Port P6
$00D1_{16}$	Port P6 directional register
$00D2_{16}$	Port P7
$00D3_{16}$	Port P7 directional register
$00D4_{16}$	
$00D5_{16}$	P7 Key on wake up register
$00D6_{16}$	
$00D7_{16}$	
$00D8_{16}$	
$00D9_{16}$	
$00DA_{16}$	
$00DB_{16}$	
$00DC_{16}$	
$00DD_{16}$	
$00DE_{16}$	
$00DF_{16}$	

$00E0_{16}$	Port P0
$00E1_{16}$	Port P0 directional register
$00E2_{16}$	Port P1
$00E3_{16}$	Port P1 directional register
$00E4_{16}$	Port P2
$00E5_{16}$	Port P2 directional register
$00E6_{16}$	
$00E7_{16}$	
$00E8_{16}$	Port P3
$00E9_{16}$	Port P3 directional register
$00EA_{16}$	Interrupt request distinguish register 2
$00EB_{16}$	Interrupt request distinguish register 1
$00EC_{16}$	Port P5
$00ED_{16}$	Port P5 directional register
$00EE_{16}$	P2 Key on wake up register
$00EF_{16}$	A-D register
$00F0_{16}$	
$00F1_{16}$	Timer 6 latch
$00F2_{16}$	A-D control register
$00F3_{16}$	PWM control register
$00F4_{16}$	
$00F5_{16}$	Port P4
$00F6_{16}$	Serial I/O mode register
$00F7_{16}$	Serial I/O register
$00F8_{16}$	Timer 4, 5, 6 mode register
$00F9_{16}$	Timer 1 latch
$00FA_{16}$	Timer 2 latch
$00FB_{16}$	Timer 3 latch
$00FC_{16}$	Timer 4 latch
$00FD_{16}$	Timer 5 latch
$00FE_{16}$	Interrupt control register
$00FF_{16}$	Timer control register

Fig. 2 SFR (Special Function Register) memory map

INTERRUPT

The M37413M4HXXXFP can be interrupted from ten sources; INT_1, Timer 2 or Serial I/O, INT_3 or Key on wake up, INT_2 or Timer 3, Timer 6 or A-D, and BRK instruction.

"Key on wake up" can only be used at power down state by STP instruction or WIT instruction. When one of the P2 or P7 is "L", an interrupt occurs.

These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same function as an interrupt

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, and the interrupt disable flag (I) is set, and the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupts are inhibited when the interrupt disable flag is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 3. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0".

The interrupt request bits are set when the following conditions occur:

(1) When the INT_1, INT_2 or INT_3 pins go from "H" to "L" or "L" to "H"
(2) When the levels any pin of P2 or P7 goes "L"(at power down mode)
(3) When the contents of timer 2, timer 3, timer 6 or the counter of serial I/O goes "0"

These request bits can be clear by a program but can not be set. The interrupt enable bit can be set and clear by a program.

When the two interrupt requests, which are the same priority and are at the same sampling, the priority process is processed by interrupt request distinguish register 1 and 2

The interrupt request distinguish bit is used by software to determine priority when two interrupt causes are allocated to the same interrupt vector(that is, the two interrupts have the same priority).

Irrespective of whether the interrupt is disabled or enabled, the interrupt request distinguish bit is automatically set to "1" when conditions arise that satisfy the interrupt cause.

However, the interrupt request distinguish bit is not automatically cleared. The bit must therefore be cleared by software in the interrupt service routine (before executing an RTI instruction).

Note that when using the instruction CLB to clear this bit, the request distinguish bit of an interrupt that is generated during execution of CLB will not be set(to "1"). Use one of the following two methods to clear interrupt request distinguish bits:

① Use instruction LDM to write directly to address $00EB_{16}$ (interrupt request distinguish register 1) or $00EA_{16}$ (interrupt request distinguish register 2).

```
LDM  #$nn, $zz
, Where zz is the address(00EB16 or 00EA16)of the interrupt request
, distinguish register that includes the interrupt request distinguish
, bit that is to be cleared and nn sets the interrupt request disting-
, uish bit to be cleared to "0" and other interrupt request distinguish
, bits to "1"
, Other control bits must be set according to the required control
, (interrupts enabled or disabled)
[Example] Clearing the INT2 interrupt request distinguish bit
  LDM  1X1X0X1XB, $00EB
         ↑ ↑ ↑ ↑
  Of the interrupt request distinguish bits,only the INT2 interrupt re-
  quest distinguish bit, which is to be cleared, should be set to "0 "
  The values of bits marked "X" are determined by the control
  being effected
```

② Use instructions LDA, ORA, AND, and STA to write via the accumulator to address $00EB_{16}$ (interrupt request distinguish register 1) or $00EA_{16}$ (interrupt request distinguish register 2).

```
  LDA  $zz
  ORA  #$nn
  AND  #$nn
  STA  $zz
, Where zz is the address(00EB16 or 00EA16)of the interrupt request
, distinguish register that includes the interrupt request distinguish
, bit that is to be cleared and nn sets the interrupt request disting-
, uish bit to be cleared to "0" and other interrupt request distinguish
, bits to "1" Other control bits must be set according to the required
, control (interrupts enabled or disabled)
[Example] Clearing the timer 6 interrupt request distinguish bit
  LDA  $00EA
  ORA  XX1X1X0XB
         ↑ ↑ ↑
  Of the interrupt request distinguish bits, only the interrupt request
  distinguish bit for timer 6, which is to be cleared, shoud be set to
  "0" The values of bits marked "x" are detemined by the control
  being effected
         ↓ ↓ ↓
  AND  XX1X1X0XB
  STA  $00EA
```

Because an interrupt request is generated only at the time the interrupt request distinguish bit is set(to "1"), no interrupt will be generated while the interrupt request distinguish bit remains in the set state. For this reason, the interrupt request distinguish bit must be cleared by software in the interrupt service routine.

Note that only method of ① can be used in the M37413M4-XXXFP.
Since the BRK instruction interrupt and the timer 6 or A-D, interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if timer 6 or A-D generated the interrupt.

Table 1. Interrupt vector address and priority

Event	Priority	Vector addresses	Remarks
$\overline{\text{RESET}}$	1	$3FFF_{16}$, $3FFE_{16}$	Non-maskable
INT_1 interrupt	2	$3FFD_{16}$, $3FFC_{16}$	External interrupt
Serial I/O or timer 2 interrupt	3	$3FFB_{16}$, $3FFA_{16}$	
INT_3 or key on wake up interrupt	4	$3FF9_{16}$, $3FF8_{16}$	External interrupt
INT_2 or timer 3 interrupt	5	$3FF7_{16}$, $3FF6_{16}$	External interrupt (INT_2)
Timer 6 or A-D interrupt (BRK instruction interrupt)	6	$3FF5_{16}$, $3FF4_{16}$	(Non-maskable software interrupt)

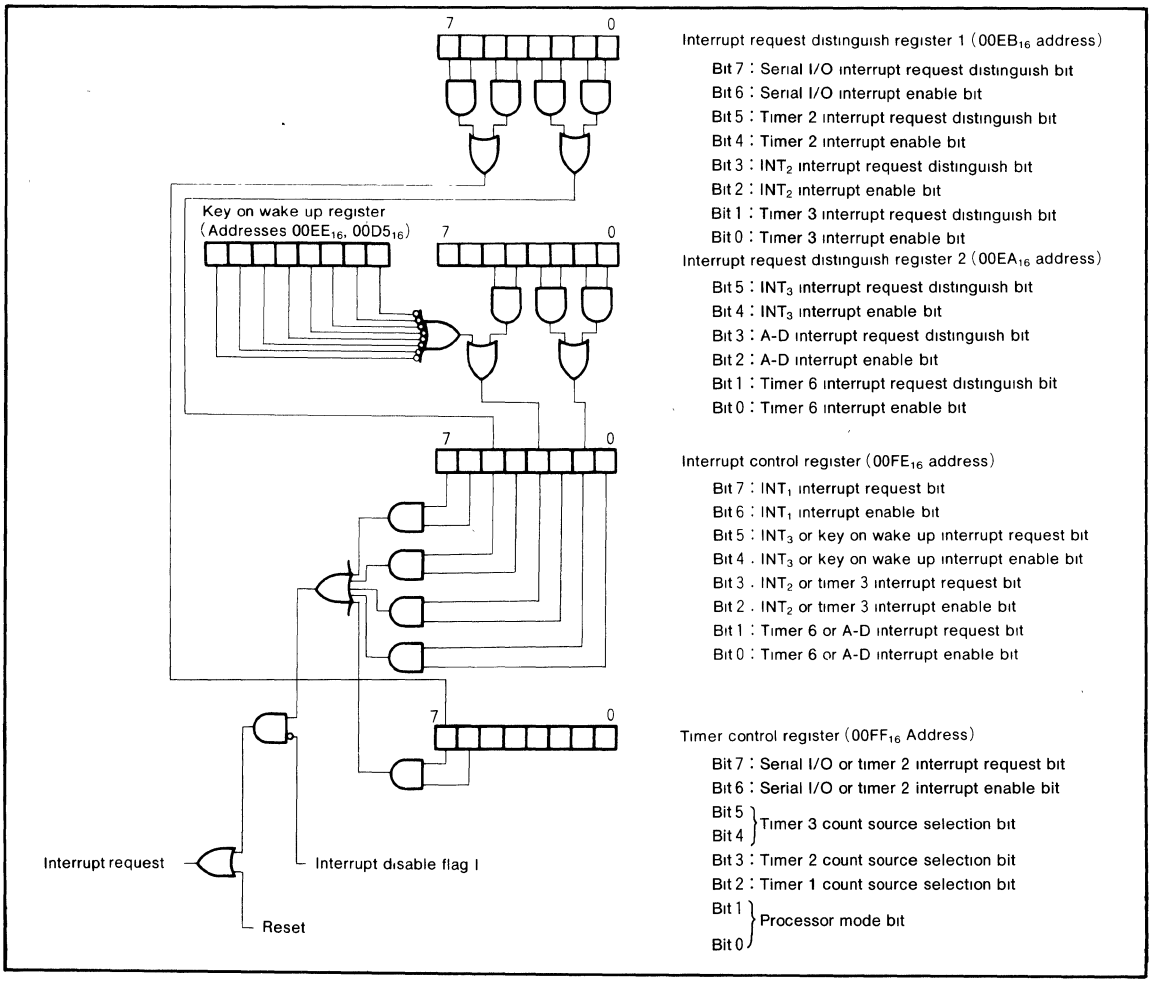

Fig. 3 Interrupt control

TIMER

The M37413M4HXXXFP has six timers; timer 1, timer 2, timer 3, timer 4, timer 5 and timer 6.

A block diagram of timer1 through 6 is shown in Figure 4.

The count source for timer 1 through 3 can be selected by using bit 2, 3, 4 and 5 of the timer control register (address $00FF_{16}$), as shown in Figure 5. All of the timers are down count timers and have 8-bit latches. When a timer reaches "0" and the next count pulse is input to a timer, the contents of the reload latch are loaded into the timer. The division ratio of the timer is $1/(n+1)$, where n is the contents of timer latch.

Timer 2, 3 and 6 has interrupt generating functions. The timer interrupt request bit which is in the interrupt distinguish register 1 or 2 (located at addresses $00EB_{16}$ and $00EA_{16}$ respectively) is set at the next count pulse after the timer reaches "0" (see interrupt section).

The starting and stopping of timer1 is controlled by bit 7 of the interrupt distinguish register 2, timer 3 by bit 6 of the interrupt distinguish register 2 and timer 4 by bit 3 of timer 4, 5 and 6 mode register ($00F8_{16}$ address). If the corresponding bit is "0". the timer starts counting, and the corresponding bit is "1", the timer stops. The timer4 overflow signal divided by 2 can be outputed from port $P3_3$ by setting the bit 4 of the serial I/O mode register ($00F6_{16}$ address) to "1".

Timer 5 and 6 work as timer mode, event counter mode and PWM mode by changing the contents of bit 5 and bit 6 of the timer 4, 5 and 6 mode register.

(1) Timer Mode

This mode is the 16-bit timer, and the count source is $\phi/4$. When the bit 6 of PWM control register ($00F3_{16}$ address) is "1", the timer6 overflow singnal divided by 2 is output from CNT_2 pin (common with $P5_2$).

(2) Event Counter Mode

The count source is input from the CNT_2 pin. The count decremented each time the input goes from "L" to "H".

(3) PWM Mode

As shown in Figure 6, the output wave is controlled by the contents of the timer latch of timer 5 and 6.

PWM output can choose among PWM0, PWM1, PWM2 and PWM3 by bit 0, bit 1, bit 2 and bit 3 of PWM control register.

When the count value of all timers, from timer 1 to timer 6, are read, be careful not to change the input source.

When the count source is inputed from the external pin, the minimum pluse width should be $8\mu s$.

After a STP instruction is executed, timer 2, timer 1, and the clock (ϕ divided by 4) are connected in series (regardless of the status of bit 2 through 5 of the timer control register). This state is canceled if timer2 interrupt request bit is set to "1", or if the system is reset. Before the STP instruction is executed, bit 7 of the interrupt request distinguish register2 (timer1 count stop bit), bit 5 of the interrupt request distinguish register1 and bit 6 and bit 7 of the timer control register must be set to "0". And also bit 4 of the interrupt request distinguish register1 must be set to "1". For more details on the STP instruction, refer to the oscillation circuit section.

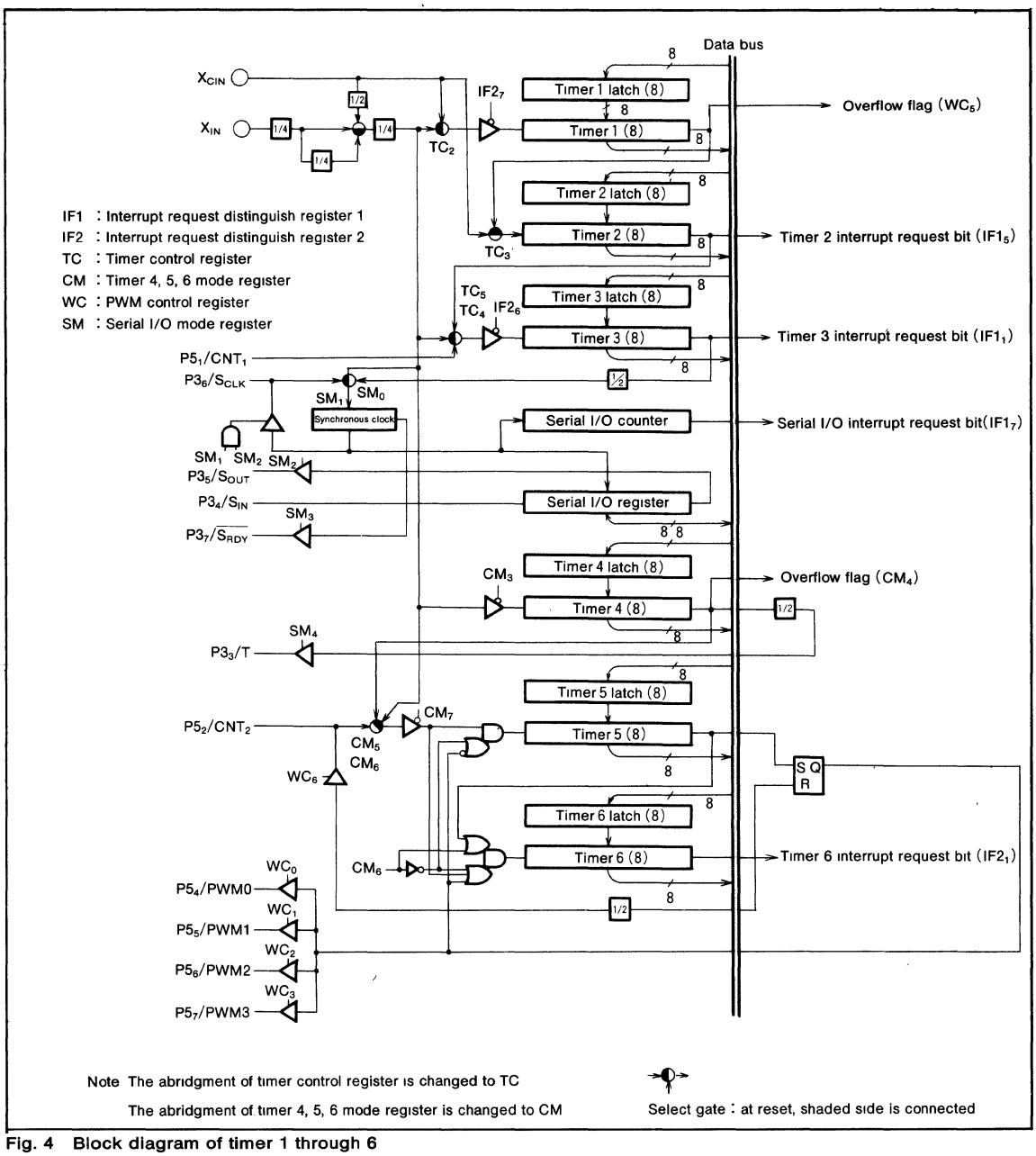

Fig. 4 Block diagram of timer 1 through 6

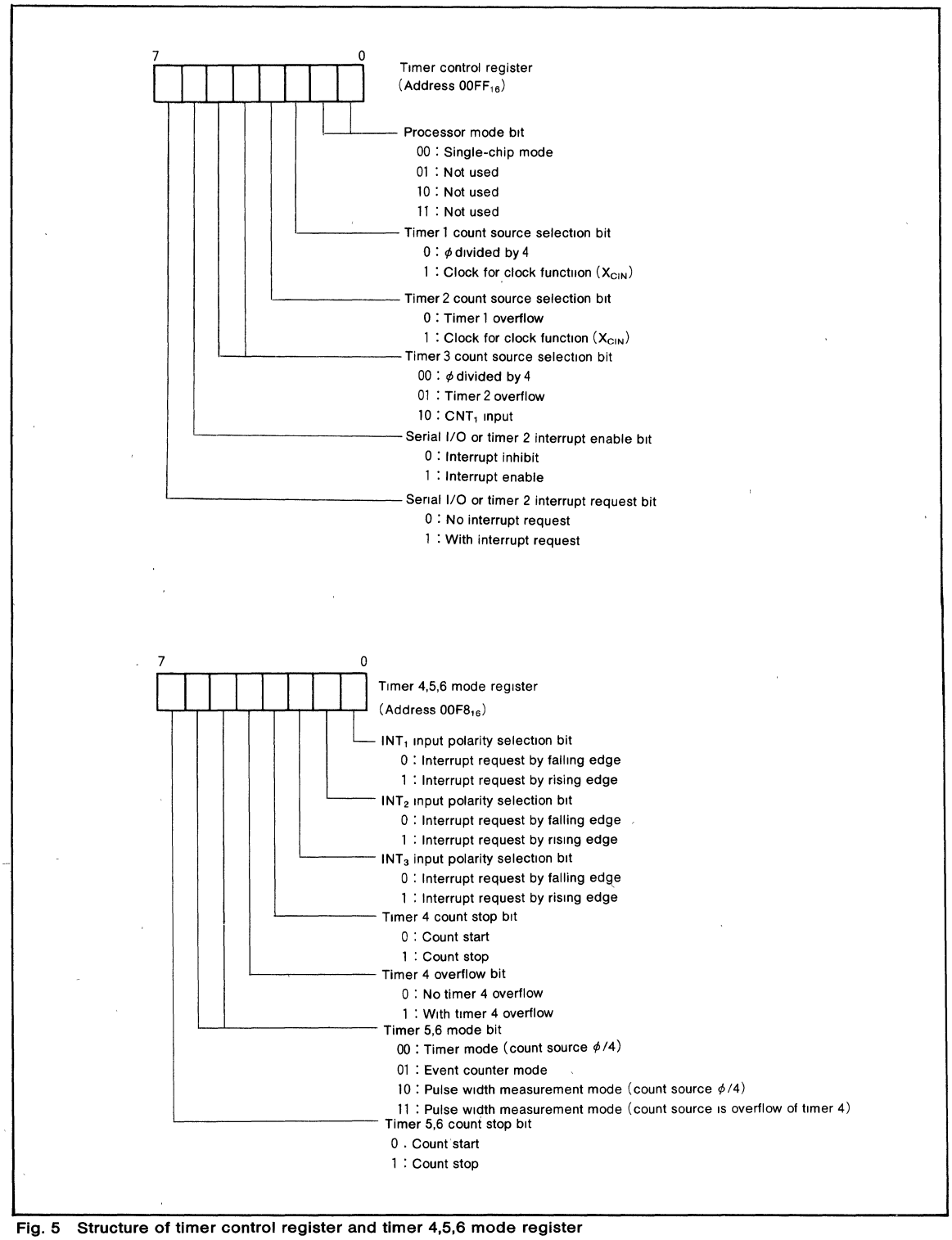

Fig. 5 Structure of timer control register and timer 4,5,6 mode register

PWM

M37413M4HXXXFP has a pulse width modulated (PWM) output control circuit connecting with timer5 and timer6.

Figure 5 shows the structure of timer 4,5,6 mode register, Figure 6 shows the PWM rectangular wave form and Figure 7 shows the structure of PWM control register.

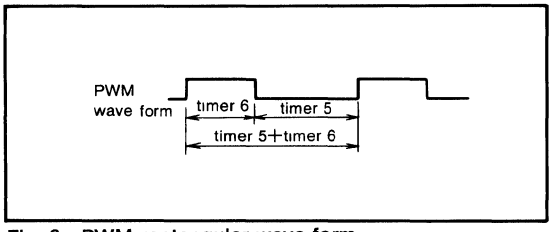

Fig. 6 PWM rectangular wave form

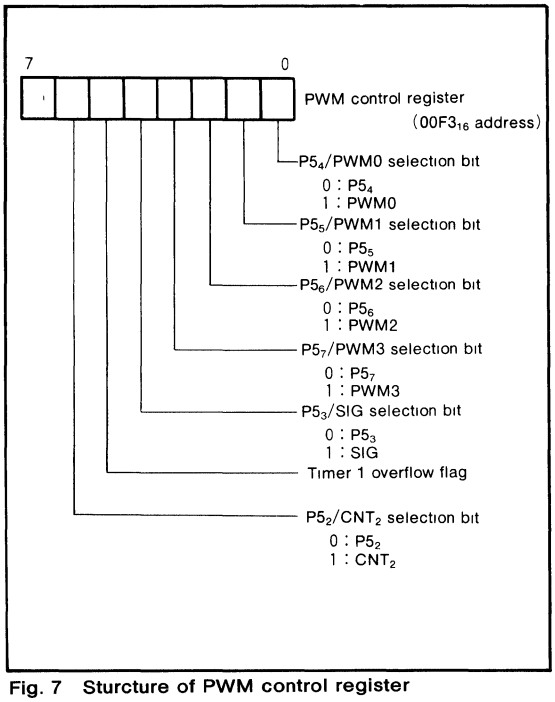

Fig. 7 Sturcture of PWM control register

SERIAL I/O

The block diagram of serial I/O is shown in Figure 9. In the serial I/O mode the receive ready signal ($\overline{S_{RDY}}$), synchronous input/output clock (CLK). and the serial I/O (S_{OUT}, S_{IN}) pins are used as $P3_7$, $P3_6$, $P3_5$, and $P3_4$, respectively.

FUNCTION OF SERIAL I/O MODE REGISTER

The serial I/O mode register (address $00F6_{16}$) is an 8-bit register. Bit 1 and 0 of this register is used to select a synchronous clock source. When these bits are [00] or [01], an external clock from $P3_6$ is selected. When these bits are [10], the overflow signal divided by two from timer 3 becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], the internal clock ϕ divided by 4 becomes the clock.

Bits 2 and 3 decide whether parts of P3 will be used as a serial I/O or not. When bit 2 is "1", $P3_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P3_6$. If the external synchronous clock is selected, the clock is input to $P3_6$. And $P3_5$ will be a serial output and $P3_4$ will be a serial input. To use $P3_4$ as a serial input, set the directional register bit which corresponds to $P3_4$, to "0". For more information on the directional register, refer to the I/O pin section.

To use the serial I/O, bit 2 needs to be set to "1", if it is "0" $P3_6$ will function as a normal I/O. Bit 3 determines if $P3_7$ is used as an output pin for the receive data ready signal (bit 3="1", $\overline{S_{RDY}}$) or used as a nomal I/O pin (bit 3="0").

OPERATION OF SERIAL I/O

The function of serial I/O differs depending on the clock source; external clock or internal clock.

Internal Clock — The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register. After the falling edge of write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M37413M4HXXXFP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 when data is stored in the serial I/O register. At each falling edge of the transfer clock, serial data is output to $P3_5$. During the rising edge of this clock, data can be input from $P3_4$ and the data in the serial I/O register will be shifted 1 bit. Data is output starting with the LSB. After the transfer clock has counted 8 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interrupt request bit will be set.

External Clock — If an external clock is used, the interrupt request bit will be set after the transfer clock has counted 8 times but the transfer clock will not stop. Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%. When the external clock is chosen, the $P3_6$ pin must be held at "H" level while the serial I/O is not used.

Timing diagrams are shown in Figure 10, and connection between two M37413M4HXXXFP's are shown in Figure 11.

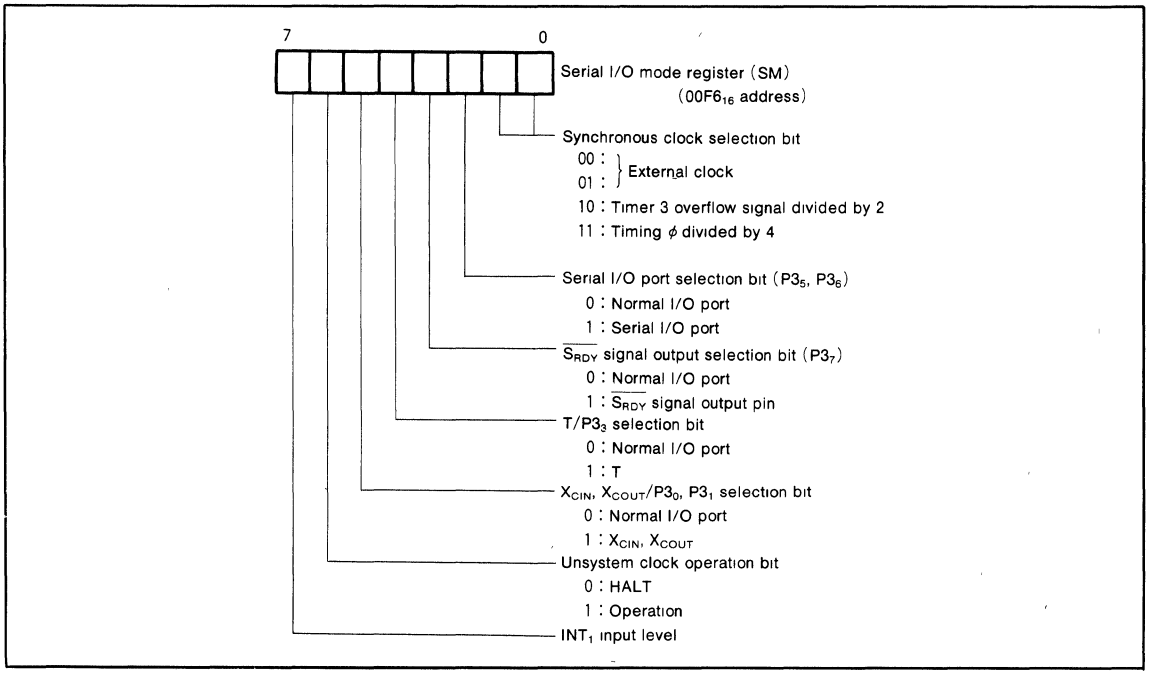

Fig. 8 Structure of serial I/O mode register

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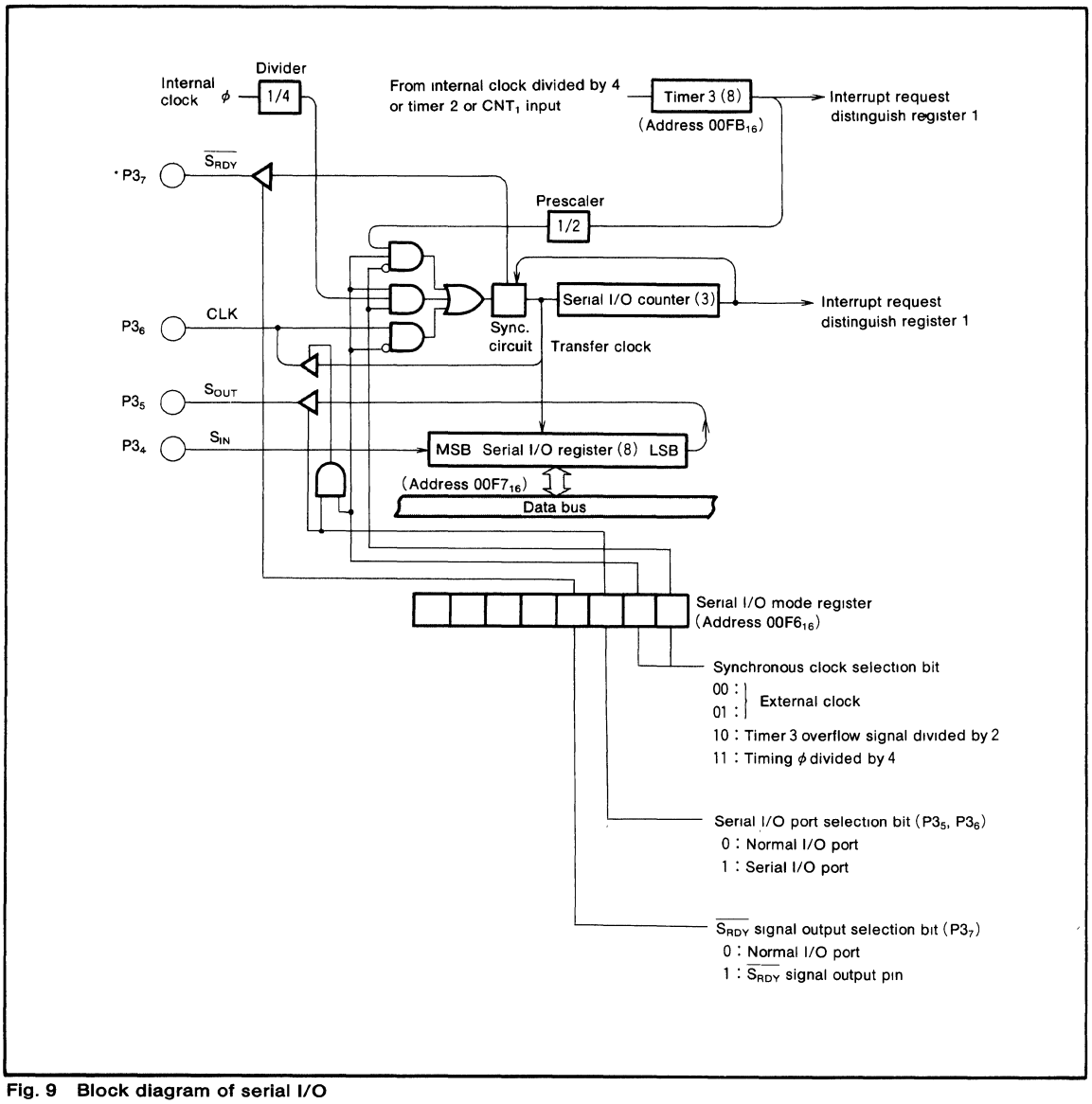


Fig. 9 Block diagram of serial I/O

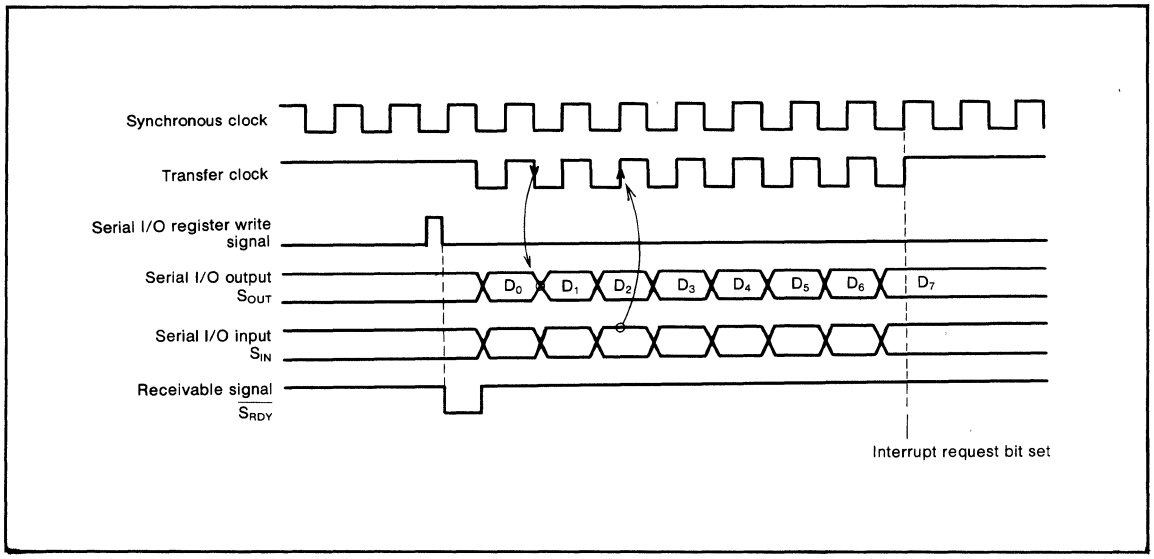


Fig. 10 Serial I/O timing

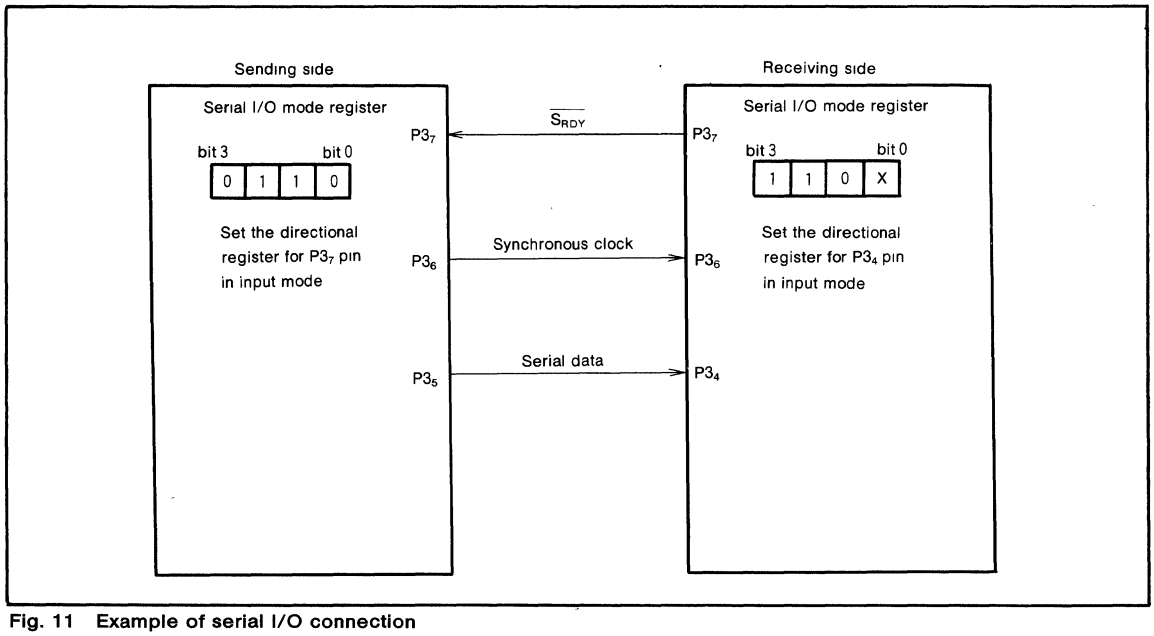


Fig. 11 Example of serial I/O connection

A-D CONVERTER

The A-D converter circuit is shown in Figure 12. One of the eight analog input ports of the A-D converter (IN_0~IN_7) are selected by bits 0, 1 and 2 of the A-D control register. The IN pins, not to use as analog input, uses as input port.

Bit 0, 1 and 2, and corresponding to analog input pin is shown in Figure 13. A-D conversion is accomplished by first selecting bit 3 and 4 of the A-D control register (address $00F2_{16}$) for the source of V_{REF}. And also the analog input pin is chosen by the analog input select bit of the A-D control register. A-D conversion starts by writing a dummy data to the A-D register or changing the input level from SIG pin "H" to "L". When A-D conversion is finished, an interrupt is generated. After A-D interrupt is accepted, the result of A-D conversion can be read from the A-D register.

Note that the A-D conversion must to be started to convert after the reference voltage reaches stable level.

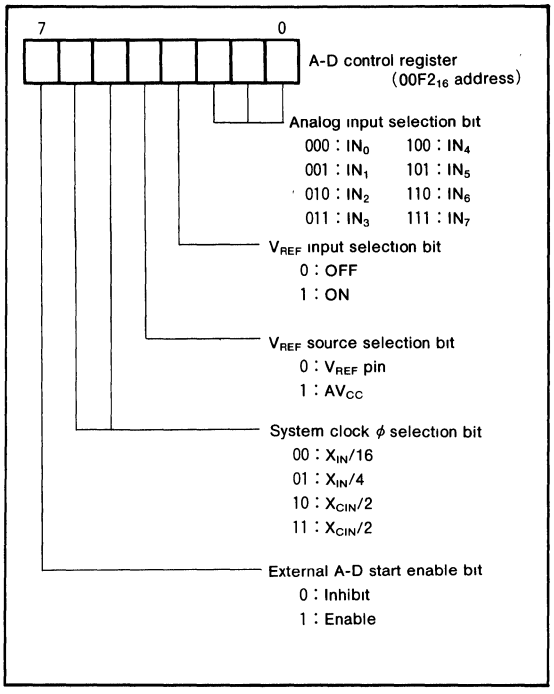


Fig. 13 Structure of segment control register

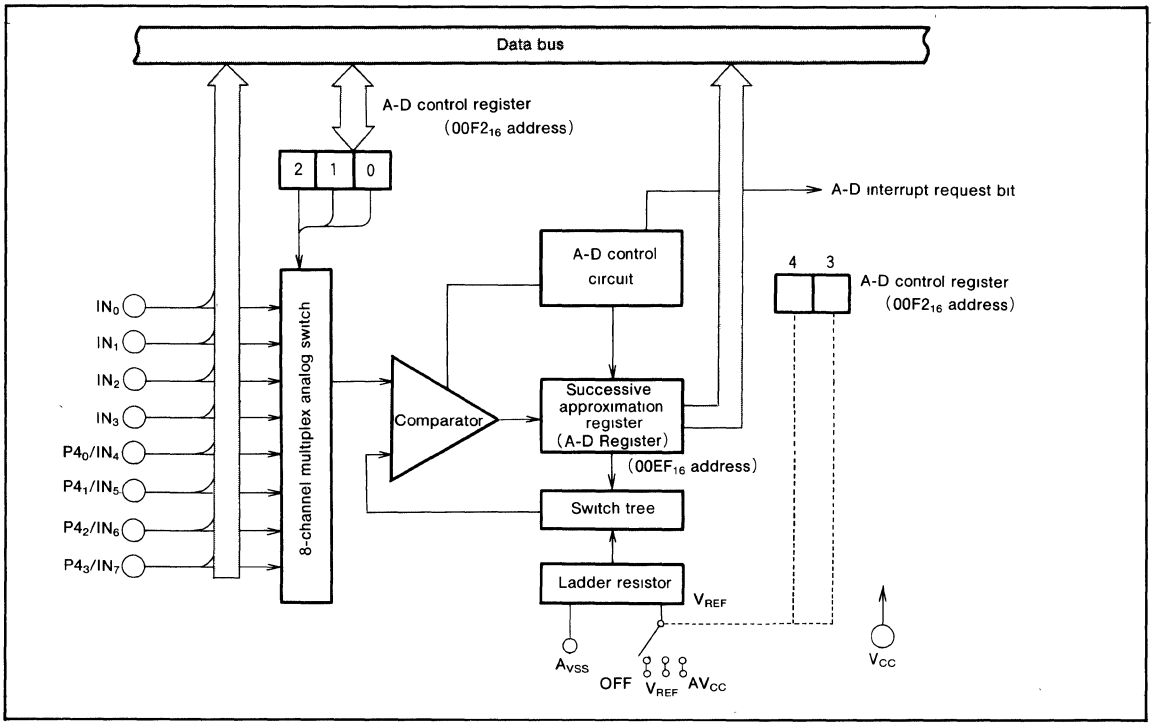


Fig. 12 A-D converter circuit

KEY ON WAKE UP

"Key on wake up" is one way of returning from a power down state caused by the STP or WIT instruction.

When the key on wake up option of port P2 and port P7 are designated and key on wake up interrupt enable bit (IC_4) is set to "1", if the key on wake up option pin of port P2, P7 have "L" level applied, key on wake up interrupt is generated and the microcomputer is returned to the normal operating state.

When the bit 4 of PWM control register (address $00F3_{16}$) is set to "1", the pulse shown in Figure 14 is outputed from $P5_3$ pin.

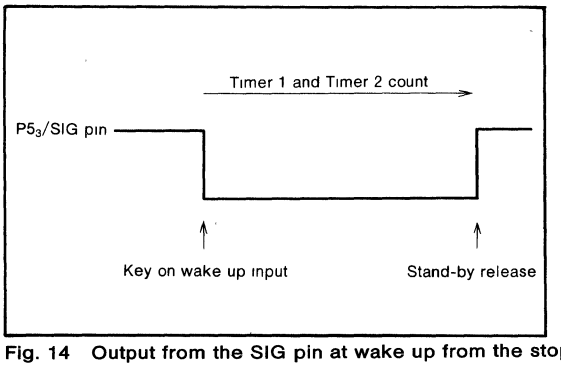
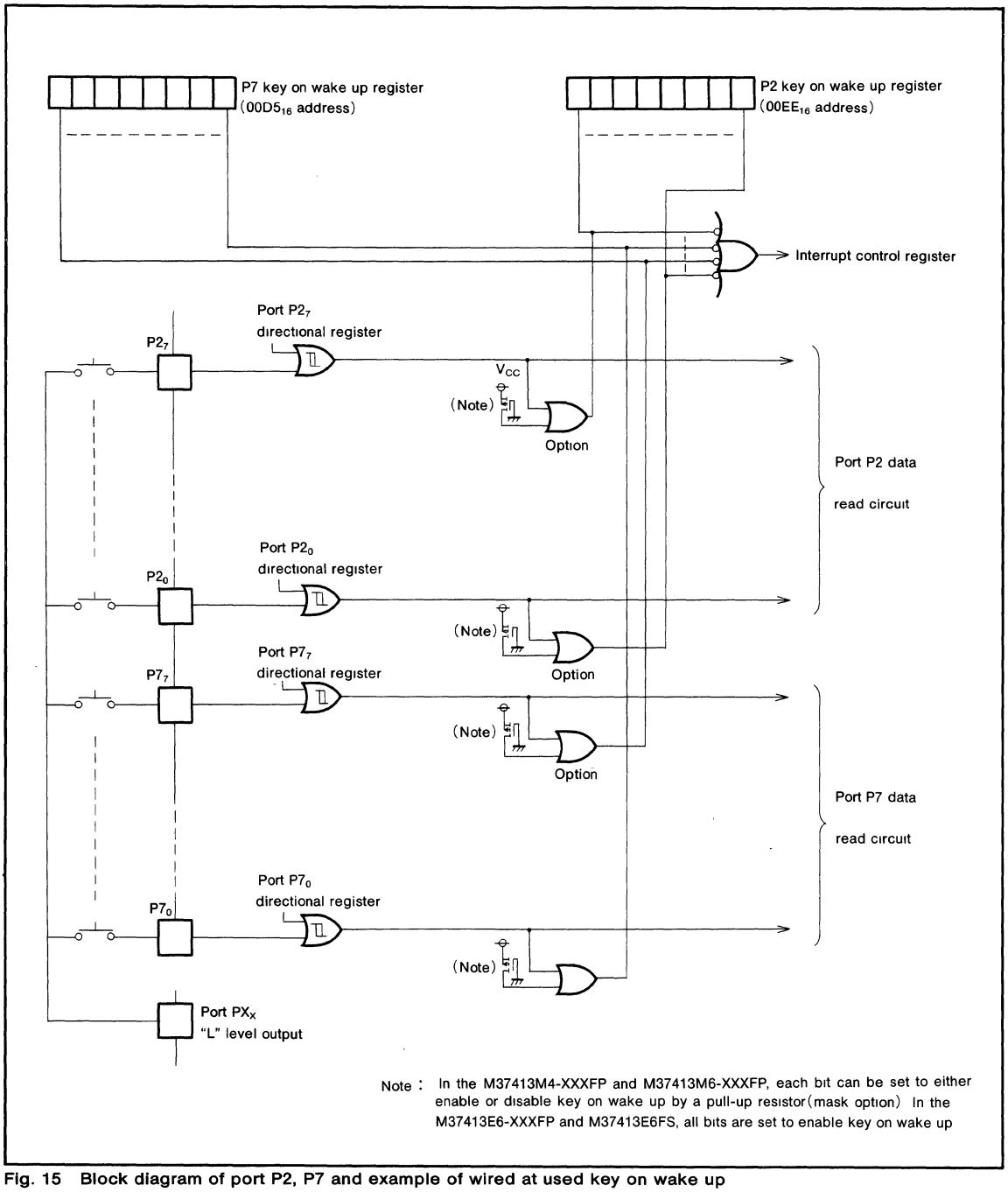


Fig. 14 Output from the SIG pin at wake up from the stop state

As shown in Figure 15, if the key matrix of active "L" to input port P2, P7 are constructed, the microcomputer is returned to normal operating state by the key push. Refer to the section of interrupt how to use the key on wake up function. In order to enter the power down state generated by the STP or WIT instruction at the interrupt disable flag (I) is "0" and IC_4 is "1", the input designated as key on wake up by option in port P2, P7 must be all "H".



Note : In the M37413M4-XXXFP and M37413M6-XXXFP, each bit can be set to either enable or disable key on wake up by a pull-up resistor (mask option) In the M37413E6-XXXFP and M37413E6FS, all bits are set to enable key on wake up

Fig. 15 Block diagram of port P2, P7 and example of wired at used key on wake up

RESET CIRCUIT

The M37413M4HXXXFP is reset according to the sequence shown in Figure 18. It starts the program from the address formed by using the content of address $3FFF_{16}$ as the high order address and the content of the address $3FFE_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for no less than 16 μs while the power voltage is between 4 and 5.5V and the crystal oscillator oscillation is stable and then returned to "H" level.

The internal initializations following reset are as shown in Figure 16 regardless of the status before reset (including stop mode or wait mode).

An example of the reset circuit is shown in Figure 17.

When the power on reset is used, the $\overline{RESET}$ pin must be input "H" after the oscillation of X_{IN}-X_{OUT} becomes stable.

		Address	
(1)	Port P0 directional register	(D0) ($E1_{16}$)···	00_{16}
(2)	Port P1 directional register	(D1) ($E3_{16}$) ·	00_{16}
(3)	Port P2 directional register	(D2) ($E5_{16}$)···	00_{16}
(4)	Port P3 directional register	(D3) ($E9_{16}$)···	00_{16}
(5)	Port P5 directional register	(D5) (ED_{16})···	00_{16}
(6)	Port P6 directional register	(D6) ($D1_{16}$)···	00_{16}
(7)	Port P7 directional register	(D7) ($D3_{16}$)···	00_{16}
(8)	Interrupt request distinguish register 1	(IF1) (EB_{16})···	00_{16}
(9)	Interrupt request distinguish register 2	(IF2) (EA_{16})···	00_{16}
(10)	PWM control register	(WC) ($F3_{16}$)···	0 0 0 0 0 0 0
(11)	Serial I/O mode register	(SM) ($F6_{16}$)···	— 0 0 0 0 0 0 0
(12)	Timer 4, 5, 6 mode register	(CM) ($F8_{16}$)···	00_{16}
(13)	Interrupt control register	(IM) (FE_{16})···	00_{16}
(14)	Timer control register	(TC) (FF_{16})···	00_{16}
(15)	A-D control register	(AC) ($F2_{16}$)···	0 0 0 0 0 — — —
(16)	Processor status register		— — — — — 1 — —
(17)	Program counter	(PC_H)···	Contens of address $3FFF_{16}$
		(PC_L)···	Contens of address $3FFE_{16}$

Note : Since the contents of both registers other than those listed above (including timers, A-D control register and the serial I/O register) and the RAM are undefined at reset, it is necessary to set initial values

Fig. 16 Internal state of microcomputer at reset

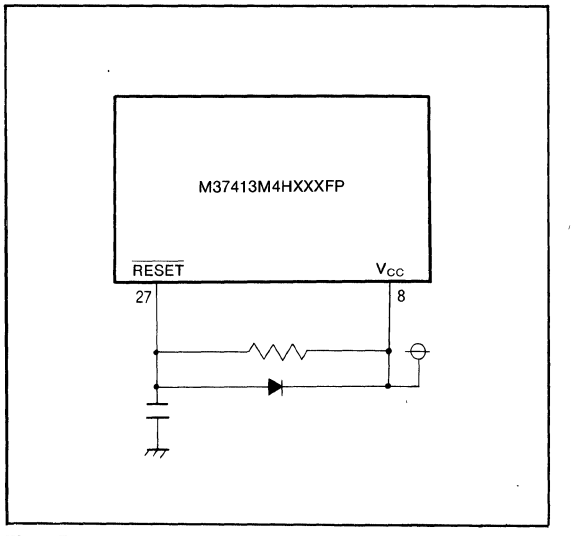


Fig. 17 Example of reset circuit

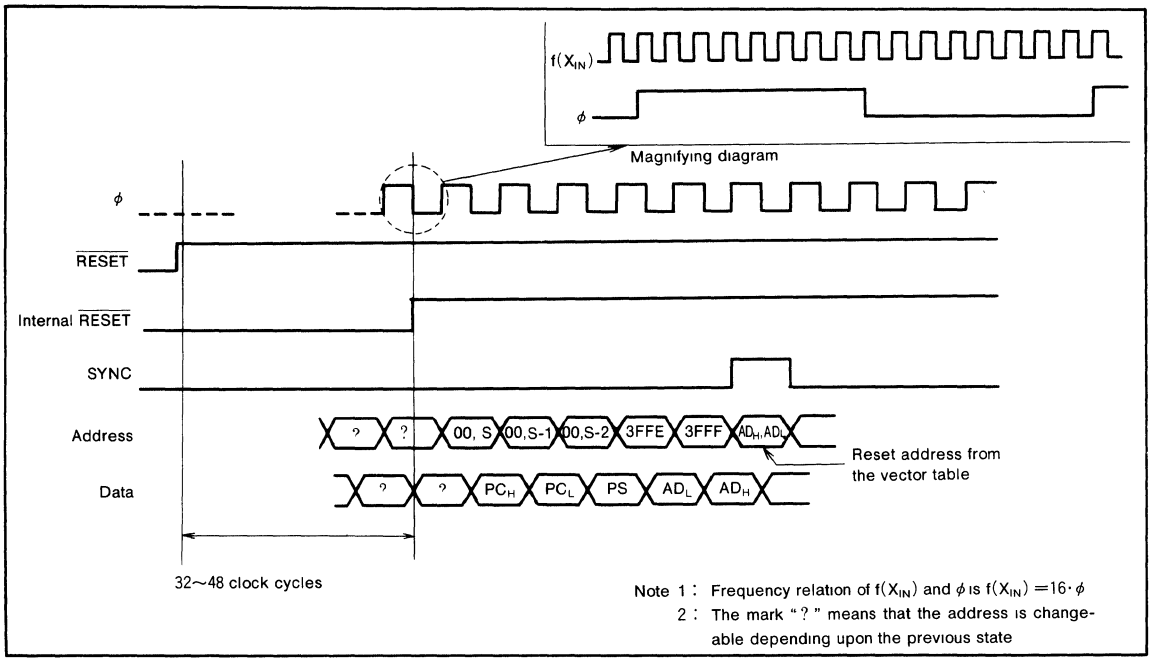


Fig. 18 Timing diagram at reset

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS outputs and pull-up transistor options available. As shown in Figure 1, P0 can be accessed as memory through zero page address $00E0_{16}$. Port P0's directional register allows each bit to be programmed individually as input or output. The directional register (zero page address $00E1_{16}$) can be programmed as input with "0", or as output with "1". When in the output mode, the data to be output is latched to the port register and output. When data is read from the output port, the output pin level is not read, only the latched data of the port register is read. Therefore, a previously output value can be read correctly even though the output voltage level has been shifted up or down. Port pins set as input are in the high impedance state so the signal level can be read. When data is written into the input port, the data is latched only to the output register and the pin still remains in the high impedance state. This port can be built in a pull-up resistor option when it is used as a input port.

(2) Port P1

Port P1 has the same function as P0 but the output structure is N-ch open drain. This port can be built in a pull-up resistor option when it is used as a input port.

(3) Port P2

Port P2 has the same function as P0. The output structure is CMOS outputs. This port can be built in a pull-up resistor option when it is used as a input port. Following the execution of STP or WIT instruction, key matrix with port P2 can be used to generate the interrupt to bring the microcomputer back in its normal state. The pin to be used as the key on wake up must be with key on wake up option and its value in directional register must be "0".

(4) Port P3

Port P3 has the same functions P0 except that part of P3 is common with the serial I/O, output of timer4, clock oscillation of timer clock and interrupt input.

The output is N-channel open drain. This port can be built in a pull-up resistor option. When $P3_0$ and $P3_1$ pins are used for X_{CIN} input, pull-up is inhibited.

(5) Port P4

Port P4 is an 8-bit input port. $P4_0 \sim P4_3$ are in common with the $IN_4 \sim IN_7$. This port can be built in a pull-up resistor option when it is used as a input port.

(6) Port P5

Port P5 has the same functions as P0 except that part of P5 is common with the counter input pin, SIG pin, and PWM output pin. The output is N-channel open drain output. This port can be built in a pull-up resistor option.

(7) Port P6

Port P6 has the same function as P0 but the output structure is N-ch open drain. This port can be built in a pull-up resistor option.

(8) Port P7

Port P7 has the same function as P0. The output structure is CMOS outputs. This port can be built in a pull-up resistor option when it is used as a input port. Following the execution of STP or WIT instruction, key matrix with port P7 can be used to generate the interrupt to bring the microcomputer back in its normal state. The pin to be used as the key on wake up must be with key on wake up option and its value in directional register must be "0".

(9) Analog input($IN_0 \sim IN_7$)

This is a port for an analog input of A-D converter. $IN_4 \sim IN_7$ are in common with the $P4_0 \sim P4_3$.

(10) INT_1

The INT_1 pin is an interrupt input pin. The INT_1 interrupt request bit (bit 7 of address $00FE_{16}$) is set to "1" when the input level of this pin changes from "H" to "L" (or "L" to "H"). This input level is read in the bit 7 of serial I/O mode register (address $00F6_{16}$).

(11) $INT_2(P3_2/INT_2)$

The INT_2 pin is an interrupt input pin common with $P3_2$. When $P3_2$'s directional register is set for input ("0"), this pin can be used as an interrupt input. The INT_2 interrupt request bit (bit 3 of address $00EB_{16}$) is automatically set to "1" when the input level of this pin changes from "H" to "L" (or from "L" to "H").

(12) $INT_3(P5_0/INT_3)$

The INT_3 pin is an interrupt input pin common with $P5_0$. The other functions are the same as INT_2.

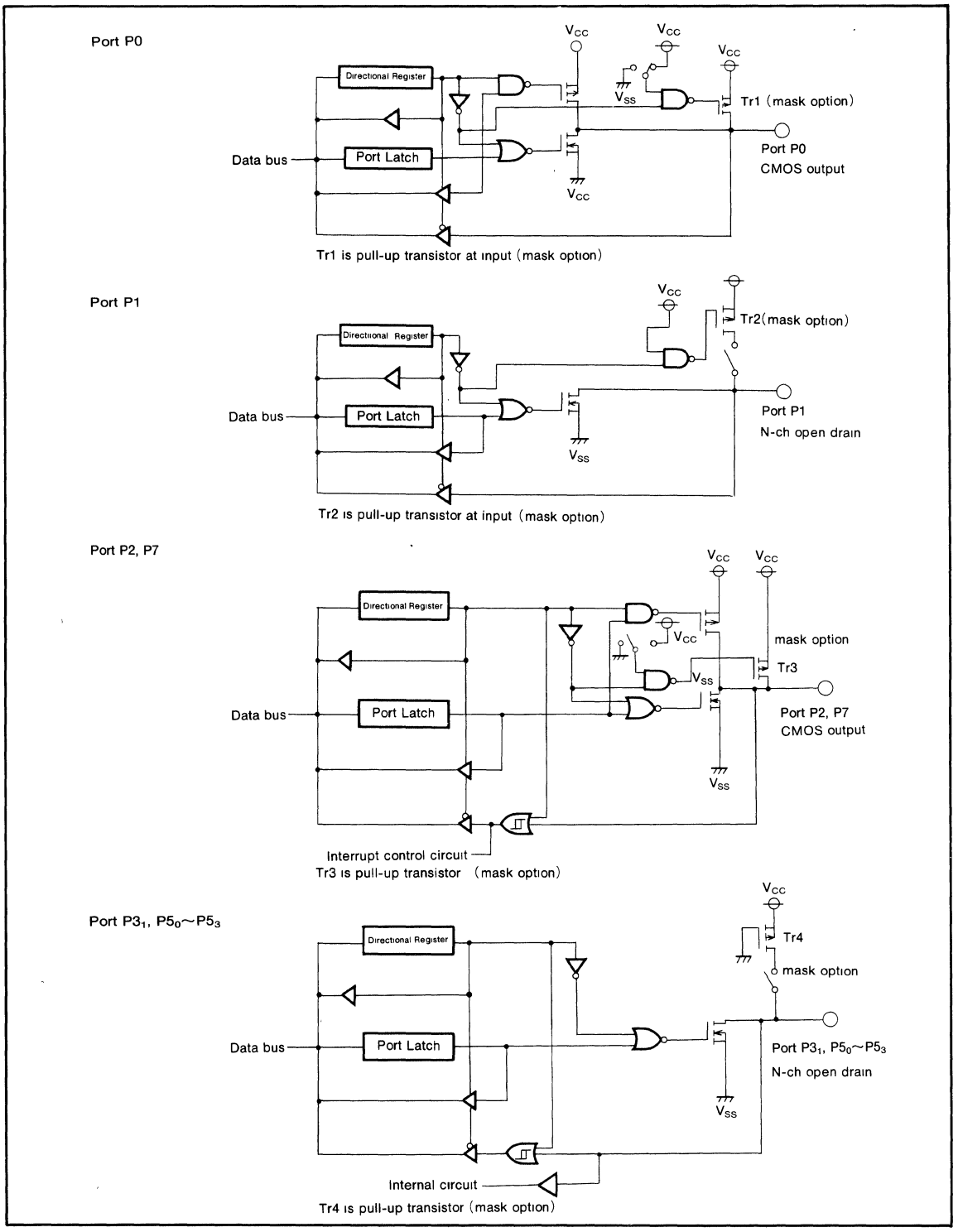


Fig. 19 Block diagram of ports P0~P2, $P3_1$, $P5_0$~$P5_3$ and P7

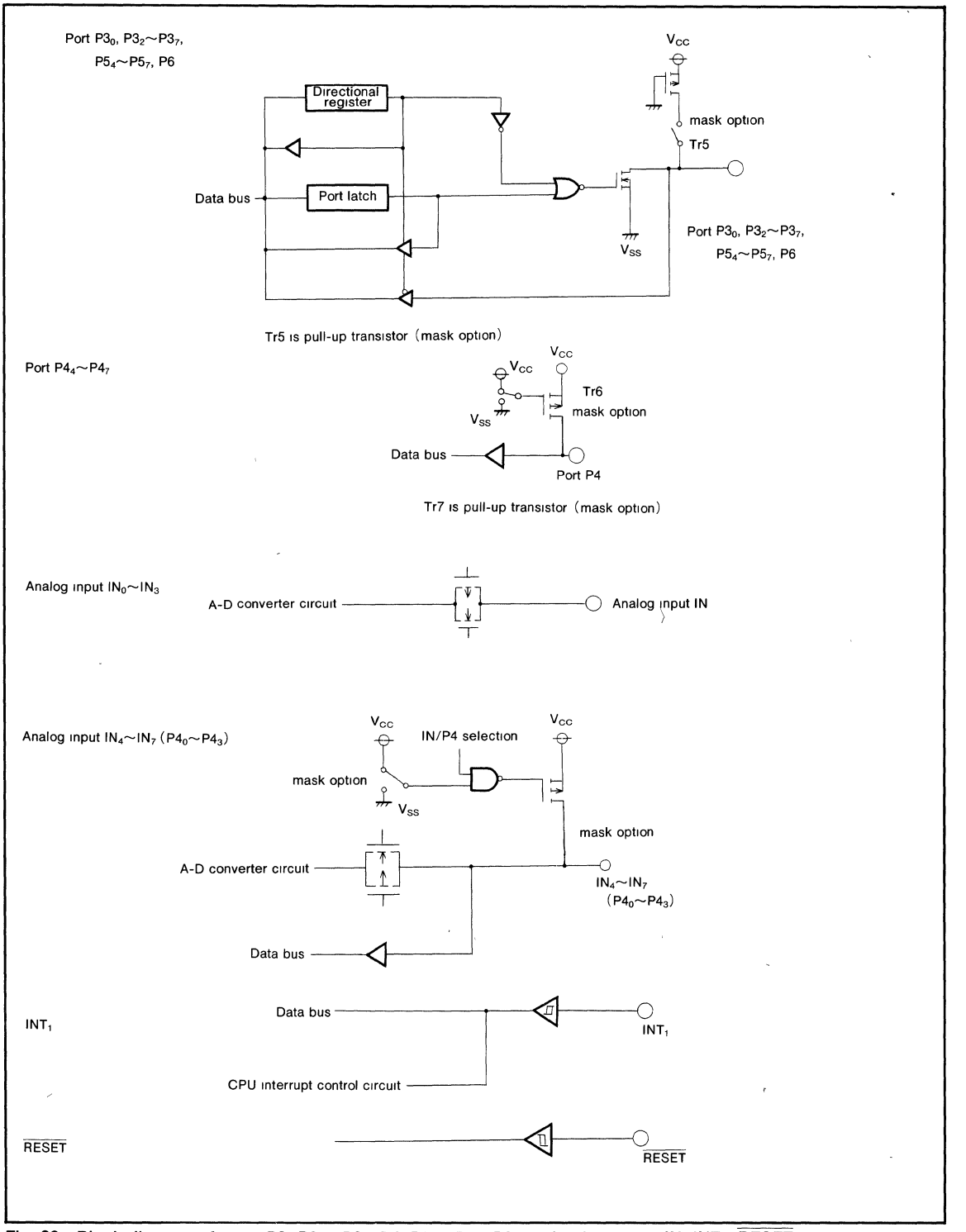


Fig. 20 Block diagram of ports $P3_0$,$P3_2$~$P3_7$, P4, $P5_4$~$P5_7$, P6, analog input port IN, INT_1, $\overline{RESET}$

CLOCK GENERATING CIRCUIT

The M37413M4HXXXFP has two internal clock generators. Figure 23 shows a block diagram of the clock generator. Normally, the frequency applied to the clock input pin X_{IN} divided by 16 is used as the internal clock (timing output) ϕ. The internal clock ϕ can be changed to 1/4 the frequency applied to the clock input pin X_{IN} or 1/2 the frequency applied to the clock input pin X_{CIN}. When $X_{CIN}/2$ is selected, the pull-up option to $P3_0$, $P3_1$ pins are inhibited.

These signals can be changed via bit5 (AC_5) and bit6 (AC_6) of the A-D control register. When AC_6 and AC_5 are [00], the internal clock is chosen $X_{IN}/16$. When they are [01], the internal clock is chosen $X_{IN}/4$. When they are [10] and [11], the internal clock is $X_{CIN}/2$. The one of clock X_{IN} and clock X_{CIN}, isn't in use for the internal clock (none system clock), stops when the bit6 (SM_6) of serial I/O mode register is "0". In order to restart the clock as the internal clock, SM_6 is set to "1" and wait until the oscillation becomes stability by the software then the internal clock is chosen AC_6 and AC_5.

The M37413M4HXXXFP has two low power consumption modes, stop and wait. The microcomputer enters a stop mode when the STP instruction is executed. The oscillator (both X_{IN} clock and X_{CIN} clock) stops with the internal clock ϕ held at "H" level. In this case timer 1 and timer 2 are forcibly connected and $\phi/4$ is selected as timer 1 input. When restarting oscillation, the internal clock ϕ is held "H" until timer 2 overflows and is not supplied to the CPU. So set the suitable value for timer 1 and timer 2 in order to enable the oscillator to stabilize. Before executing the STP instruction, the timer 1 count stop bit ($IF2_7$) must be set to supply ("0"), timer 2 interrupt enable bit ($IF1_4$) of interrupt request distinguish register 1 must be set to enable ("1"), timer 2 interrupt request bit ($IF1_5$) of interrupt request distinguish register 1 must be set to "0". And serial I/O or timer 2 interrupt enable bit (TC_6) and serial I/O or timer 2 interrupt request bit (TC_7) of timer control register must be set to "0".

Oscillation is restarted (reset stop mode) when an external interrupt is received. The interrupt enable bit of the interrupt used to reset the stop mode must be set to "1".

The microcomputer enters a wait mode when WIT instruction is executed. The internal clock ϕ stops at "H" level, but the oscillator does not stop. ϕ is re-supplied (wait mode reset) when it receives an external interrupt or internal timer interrupt. Instructions can be executed immediately because the oscillator is not stopped. The interrupt enable bit of the interrupt used to reset the wait mode must be set to "1" before executing the WIT instruction.

When the interrupt is accepted and after the interrupt subroutine is executed, the next instruction to STP or WIT is executed. It is possible to cancel stop and wait mode by reset. In this case, the execution is started from the address is set to reset vector.

Transition of states for the system clock is shown in Figure 24. The change order of the internal clock is shown in Figure 24.

When STP instruction is executed from the states of A, B, C, D and E, it will be the same state as H (stop state). If the interrupt is executed in stop state, it will return the state before STP instruction is executed.

Figure 21 shows a circuit example using a ceramic (or crystal) oscillator. Use the manufacturer's recommended values for constants such as capacitance which is unique for each oscillator. There are slight differences in constants in the M37413M4HXXXFP and M37413M6HXXXFP. If using one of these chips in applications such as high-precision clocks, ask the resonator manufacturer for measurements of these constants. When using an external clock signal, input from the $X_{IN}(X_{CIN})$ pin and leave the $X_{OUT}(X_{COUT})$ pin open. A circuit example is shown in Figure 22.

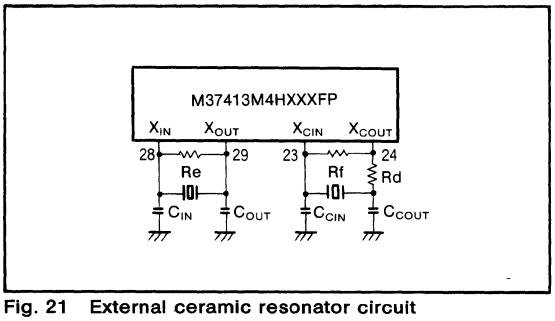


Fig. 21 External ceramic resonator circuit

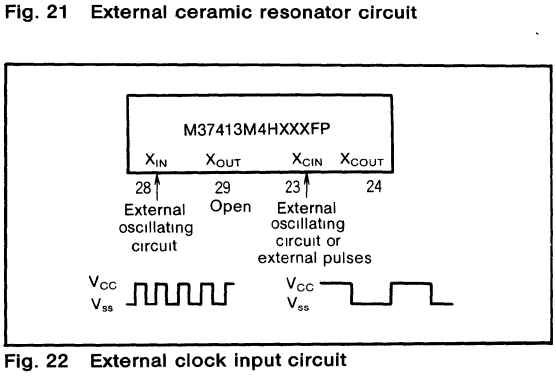


Fig. 22 External clock input circuit

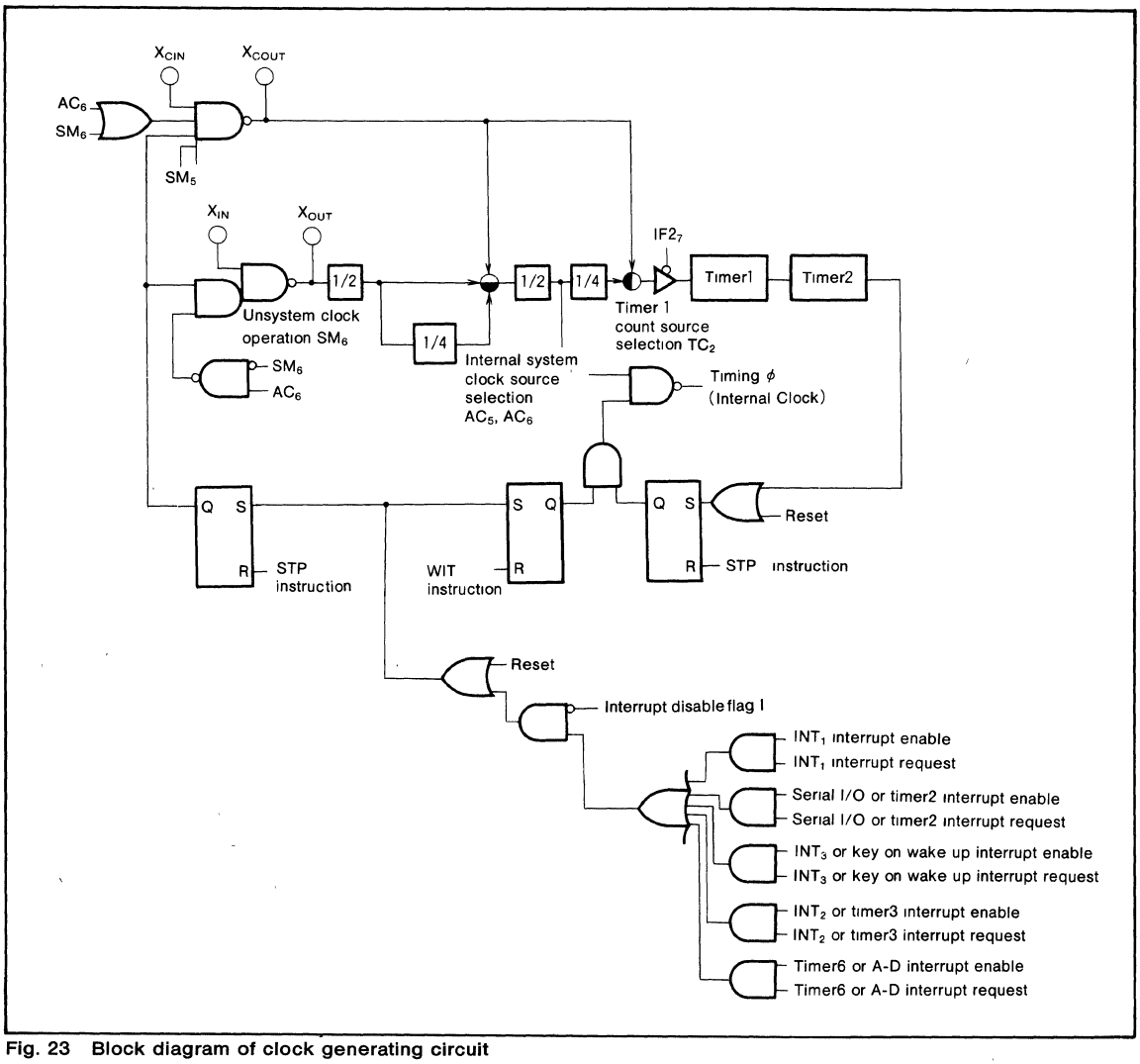
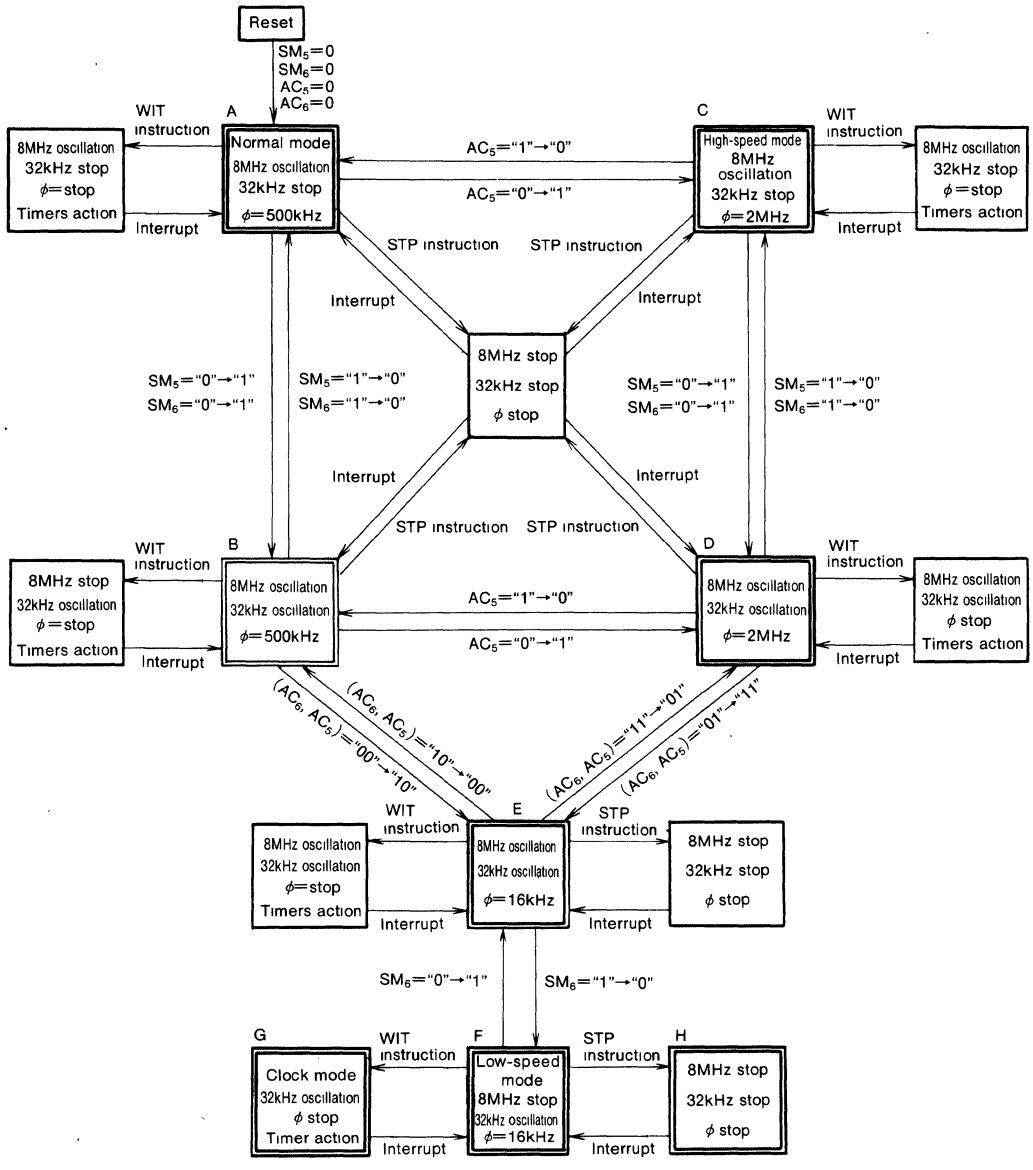


Fig. 23 Block diagram of clock generating circuit



The case of example clock X_{IN}=8MHz, clock X_{CIN}=32kHz. ϕ is internal clock

Note : When a stop mode is canceled, wait time occurs automatically by connection of timers 1 and 2 This time can be set by program.

When SM_6=1, unsystem clock is operated and system clock is changed, wait time necessary by program until oscillation becomes stable

Return to the normal mode once in case changed to the low-speed mode from the normal mode

Also return to the high-speed mode once in case changed to the low-speed mode from the high-speed mode

Transitions B→E→D and D→E→B are not possible

Fig. 24 Transition of states for the system clock

PROGRAMMING NOTES

(1) The frequency ratio of the timer is $1/(n+1)$.

(2) The count value of timers 1, 2, 3, 4 can be read at an arbitrary timing when the timing ϕ divided by 4 or timer overflow is input to these timers. If X_{CIN} or CNT_1 input is input to these timers, the value of timer 1, 2, 3, 4 must be read only when the input of timers is not changing or the timer count is stopped.
Also the count value of timers 5, 6 which are used in the event counter mode must be read when the external input is at the "L" level. When timers 5, 6 are used in the timer mode, the count value of these timers cannot be read.

(3) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(4) ① After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
② In decimal mode, the negative (N), overflow (V) and zero (Z) flags are invalidated.

(5) A NOP instruction must be used after the exection of a PLP instruction.

(6) ① The timer 1 and timer 2 must be set the necessary value immediately before the execution of a STP instruction.
Also the following conditions must be satisfied:
- Timer 1 count stop bit is set to "0"
- Timer 2 interrupt enable bit is set to "1"
- Timer 2 interrupt request bit is set to "0"
- Serial I/O or timer 2 interrupt enable bit is set to "0"
- Serial I/O or timer 2 interrupt request bit is set to "0"

② To restart oscillation when it is stopped by STP instruction or unsystem clock operation bit, wait for a specified time which is needed for the oscillator to stabilize.
③ Connect I/O ports which are in input mode to V_{CC} or GND to get less power supply current after executing STP or WIT instruction. Connect $P5_0 \sim P5_3$ to V_{CC} or GND also in output mode.

(7) Some instructions can be used to write contents of the interrupt request distinguish register 1, 2. If the SEB or CLB instruction or a set of instruction that acts as the SEB or CLB instruction (for instance, LDA TC+SEB 7, A +STA TC) is used, an interrupt request which is input during execution of these instructions may be cleared. Therefore, these instructions should be used only when there is no problem even if such an interrupt request is cleared. Usually, the LDM instruction or STA instruction is used. Especially to write contents of the interrupt request distinguish register 1, 2, use the flow chart as shown in Figure 26.

(8) After switching the serial I/O transfer clock, initialize the serial I/O counter (write to address $00F7_{16}$).

(9) To use an external clock as the serial I/O transfer clock, initialize the serial I/O counter when the external clock is "H" level.

(10) To use the $P3_0$ and $P3_1$ pins as the I/O pins of the clock for clock function, do not use the pull-up resistors by option.

(11) If using the A-D converter, supply power to the V_{REF} pin(set bits 3 and 4 of address $00F2_{16}$), and make sure that the voltage of the V_{REF} pin has stabilized before activating the A-D conversion.

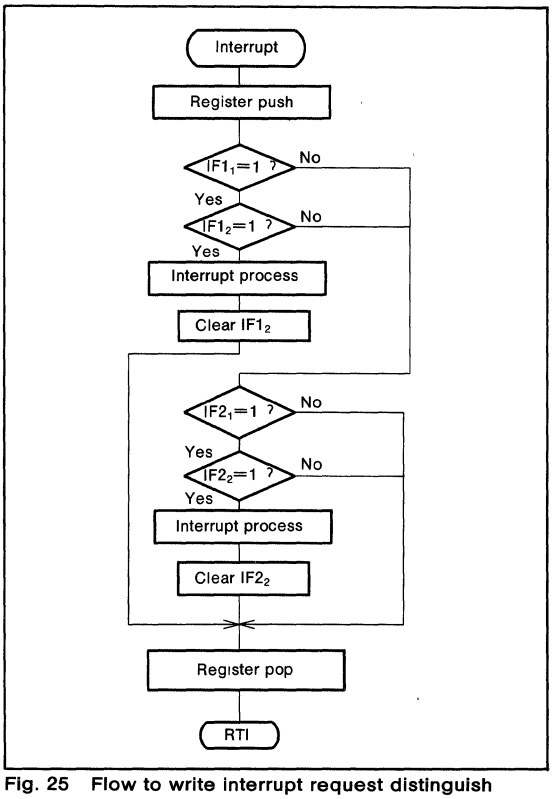


Fig. 25 Flow to write interrupt request distinguish registers

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

(1) mask ROM confirmation form

(2) mark specification form

(3) ROM data ..... EPROM 3sets

Write the following option on the mask ROM confirmation form

- Port P0 pull-up transistor bit
- Port P1 pull-up transistor bit
- Port P2 pull-up transistor bit
- Port P3 pull-up transistor bit
- Port P4 pull-up transistor bit
- Port P5 pull-up transistor bit
- Port P6 pull-up transistor bit
- Port P7 pull-up transistor bit
- Port P2 key on wake up
- Port P7 key on wake up

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.3∼7	V
AV_{CC}	Analog supply voltage	V_{CC}=AV_{CC}	−0.3∼7	V
V_I	Input voltage $P0_0$∼$P0_7$, $P2_0$∼$P2_7$, $P3_0$, $P3_1$, $P4_0$∼$P4_3$, $P7_0$∼$P7_7$, IN_0∼IN_7, V_{REF}, X_{IN}		−0.3∼V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3∼7	V
V_I	Input voltage INT_1, $\overline{RESET}$, $P1_0$∼$P1_7$, $P3_2$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (Note 1)		−0.3∼10	V
V_O	Output voltage $P0_0$∼$P0_7$, $P2_0$∼$P2_7$, $P3_0$, $P3_1$, $P7_0$∼$P7_7$, X_{OUT}		−0.3∼V_{CC}+0.3	V
V_O	Output voltage $P1_0$∼$P1_7$, $P3_2$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (Note 1)		−0.3∼10	V
P_d	Power dissipation	T_a = 25℃	300	mW
Topr	Operating temperature		−20∼75	℃
Tstg	Storage temperature		−40∼125	℃

Note 1 : When these ports are built in a pull-up resistor option, the value is −0.3∼V_{CC}+0.3V

RECOMMENDED OPERATING CONDITIONS (V_{CC}=2.5∼5.5V, V_{SS}=0V, T_a=−20∼75℃, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ	Max	
V_{CC}	Supply voltage (Note 1)	f(X_{IN})= 8 MHz High-speed mode	4.5		5.5	V
		f(X_{IN})= 8 MHz Normal mode or f(X_{IN})= 2 MHz High-speed mode (Note 2)	2.5		5.5	
V_{SS}	Supply voltage			0		V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$, $P3_0$, $P3_1$, $P4_0$∼$P4_7$, CNV_{SS} (Note 3)		0.7V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P2_0$∼$P2_7$		0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P1_0$∼$P1_7$, $P5_1$∼$P5_7$, $P6_0$∼$P6_7$, S_{IN}		0.7V_{CC}		10	V
V_{IH}	"H" input voltage $P3_2$∼$P3_7$, $P5_0$, INT_1, INT_2, INT_3, CNT_1, CNT_2, SIG, CLK		0.8V_{CC}		10	V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, X_{CIN}		0.85V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$, $P3_1$, $P4_0$∼$P4_3$, $P5_1$∼$P5_7$, $P6_0$∼$P6_7$, S_{IN}		0		0.25V_{CC}	V
V_{IL}	"L" input voltage $P2_0$∼$P2_7$, $P3_2$∼$P3_7$, $P5_0$, INT_1, INT_2, INT_3, CNT_1, CNT_2, SIG, CLK		0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$, X_{IN}, X_{CIN}		0		0.15V_{CC}	V
I_{OH}	"H" output current $P0_0$∼$P0_7$, $P2_0$∼$P2_7$, $P7_0$∼$P7_7$, X_{OUT} (Note 4)				−1	mA
I_{OL}	"L" output current $P0_0$∼$P0_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, $P7_0$∼$P7_7$, X_{OUT} (Note 5)				1	mA
I_{OL}	"L" output current $P1_0$∼$P1_7$ (Note 6)	V_{CC}=3V			10	mA
		V_{CC}=5V			20	
f(X_{IN})	Clock oscillating frequency		0.2		8.2	MHz
f(X_{CIN})	Clock oscillating frequency for clock function		30		50	kHz

Note 1 : When only maintaining the RAM data, minimum value of V_{CC} is 2V
2 : We say the high-speed mode, when the system clock is chosen X_{IN}/4, and the low-speed mode, when the system clock is chosen X_{IN}/16
3 : When $P3_1$ is used as X_{CIN}, V_{IH} and V_{IL} of $P3_1$ is 0.85V_{CC}≦V_{IH}≦V_{CC} and 0≦V_{IL}≦0.15V_{CC}
4 : The total $I_{OH(peak)}$ of port P0, P2, P7 and X_{OUT} is less than 35mA.
5 : The total $I_{OH(peak)}$ of port P0, P2, P3, P5, P6 and P7 is less than 32mA
6 : The total peak current of I_{OL} of port P1 is less than 80mA and the average current of total I_{OL} of port P1 is less than 40mA

ELECTRICAL CHARACTERICS (V_{SS}= 0 V, T_a=−20~75℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max.	
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P2_0$~$P2_7$, $P7_0$~$P7_7$		V_{CC}=5V, I_{OH}=−0.5mA	4			V
			V_{CC}=3V, I_{OH}=−0.3mA	2.4			
V_{OH}	"H" output voltage X_{OUT}		V_{CC}=5V, I_{OH}=−0.3mA	4			V
			V_{CC}=3V, I_{OH}=−0.1mA	2.4			
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $P7_0$~$P7_7$, T, S_{OUT}, CLK, $\overline{S_{RDY}}$, SIG, PWM0~PWM3		V_{CC}=5V, I_{OL}=1mA			1	V
			V_{CC}=3V, I_{OL}=0.5mA			0.6	
V_{OL}	"L" output voltage $P1_0$~$P1_7$		V_{CC}=5V, I_{OL}=20mA			2	V
			V_{CC}=3V, I_{OL}=10mA			1.5	
V_{OL}	"L" output voltage X_{OUT}		V_{CC}=5V, I_{OL}=0.3mA			1	V
			V_{CC}=3V, I_{OL}=0.1mA			0.6	
V_{T+}−V_{T-}	Hysteresis INT_1, INT_2, INT_3, CLK, CNT_1, CNT_2, SIG, S_{IN}, $P2_0$~$P2_7$, $P7_0$~$P7_7$, X_{CIN}		V_{CC}=5V		0.7		V
			V_{CC}=3V		0.5		
V_{T+}−V_{T-}	Hysteresis $\overline{RESET}$		V_{CC}=5V		2		V
			V_{CC}=3V		1.2		
V_{T+}−V_{T-}	Hysteresis X_{IN}		V_{CC}=5V		0.5		V
			V_{CC}=3V		0.35		
I_{IL}	"L" input current [$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $P7_0$~$P7_7$] without pull-up T_f, (Note 1), INT_1, $\overline{RESET}$, X_{IN}		V_{CC}=5V V_I=0V			−5	μA
			V_{CC}=3V V_I=0V			−3	
I_{IH}	"H" input current $P0_0$~$P0_7$, $P2_0$~$P2_7$, $P3_0$, $P3_1$, $P4_0$~$P4_7$, $P7_0$~$P7_7$, X_{IN}, X_{CIN}, CNV_{SS}		V_{CC}=5V V_I=5V			5	μA
			V_{CC}=3V V_I=3V			3	
I_{IH}	"H" input current [$P1_0$~$P1_7$, $P3_0$~$P3_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$] without pull-up T_f, INT_1, $\overline{RESET}$		V_I=10V			10	μA
R_{PL}	Pull-up T_f $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_3$, $P5_0$~$P5_7$		V_{CC}=5V, V_I=0V	12	25	50	kΩ
			V_{CC}=3V, V_I=0V	25	50	100	
I_{CC}	Supply current (Note 2)	at operation	f(X_{IN})=8MHz High-speed mode V_{CC}=5V		6	12	mA
			f(X_{IN})=8MHz Normal mode V_{CC}=3V		1	4	
			f(X_{CIN})=32kHz, V_{CC}=3V		18	36	μA
		at wait mode	f(X_{IN})=8MHz, V_{CC}=3V			3	mA
			f(X_{CIN})=32kHz, V_{CC}=3V		4	12	μA
		at stop mode	T_a=25℃		0.1	1.0	
			T_a=75℃			6.0	
V_{RAM}	RAM retention voltage			2		5.5	V

Note 1 : Also the same when each port is used as INT_2, INT_3, CNT_1, CNT_2, SIG, S_{IN} and X_{CIN}, respectively.
2 : I/O ports or input ports are connected to V_{CC} Output ports are opened

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=AV_{SS}= 0 V, T_a=25℃, f(X_{IN})= 8 MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max.	
——	Resolution				8	bits
——	Non-linearity error	V_{CC}=V_{REF}=5.12V			±2	LSB
		V_{CC}=V_{REF}=3.072V			±2	
——	Differential non-linearity	V_{CC}=V_{REF}=5.12V			±0.9	LSB
		V_{CC}=V_{REF}=3.072V			±0.9	
V_{OT}	Zero transition error	V_{CC}=V_{REF}=5.12V			2	LSB
		V_{CC}=V_{REF}=3.072V			2	
V_{FST}	Full-scale transition error	V_{CC}=V_{REF}=5.12V			6	LSB
		V_{CC}=V_{REF}=3.072V			10	
T_C	Conversion time	V_{CC}=2.5~5.5V High-speed mode		200/f(X_{IN})		μs
		V_{CC}=2.5~5.5V Normal mode		800/f(X_{IN})		
I_{REF}	Reference input current	V_{REF}=5V		1.0	2.5	mA
		V_{REF}=3V		0.5	1.5	
I_{IN}	Analog port input current	V_{IN}=0~V_{CC}		1	10	μA
V_{IN}	Analog input voltage	V_{CC}=2.5~5.5V	AV_{SS}		V_{CC}	V
V_{REF}	Reference input voltage		2.5		V_{CC}	V