

# MITSUBISHI MICROCOMPUTERS M37414E5-XXXFP

PROM VERSION of M37414M5-XXXFP

## DESCRIPTION

The M37414E5-XXXFP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 72-pin plastic molded QFP. The features of this chip are similar to those of the M37414M5-XXXFP except that this chip has a 10240 bytes PROM built in. This single-chip microcomputer is useful for home electrical appliances and consumer appliance controllers.

In addition to its simple instruction set, the PROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming. Since general purpose PROM writers can be used for the built-in PROM, this chip is suitable for small quantity production runs.

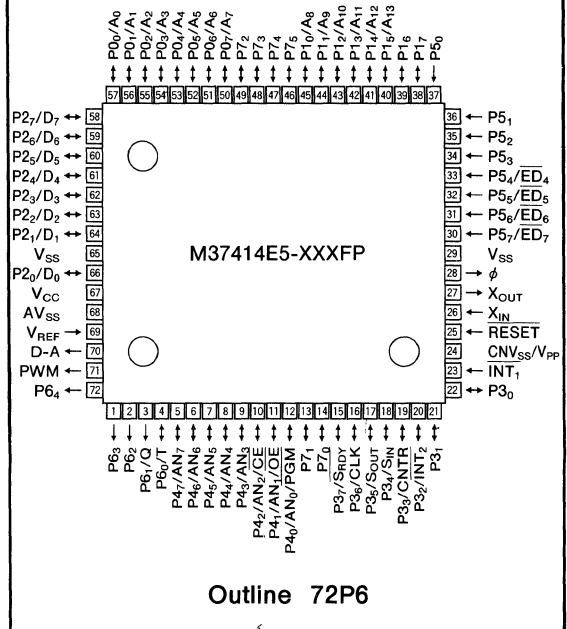
## FEATURES

- Number of basic instructions ..... 69
- Memory size ROM ..... 10240 bytes  
RAM ..... 160 bytes
- Instruction execution time  
..... 2 $\mu$ s (minimum instructions at 4MHz frequency)
- Single power supply ..... 5V $\pm$ 5%
- Power dissipation  
normal operation mode (at 4MHz frequency) ..... 15mW
- Subroutine nesting ..... 80 levels (Max.)
- Interrupt ..... 7 types, 5 vectors
- 8-bit timer ..... 4
- Programmable I/O ports  
(Ports P0, P1, P2, P3, P4, P7) ..... 46
- Input port (Port P5) ..... 8
- Output port (Port P6) ..... 5
- Serial I/O (8-bit) ..... 1
- A-D converter (8-bit resolution) ..... 8 channels
- D-A converter (5-bit resolution) ..... 1 channels
- 8-bit PWM function
- Watchdog timer
- PROM (equivalent to the M5L27128)  
program voltage ..... 21V

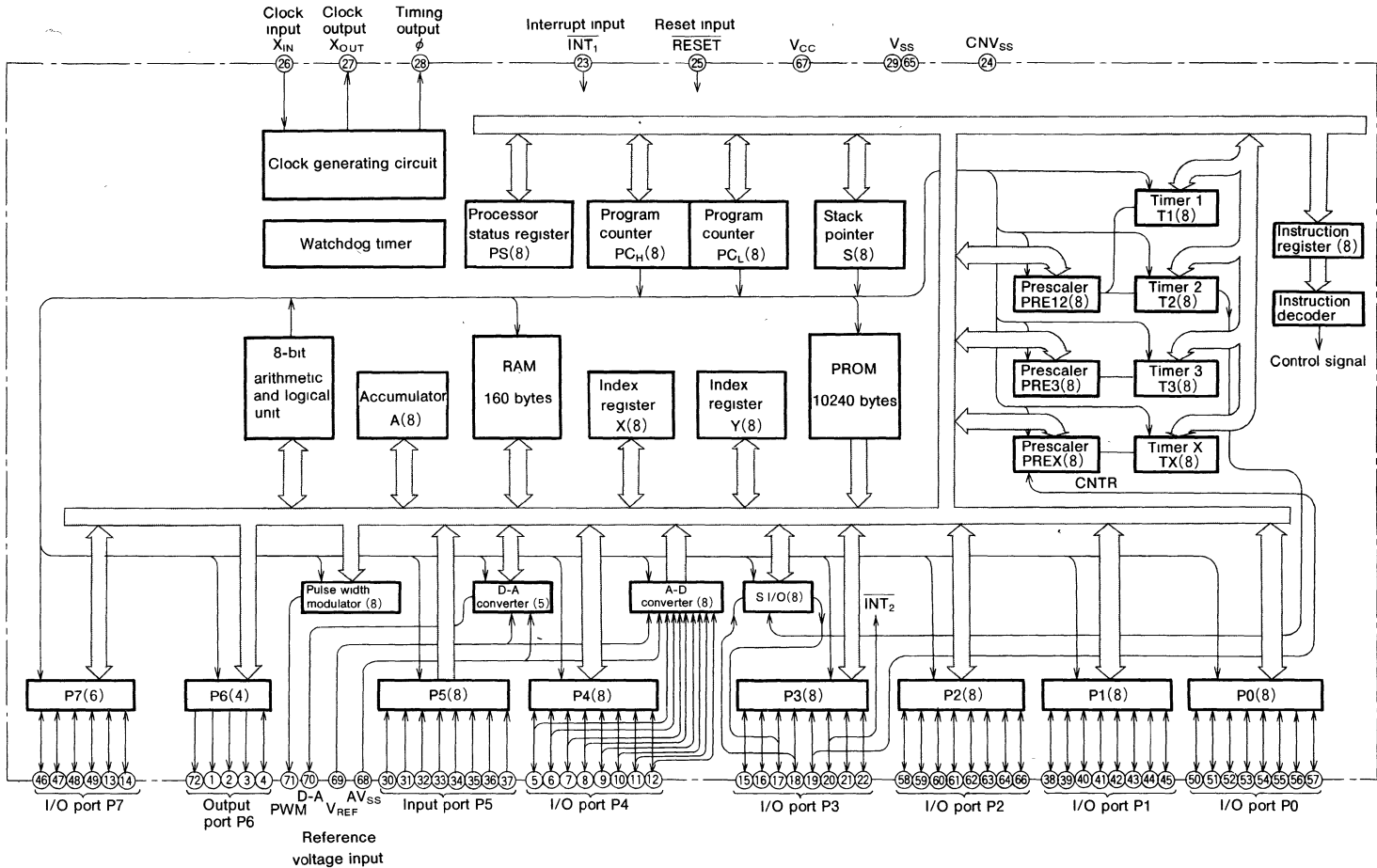
## APPLICATION

Office automation equipment  
VTR, Tuner, Audio-visual equipment

## PIN CONFIGURATION (TOP VIEW)



# M37414E5-XXXFP BLOCK DIAGRAM



PROM VERSION of M37414MS-XXXFP

MITSUBISHI MICROCOMPUTERS  
M37414E5-XXXFP

**FUNCTIONS OF M37414E5-XXXFP**

Parameter		Functions
Number of basic instructions		69
Instruction execution time		2 $\mu$ s (minimum instructions, at 4MHz frequency)
Clock frequency		4MHz
Memory Size	PROM	10240bytes (Note 1)
	RAM	160bytes
Input/Output port	INT <sub>1</sub>	Input 1-bitX1
	P0, P1, P2, P3, P4	I/O 8-bitX5 (a part of P3 is in common with serial I/O, timer I/O, and interrupt input)
	P5	Input 8-bitX1
	P6	Output 5-bitX1 (a part of P6 is in common with external trigger output pin)
	P7	I/O 6-bitX1
Serial I/O		8-bitX1
Timers		8-bit prescalerX3+8-bit timerX4
A-D converter		8-bitX1 (8 channels)
D-A converter		5-bitX1
Pulse width modulator		8-bitX1
Watchdog timer		15-bitX1
Subroutine nesting		80 levels (max)
Interrupt		Two external interrupts, three internal timer interrupts
Clock generating circuit		built-in (ceramic or quartz crystal oscillator)
Supply voltage		5V $\pm$ 5%
Power dissipation	at high-speed operation	15mW (at 4MHz frequency)
Input/Output characteristics	Input/Output voltage	12V (Ports P3, P4, P5, P6, P7 <sub>0</sub> , P7 <sub>1</sub> , INT <sub>1</sub> )
	Output current	5mA (Ports P0, P1, P2, P3, P4, P7)
Memory expansion		Possible
Operating temperature range		-10~70°C
Device structure		CMOS silicon gate process
Package		72-pin plastic molded QFP

Note 1 : The PROM programing voltage is 21V (equivalent to the M5L27128)

PROM VERSION of M37414M5-XXXFP

PIN DESCRIPTION

Pin	Mode	Name	Input/ Output	Functions
V <sub>CC</sub> , V <sub>SS</sub>	Single-chip /EPROM	Power supply		Supply 5V±5% to V <sub>CC</sub> and 0V to V <sub>SS</sub>
CNV <sub>SS</sub>	Single-chip	CNV <sub>SS</sub> input	Input	Connect to 0V
	EPROM	V <sub>PP</sub> input		Connect to V <sub>PP</sub> when programming or verifying
RESET	Single-chip	RESET input	Input	To reset, keep this input terminal low for more than 2μs (min) under normal V <sub>CC</sub> conditions. If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
	EPROM	RESET input		Connect to V <sub>SS</sub>
X <sub>IN</sub>	Single-chip /EPROM	Clock input	Input	Connect a ceramic or a quartz crystal oscillator between X <sub>IN</sub> and X <sub>OUT</sub> for clock oscillation. If an external clock input is used, connect the clock input to the X <sub>IN</sub> pin and open the X <sub>OUT</sub> pin.
X <sub>OUT</sub>		Clock output	Output	
φ	Single-chip /EPROM	Timing output	Output	For timing output
INT <sub>1</sub>	Single-chip	Interrupt input	Input	Interrupt input INT <sub>1</sub> .
	EPROM	Interrupt input	Input	Connect to 0V
P0 <sub>0</sub> ~P0 <sub>7</sub>	Single-chip	I/O port P0	I/O	Port P0 is an 8-bit I/O port with direction registers which can program each bit as input or output. It is set to input mode at reset. The output format is CMOS output.
	EPROM	Address input A <sub>0</sub> ~A <sub>7</sub>	Input	P0 works as the lower 8 bit address input (A <sub>0</sub> ~A <sub>7</sub> )
P1 <sub>0</sub> ~P1 <sub>7</sub>	Single-chip	I/O port P1	I/O	Port P1 is an 8-bit I/O port which has the same function as Port P0.
	EPROM	Address input A <sub>8</sub> ~A <sub>13</sub>	Input	P1 <sub>0</sub> ~P1 <sub>5</sub> works as the higher 6 bit address inputs (A <sub>8</sub> ~A <sub>13</sub> ). Connect P1 <sub>6</sub> ~P1 <sub>7</sub> to V <sub>CC</sub> .
P2 <sub>0</sub> ~P2 <sub>7</sub>	Single-chip	I/O port P2	I/O	Port P2 is an 8-bit I/O port which has the same function as Port P0.
	EPROM	Data input/ output D <sub>0</sub> ~D <sub>7</sub>	I/O	Port 2 works as an 8 bit data bus (D <sub>0</sub> ~D <sub>7</sub> ).
P3 <sub>0</sub> ~P3 <sub>7</sub>	Single-chip	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions Port P0. When serial I/O is used, P3 <sub>7</sub> , P3 <sub>6</sub> , P3 <sub>5</sub> , and P3 <sub>4</sub> work as $\overline{S_{RDV}}$ , CLK, S <sub>OUT</sub> , and S <sub>IN</sub> pins, respectively. Also P3 <sub>3</sub> and P3 <sub>2</sub> work as CNTR pin and the lowest interrupt pin (INT <sub>2</sub> ), respectively. The output format is N-ch open drain.
	EPROM	Input Port P3	Input	Connect to 0V
P4 <sub>0</sub> ~P4 <sub>7</sub>	Single-chip	I/O port P4	I/O	Port P4 is an 8-bit I/O port which has the same function as Port P0. Ports P4 <sub>7</sub> ~P4 <sub>0</sub> are common with Analog inputs AN <sub>7</sub> ~AN <sub>0</sub> . The output format is N-ch open drain.
	EPROM	Select mode	Input	P4 <sub>2</sub> , P4 <sub>1</sub> , P4 <sub>0</sub> work as $\overline{CE}$ , $\overline{OE}$ and PGM inputs, respectively. Connect P4 <sub>5</sub> ~P4 <sub>7</sub> to 0V and P4 <sub>4</sub> and P4 <sub>3</sub> to V <sub>CC</sub> .
P5 <sub>0</sub> ~P5 <sub>7</sub>	Single-chip	Input port	Input	Port P5 is an 8-bit input port. Ports P5 <sub>7</sub> ~P5 <sub>4</sub> have edge sense functions.
	EPROM	Input port	Input	Connect to 0V

**PIN DESCRIPTION (Continued)**

Pin	Mode	Name	Input/ Output	Functions
P6 <sub>0</sub> ~P6 <sub>4</sub>	Single-chip	Output port	Output	Port P6 is an 5-bit output port. At external trigger output mode, P6 <sub>0</sub> and P6 <sub>1</sub> are in common with the trigger input pin (T) and the trigger output pin (Q), respectively. The output structure is N-channel open drain.
	EPROM	Output port	Output	Connect to 0V.
P7 <sub>0</sub> ~P7 <sub>5</sub>	Single-chip	I/O port	I/O	Port P7 is an 6-bit I/O port and has basically the same functions as port P0. The output structure of P7 <sub>0</sub> , P7 <sub>1</sub> is N-channel open drain, and the output structure of P7 <sub>2</sub> ~P7 <sub>5</sub> is CMOS output.
	EPROM	Input port	Input	Connect to 0V.
AV <sub>SS</sub>	Single-chip	Analog voltage input	Input	GND pin for the A-D and D-A converters.
	EPROM	Analog voltage input	Input	Connect to 0V.
V <sub>REF</sub>	Single-chip	Reference voltage input	Input	Reference input for A-D and D-A converters.
	EPROM	Reference voltage input	Input	Connect to 0V.
D-A	Single-chip	D-A output	Output	D-A converter output pin.
	EPROM	D-A output	Output	Connect to 0V.
PWM	Single-chip	PWM output	Output	Pulse width modulation output pin (N channel open drain format).
	EPROM	PWM output	Output	Connect to 0V.

**PROM VERSION of M37414M5-XXXFP**

**EPROM MODE**

The M37414E5-XXXFP features an EPROM mode in addition to its normal modes. When the RESET signal level is low ("L"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1 gives the pin connection in the EPROM mode. When in the EPROM mode, ports P0, P1, P2, P4<sub>0</sub>~P4<sub>2</sub>, and CNV<sub>SS</sub> are used for the PROM (equivalent to the M5L27128). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5L27128. The oscillator should be connected to the X<sub>IN</sub> and X<sub>OUT</sub> pins, or external clock should be connected to the X<sub>IN</sub> pin.

Table 1. Pin function in EPROM mode

	M37414E5-XXXFP	M5L27128
V <sub>CC</sub>	V <sub>CC</sub>	V <sub>CC</sub>
V <sub>PP</sub>	CNV <sub>SS</sub> /V <sub>PP</sub>	V <sub>PP</sub>
V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>
Address input	Ports P0, P1 <sub>0</sub> ~P1 <sub>5</sub>	A <sub>0</sub> ~A <sub>13</sub>
Data I/O	Port P2	D <sub>0</sub> ~D <sub>7</sub>
CE	P4 <sub>2</sub> /CE	CE
OE	P4 <sub>1</sub> /OE	OE
PGM	P4 <sub>0</sub> /PGM	PGM

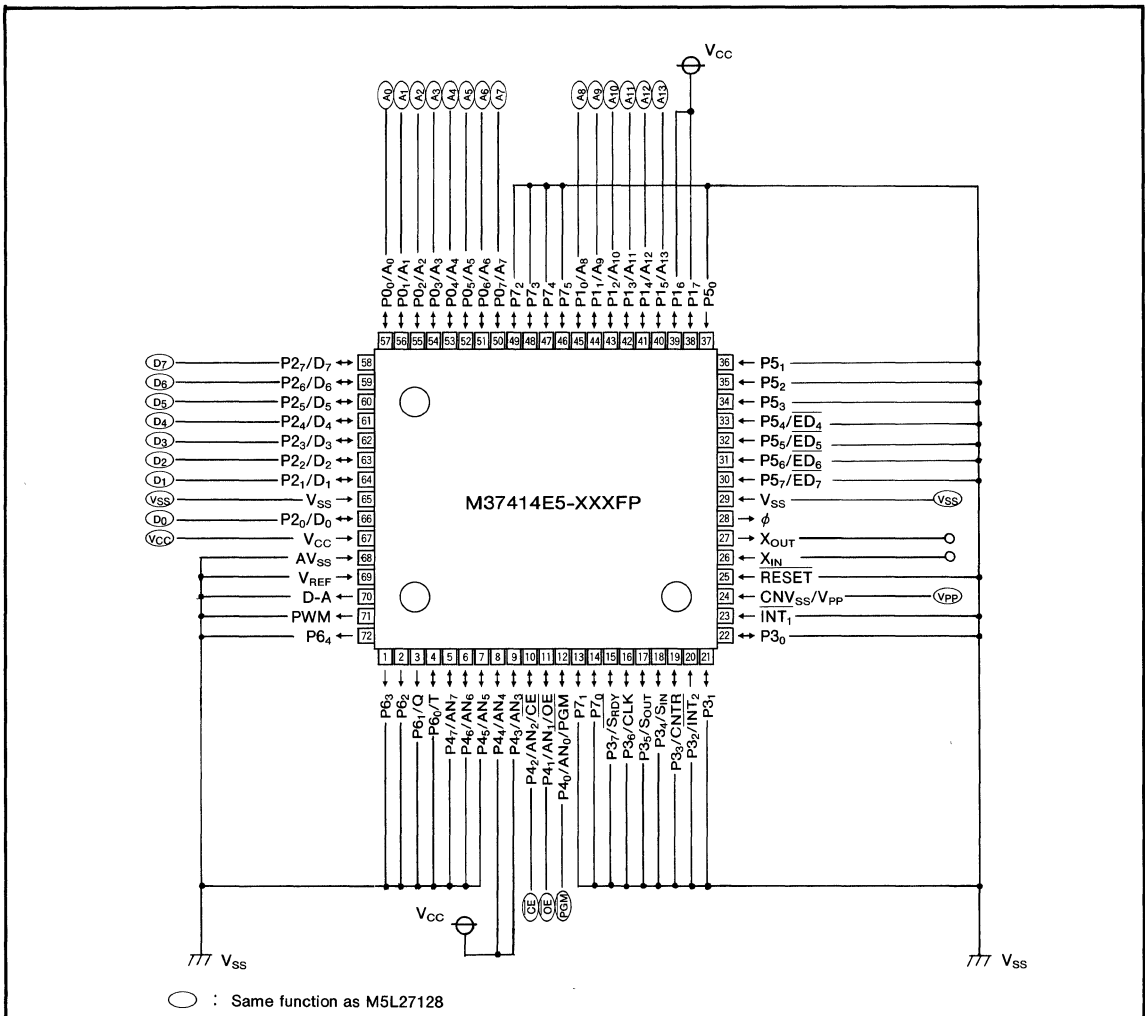


Fig. 1 Pin connection in EPROM programming mode

PROM VERSION of M37414M5-XXXFP

**PROM READING AND WRITING**

**Reading**

To read the PROM, set the  $\overline{CE}$  and  $\overline{OE}$  pins to a "L" level, and the  $\overline{PGM}$  pin to a "H" level. Input the address of the data ( $A_0 \sim A_{13}$ ) to be read and the data will be output to the I/O pins  $D_0 \sim D_7$ . The data I/O pins will be floating when either the  $\overline{CE}$  or  $\overline{OE}$  pins are in the "H" state.

**Writing**

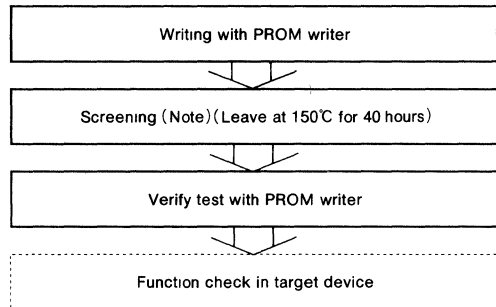
To write to the PROM, set the  $\overline{CE}$  pin to a "L" level and the  $\overline{OE}$  pin to a "H" level. The CPU will enter the program mode when  $V_{PP}$  is applied to the  $V_{PP}$  pin. The address to be written to is selected with pins  $A_0 \sim A_{13}$ , and the data to be written is input to pins  $D_0 \sim D_7$ . Set the  $\overline{PGM}$  pin to a "L" level to begin writing.

**Notes on Writing**

When using an PROM writer, the address range should be between  $1800_{16}$  and  $3FFF_{16}$ . When data is written between addresses  $0000_{16}$  and  $3FFF_{16}$ , fill addresses  $0000_{16}$  to  $17FF_{16}$  with  $00_{16}$ .

**NOTES ON HANDLING**

- (1) Since a high voltage (21V) is used to write data, care should be taken when turning on the PROM writer's power.
- (2) For the programmable microcomputer (shipped in blank or OTP type), Mitsubishi does not perform PROM write test and screening in the assembly process and following processes. To improve reliability after write, performing write and test according to the flow below before use is recommended.



Note : Since the screening temperature is higher than storage temperature, never expose to  $150^{\circ}\text{C}$  exceeding 100 hours.

Table 2. I/O signal in each mode

Mode \ Pin	$\overline{CE}(10)$	$\overline{OE}(11)$	$\overline{PGM}(12)$	$V_{PP}(24)$	$V_{CC}(67)$	Data I/O (58~64, 66)
Read-out	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{CC}$	$V_{CC}$	Output
Programming	$V_{IL}$	$V_{IH}$	Pulse ( $V_{IH} \rightarrow V_{IL}$ )	$V_{PP}$	$V_{CC}$	Input
Programming verify	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{PP}$	$V_{CC}$	Output
Program disable	$V_{IH}$	X	X	$V_{PP}$	$V_{CC}$	Floating

Note 1 :  $V_{IL}$  and  $V_{IH}$  indicate a "L" and "H" input voltage, respectively  
 2 : An X indicates either  $V_{IL}$  or  $V_{IH}$

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC}$	Supply voltage	With respect to $V_{SS}$ With the output transistor cut-off	-0.3 ~ 7	V
$V_I$	Input voltage $X_{IN}$		-0.3 ~ 7	V
$V_I$	Input voltage $P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7, P4_0 \sim P4_7, P7_2 \sim P7_5$		-0.3 ~ $V_{CC} + 0.3$	V
$V_I$	Input voltage $P3_0 \sim P3_7, P5_0 \sim P5_7, P6_0, P7_0, P7_1, \overline{INT}_1$		-0.3 ~ 13	V
$V_I$	Input voltage $CNV_{SS}, RESET$		-0.3 ~ 13 (Note 1)	V
$V_O$	Output voltage $P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7, P4_0 \sim P4_7, P7_2 \sim P7_5, X_{OUT}, \phi, D-A$		-0.3 ~ $V_{CC} + 0.3$	V
$V_O$	Output voltage $P3_0 \sim P3_7, P6_0 \sim P6_4, P7_0, P7_1, PWM$		-0.3 ~ 13	V
$P_d$	Power dissipation	$T_a = 25^\circ C$	300	mW
$T_{opr}$	Operating temperature		-10 ~ 70	$^\circ C$
$T_{stg}$	Storage temperature		-40 ~ 125	$^\circ C$

Note 1 : In PROM programming mode,  $CNV_{SS}$  is 22.0V

**RECOMMENDED OPERATING CONDITIONS** ( $V_{CC} = 5V \pm 5\%$ ,  $T_a = -10 \sim 70^\circ C$ , unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$V_{CC}$	Supply voltage	4.75	5	5.25	V
$V_{SS}$	Supply voltage		0		V
$V_{REF}$	Reference voltage	4		$V_{CC}$	V
$V_{IH}$	"H" input voltage $P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7, P3_0 \sim P3_7, P4_0 \sim P4_7, P5_0 \sim P5_7, \overline{INT}_1, RESET, X_{IN}, CNV_{SS}, P6_0, P7_0 \sim P7_5$	$0.8V_{CC}$		$V_{CC}$	V
$V_{IL}$	"L" input voltage $P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7, P3_0 \sim P3_7, P4_0 \sim P4_7, P5_0 \sim P5_7, \overline{INT}_1, CNV_{SS}, P6_0, P7_0 \sim P7_5$	0		$0.2V_{CC}$	V
$V_{IL}$	"L" input voltage RESET	0		$0.12V_{CC}$	V
$V_{IL}$	"L" input voltage $X_{IN}$	0		$0.16V_{CC}$	V
$I_{OL(peak)}$	"L" peak output current $P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7, P3_0 \sim P3_7, P4_0 \sim P4_7, P7_0 \sim P7_5$ (Note 2)			10	mA
$I_{OL(peak)}$	"L" peak output current $P6_0 \sim P6_3$ (Note 2)			15	mA
$I_{OL(peak)}$	"L" peak output current PWM, $P6_4$ (Note 2)			5	mA
$I_{OL(avg)}$	"L" average output current $P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7, P3_0 \sim P3_7, P4_0 \sim P4_7, P7_0 \sim P7_5$ (Note 1)			5	mA
$I_{OL(avg)}$	"L" average output current $P6_0 \sim P6_3$ (Note 1)			7	mA
$I_{OL(avg)}$	"L" average output current PWM, $P6_4$ (Note 1)			2.5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7, P7_2 \sim P7_5$ (Note 2)			-10	mA
$I_{OH(avg)}$	"H" average output current $P0_0 \sim P0_7, P1_0 \sim P1_7, P2_0 \sim P2_7, P7_2 \sim P7_5$ (Note 1)			-5	mA
$f(X_{IN})$	Internal clock oscillating frequency			4	MHz

- Note 1 : The average output currents  $I_{OL(avg)}$  and  $I_{OH(avg)}$  are the average value of a period of 100ms  
 2 : Do not allow the combined low-level output current of ports P0, P1, P2, P3, P4, P6, P7 and PWM to exceed 80mA.  
 Do not allow the combined high-level output current of port P0, P1, P2 P7<sub>2</sub>~P7<sub>5</sub> to exceed 50mA  
 3 : "H" input voltage of ports P3, P5, P6<sub>0</sub>, P7<sub>0</sub>, P7<sub>1</sub> and  $\overline{INT}_1$  is available up to +12V



PROM VERSION of M37414M5-XXXFP

**ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V$ ,  $V_{SS}=0V$ ,  $T_a=25^\circ C$ ,  $f(X_{IN})=4MHz$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ	Max.	
$V_{OH}$	"H" output voltage P0 <sub>0</sub> ~P0 <sub>7</sub> , P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> , P7 <sub>2</sub> ~P7 <sub>5</sub>	$I_{OH}=-10mA$	3			V
$V_{OH}$	"H" output voltage $\phi$	$I_{OH}=-2.5mA$	3			V
$V_{OL}$	"L" output voltage P0 <sub>0</sub> ~P0 <sub>7</sub> , P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> , P3 <sub>0</sub> ~P3 <sub>7</sub> , P4 <sub>0</sub> ~P4 <sub>7</sub> , P6 <sub>0</sub> ~P6 <sub>3</sub> , P7 <sub>0</sub> ~P7 <sub>5</sub>	$I_{OL}=10mA$			2	V
$V_{OL}$	"L" output voltage $\phi$ , PWM, P6 <sub>4</sub>	$I_{OL}=5mA$			2	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{INT}_1$		0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis P3 <sub>6</sub>	When used as CLK input	0.3	0.8		V
$V_{T+}-V_{T-}$	Hysteresis P3 <sub>2</sub>	When used as $\overline{INT}_2$ input	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis P3 <sub>3</sub>	When used as CNTR input	0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis P6 <sub>0</sub>	When used as T input	0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis RESET			0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis $X_{IN}$		0.1		0.5	V
$I_{IL}$	"L" input current P0 <sub>0</sub> ~P0 <sub>7</sub> , P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> , P3 <sub>0</sub> ~P3 <sub>7</sub> , P4 <sub>0</sub> ~P4 <sub>7</sub> , P5 <sub>0</sub> ~P5 <sub>7</sub> , P6 <sub>0</sub> , P7 <sub>0</sub> ~P7 <sub>5</sub> , PWM	$V_I=0V$			-5	$\mu A$
$I_{IL}$	"L" input current $\overline{INT}_1$ , RESET, $X_{IN}$	$V_I=0V$			-5	$\mu A$
$I_{IH}$	"H" input current P3 <sub>0</sub> ~P3 <sub>7</sub> , P5 <sub>0</sub> ~P5 <sub>7</sub> , P6 <sub>0</sub> , P7 <sub>0</sub> , P7 <sub>1</sub> , PWM	$V_I=12V$			12	$\mu A$
$I_{IH}$	"H" input current $\overline{INT}_1$ , RESET, $X_{IN}$ , P0 <sub>0</sub> ~P0 <sub>7</sub> , P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> , P4 <sub>0</sub> ~P4 <sub>7</sub> , P7 <sub>2</sub> ~P7 <sub>5</sub>	$V_I=5V$			5	$\mu A$
$V_{RAM}$	RAM retention voltage	At clock stop	2			V
$I_{CC}$	Supply current	$\phi$ , $X_{OUT}$ , and D-A pins opened, other pins at $V_{SS}$ , and A-D converter in the finished condition.	$f(X_{IN})=4MHz$ Square wave	3	6	$\mu A$
			At clock stop $T_a=25^\circ C$		1	
			At clock stop $T_a=75^\circ C$		10	

**A-D CONVERTER CHARACTERISTICS** ( $V_{CC}=5V$ ,  $V_{SS}=AV_{SS}=0V$ ,  $T_a=25^\circ C$ ,  $f(X_{IN})=4MHz$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max	
—	Resolution	$V_{REF}=V_{CC}$			8	Bits
—	Absolute accuracy	$V_{REF}=V_{CC}$			$\pm 3$	LSB
$R_{LADDER}$	Ladder resistance value	$V_{REF}=V_{CC}$	2		10	k $\Omega$
$t_{CONV}$	Conversion time				50	$\mu s$
$V_{REF}$	Reference input voltage		2		$V_{CC}$	V
$V_{IA}$	Analog input voltage		0		$V_{REF}$	V

**D-A CONVERTER CHARACTERISTICS** ( $V_{CC}=5V$ ,  $V_{SS}=AV_{SS}=0V$ ,  $T_a=25^\circ C$ ,  $f(X_{IN})=4MHz$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ	Max	
—	Resolution	$V_{REF}=V_{CC}$			5	Bits
—	Error in full scale range	$V_{REF}=V_{CC}$			$\pm 1$	%
$t_{SU}$	Setup time	$V_{REF}=V_{CC}$			3	$\mu s$
$R_O$	Output resistance	$V_{REF}=V_{CC}$			3	k $\Omega$
$V_{REF}$	Reference voltage		4		$V_{CC}$	V

**TIMING REQUIREMENTS**

**Single-chip mode** ( $V_{CC}=5V\pm 5\%$ ,  $V_{SS}=0V$ ,  $T_A=25^\circ C$ ,  $f(X_{IN})=4MHz$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max.	
$t_{SU(P0D-\phi)}$	Port P0 input setup time		270			ns
$t_{SU(P1D-\phi)}$	Port P1 input setup time		270			ns
$t_{SU(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{SU(P3D-\phi)}$	Port P3 input setup time		270			ns
$t_{SU(P4D-\phi)}$	Port P4 input setup time		270			ns
$t_{SU(P5D-\phi)}$	Port P5 input setup time		270			ns
$t_{SU(P7D-\phi)}$	Port P7 input setup time		270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		20			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		20			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time		20			ns
$t_{h(\phi-P7D)}$	Port P7 input hold time		20			ns
$t_C$	External clock input cycle time		250			ns
$t_W$	External clock input pulse width		75			ns
$t_r$	External clock rising edge time				25	ns
$t_f$	External clock falling edge time				25	ns

**Eva-chip mode** ( $V_{CC}=5V\pm 5\%$ ,  $V_{SS}=0V$ ,  $T_A=25^\circ C$ ,  $f(X_{IN})=4MHz$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{SU(P0D-\phi)}$	Port P0 input setup time		270			ns
$t_{SU(P1D-\phi)}$	Port P1 input setup time		270			ns
$t_{SU(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		20			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		20			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		20			ns

**Memory expanding mode and microprocessor mode**

( $V_{CC}=5V\pm 5\%$ ,  $V_{SS}=0V$ ,  $T_A=25^\circ C$ ,  $f(X_{IN})=4MHz$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{SU(P2D-\phi)}$	Port P2 input setup time		270			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		30			ns

**SWITCHING CHARACTERISTICS**

**Single-chip mode** ( $V_{CC}=5V\pm 5\%$ ,  $V_{SS}=0V$ ,  $T_a=25^\circ C$ ,  $f(X_{IN})=4MHz$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig 3			230	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				230	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				230	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time	Fig. 2			230	ns
$t_{d(\phi-P4Q)}$	Port P4 data output delay time				230	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				230	ns
$t_{d(\phi-P7Q)}$	Port P7 <sub>0</sub> , P7 <sub>1</sub> data output delay time	Fig 3			230	ns
$t_{d(\phi-P7Q)}$	Port P7 <sub>2</sub> ~P7 <sub>5</sub> data output delay time				230	ns

**Eva-chip mode** ( $V_{CC}=5V\pm 5\%$ ,  $V_{SS}=0V$ ,  $T_a=25^\circ C$ ,  $f(X_{IN})=4MHz$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min	Typ	Max		
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig 3			250	ns	
$t_{d(\phi-P0AF)}$	Port P0 address output delay time				250	ns	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time				200	ns	
$t_{d(\phi-P0QF)}$	Port P0 data output delay time				200	ns	
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns	
$t_{d(\phi-P1AF)}$	Port P1 address output delay time				250	ns	
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns	
$t_{d(\phi-P1QF)}$	Port P1 data output delay time				200	ns	
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				300	ns	
$t_{d(\phi-P2QF)}$	Port P2 data output delay time				300	ns	
$t_{d(\phi-R/W)}$	R/W signal output delay time		Fig 2			250	ns
$t_{d(\phi-R/WF)}$	R/W signal output delay time					250	ns
$t_{d(\phi-P3_0Q)}$	Port P3 <sub>0</sub> data output delay time				200	ns	
$t_{d(\phi-P3_0QF)}$	Port P3 <sub>0</sub> data output delay time				200	ns	
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns	
$t_{d(\phi-SYNCF)}$	SYNC signal output delay time				250	ns	
$t_{d(\phi-P3_1Q)}$	Port P3 <sub>1</sub> data output delay time				200	ns	
$t_{d(\phi-P3_1QF)}$	Port P3 <sub>1</sub> data output delay time				200	ns	

**Memory expanding mode and microprocessor mode**

( $V_{CC}=5V\pm 5\%$ ,  $V_{SS}=0V$ ,  $T_a=25^\circ C$ ,  $f(X_{IN})=4MHz$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max.	
$t_{d(\phi-P0A)}$	Port P0 address output delay time	Fig 3			250	ns
$t_{d(\phi-P1A)}$	Port P1 address output delay time				250	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				300	ns
$t_{d(\phi-P2QF)}$	Port P2 data output delay time	Fig 2			300	ns
$t_{d(\phi-R/W)}$	R/W signal output delay time				250	ns
$t_{d(\phi-SYNC)}$	SYNC signal output delay time				250	ns

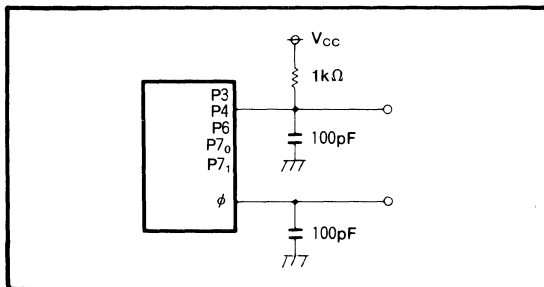


Fig. 2 Ports P3, P4, P6, P7<sub>0</sub>, P7<sub>1</sub> test circuit

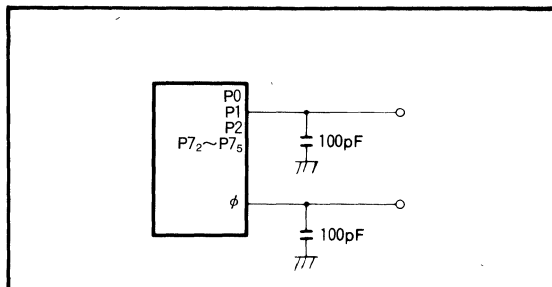
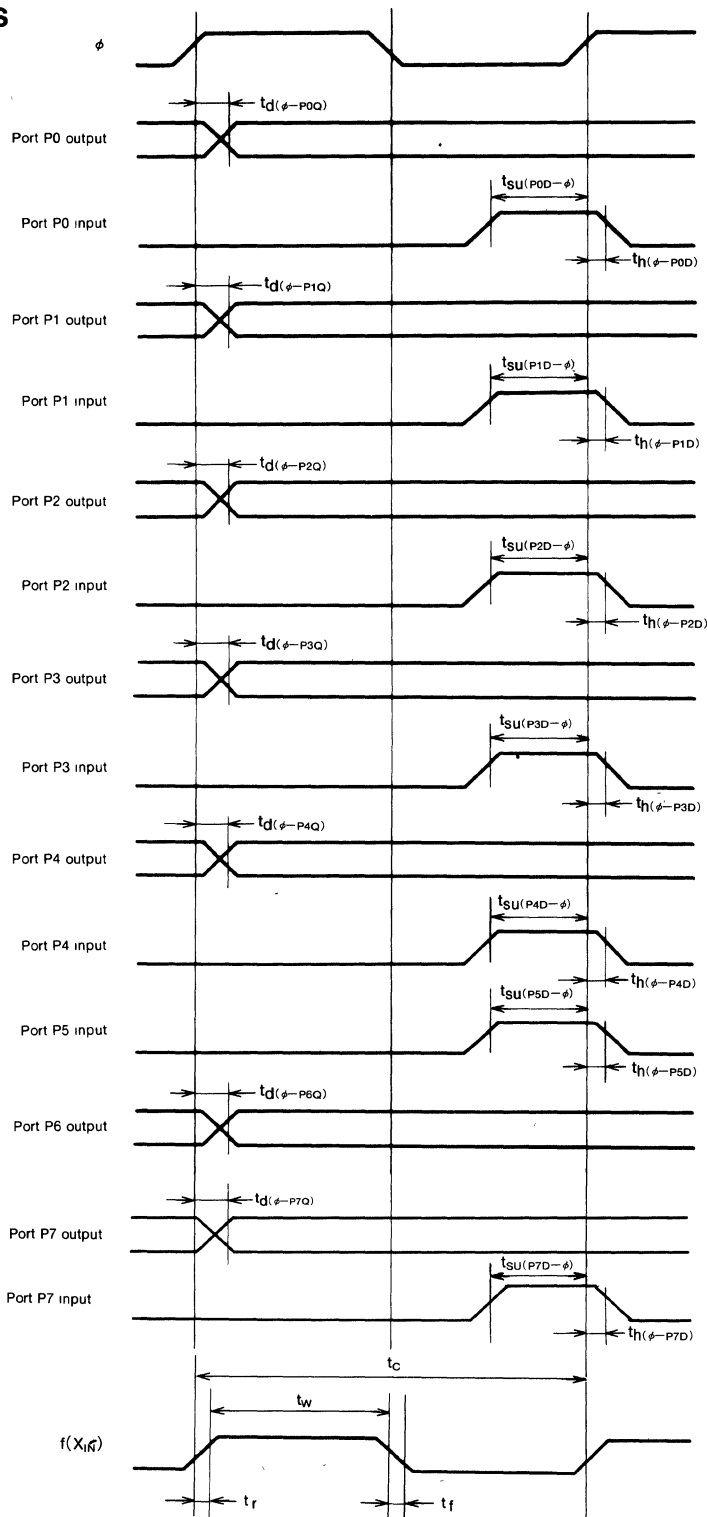


Fig. 3 Port P0, P1, P2, P7<sub>2</sub>~P7<sub>5</sub> test circuit

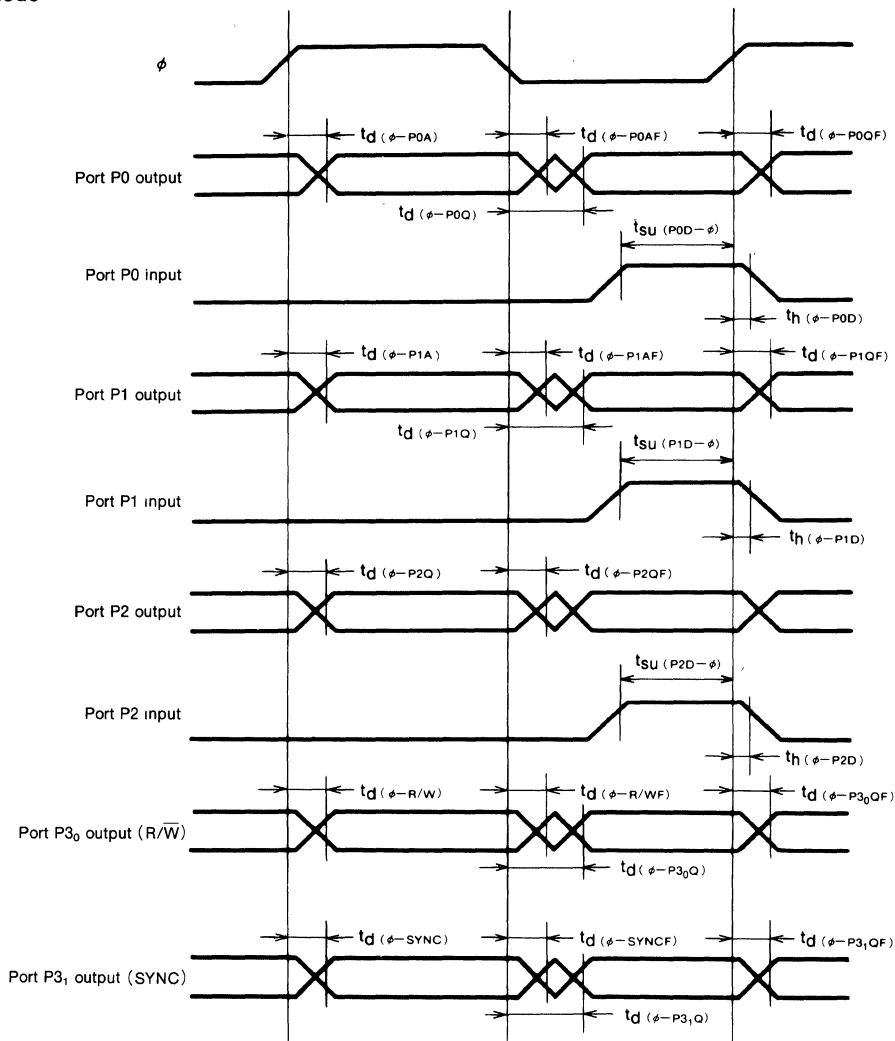
**TIMING DIAGRAMS**

In single-chip mode



**PROM VERSION of M37414M5-XXXFP**

In eva-chip mode



**PROM VERSION of M37414M5-XXXFP**

In memory expanding mode and microprocessor mode

