M37416M2-XXXSP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37416M2-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 52-pin shrink plastic molded DIP (flat package type also available). This single-chip microcomputer is useful for office automation equipment and other consumer applications.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M37416M2-XXXSP and the M37416M2-XXXFP are the package outline and power dissipation ability (absolute maximum ratings).

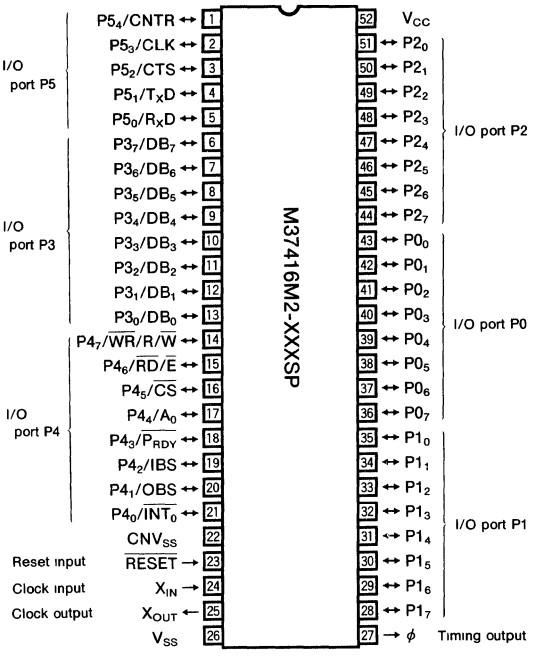
FEATURES

- Number of basic instructions 69
- Memory size ROM ..... 4096 bytes
  RAM ..... 128 bytes
- Instruction execution time
  ..... 1 μs (minimum instructions at 8MHz frequency)
- Single power supply f(X_{IN})=8MHz ..... 5V±10%
- Power dissipation
  normal operation mode (at 8MHz frequency) 50mW
- Subroutine nesting ..... 64 levels (max.)
- Interrupt 9
- 8-bit timer 2
- Programmable I/O ports
  (Ports P0, P1, P2, P3, P4, P5) 45
- UART (full duplex) 1
- Master CPU bus interface ..... 1 byte
- Comparator 8-channel
- Key on wake up 8

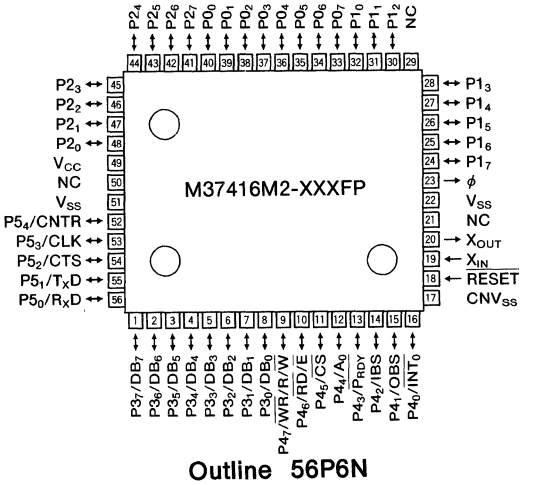
APPLICATION

Office automation equipment
Key pad, Key board

PIN CONFIGURATION (TOP VIEW)



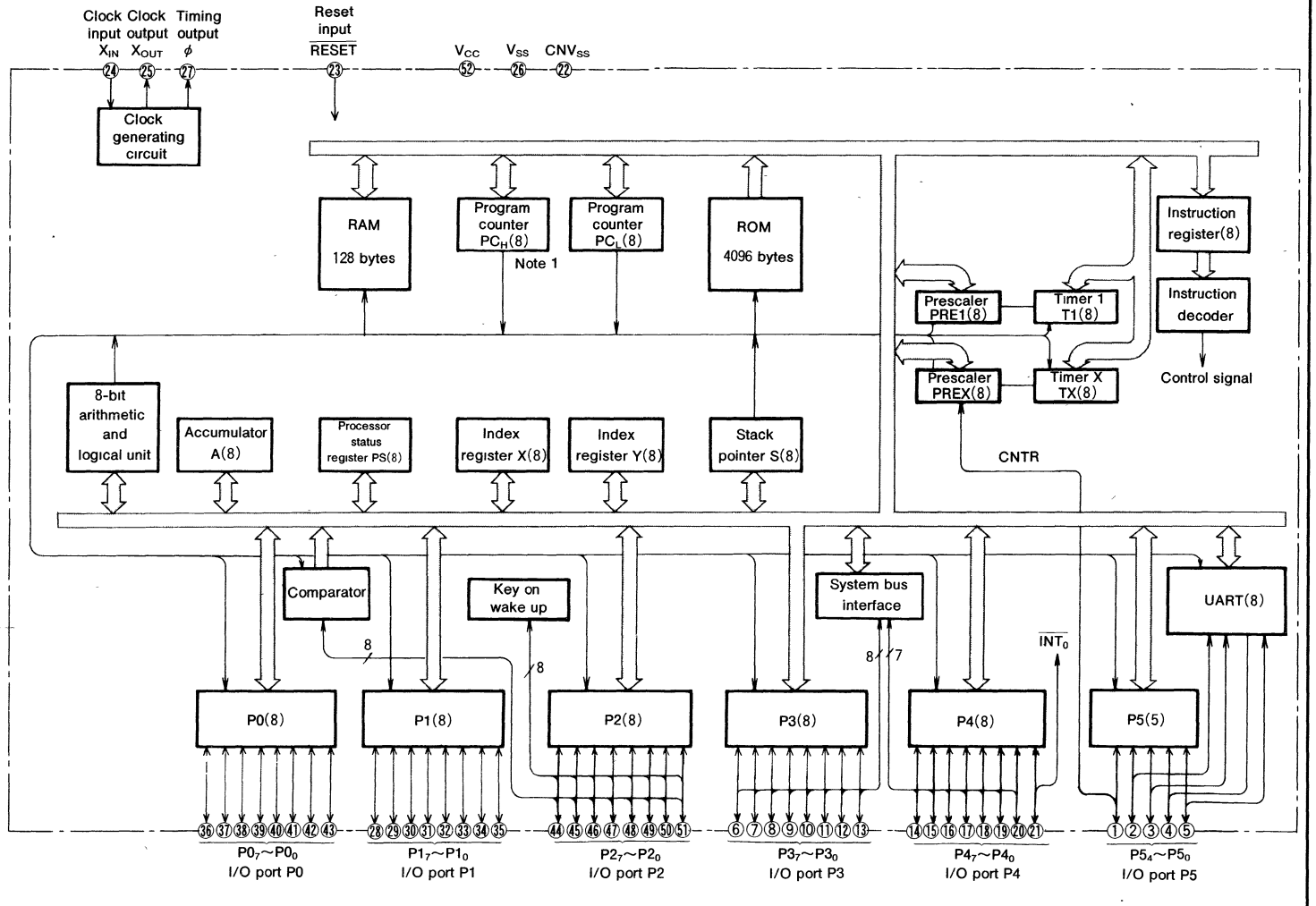
Outline 52P4B



Outline 56P6N

NC : No connection

M37416M2-XXXSP BLOCK DIAGRAM



Note 1 : Program counter PC_H is only 5 bits long

FUNCTIONS OF M37416M2-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			1 μs (minimum instructions, at 8MHz frequency)
Clock frequency			8MHz
Memory size	ROM		4096 bytes
	RAM		128 bytes
Input/Output ports	$P0_0$~$P0_7$	I/O	8-bitX1
	$P1_0$~$P1_7$	I/O	8-bitX1
	$P2_0$~$P2_7$	I/O	8-bitX1 (common with comparator input and key on wake up)
	$P3_0$~$P3_7$	I/O	8-bitX1 (common with data bus of system bus interface)
	$P4_0$~$P4_7$	I/O	8-bitX1 (common with control ports of system bus interface and $\overline{INT_0}$)
	$P5_0$~$P5_4$	I/O	5-bitX1 (common with UART)
UART			1 with programmable baud rate generator
Timers			8-bitX2 (with 8-bit prescaler)
Comparator			8-bitX1 (port P2) Built-in 3-bit DAC (can be used as variable V_{TH} input port)
Subroutine nesting			64 levels (max.)
Interrupt			2 external, 6 internal, 1 software interrupts
System bus interface buffer			1-byte (separate input and output buffers)
Clock generating circuit			Built-in (Ceramic or quartz crystal oscillator)
Supply voltage			5V$\pm$10%
Power dissipation	at operation		50mW
	at wait mode		5mW
	at stop mode	Ta=25°C	0.05mW
		Ta=70°C	0.5mW
Input/Output characteristics	Input/Output voltage		V_{SS}−0.3~V_{CC}+0.3
	Output current		$\pm$5mA (max.)
Operating temperature range			−10~70°C
Device structure			CMOS silicon gate
Package	M37416M2-XXXSP		52-pin shrink plastic molded DIP
	M37416M2-XXXFP		56-pin plastic molded QFP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
CNTR	Timer I/O	I/O	This is an I/O pin for the timer X
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. The output structure is CMOS output
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same function as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same function as port P0. Analog input of comparator or key on wake up function can be selected with a program.
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same function as port P0 This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program
$P4_0$~$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same function as port P0. $P4_1$~$P4_7$ change to a control bus for the master CPU when slave mode is selected with a program. $P4_0$ can be used as external interrupt input pin.
$P5_0$~$P5_4$	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same function as port P0 UART function, CNTR input and timer output can be selected with a program

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The M37416 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions are not provided.

The WIT instruction can be used.

The STP instruction can be used.

MEMORY

• Special Function Register (SFR) Area

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• RAM

RAM is used for data storage as well as a stack area.

• ROM

ROM is used for storing user programs as well as the interrupt vector area.

• Interrupt Vector Area

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• Zero Page

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

• Special Page

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

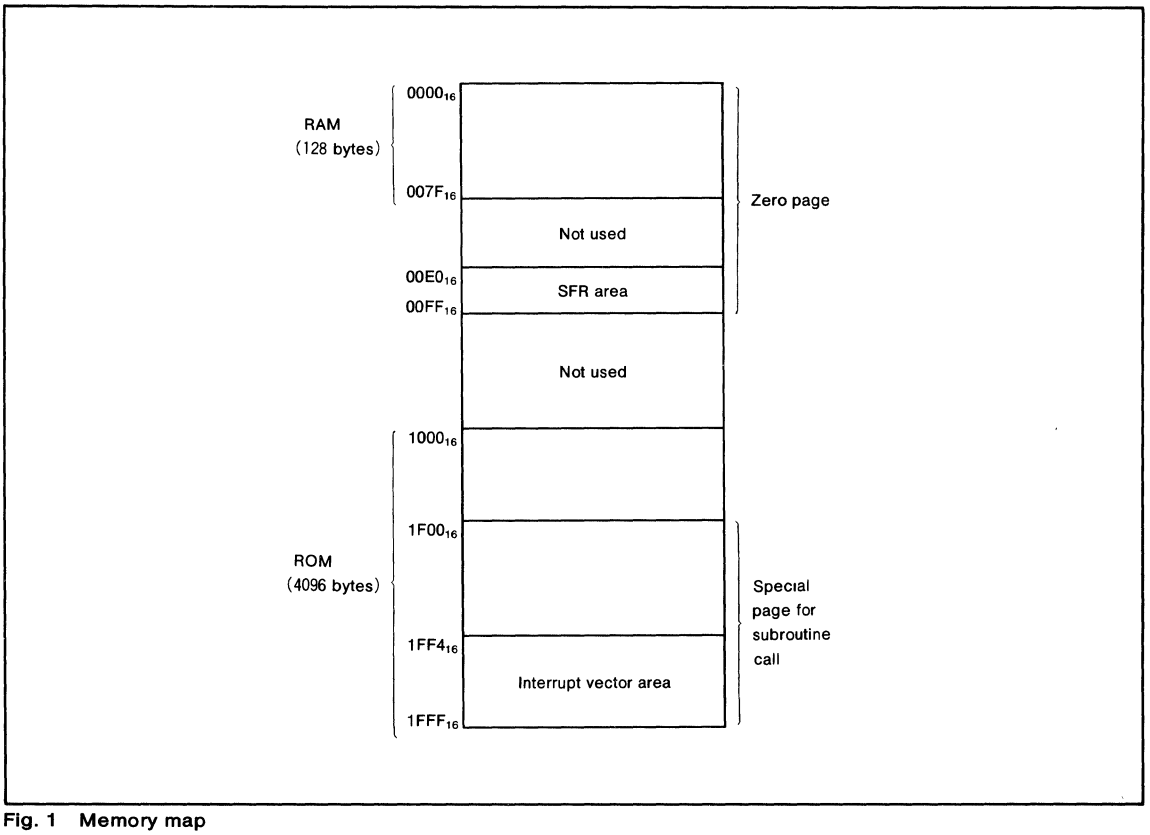


Fig. 1 Memory map

$00E0_{16}$	Port P0	$00F0_{16}$	Data bus receive buffer register
$00E1_{16}$	Port P0 directional register	$00F1_{16}$	Data bus buffer status register
$00E2_{16}$	Port P1	$00F2_{16}$	Data bus buffer control register
$00E3_{16}$	Port P1 directional register	$00F3_{16}$	UART transmit buffer register
$00E4_{16}$	Port P2	$00F4_{16}$	UART receive buffer register
$00E5_{16}$	Port P2 directional register	$00F5_{16}$	UART status register
$00E6_{16}$	Port P3	$00F6_{16}$	UART mode register
$00E7_{16}$	Port P3 directional register	$00F7_{16}$	UART control register
$00E8_{16}$	Port P4	$00F8_{16}$	Driver for UART baud rate generator
$00E9_{16}$	Port P4 directional register	$00F9_{16}$	
$00EA_{16}$	Port P5	$00FA_{16}$	Prescaler 1
$00EB_{16}$	Port P5 directional register	$00FB_{16}$	Timer 1
$00EC_{16}$	Comparator control register	$00FC_{16}$	Timer X prescaler
$00ED_{16}$	Comparator data register	$00FD_{16}$	Timer X
$00EE_{16}$	Interrupt request distinguish register	$00FE_{16}$	Interrupt control register
$00EF_{16}$	Data bus transmit buffer register	$00FF_{16}$	Timer control register

Fig. 2 SFR (Special Function Register) memory map

INTERRUPTS

Interrupts can be caused by 9 different events.

Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed interrupt inhibit flag I is set, and the program jumps to the address specified in the vector table. The reset and BRK instruction interrupt can never be inhibited. Other interrupts are disabled when the interrupt inhibit flag is set.

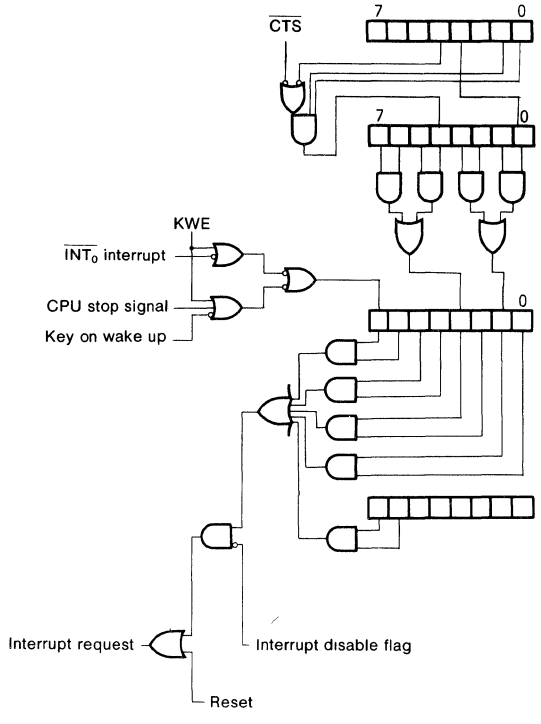
All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt inhibit bit is "0". There are two interrupt (three for UART transmit and UART receive) the interrupt becomes enable when both enable bits are "0".

The value of bit 3 of the data bus buffer control register (address $00F2_{16}$) determines whether the interrupt is from $\overline{INT_0}$ or from key on wake up. Only $\overline{INT_0}$ interrupt is effective when this bit is "1" at power down condition by STP or WIT instruction. When this bit is "1", interrupt is caused by inputting "L" level to any port P2 using input mode. The value of bit 1 and bit 3 of interrupt request distinguish register (address $00EE_{16}$) determine whether the interrupt is from input buffer full or from UART receive. When bit 3 is "1", the interrupt is from the input buffer full interrupt, and bit 1 is "1", the interrupt is from UART receive. Also bit 5 and bit 7 of interrupt request distinguish register determine whether the interrupt is from output buffer empty or from UART transmit. When bit 7 is "1", the interrupt is from output buffer empty and when bit 5 is "1", the interrupt is from UART transmit.

Table 1. Interrupt vector address and priority

Interrupt	Priority	Vector address
$\overline{RESET}$	1	$FFFF_{16}$, $FFFE_{16}$
$\overline{INT_0}$ or key on wake up	2	$FFFD_{16}$, $FFFC_{16}$
Timer X	3	$FFFB_{16}$, $FFFA_{16}$
Timer 1	4	$FFF9_{16}$, $FFF8_{16}$
Input bus buffer full or UART receive	5	$FFF7_{16}$, $FFF6_{16}$
Output bus buffer full or UART transmit	6	$FFF5_{16}$, $FFF4_{16}$



UART control register (address $00F7_{16}$)
- Bit 4 : CTS function select bit
- Bit 3 : Receive interrupt enable bit
- Bit 1 : Transmit interrupt enable bit
- Bit 0 : UART transmit enable bit

Interrupt request distinguish register (address $00EE_{16}$)
- Bit 7 : Output buffer empty interrupt request bit
- Bit 6 : Output buffer empty interrupt enable bit
- Bit 5 : UART transmit interrupt request bit
- Bit 4 : UART transmit interrupt enable bit
- Bit 3 : Input buffer full interrupt request bit
- Bit 2 : Input buffer full interrupt enable bit
- Bit 1 : UART receive interrupt request bit
- Bit 0 : UART receive interrupt enable bit

Interrupt control register (address $00FE_{16}$)
- Bit 7 : $\overline{INT_0}$ or key on wake up interrupt request bit
- Bit 6 : $\overline{INT_0}$ or key on wake up interrupt enable bit
- Bit 5 : Timer 1 interrupt request bit
- Bit 4 : Timer 1 interrupt enable bit
- Bit 3 : Input buffer full or UART receive request bit
- Bit 2 : Input buffer full or UART receive enable bit
- Bit 1 : Output buffer empty or UART transmit interrupt request bit
- Bit 0 : Output buffer empty or UART transmit interrupt enable bit

Timer control register (address $00FF_{16}$)
- Bit 7 : Timer X interrupt request bit
- Bit 6 : Timer X interrupt enable bit

Fig. 3 Interrupt control

When the two interrupt requests, which are the same priority, are at the same sampling, the priority process is processed by interrupt request distinguish register.

These request bits can be reset by a program but can not be set. The interrupt requests bits which are in the interrupt control register and timer control register are reset automatically when interrupts are accepted. But the interrupt request bits which are in the interrupt request distinguish register are not reset automatically, so they must be reset by software. The contents of the B flag must be checked to determine if the BRK instruction caused or not.

TIMER

The M37416M2-XXXSP has two timers; timer X, and timer 1. Timer X has four modes which can be selected by bit 2 and 3 of the timer control register. When the timer X count stop bit (bit 5) is set to "1", the timer X will stop regardless of which mode it is in. A block diagram of timer X, and timer 1 is shown in Figure 4. The CNTR pin is common with $P5_4$ and can not be used when this pin is used as normal port.

The prescaler has an 8-bit programmable latch used as a frequency divider. The division ratio is defined as $1/(n+1)$, where n is the decimal contents of the prescaler latch. All timers are down-count timers which are reloaded from the timer latch following the zero cycle of the timer (i.e. the cycle after the timer counts to zero).

The timer interrupt request bit is set to "1" during the next clock pulse after the timer reaches zero. The interrupt and timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see interrupt section). The prescaler latch and timer latch can be loaded with any number except zero.

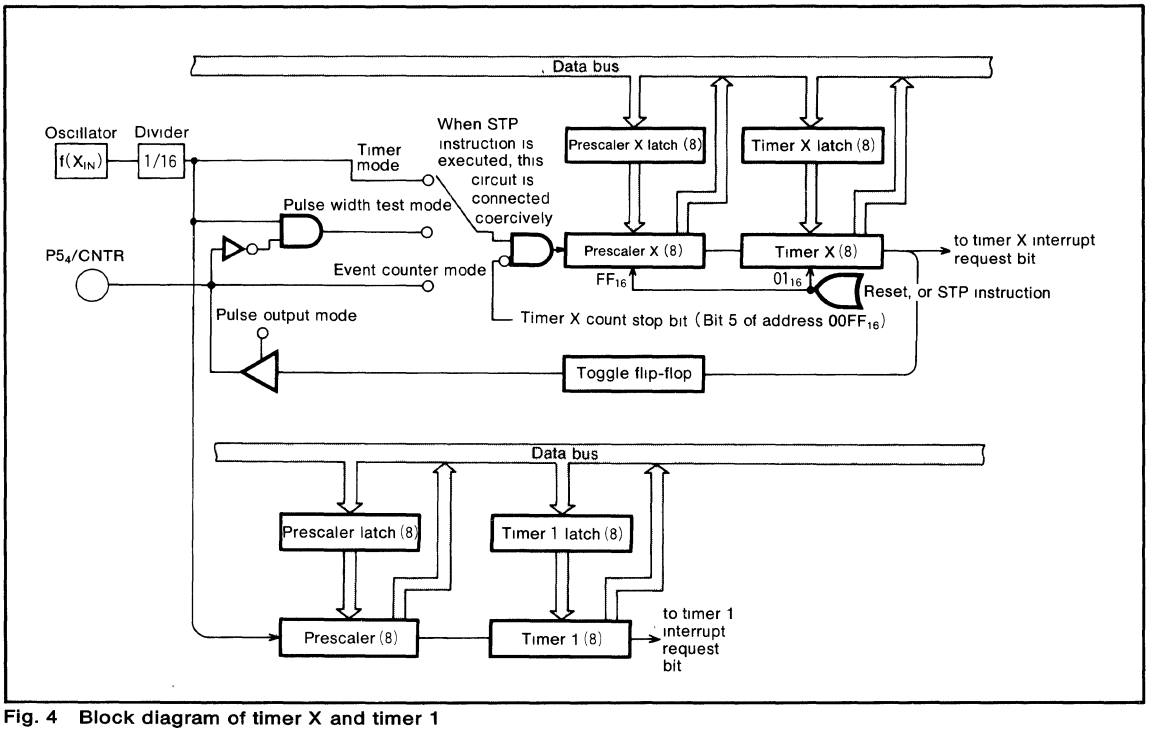


Fig. 4 Block diagram of timer X and timer 1

The four modes of timer X as follows:

(1) Timer mode [00]
In this mode the clock is driven by the oscillator frequency divided by 16. When the timer down-counts to zero, the timer interrupt request bit is set to "1" and the contents of the timer's latch is reloaded into the timer and the counting begins again.

(2) Pulse output mode [01]
In this mode, the polarity of the $P5_4$/CNTR signal is reversed each time the timer down-counts to zero.

(3) Event counter mode [10]
This mode operates in the same manner as the timer mode except the clock source is input to the CNTR pin. This mode will allow an interrupt to be generated whenever a specified number of external events have been generated. The timer down-counts every rising edge of the clock source.

(4) Pulse width measurement mode [11]
This mode measures the pulse width (between lows) input to the $P5_4$/CNTR pin. The timer, driven by the oscillator frequency divided by 16, continues counting during the low cycle of the CNTR pin. When the timer contents reaches "0", the interrupt request bit is set to "1", the timer's reload latch is reloaded and the counting resumes.

The structure of the timer control register is shown in Figure 5.

When the STP instruction is executed, or after reset, the prescaler and timer latch are set to FF_{16} and 01_{16}, respectively. Also, when the STP instruction is executed, the oscillator's frequency (divided by 16) will become the counting source, regardless of the timer X mode setting. This state will be released when the timer X interrupt request bit is set to "1", or after a reset. Timer X will then enter the mode specified by its mode bits. For more details on the STP instruction, refer to the oscillation circuit section.

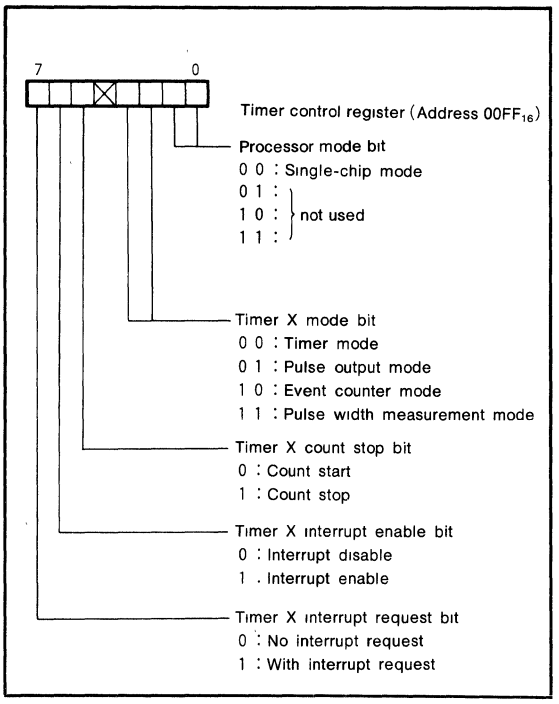


Fig. 5 Structure of timer control register

BUS INTERFACE

The M37416M2-XXXSP is equipped with a bus interface that is functionally similar to the M5L8041-XXXSP. Its operation can be controlled with control signals from the master CPU (slave mode).

The M37416M2-XXXSP bus interface can be connected directly to either a R/$\overline{W}$ type CPU or separate $\overline{RD}$, $\overline{WR}$ type CPU. Figure 7 shows a block diagram of the bus interface function.

Slave mode is selected with data bus buffer control register (address $00F2_{16}$) bit 0 and 1 as shown in Figure 6.

An input buffer full interrupt occurs when data is received from the master CPU and an output buffer empty interrupt occurs when data is read by the master CPU.

In slave mode, ports $P3_0 \sim P3_7$ become a tri-state data bus used to transfer data, commands, and status to and from the master CPU.

Furthermore, ports $P4_4 \sim P4_7$ become master CPU control signal input pins and $P4_1 \sim P4_3$ becomes a slave status output pins.

[Data bus buffer status register] DBBSTS

This is an 8-bit register. Bits 0, 1, and 3 are read-only bits indicating the status of the data bus buffer. Bits 2, 4, 5, 6, and 7 are read/write enabled user-definable flags that can be set with a program. The host CPU can only read these flags by setting the A0 pin to "H".

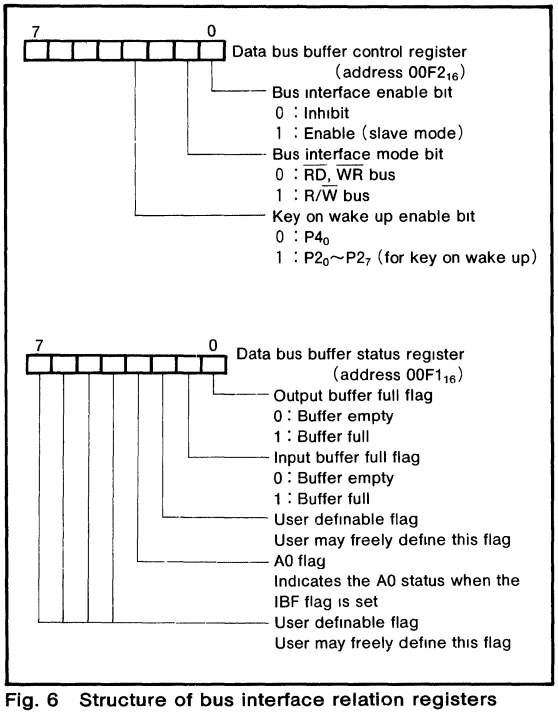


Fig. 6 Structure of bus interface relation registers

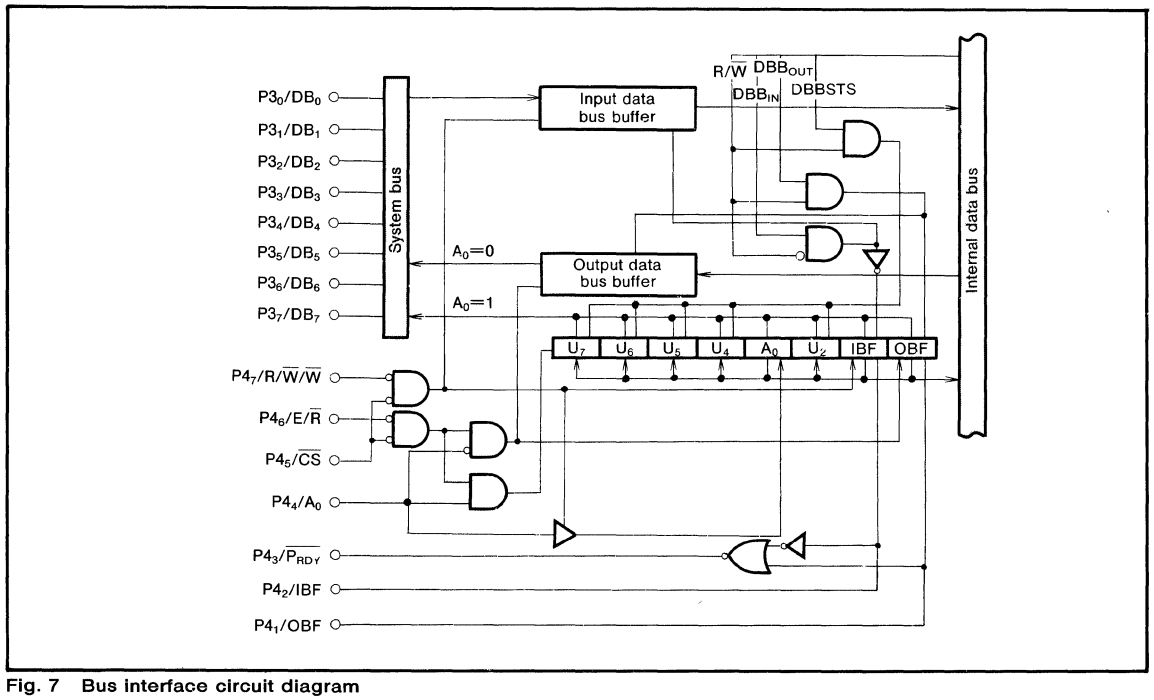


Fig. 7 Bus interface circuit diagram

• Output buffer full flag OBF

This flag is set when data is written in the output data bus buffer and cleared when the host CPU reads the data in the output data bus buffer. It is initialized to "1" at reset and cleared to "0" when the slave mode is selected with the bus interface enable bit set.

• input buffer full flag IBF

This flag is set when the host CPU writes data in the input data bus buffer and cleared when the slave CPU reads the data in the input data bus buffer. This bit is initialized to "0" at reset.

Execute the dummy write instruction to the input data bus buffer to clear this flag from the slave CPU side. The contents of input data bus buffer is not change because it is read only register.

A_0 flag

The level of the A_0 pin is latched when the host CPU writes data in the input data bus buffer.

[Input data bus buffer] DBBIN

Data on the data bus is latched in DBBIN when there is a write request from the host CPU. The data in DBBIN can be read from the data bus buffer register (SFR address $00F0_{16}$).

[Output data bus buffer] DBBOUT

Data is written in DBBOUT by writing data in data bus buffer register (SFR address $00EF_{16}$). The data in DBBOUT is output to the data bus (P5) when the host CPU issues a read request with setting the A_0 pin to "L".

Table 2. Control I/O pin functions when bus interface function is selected

Pin	Name	Bus interface mode bit	Input/ Output	Function
$P4_1$	OBF	—	Output	Status output OBF signal is output
$P4_2$	IBF	—	Output	Status output IBF signal is output
$P4_3$	$\overline{P_{RDY}}$	—	Output	Status output The NOR of OBF and IBE is outnput.
$P4_4$	A_0	—	Input	Address input Used to select between DBBSTS and DBBOUT during host CPU read Also used to identify commands and data during write
$P4_5$	CS	—	Input	Chip select input Used to select the data bus buffer Select when "L"
$P4_6$	$\overline{R}$	0	Input	Timing signal used by the host CPU to read data from the data bus buffer
	E	1	Input	Inputs a timing signal E or inverse of ϕ
$P4_7$	$\overline{W}$	0	Input	Timing signal used by the host CPU to write data to the data bus buffer
	R/$\overline{W}$	1	Input	Input R/$\overline{W}$ signal used to control the data transfer direction When this signal is "L", data bus buffer write is synchronized with the E signal When it is "H", data bus buffer read is synchronized with the E signal

[Transmit operation]

When the send data is written to the transmit buffer register, the start bit, the parity bit, and the stop bit are added to the data, which is transferred to the transmit shift register. The transmit shift register begins shift when it becomes enable for transmission, sending the serial data to TxD pin. For the description of the transmit enable state, see Table 3.

In the transmit enable state, each time transmission of the stop bit of the serial data being transmitted has been completed, it is checked whether the next data has been written to the transmit buffer register. If the data is found written, transmission of the next data begins. If the data is found not written, TxD pin is held at "H" until the next transmit data is written, setting the transmitter empty flag. When the transmit enable state is cleared during transmission, the transmission is stopped after completing the transmisslon of the transmit data so far written to the transmit buffer register.

When the transmitter ready flag (bit 0 of the UART status register) is "1", it indicates that the transmit buffer is ready for writing data. The immediately preceding data is transferred from the transmit buffer register to the transmit shift register. Every time the start bit is output from TxD pin, this flag is set. Every time the transmitter ready flag is set, the UART transmit interrupt request bit (bit 5 of the interrupt request distinguish register) is set. An interrupt is acknowledged when two UART transmit interrupt enable bits (bit 1 of the UART control register, and bit 0 of interrupt control register) are all "1" and the interrupt disable flag I is "0". Interrupt request bit (bit 1 of interrupt control register) is reset when the UART transmit interrupt is accepted.

Note that an interrupt occurs only in the transmit ready state.

Bit 6 of the UART control register initializes the UART transmit side. When this bit "0", the transmit side is in the initial state.

Table 3. Bit and pin status when transmission is ready

TE	CTSE	$\overline{CTS}$
1	0	X
	1	L

TE : UART transmit enable bit
CTSE: $\overline{CTS}$ pin function selection bit
$\overline{CTS}$: $\overline{CTS}$ pin input level

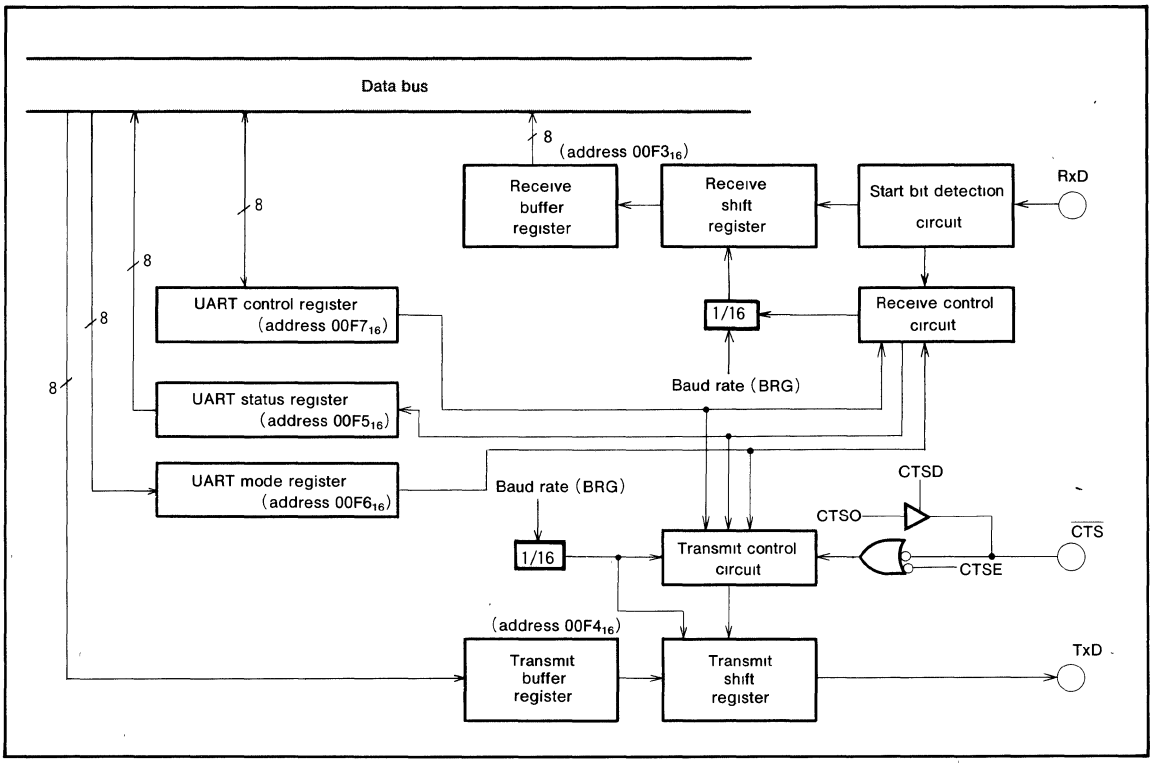


Fig. 8 UART block diagram

UART

The M37416M2-XXXSP contains one channel UART. It has three pins (TxD (transmit output), RxD (receive input) and $\overline{CTS}$ (clear to send)). The three pins RxD, TxD and $\overline{CTS}$ are common with $P5_0$, $P5_1$ and $P5_2$ respectively. $P5_0 \sim P5_2$ are selected to UART function pins when UART enable bit (bit 6 of UART mode register) to "1". And it also has a CLK pin (the input pin of the external clock for band rate generation). This pin is selected as CLK function when the synchronous clock for baud rate generating synchronous clock select bit (bit 5 of UART mode register) is set to "1". An interrupt can be generated at receive and transmit independently.

[Receive operation]

Setting the receive enable bit (bit 2 of the UART control register) to "1" puts the system in the receive ready state. When there is no input of receive data, "H" is input to RxD pin. When the falling edge is input to RxD pin and "L" input is detected twice consecutively by sampling with the clock having a frequency 16 times the baud rate, the start bit is triggered. Then, sampling is performed three time in the middle of the start bit. When "L" is detected twice or more, the receive operation begins, capturing the data bits into the receive shift register. If "L" has not been detected twice or more, start bit detection begins again. When the data bits and parity bit have been captured into the receive shift register and the stop bit is detected, the receive data is transferred from the receive shift register to the receive buffer register, setting the receiver ready flag (bit 1 of the UART status register). If a parity error occurred, the parity error flag is set. The framing error flag is set when the first stop bit is found "L". If the previous data has not been read out of the receive buffer register, the overrun error flag is set, clearing the previous data. Execute the dummy write instruction to the receive buffer register to clear the receiver ready flag. The contents of receive buffer register is not changed because it is read only register. Each error flag can be reset by writing "1" to the error flag reset bit (bit 7 of the UART control register). Any of these errors does not affect the receive operation. The data bit, the parity bit, and the stop bit are sampled three times in the middle of them each. When "L" or "H" is detected twice or more, "0" or "1" is determined respectively.

Each time a receive operation has been completed, setting the receiver ready flag, the UART receive interrupt request bit (bit 1 of the interrupt request distinguish register) is set. An interrupt is acknowledged when the two UART receive interrupt enable bits (bit 2 of interrupt control register and bit 3 of UART control register) are all "1" and the interrupt disable flag 1 is "0". The UART receive interrupt request bit which is in interrupt control register (address $00FE_{16}$) is reset when a UART receive interrupt is acknowledged.

Setting the receive enable bit (bit 2 of the UART control register) to "0" puts the system in the receive stopped state. At this time, the receiver ready flag is "0" (ready), the receive shift register is in the stopped state, and the start bit detection is stopped.

[UART divider for baud rate generator]

This is an 8-bit programmable divider which generates the baud rate for the UARTi receive or transmit operation.

When the setting value is N_{BR} (0 to 255), the divide ratio becomes $1/(N_{BR}+1)$. There are three count sources; X_{IN} clock divided by 2, X_{IN} clock divided by 32, and the external clock. Choose sources by bits 4 and 5 of the UARTi mode register. Table 4 shows the baud rate calculation and example for each bit combination.

When the external clock is used, the frequency of the input clock must be below 1.6 MHz. Writing to the baud rate generating divider must be performed when bits 2 and 6 of the UARTi control register are both "0".

Table 4. Baud rate calculation and example

EX	BR	Calculation	Count source	Baud rate
0	0	baud rate(bps)$=\frac{f(X_{IN})}{32(N_{BR}+1)}$	$f(X_{IN})$=8.0 MHz	250000 bps
0	1	baud rate(bps)$=\frac{f(X_{IN})}{512(N_{BR}+1)}$	$f(X_{IN})$=7.3728 MHz	4800 bps
1	X	baud rate(bps)$=\frac{f(CLK)}{16(N_{BR}+1)}$	$f(X_{IN})$=1.536 MHz	9600 bps

EX : Clock selection bit for baud rate generator
BR : Divide ratio selection bit for baud rate generator

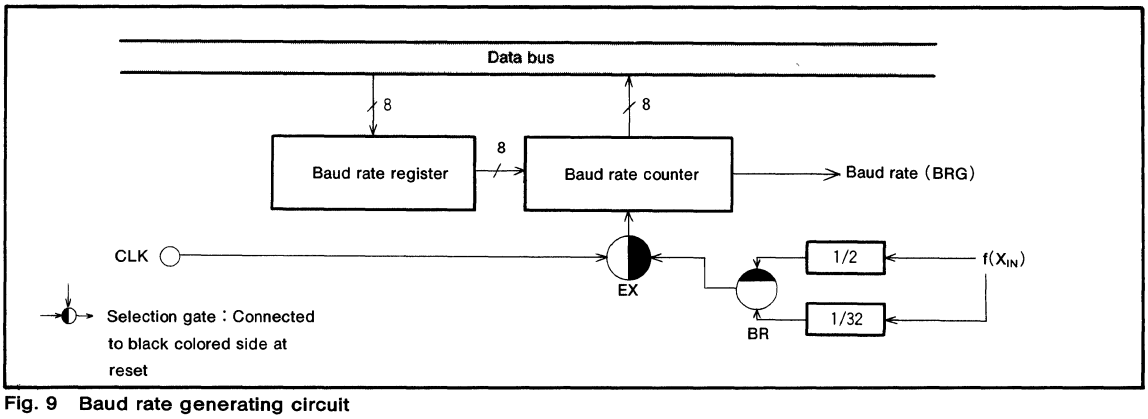


Fig. 9 Baud rate generating circuit

[$\overline{\text{CTS}}$ pin]

The $\overline{\text{CTS}}$ pin can be used as the 1-bit I/O port when bit 4 of the UART control register is "0". In this case, the input/output direction can be determined by bit 7 of the UART mode register and the output data can be set by bit 5 of the UART control register. Additionally, the input level can be known by bit 7 of the UART status register.

[UART mode register]

This register except the bit 6 is write-only register and cannot be read out. Use the LDM instruction to write to this register.

· Parity enable bit: PEN

Setting this bit to "1" adds a parity bit to the transmit data. In a receive operation, this bit is used for parity evaluation.

· Parity select bit: EVN

This bit specifies the parity bit to be generated in a transmit operation and the parity bit to be evaluated in a receive operation. Depending on the content of this bit, the number of 1's in data is made even or odd.

· Character length select bit: CHL

This bit specifies the character length of data.

· Stop bit length select bit: ST

This bit specifies the stop bit length.

· Baud rate generating prescaler divide ratio select bit: BR

When this bit is "0", the signal obtained by dividing X_{IN} clock by 2 becomes the count source of the baud rate divider. When this bit is "1", the signal is obtained by dividing the clock by 32.

· Baud rate generating synchronous clock selection bit: EX

This bit specifies baud rate synchronous clock. When this bit is "1", external clock is input from the clock pin.

· UART enable bit: UARTE

$P5_0 \sim P5_2$ is selected UART function when this bit is "1".

· $\overline{\text{CTS}}$ pin I/O select bit: CTSD

When this bit is "0", the CTSi pin is the input pin.

When this bit is "1", the pin is the output pin. To use the $\overline{\text{CTS}}$ pin as the $\overline{\text{CTS}}$ input, set "0".

[UART control register]

· Transmit enable bit: TE

Setting this bit to "1" enables a transmit operation.

· Transmit interrupt enable bit: TIE

When this bit is "1", the interrupt in a transmit operation is enabled.

· Receive enable bit: RE

Setting this bit to "1" enables a receive operation.

· Receive interrupt enable bit: RIE

When this bit is "1", the interrupt in a receive operation is enabled.

· $\overline{\text{CTS}}$ pin function select bit: CTSE

When this bit is "1", the $\overline{\text{CTS}}$ pin becomes the $\overline{\text{CTS}}$ input.

· $\overline{\text{CTS}}$ output data select bit: CTSO

When this bit is "0", "L" is output. When it is "1", "H" is output.

· Transmit side initialize bit: MR

When this bit is "0", the transmit side is initialized.

· Error flag reset select bit: ERST

Setting this bit to "1" resets all error flags. When this bit is read, "0" is always read.

[UART status register]

· Transmitter ready flag: TxRDY

When this flag is "1", it indicates that the transmit buffer register is empty and ready for writing transmit data.

· Receiver ready flag: RxRDY

When this flag is "1", it indicates that the receive buffer register is holding receive data. When the receive buffer register is read, it is cleared.

· Transmitter empty flag: TEMP

When this flag is "1", it indicates that neither the transmit shift register nor the transmit buffer register hold the data to be transmitted.

· Parity error flag: PE

This bit is set to "1" when the parity of the received data is different from the parity which was set.

· Overrun error flag: OR

When this flag is "1", it indicates that, before the data in the receive buffer register is read, the next data is transferred from the receive shift register to the receive buffer register and the previous data is lost.

· Framing error flag: FE

This flag is set to "1" when the stop bit is found "L" when data is transferred from the receive shift register to the receive buffer register.

· $\overline{\text{CTS}}$ pin input level flag: $\overline{\text{CTS}}$

When the input level of the $\overline{\text{CTS}}$ pin is "L", "0" is read, when it is "H", "1" is read.

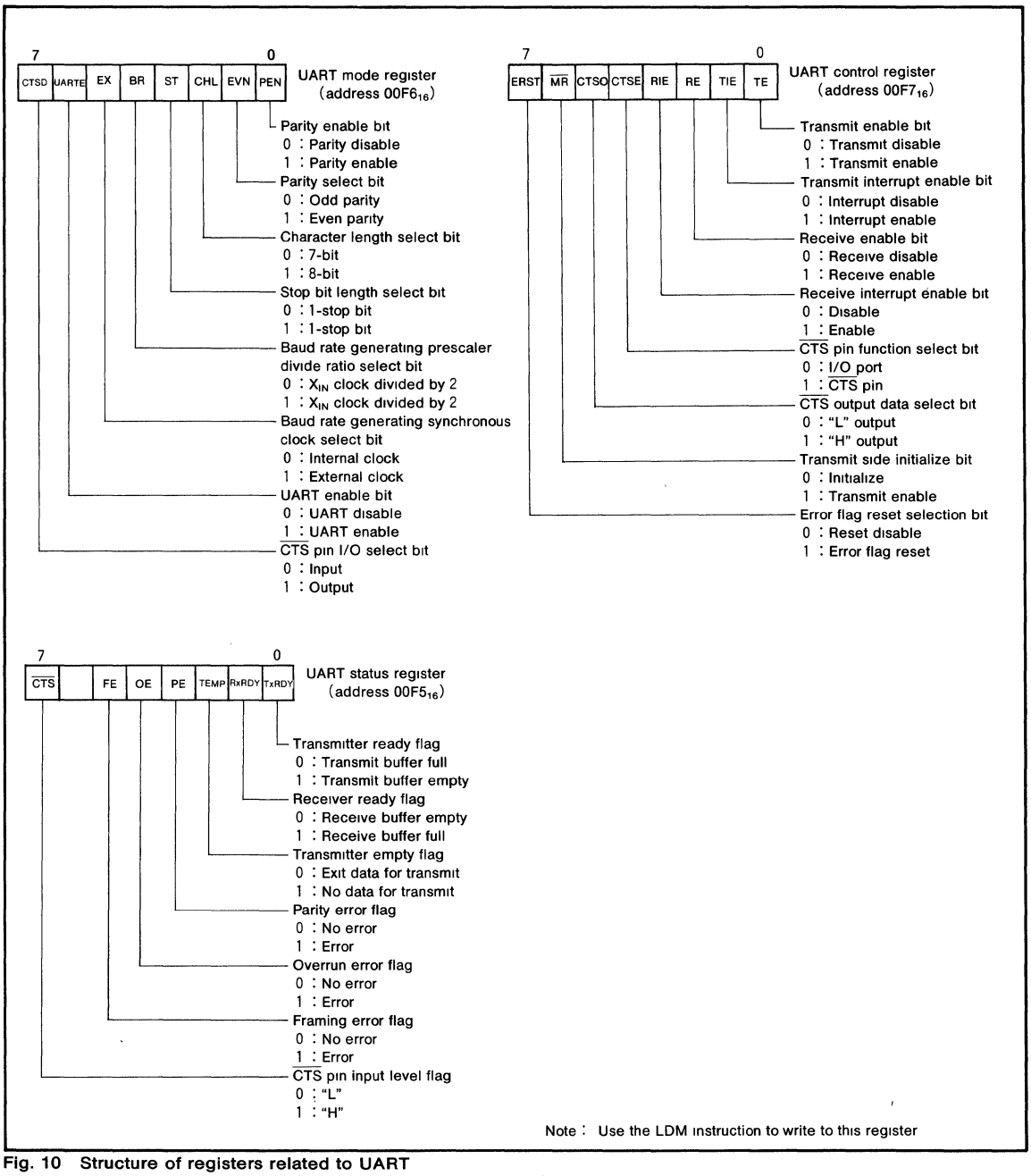


Fig. 10 Structure of registers related to UART

COMPARATOR CIRCUIT

The comparator circuit is shown in Figure 11. The comparator circuit consists of the switch tree, ladder resistor, comparator, comparator control circuit, comparator control register (address $00EC_{16}$), comparator data register (address $00FD_{16}$), and analog signal input pins, $P2_0 \sim P2_7$.

These analog input pins are common with the digital input/output terminal to the data bus.

The 3-bit comparator register can generate $1/8V_{CC}$-step internal analog voltage, based on the settings of bits 0 to 2.

Table 5 gives the relation between the descriptions of comparator register bits 0 to 2 and the generated internal analog voltage. The comparator result of the analog input voltage and the internal analog voltage is stored in the comparator data register.

The digital value corresponding to the internal analog voltage to be compared is written in the comparator control register (address $00FC_{16}$), bits 0 to 2. The voltage comparision starts as soon as the writing is completed. 4-cycle (required for comparating) later, the result of comparision is stored in the comparator data register. Each bit of comparator data register is "1" when analog input voltage > internal analog voltage and "0" when analog input voltage < internal analog voltage.

When voltage is compared to by setting bits 0 to 2 of the comparator register "0", each bit of the comparator data register becomes "1" regardless of the analog input voltage. The reference voltage is generated for 4 cycles, when ladder resistor is ON. The ladder resistor is OFF for current power save, when the comparator does not operate.

Since the comparator consists of the capacitive coupled configuration, f (X_{IN}) is needed larger than 1MHz during comparision.

Table 5. Relationship between the contents of comparator register and internal voltage

Comparator register			Internal analog voltage
bit 2	bit 1	bit 0	
0	0	1	$1/8V_{CC}-1/16V_{CC}$
0	1	0	$2/8V_{CC}-1/16V_{CC}$
0	1	1	$3/8V_{CC}-1/16V_{CC}$
1	0	0	$4/8V_{CC}-1/16V_{CC}$
1	0	1	$5/8V_{CC}-1/16V_{CC}$
1	1	0	$6/8V_{CC}-1/16V_{CC}$
1	1	1	$7/8V_{CC}-1/16V_{CC}$

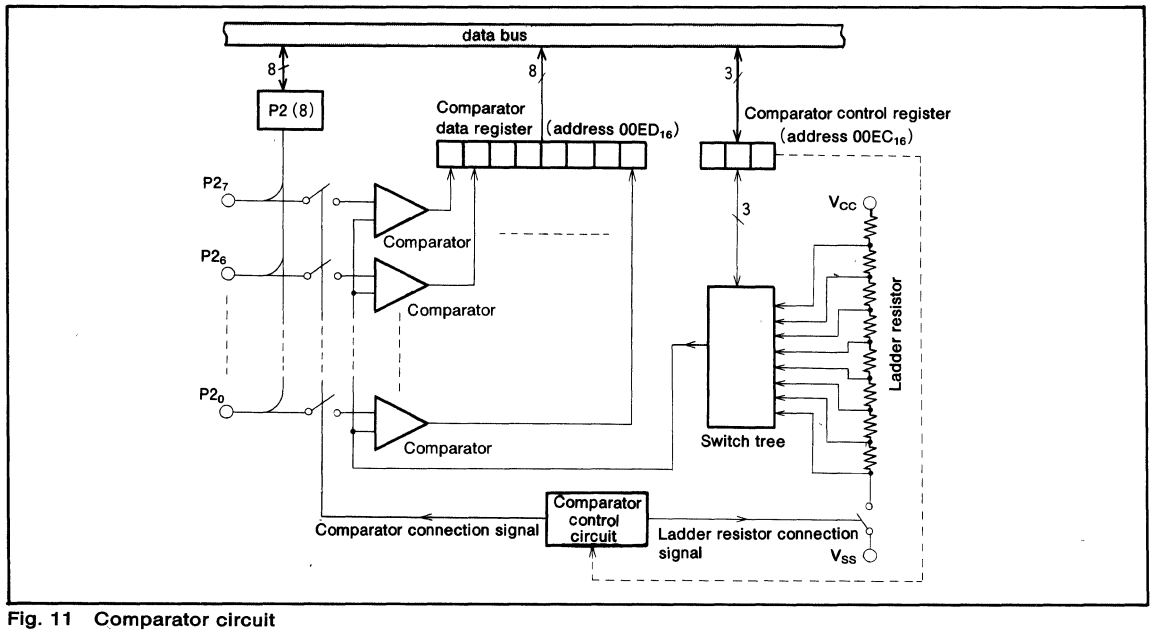


Fig. 11 Comparator circuit

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KEY ON WAKE UP

"Key on wake up" is one way of returning from a power down state caused by the STP or WIT instruction. If any terminal of port P2 has a "L" level applied, after bit 3 of the data bus buffer control register (KWE) is set to "1", an interrupt is generated and the microcomputer is returned to the normal operating state. As shown in Figure 12, a key matrix can be connected to port P2 and the microcomputer can be returned to a normal state by pushing any key.

The key on wake up interrupt is common with the $\overline{INT_0}$ interrupt. When KWE is set to "1", the key on wake up function is selected. However, key on wake up cannot be used in the normal operating state. When the microcomputer is in the normal operating state, both key on wake up and $\overline{INT_0}$ are invalid.

In order to enter the power down state generated by the STP or WIT instruction at the interrupt disable flag (I) is "0" and KWE is "1", all of port P2 must be input "H".

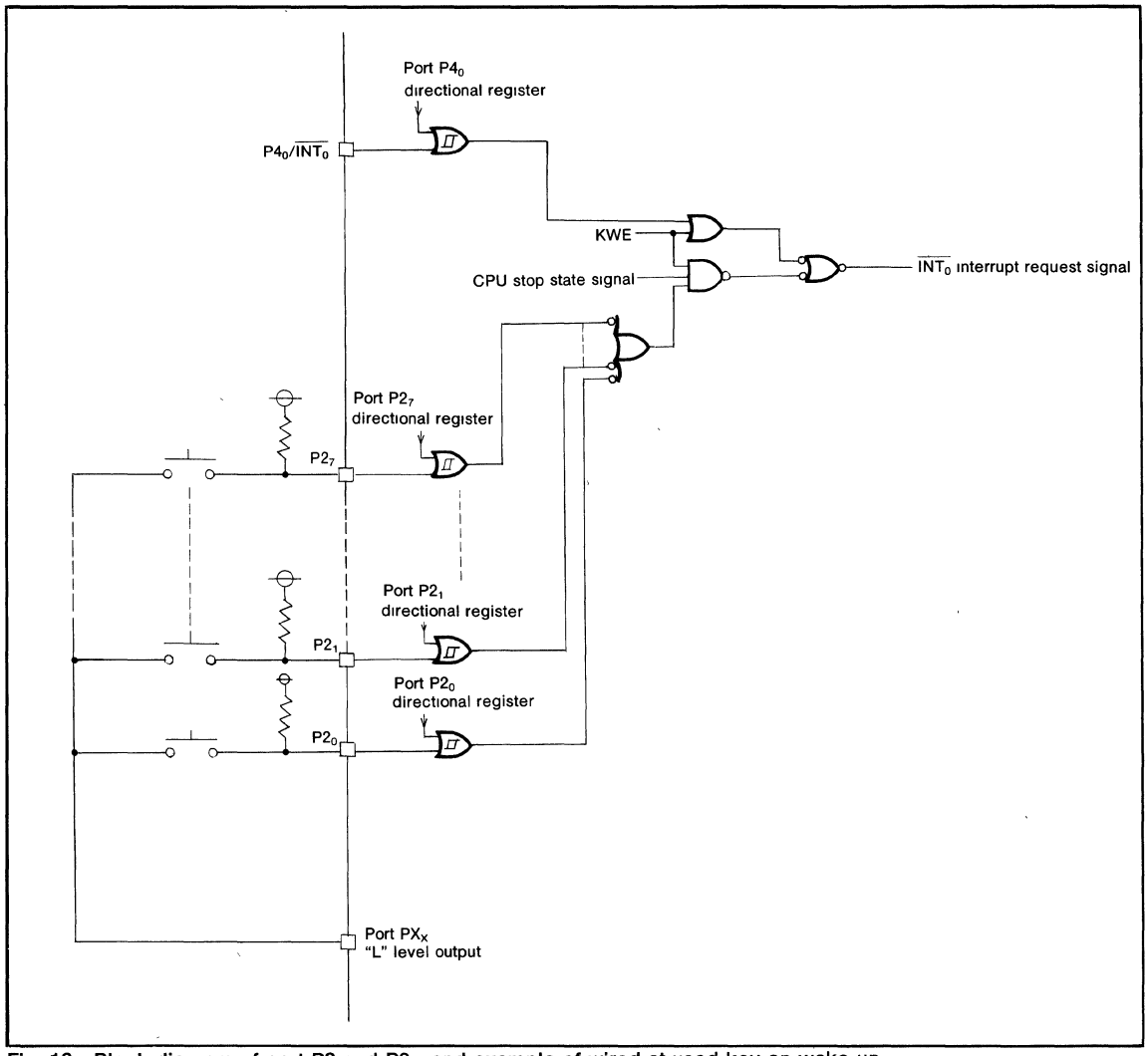

Fig. 12 Block diagram of port P2 and P3$_2$, and example of wired at used key on wake up

RESET CIRCUIT

The M37416M2-XXXSP is reset according to the sequence shown in Figure 15. It starts the program from the address formed by using the content of address $1FFF_{16}$ as the high order address and the content of the address $1FFE_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for more than $2\mu s$ while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 14.
An example of the reset circuit is shown in Figure 13.
When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

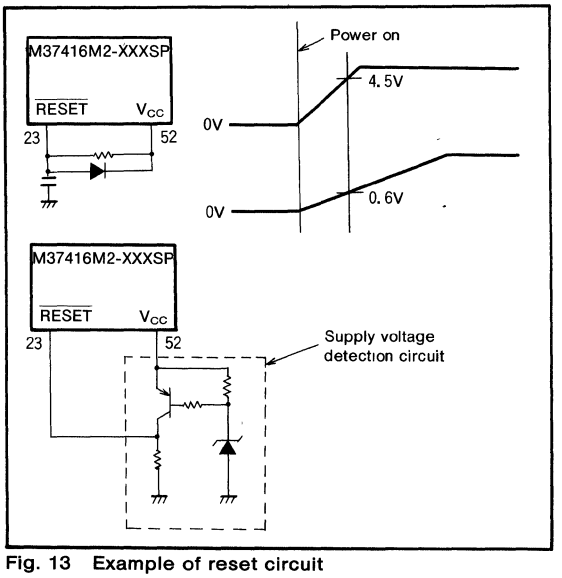

Fig. 13 Example of reset circuit

		Address	
(1)	Port P0 directional register	$(E1_{16})$···	00_{16}
(2)	Port P1 directional register	$(E3_{16})$···	00_{16}
(3)	Port P2 directional register	$(E5_{16})$···	00_{16}
(4)	Port P3 directional register	$(E7_{16})$···	00_{16}
(5)	Port P4 directional register	$(E9_{16})$···	00_{16}
(6)	Port P5 directional register	(EB_{16})···	— — — 0 0 0 0 0
(7)	Comparator control register	(EC_{16})···	00_{16}
(8)	Interrupt request distinguish register	(EE_{16})···	00_{16}
(9)	Data bus buffer status register	$(F1_{16})$···	X X X X X X 0 1
(10)	Data bus buffer control register	$(F2_{16})$ ··	0 0 0 0 X 0 0 0
(11)	UART mode register	$(F6_{16})$···	00_{16}
(12)	UART control register	$(F7_{16})$···	X 0 0 0 0 0 0 0
(13)	Prescaler X	(FC_{16})···	FF_{16}
(14)	Timer X	(FD_{16})···	01_{16}
(15)	Interrupt control register	(FE_{16})···	00_{16}
(16)	Timer control register	(FF_{16})···	0 0 0 X 0 0 0 0
(17)	Interrupt disable flag for processor status register	(PS)···	1
(18)	Program counter	(PC_H)···	Contents of address $1FFF_{16}$
		(PC_L)···	Contents of address $1FFE_{16}$

Since the contents both registers other than those listed above and the RAM are undefined at reset, it is necessary to set initial values
Note : * means mask option

Fig. 14 Internal state of microcomputer at reset

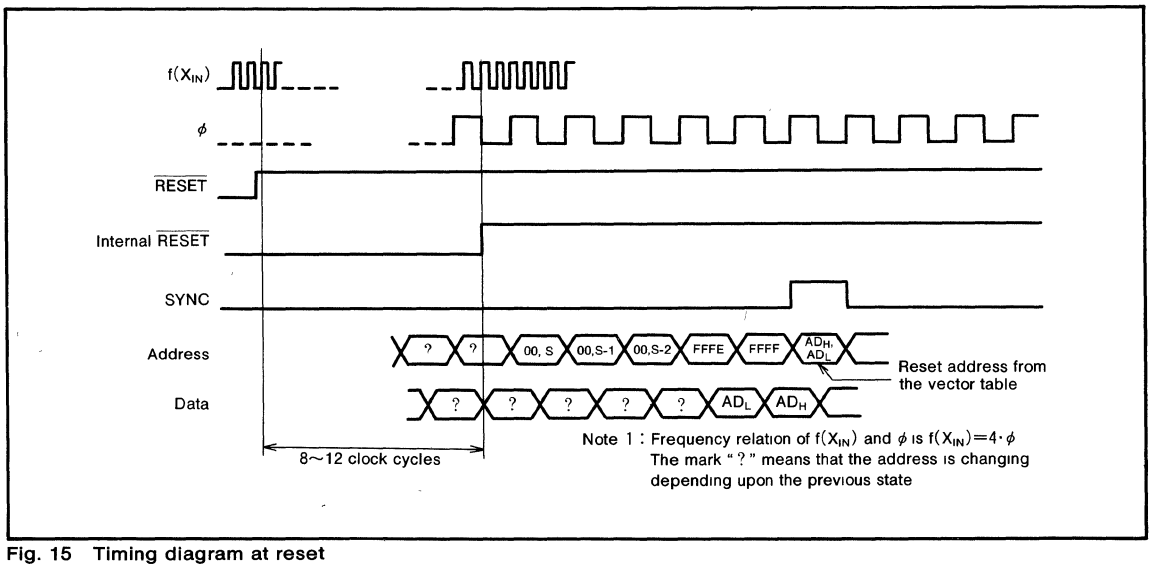

Fig. 15 Timing diagram at reset

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I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS output.

As shown in the memory map (Figure 1), port P0 can be accessed at zero page memory address $00E0_{16}$. Port P0 has a directional register (address $00E1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

(2) Port P1

Port P1 has the same function as port P0. The I/O level is TTL compatible.

(3) Port P2

Port P2 has the same function as P0. Following the execution of STP or WIT instruction, P2 can be used to generate the "wake up mode". This mode is used to bring the microcomputer back in its normal operating mode after being in the power-down mode. Also this port has comparator function. For more detailes, see the comparator information.

(4) Port P3

This is an 8-bit I/O port with function similar to port P0. When slave mode is selected with a program, all ports change to the data bus for the master CPU. In this case, port input/output is unaffected by the directional register. The I/O level is TTL compatible.

(5) Port P4

This is an 8-bit input/output port with function similar to port P0. When slave mode is selected with a program, ports $P4_1 \sim P4_7$ change to the control bus for the bus interface function. In this case, port input/output is unaffected by the directional register.

Port $P4_0$ are shared with the external interrupt input pin ($\overline{INT_0}$). The $\overline{INT_0}$ interrupt constantly monitors the status of this port and generates an interrupt at a valide edge. Therefore, if the $\overline{INT_0}$ interrupt is not used, it must be disabled and if it is used, this port must be set to input. The I/O level of port P4 is TTL compatible except the case that the input level of some ports which function as $\overline{INT_0}$. A_0 or $\overline{CS}$ are CMOS compatible.

(6) Port P5

Port P5 is an 5-bit I/O port with function similar to port P0. All pins have program selectable dual functions. When a UART function is selected, the input and output from pins $P5_0 \sim P5_3$ are determined by the contents of the UART mode register and UART control register.

Port $P5_4$ is common with CNTR pin.

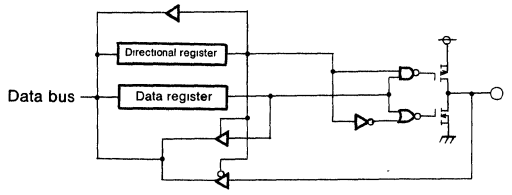
The I/O level is TTL compatible except the case when some ports which function as RxD, $\overline{CTS}$, CLK and CNTR are CMOS compatible.

(7) Clock ϕ output pin

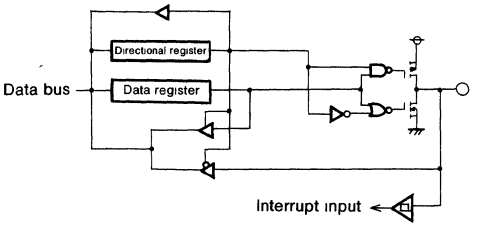
This is the timing output pin. When selected the main clock (X_{IN}-X_{OUT}) as the internal system clock, the clock frequency divided by four is outputed.

"H" is output from this pin when STP or WIT instruction is executed.

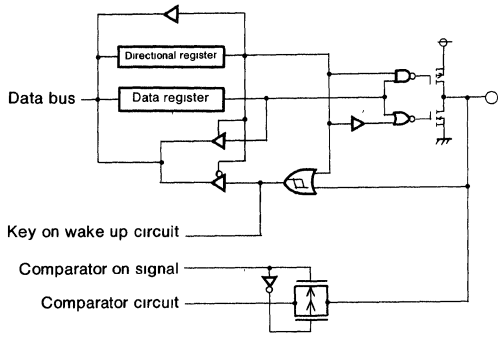
Port P0, P1



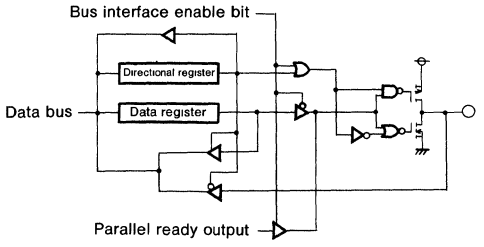
$P4_0$



Port P2

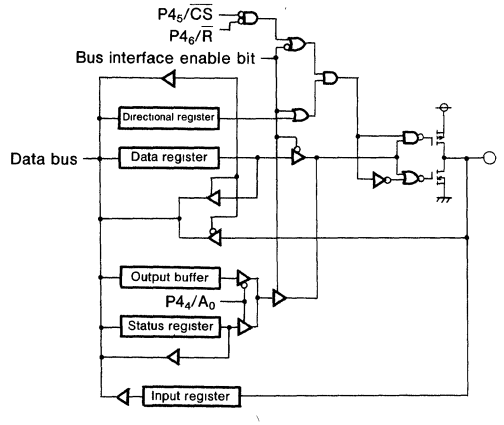


$P4_1 \sim P4_3$



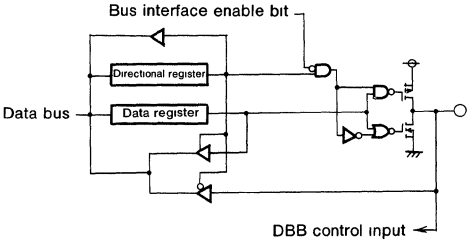
DBB control output $P4_1$……OBS output
$P4_2$……$\overline{IBS}$ output
$P4_3$……$P_{\overline{RDY}}$ output

$P3_0 \sim P3_7$



①$P3_0$ does not have a status register and OBF flag is set
②$P3_1$ does not have a status register and IBF flag is set.
③$P3_3$ does not have a status register and A_0 flag is set

$P4_4 \sim P4_7$



DBB control input $P4_4$……A_0 input
$P4_5$……$\overline{CS}$ input
$P4_6$……R/$\overline{E}$ input
$P4_7$……$\overline{W}$/R/$\overline{W}$ input

Fig. 16 Ports P0~P6 block diagram

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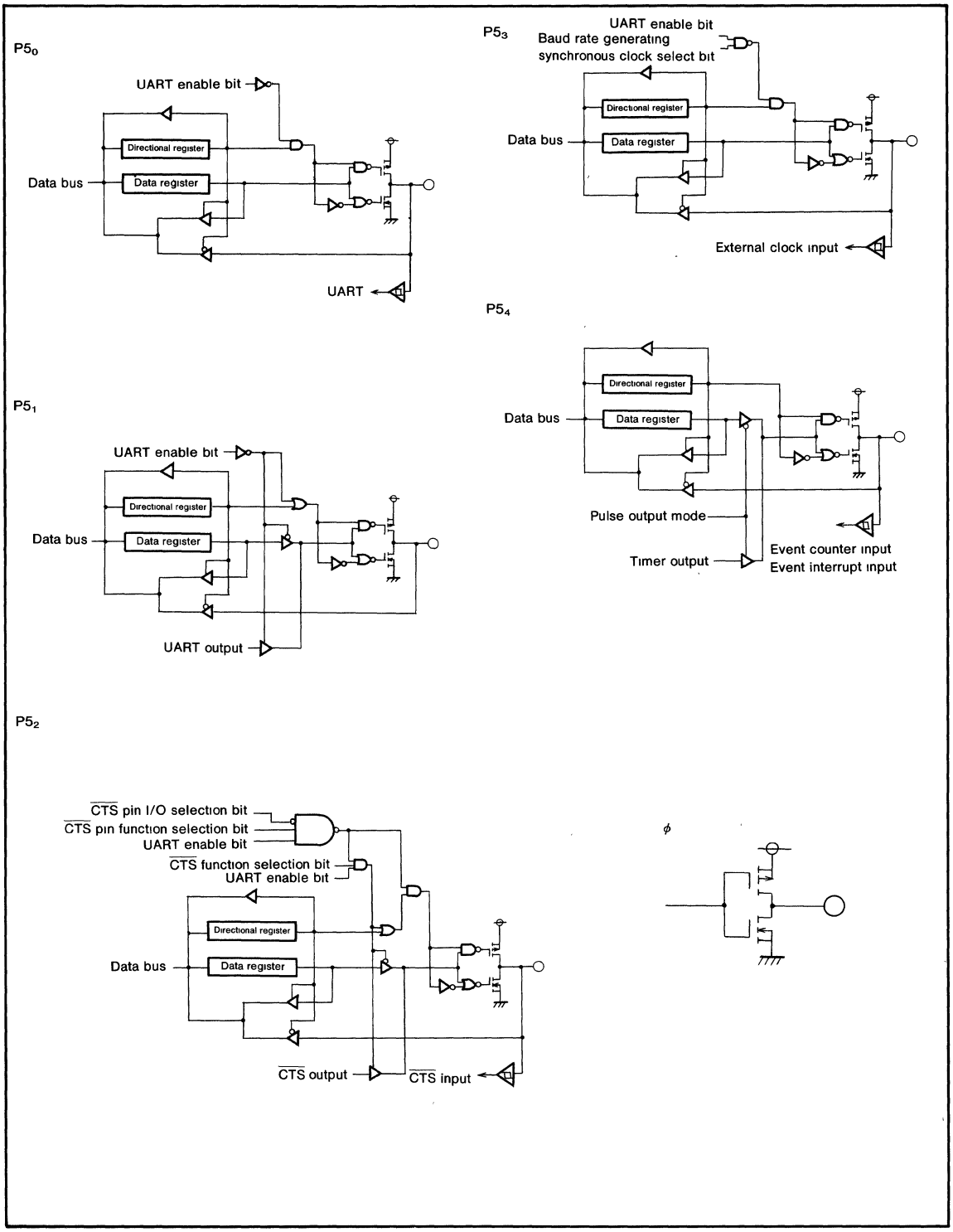

Fig. 17 Ports P5 and φ block diagram

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 21.

When the STP instruction is executed, the oscillation of internal clock ϕ is stopped in the "H" state.

Also, the prescaler X and timer X are loaded with FF_{16} and 01_{16}, respectively. The oscillator (dividing by 16) is then connected to the prescaler input. This connection is cleard when timer X overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the internal clock ϕ keeps its "H" level until timer X overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction. Especially, to return from the stop status, the timer X count stop bit (bit 5 of address $00FF_{16}$) must be set to "0" before executing STP instruction.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figures 18 and 19.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock uasge is shown in Figure 20. X_{IN} is the input, and X_{OUT} is open.

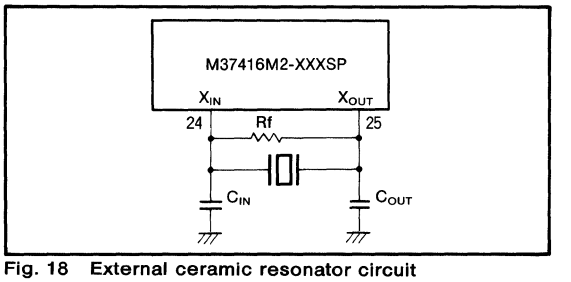

Fig. 18 External ceramic resonator circuit

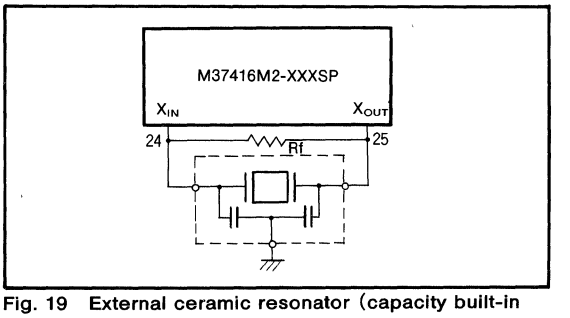

Fig. 19 External ceramic resonator (capacity built-in type) circuit

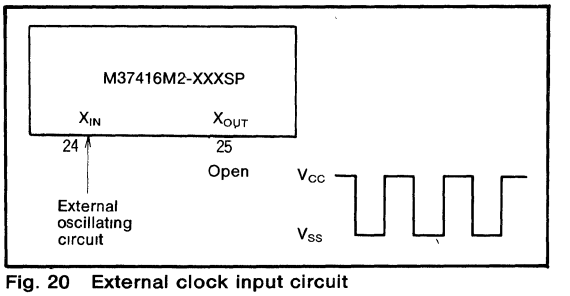

Fig. 20 External clock input circuit

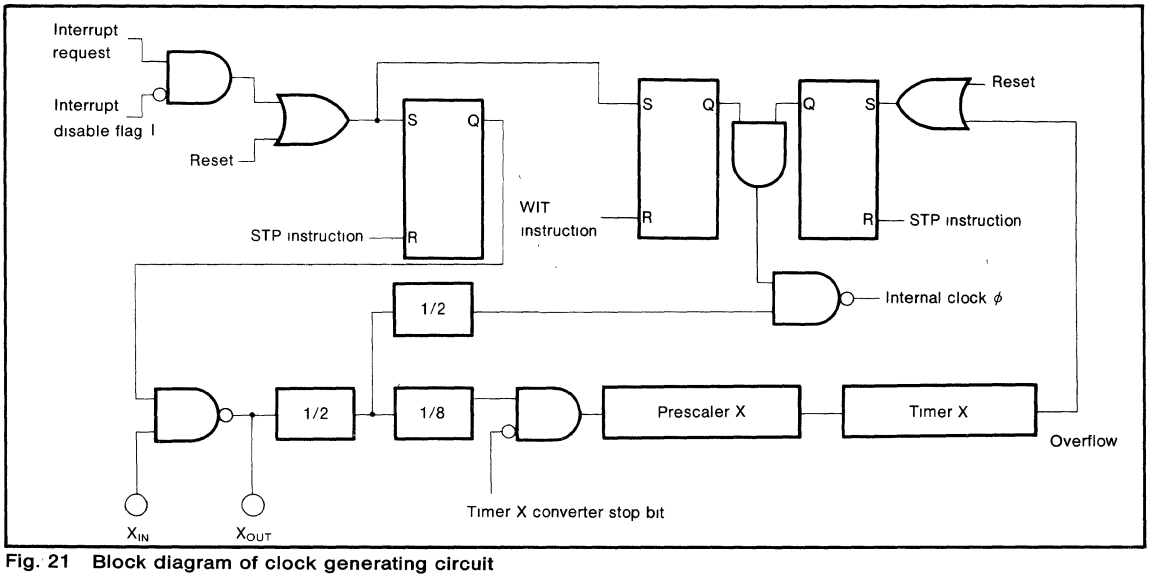

Fig. 21 Block diagram of clock generating circuit

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PROGRAMMING NOTES

(1) The frequency ratio of the timer and the prescaler is 1/(n+1).

(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) When the timer X or timer 1 is input the clock except $\phi/4$ or it divided by timer, read the contents of these timers either while the input of these timers are not changing or after counting of timers are stopped.

(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.

(5) A NOP instruction must be used after the execution of a PLP instruction.

(6) The STP instruction must be executed after setting timer X count enable bit to enable "0", timer X interrupt enable bit to inhibit ("0"), and timer X interrupt request bit to no request ("0").

(7) Use the LDA (immidiate, T = 1) instruction to modify the interrupt request distinguish register. SEB and CLB instructions can be used only when interrupts in the register are not generated at executing these instructions.

(8) Do not write any data into an address where no register nor port is assigned.

(9) The power current is max. 10mA in DC. However, because a rush current and a bus charge-discharge current flow transiently, a bypass capacitor must be connected between V_{SS} and V_{CC}.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- mask ROM order confirmation form
- mark specification form
- ROM data·····EPROM 3 sets

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "off" state.	−0.3∼7	V
V_I	Input voltage X_{IN}, $\overline{RESET}$		−0.3∼7	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_4$, CNV_{SS}		−0.3∼V_{CC}+0.3	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_4$, X_{OUT}, ϕ		−0.3∼V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000(Note 1)	mW
Topr	Operating temperature		−10∼70	℃
Tstg	Storage temperature		−40∼125	℃

Note 1 : 500mW in case of the flat package

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=−10∼70℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, CNV_{SS} (Note 1)	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P1_0$∼$P1_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_4$, (expect Note 1)	2.0		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$, $P2_0$∼$P2_7$ (Note 2)	0.7V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage CNV_{SS} (Note 1)	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $P1_0$∼$P1_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_4$, (expect Note 1)	0		0.8	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$	0		0.3V_{CC}	V
V_{IL}	"L" input voltage $P2_0$∼$P2_7$ (Note 2)	0		0.26V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_4$			10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_4$ (Note 3)			5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_4$			−10	mA
$I_{OH(avg)}$	"H" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P5_0$∼$P5_4$ (Note 3)			−5	mA
$f(x_{IN})$	Internal clock oscillating frequency	1		8	MHz

Note 1 : Ports operating as special function pins INT_0($P4_0$), A_0($P4_0$), $\overline{CS}$($P4_5$), RxD($P5_0$), CTS($P5_2$), CLK($P5_3$), CNTR

2 : See comparator characteristics for input voltage as comparator input

3 : The total of I_{OL} of Port P0, P1, P2 and ϕ should be 40mA (max.).
The total of I_{OL} of Port P3 and P5 should be 40mA (max)
The total of I_{OH} of Port P0, P1, P2 andϕ should be 40mA (max).
The total of I_{OH} of Port P3 and P5 should be 40mA (max.)

ELECTRIC CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}= 0 V, T_a=−10~70℃, f(X_{IN})=8MHz)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	"H" output voltage ϕ	I_{OH} =− 2 mA	V_{CC}−1			V
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_4$	I_{OH} =− 5 mA	V_{CC}−1			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_4$	I_{OL} =2 mA			0.45	V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P5_0$~$P5_4$	I_{OL} =5 mA			1	V
V_{T+} − V_{T-}	Hysteresis $P2_0$~$P2_7$, INT_0($P4_0$), A_0($P4_4$), $\overline{CS}$($P4_5$), RxD($P5_0$), $\overline{CTS}$($P5_2$), CLK($P5_3$), CNTR	Function input level	0.3		1	V
V_{T+} − V_{T-}	Hysteresis $\overline{RESET}$				0.7	V
V_{T+} − V_{T-}	Hysteresis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_4$, $\overline{RESET}$, X_{IN}	V_I =V_{SS}	−5		5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_4$, $\overline{RESET}$, X_{IN}	V_I =V_{CC}	−5		5	μA
V_{RAM}	RAM retention voltage	At stop mode	2			V
I_{CC}	Supply current	f(X_{IN})=8MHz, At system operation, comparator not operation			10	mA
		f(X_{IN})=8MHz, Comparator is operation, At system operation, square wave			15	mA
		At stop mode (Note 1), Ta=25℃			1	μA
		At stop mode (Note 1), Ta=70℃			10	μA

Note 1 : Output pin ϕ is open V_{SS} is inputs to ports Comparator conversion is complete condition

COMPARATOR CHARACTERISTICS (V_{CC}=5V±5%, V_{CC}=0V, T_a=25℃, f(X_{IN})=8MHz)

Parameter	Limits			Unit
	Min.	Typ	Max	
Resolution	—	—	(1/8)V_{CC}	V
Internal analog voltage error	—	—	±(1/8)V_{CC}	V
Analog input voltage	0	—	V_{CC}	V

TIMING REQUIREMENTS

Port/single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	Fig 22	200			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time		200			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time		200			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time		200			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time		200			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time		200			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		40			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		40			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		40			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		40			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		40			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time		40			ns
$t_C(X_{IN})$	External clock input cycle time		125		1000	ns
$t_W(X_{IN}L)$	External clock input "L" pulse width		30			ns
$t_W(X_{IN}H)$	External clock input "H" pulse width		30			ns
$t_r(X_{IN})$	External clock rising edge time				20	ns
$t_f(X_{IN})$	External clock falling edge time				20	ns

Master CPU bus interface timing ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{su(CS-R)}$	$\overline{CS}$ setup time	Fig 23	0			ns
$t_{su(CS-W)}$	$\overline{CS}$ setup time		0			ns
$t_{h(R-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{h(W-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-R)}$	A_0 setup time		40			ns
$t_{su(A-W)}$	A_0 setup time		40			ns
$t_{h(R-A)}$	A_0 hold time		10			ns
$t_{h(W-A)}$	A_0 hold time		10			ns
$t_{W(R)}$	Read pulse width		160			ns
$t_{W(W)}$	Write pulse width		160			ns
$t_{su(D-W)}$	Date input setup time before write		100			ns
$t_{h(W-D)}$	Date input hold time after write		10			ns

Master CPU bus interface timing (R/$\overline{W}$ type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{su(CS-E)}$	$\overline{CS}$ setup time	Fig 23	0			ns
$t_{h(E-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-E)}$	A_0 setup time		40			ns
$t_{h(E-A)}$	A_0 hold time		10			ns
$t_{su(RW-E)}$	R/$\overline{W}$ setup time		40			ns
$t_{h(E-RW)}$	R/$\overline{W}$ hold time		10			ns
$t_{W(EL)}$	Enable clock "L" pulse width		160			ns
$t_{W(EH)}$	Enable clock "H" pulse width		160			ns
$t_{r(E)}$	Enable clock rising edge time				25	ns
$t_{f(E)}$	Enable clock falling edge time				25	ns
$t_{su(D-E)}$	Data input setup time before write		100			ns
$t_{h(E-D)}$	Data input hold time after write		10			ns

SWITCHING CHARACTERISTICS

Port/single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, f(X_{IN})=8MHz unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ.	Max.	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig 22			200	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				200	ns
$t_{d(\phi-P5Q)}$	Port P5 data output delay time				200	ns

Master CPU bus interface ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, f(X_{IN})=8MHz unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max	
$t_{a(R-D)}$	Data output enable time after read	Fig 23			120	ns
$t_{v(R-D)}$	Data output disable time after read		10		85	ns
$t_{PHL(R-OBF)}$	OBF output transmission time after read				150	ns
$t_{PLH(R-PR)}$	$\overline{P_{RDY}}$ output transmission time after read				150	ns
$t_{PHL(W-IBF)}$	IBF output transmission time after write				150	ns
$t_{PLH(W-PR)}$	$\overline{P_{RDY}}$ output transmission time after write				150	ns

Master CPU bus interface (R/$\overline{W}$ type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, f(X_{IN})=8MHz unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ.	Max	
$t_{a(E-D)}$	Data output enable time after read	Fig.23			120	ns
$t_{v(E-D)}$	Data output disable time after read		10		85	ns
$t_{PHL(E-OBF)}$	OBF output transmission time after E clock				150	ns
$t_{PLH(E-IBF)}$	IBF output transmission time after E clock				150	ns
$t_{PLH(E-PR)}$	$\overline{P_{RDY}}$ output transmission time after E clock				150	ns

TEST CONDITION

Input voltage level : V_{IH} 2.4V

V_{IL} 0.4V

Output test level : V_{OH} 2.0V

V_{OL} 0.8V

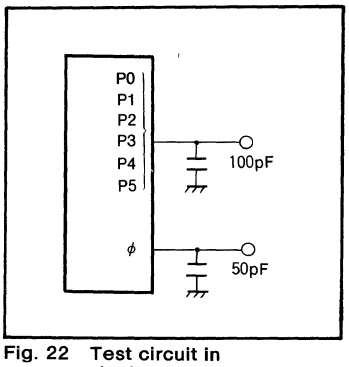


Fig. 22 Test circuit in single-chip mode

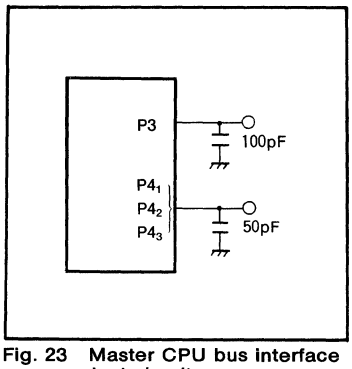
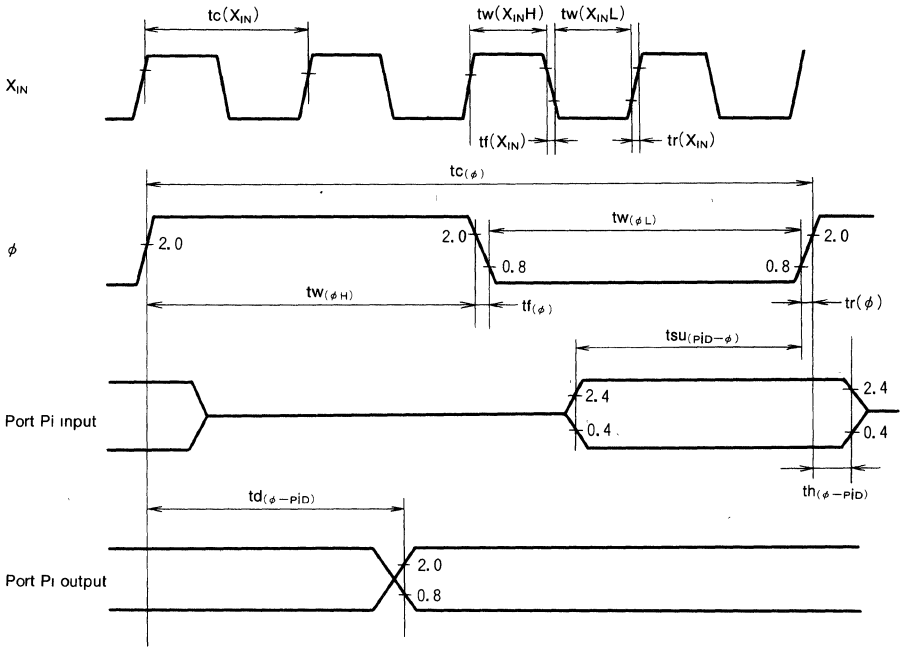


Fig. 23 Master CPU bus interface test circuit

TIMING DIAGRAM

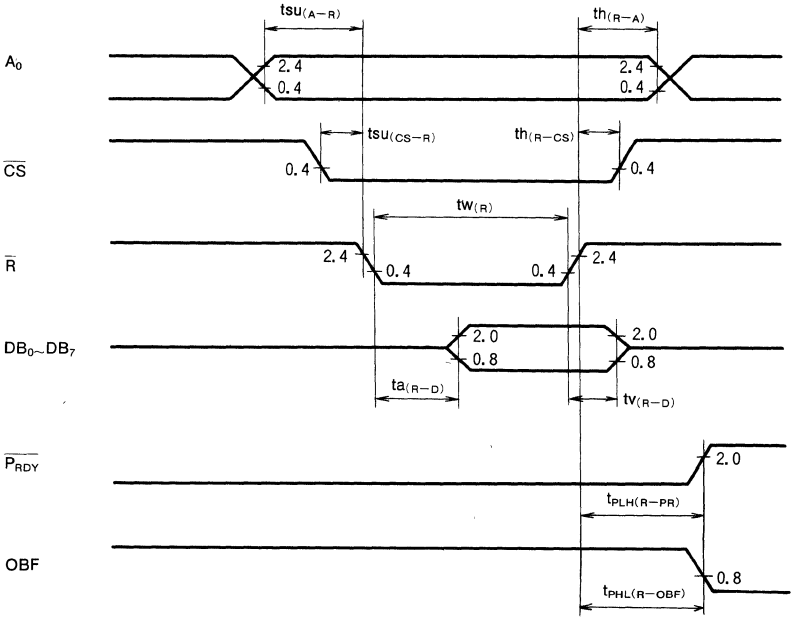
Port/single-chip mode timing diagram



Note : V_{IH}=0.8V_{CC}, V_{IL}=0.16V_{CC} of X_{IN}

Master CPU bus interface/ $\overline{R}$ and $\overline{W}$ separation type timing diagram

Read



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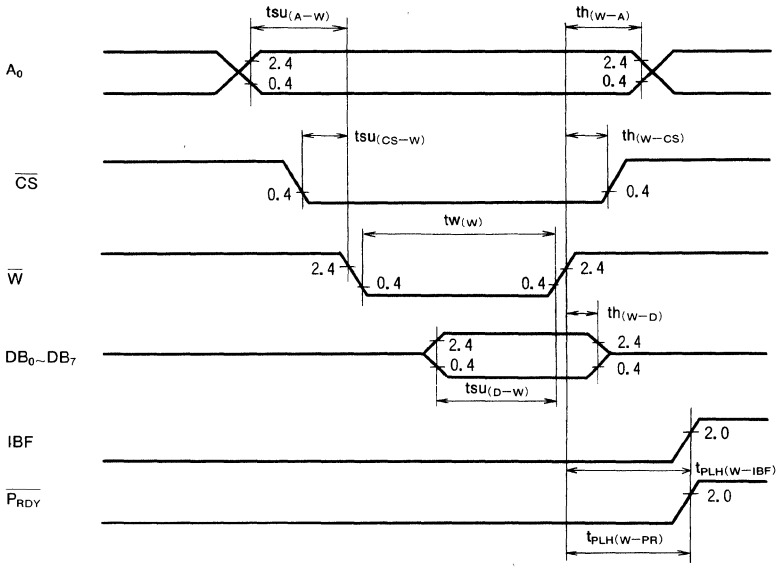
Write



Master CPU interface/ R/$\overline{W}$ type timing diagram