M37415PFS

PIGGYBACK for M37415M4-XXXFP

DESCRIPTION

The M37415PFS is an EPROM mounted-type microcomputer which utilizes CMOS technology, and is designed for developing programs for single-chip, 8-bit microcomputer M37415M4-XXXFP. It is housed in a piggyback-type 80-pin QFP.

There is a 32-pin socket on the package.

The M37415PFS simplifies the development of programs for the M37415M4-XXXFP and is excellent for making prototypes.

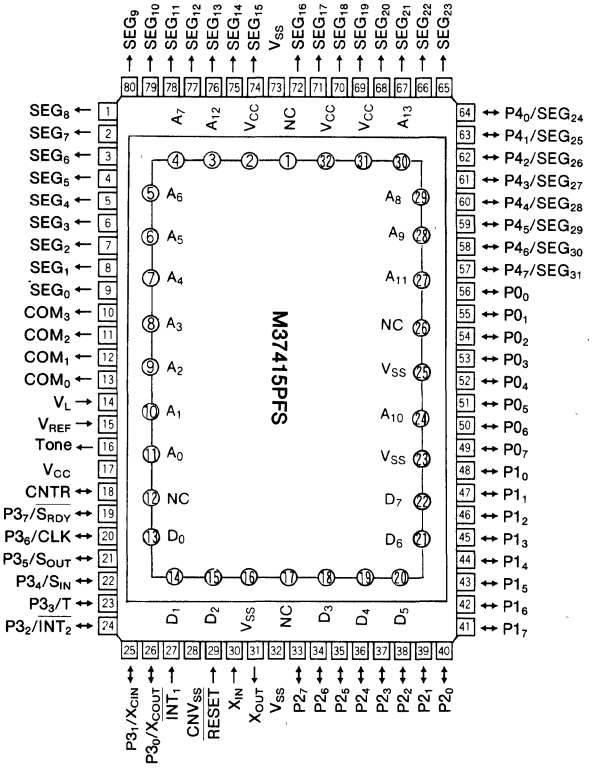
FEATURES

- Diffierence with the M37415M4-XXXFP are:
  ROMless, EPROM is attached externally.

APPLICATION

Development of programs for home telephone, multi function telephone

PIN CONFIGURATION (TOP VIEW)



Outline 80S6M

The symbol "○" indicates sockets for EPROM
NC No connection.

MITSUBISHI ELECTRIC

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage input		Power supply inputs 5V±10% to V_{CC} and 0V to V_{SS}.
CNV_{SS}	CNV_{SS} input		Connect to V_{SS}
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
$\overline{INT_1}$	Interrupt input	Input	This is the highest order interrupt input pin. It can be measured input voltage level
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional register allowing each I/O bit to be individually programmed as input or output At reset, this port is set to input mode The output structure is CMOS output
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0 When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively Also $P3_3$, $P3_2$, $P3_1$, and $P3_0$ work as timer 3 overflow signal divided by 2 output pin (T), $\overline{INT_2}$ pin, X_{CIN} and X_{COUT} pins, respectively
$P4_0$~$P4_7$	Input port P4	Input	Port P4 is an 8-bit input port and can be used as segment output pins
V_L	Voltage input for LCD	Input	This is a voltage input pin for LCD Supply voltage is $0V \leqq V_L \leqq V_{CC}$ 0V~V_{LV} is supplied to LCD.
COM_0~ COM_3	Common output	Output	These are the LCD common output pins At 1/2 duty, COM_2 and COM_3 pins are not use At 1/3 duty, COM_3 pin is not used
SEG_0~ SEG_{23}	Segment output	Output	These are LCD segment output pins
CNTR	Counter I/O	I/O	This is an output pin for timer 4 and 5 It can be measured input voltage level
V_{REF}	D-A convert power supply for DTMF		Reference voltage input for A-D converter of DTMF
Tone	DTMF output	Output	This is DTMF output pin.
A_0~A_{13}	Output port A	Output	These are for addresses to an EPROM mounted on the package
D_0~D_7	Input port D	Input	These are for input data from the EPROM mounted on the package

EXPLANATION OF FUNCTION BLOCK OPERATION

The differences between the M37415PFS and the M37415M4-XXXFP are noted below. The following explanations apply to the M37415PFS. Specification variations for other chips are noted accordingly.

MEMORY

The M37415PFS is mounted an EPROM instead of an internal ROM. The address of an EPROM is from 1000_{16} to $3FFF_{16}$, and this memory size is 12288 bytes. The memory size of a RAM is 512 bytes as same as the M37415M4-XXXFP.

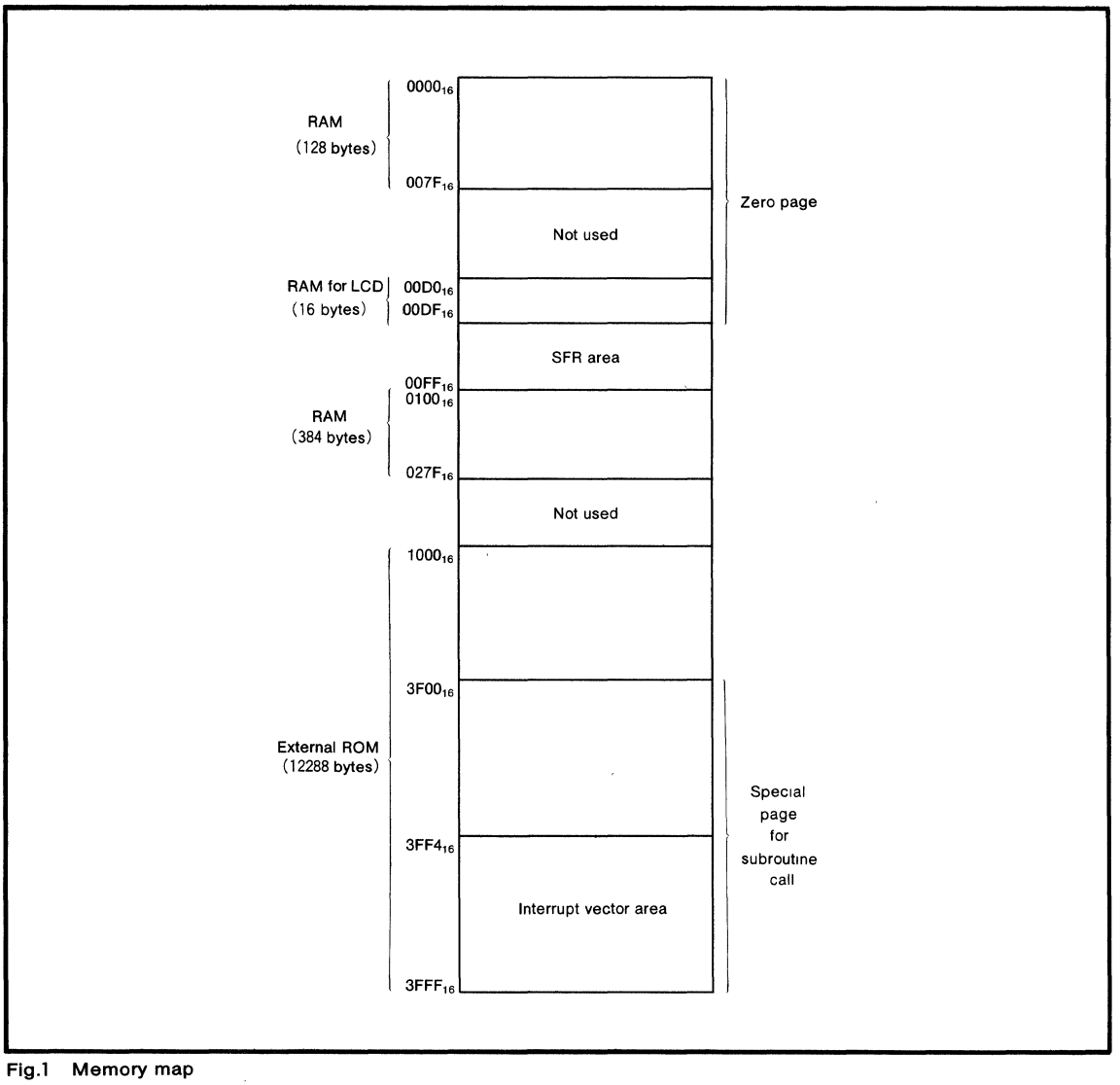


Fig.1 Memory map

$00E0_{16}$	Port P0	$00F0_{16}$	
$00E1_{16}$	Port P0 directional register	$00F1_{16}$	
$00E2_{16}$	Port P1	$00F2_{16}$	
$00E3_{16}$	Port P1 directional register	$00F3_{16}$	
$00E4_{16}$	Port P2	$00F4_{16}$	DTMF register
$00E5_{16}$	Port P2 directional register	$00F5_{16}$	LCD mode register
$00E6_{16}$		$00F6_{16}$	Serial I/O mode register
$00E7_{16}$		$00F7_{16}$	Serial I/O register
$00E8_{16}$	Port P3	$00F8_{16}$	Timer 4, 5 mode register
$00E9_{16}$	Port P3 directional register	$00F9_{16}$	Timer 1
$00EA_{16}$	Port P4	$00FA_{16}$	Timer 2
$00EB_{16}$		$00FB_{16}$	Timer 3
$00EC_{16}$		$00FC_{16}$	Timer 4
$00ED_{16}$		$00FD_{16}$	Timer 5
$00EE_{16}$		$00FE_{16}$	Interrupt control register
$00EF_{16}$		$00FF_{16}$	Timer control register

Fig. 2 SFR (Special Function Register) memory map

PRECAUTION FOR USE

(1) When developing programs with the M37415PFS, carefully consider the ROM capacity of the M37415M4-XXXFP.
Use the ROM area from 2000_{16} to $3FFF_{16}$.

(2) The M37415PFS has no options as the M37415M4-XXXFP. The condition of ports P0 ~ P3 and CNTR is noted below.
P0~P3, CNTR ..... without the pull-up transistor
$P3_5/S_{OUT}$ ..... N-channel open drain output

(3) The way of mounting an EPROM is shown in Figure 3.

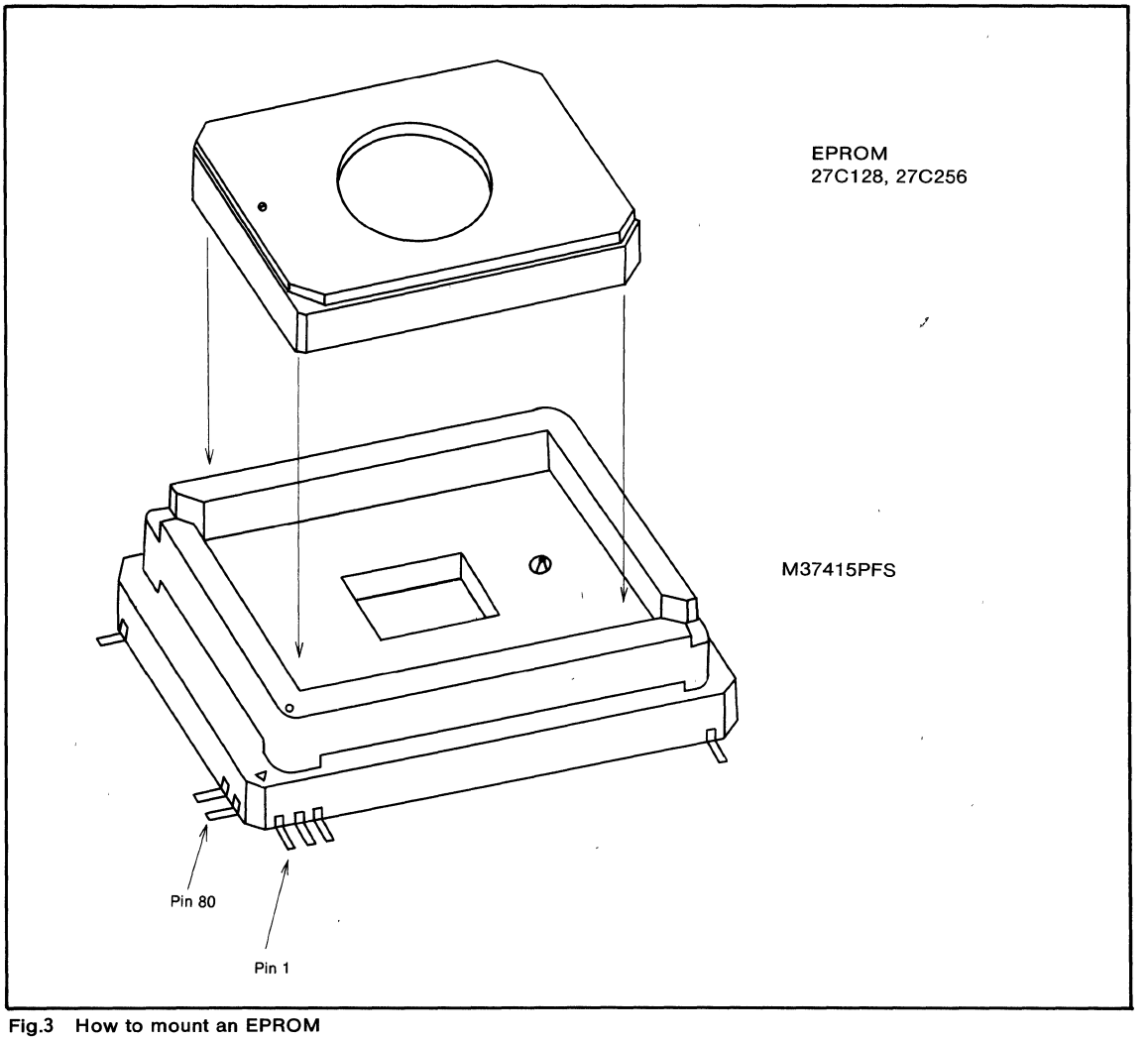


Fig.3 How to mount an EPROM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS}	−0.3∼7	V
V_I	Supply voltage for LCD V_L		−0.3∼V_{CC}+0.3	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, SEG_{24}∼SEG_{31}, X_{IN}		−0.3∼V_{CC}+0.3	V
V_I	Input voltage $\overline{INT_1}$, CNV_{SS}, V_{REF}		−0.3∼7	V
V_I	Input voltage $\overline{RESET}$, CNTR		−0.3∼13	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, COM_0∼COM_3, SEG_0∼SEG_{31}, X_{OUT}		−0.3∼V_{CC}+0.3	V
V_O	Output voltage CNTR		−0.3∼7	V
P_d	Power Dissipation	T_a = 25℃	300	mW
T_{opr}	Operating temperature		−10∼70	℃
T_{stg}	Strage temperature		−40∼125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=3.0(Note 1)∼5.5V, V_{SS}= 0 V, T_a=−10∼70℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{CC}	Supply voltage (Note 2)	f(X_{IN})=3.2MHz	4.5		5.5	V
		f(X_{IN})=800kHz	3.0(Note 1)		5.5	
V_{SS}	Supply voltage			0		V
V_{REF}	Supply voltage for DTMF	R_L≧20kΩ	1.5		V_{CC}−0.5	V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$, $P3_1$ (Note 3), $P3_3$∼$P3_7$ (Note 4), $P4_0$∼$P4_7$, $\overline{RESET}$, X_{IN}, CNV_{SS}		0.7V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P2_0$∼$P2_7$, $P3_2$, $P3_6$ (Note 5) $\overline{INT_1}$, CNTR		0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$, $P3_1$ (Note 3), $P3_3$∼$P3_7$ (Note 4), $P4_0$∼$P4_7$, CNV_{SS}		0		0.3V_{CC}	V
V_{IL}	"L" input voltage $P2_0$∼$P2_7$, $P3_2$, $P3_6$ (Note 5), $\overline{INT_1}$, CNTR		0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$		0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}		0		0.16V_{CC}	V
I_{OH}	"H" Output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$ (Note 6), X_{OUT}				−2	mA
$I_{OL(peak)}$	"L" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, CNTR, X_{OUT}(Note 7)				10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, CNTR, X_{OUT}(Note 8)				5	mA
f(X_{IN})	Clock oscillating frequency (Note 9)	V_{CC}=4.5∼5.5V	380		3300	kHz
		V_{CC}=3.0(Note 1)∼5.5V	380		1000	
f(X_{CIN})	Clock oscillating frequency for clock function		32		50	kHz

Note 1 : Minimum value of V_{CC} is dependent on the EPROM used. At normal temperature, this value is about 2.5V. Therefore, 3.0V is dependent on the proper operation of the EPROM at that voltage

2 : When only operating the RAM data retention, minimum value of V_{CC} is 2V

3 : When using port $P3_1$ as X_{CIN}, 0.85≦V_{CC}≦V_{IH}≦V_{CC}, 0≦V_{IL}≦0.15V_{CC} for port $P3_1$

4 : In this case of using port $P3_6$ as normal input

5 : In this case of using port $P3_6$ as CLK input

6 : The total of I_{OH} of port P0, P1, P2, P3 and X_{OUT} should be 35mA max

7 : The total of I_{OL} (peak) of port P0, P1, P2, P3 should be 55mA max, and the total of I_{OL} (peak) of port P3, CNTR, and X_{OUT} should be 45mA max

8 : I_{OL} (avg) is the average current in 100ms

9 : When using DTMF function, f(X_{IN}) should be 400kHz, 800kHz, 1.6MHz, or 3.2MHz

ELECTRICAL CHARACTERICS (V_{SS}= 0 V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_4$(Note 1), $P3_6$, $P3_7$	V_{CC}=5V, I_{OH}=−2mA		3			V
		V_{CC}=3V, I_{OH}=−0.7mA		2			
V_{OH}	"H" output voltage X_{OUT}	V_{CC}=5V, I_{OH}=−1.5mA		3			V
		V_{CC}=3V, I_{OH}=−0.3mA		2			
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$(Note 1), CNTR	V_{CC}=5V, I_{OL}=10mA				2	V
		V_{CC}=3V, I_{OL}=3mA				1	
V_{OL}	"L" output voltage X_{OUT}	V_{CC}=5V, I_{OL}=1.5mA				2	V
		V_{CC}=3V, I_{OL}=0.3mA				1	
V_{T+}−V_{T-}	Hysteresis $\overline{INT_1}$, CNTR	V_{CC}=5V		0.25		1	V
		V_{CC}=3V		0.15		0.7	
V_{T+}−V_{T-}	Hysteresis $P3_6$	When used as CLK input	V_{CC}=5V		0.5		V
			V_{CC}=3V		0.4		
V_{T+}−V_{T-}	Hysteresis $P3_1$	When used as X_{CIN} input	V_{CC}=5V		0.7		V
			V_{CC}=3V		0.5		
V_{T+}−V_{T-}	Hysteresis $P2_0$~$P2_7$, $P3_2$	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.4		
V_{T+}−V_{T-}	Hysteresis $\overline{RESET}$	V_{CC}=5V			0.5	0.7	V
		V_{CC}=3V			0.35		
V_{T+}−V_{T-}	Hysteresis X_{IN}	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.35		
I_{IL}	"L" input current SEG_{24}~SEG_{31} (except reset state) {$P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$} without pull-up Tr $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_{CC}=5V, V_I=0V				−5	μA
		V_{CC}=3V, V_I=0V				−4	
I_{IL}	"L" input current SEG_{24}~SEG_{31} (at reset state)	V_{CC}=5V, V_L=5V, V_I=0V		−30		−140	μA
		V_{CC}=3V, V_L=3V, V_I=0V		−6		−45	
I_{IH}	"H" input current SEG_{24}~SEG_{31} (except reset state) $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $\overline{INT_1}$, $\overline{RESET}$, X_{IN}	V_{CC}=5V, V_I=5V				5	μA
		V_{CC}=3V, V_I=3V				4	
I_{IH}	"H" input current SEG_{24}~SEG_{31} (at reset state)	V_{CC}=5V, V_L=5V, V_I=5V				5	μA
		V_{CC}=3V, V_L=3V, V_I=3V				4	
I_{CC}	Supply current. Output pins are opened. $\overline{RESET}$, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, and $P3_0$~$P3_7$ are connected to V_{CC}. Except the above pins are connected to V_{SS}. However, X_{IN} and X_{CIN} are input signal according to the conditions Without supply current for EPROM	at stop state: $f(X_{IN})$=3.2MHz, V_{CC}=5V	at DTMF wave form output		4		mA
			at DTMF wave form stop		3		
		at stop state: $f(X_{IN})$=800kMHz, V_{CC}=3V	at DTMF wave form output		0.8		
			at DTMF wave form stop		0.5		
		at stop state: T_a=25℃, X_{IN}=0V, $f(X_{CIN})$=32.8kHz at low power mode (LM_6=1)	V_{CC}=5V		45		μA
			V_{CC}=3V		18		
		at wait state: $f(X_{IN})$=3.2MHz, V_{CC}=5V			1		mA
		at wait state: $f(X_{IN})$=800kHz, V_{CC}=3V			0.3		
		at wait state: T_a=25℃, X_{IN}=0V, $f(X_{CIN})$=32.8kHz at low power mode (LM_6=1)	V_{CC}=5V		20		μA
			V_{CC}=3V		4		
		at operation: $f(X_{IN})$=0, $f(X_{CIN})$=0, V_{CC}=5V	T_a=25℃		0.1		
			T_a=70℃				
V_{RAM}	RAM retention voltage	$f(X_{IN})$=0, $f(X_{CIN})$=0		2		5.5	V

Note 1 : If $P3_0$ is used as X_{COUT}, capability of load driving is lower than the above

DTMF CHARACTERISTICS (V_{SS}= 0 V, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter		Tes conditions	Limits			Units
				Min	Typ	Max	
V_{OT}	Output voltage T_{one}	High frequency band group	V_{CC}=5V, V_{REF}=4.5V, R_L=20kΩ	470	490	510	mVrms
			V_{CC}=3V, V_{REF}=2.5V, R_L=20kΩ	257	270	283	
		Low frequency band group	V_{CC}=5V, V_{REF}=4.5V, R_L=20kΩ	325	345	365	
			V_{CC}=3V, V_{REF}=2.5V, R_L=20kΩ	177	190	203	
dB_{CR}	Output ratio of high frequency band to low frequency band		R_L=20kΩ	2.5	3	3.5	dB
DIS	Disportional percentage		R_L=20kΩ, T_a=25℃		13		%

Accuracy of DTMF output (at low frequency band value)

Standard frequency value [Hz]	Output frequency value [Hz]	Deflection	Error [%]
697	694.44	−2.555	−0.367
770	769.23	−0.769	−0.1
852	854.7	2.7	0.317
941	938.97	−2.033	−0.216

Accuracy of DTMF output (at high frequency band value)

Standard frequency value [Hz]	Output frequency value [Hz]	Deflection	Error [%]
1209	1204.8	−4.181	−0.346
1336	1333.3	−2.667	−0.2
1477	1470.6	−6.412	−0.434
1633	1639.3	6.344	0.389