M37420M4-XXXSP
M37420M6-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37420M4-XXXSP and the M37420M6-XXXSP are single-chip microcomputers designed with CMOS silicon gate technology. All are housed in a 52-pin shrink plastic molded DIP.

These single-chip microcomputers are useful for household appliance and other consumer applications.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M37420M4-XXXSP and the M37420M6-XXXSP are noted below. The following explanations apply to the M37420M6-XXXSP.

Specification variations for other chips are noted accordingly.

Type name	ROM size	RAM size
M37420M4-XXXSP	8192 bytes	192 bytes
M37420M6-XXXSP	12288 bytes	256 bytes

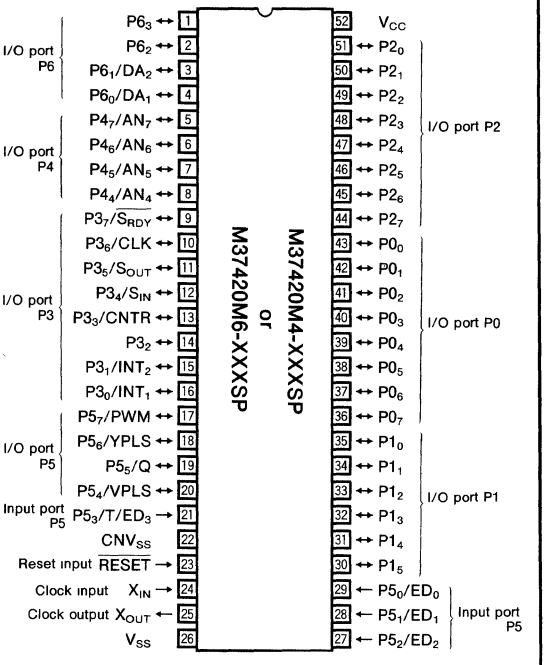
FEATURES

- Number of basic instructions 69
- Memory size ROM ...12288 bytes (M37420M6-XXXSP)
  8192 bytes (M37420M4-XXXSP)
  RAM ..... 256 bytes (M37420M6-XXXSP)
  192 bytes (M37420M4-XXXSP)
- Instruction execution time
  ..... 1μs (minimum instructions, at 8MHz frequency)
- Single power supply f(X_{IN})=8MHz ..... 5V±10%
- Power dissipation
  normal operation mode (at 8MHz frequency) 30mW
- Subroutine nesting ..... 96 levels (Max.)
- Interrupt ..... 7 types, 5 vectors
- 8-bit timer 4
- Programmable I/O ports (Ports P0, P1, P2, P3, P4) 42
- Input port (Port P5) 8
- Serial I/O (8-bit/16-bit) 1
- A-D converter ..... 8-bit successive approximation
- D-A converter
- 14-bit PWM function
- Watchdog timer

APPLICATION

VCR, TV, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



Outline 52P4B

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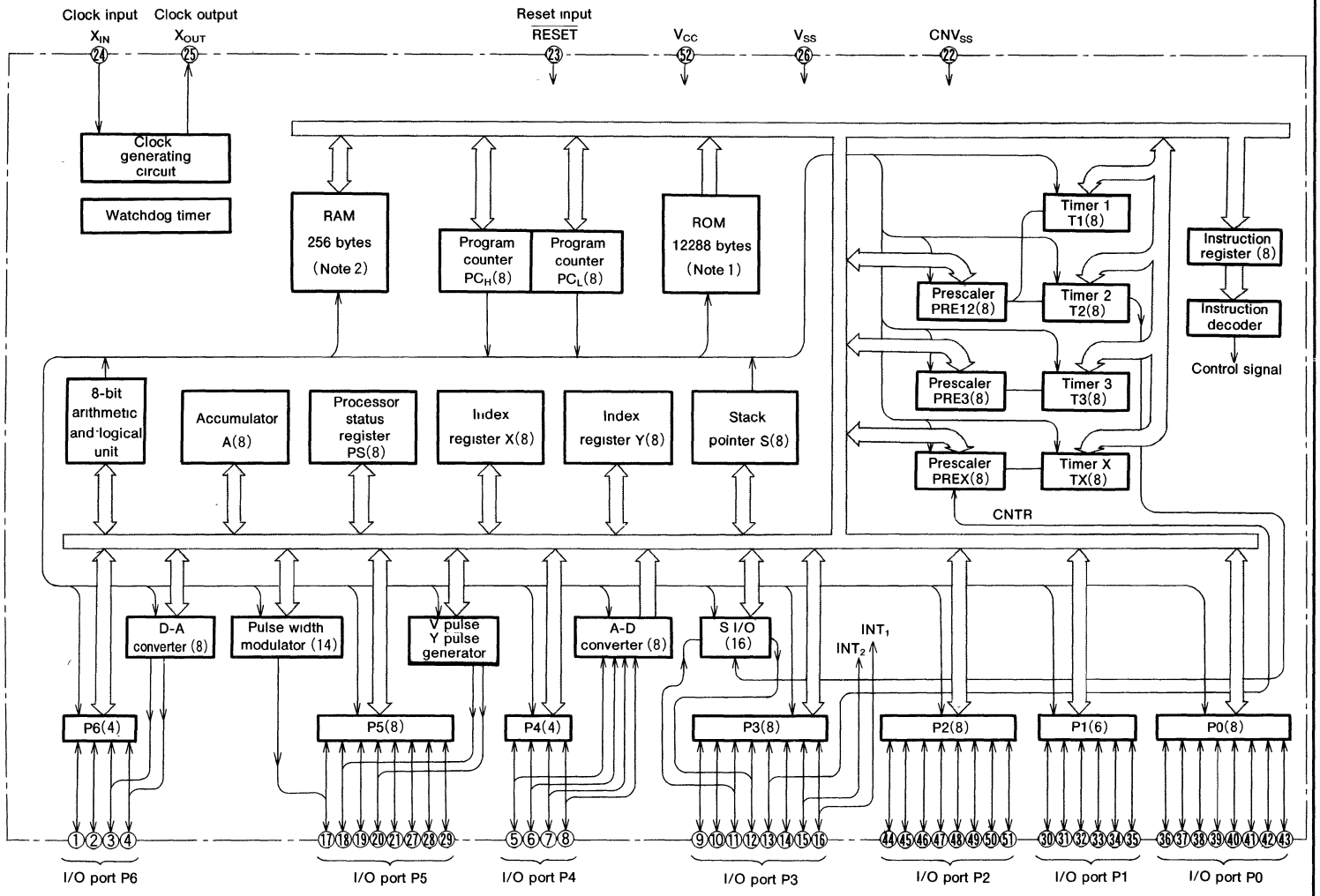
M37420M6-XXXSP BLOCK DIAGRAM



Note 1 : 8192 bytes for M37420M4-XXXSP
2 : 192 bytes for M37420M4-XXXSP

FUNCTIONS OF M37420M6-XXXSP

Parameter			Functions
Number of basic instructions			69
Instruction execution time			1μs (minimum instructions, at 8MHz frequency)
Clock frequency			8MHz
Memory size	ROM		12288bytes (8192 bytes for M37420M4-XXXSP)
	RAM		256bytes (192 bytes for M37420M4-XXXSP)
Input/Output ports	P0, P1, P2, P3, P4, $P5_4$~$P5_7$, P6	I/O	8-bit×3, 6-bit×1, 4-bit×3
	$P5_0$~$P5_3$	Input	4-bit×1
Serial I/O			8-bit×1 or 16-bit×1
Timers			8-bit prescaler×3+8-bit timer×4
A-D conversion			8-bit×1 (4 channels)
D-A conversion			8-bit×2
Pulse width modulator			14-bit×1
Watchdog timer			15-bit×1
Subroutine nesting			96 levels (max)
Interrupts			Two external interrupts, Three internal timer interrupts (or timer×2, SI/O×1)
Clock generating circuit			Built-in (ceramic or quartz crystal oscillator)
Supply voltage			5V±10%
Power dissipation	at high-speed operation		30mW (at 8MHz frequency)
Input/Output characteristics	Input/Output voltage		12V (Ports P0, P1, P3)
Operating temperature range			−10~70℃
Device structure			CMOS silicon gate process
Package			52-pin shrink plastic molded DIP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open
X_{OUT}	Clock output	Output	
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional register allowing each I/O bit to be individually programmed as input or output At reset, this port is set to input mode The output structure is N-channel open drain
$P1_0$~$P1_5$	I/O port P1	I/O	Port P1 is an 6-bit I/O port and has basically the same functions as port P0 The output structure is N-channel open drain
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is CMOS output
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0 When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively Also $P3_3$ and $P3_2$ work as CNTR pin and the lowest interrupt input pin ($\overline{INT_2}$) , respectively
$P4_4$~$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0 $P4_2$~$P4_7$ work as analog input port AN_4~AN_7
$P5_0$~$P5_3$	Input port P5	Input	Low-order 4-bit of port P5 is input port These can be used as the edge sence inputs $P5_0$~$P5_2$ detect the rising edge and $P5_3$ detects both edges Also, $P5_3$ is common with the external trigger and V pulse, Y pulse generator trigger input
$P5_4$~$P5_7$	I/O port P5	I/O	High-order 4-bit of port P5 is I/O port and has basically the same function as port P0 $P5_7$ is common with the 14-bit PWM. The output structure is CMOS output
$P6_0$~$P6_3$	Output port P6	Output	Port P6 is an 4-bit output port At external trigger output mode, $P6_0$ and $P6_1$ are in common with the trigger input pin (T) and the trigger output pin (Q), respectively The output structure is N-channel open drain.

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The M37420 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions are not provided.

The WIT instruction can be used.

The STP instruction can be used.

Timer Control Register

The timer control register is allocated to address $00FF_{16}$. This register has a stack page bit.

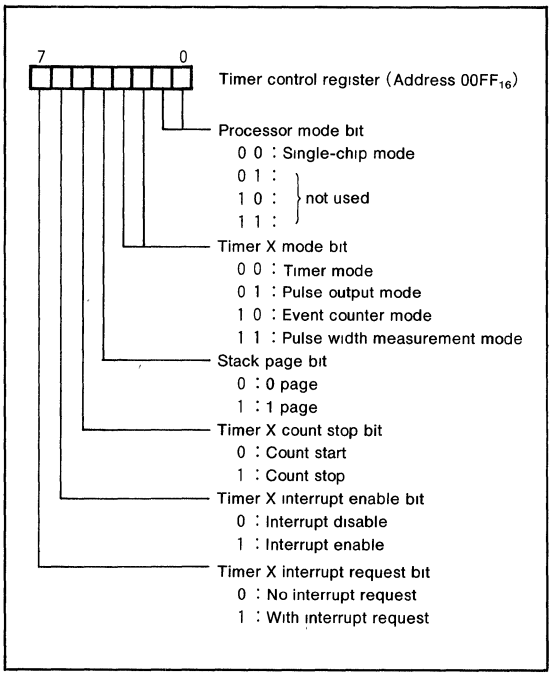


Fig.1 Structure of timer control register

MEMORY

• **Special Function Register (SFR) Area**

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• **RAM**

RAM is used for data storage as well as a stack area.

• **ROM**

ROM is used for storing user programs as well as the interrupt vector area.

• **Interrupt Vector Area**

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• **Zero Page**

Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.

• **Special Page**

Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

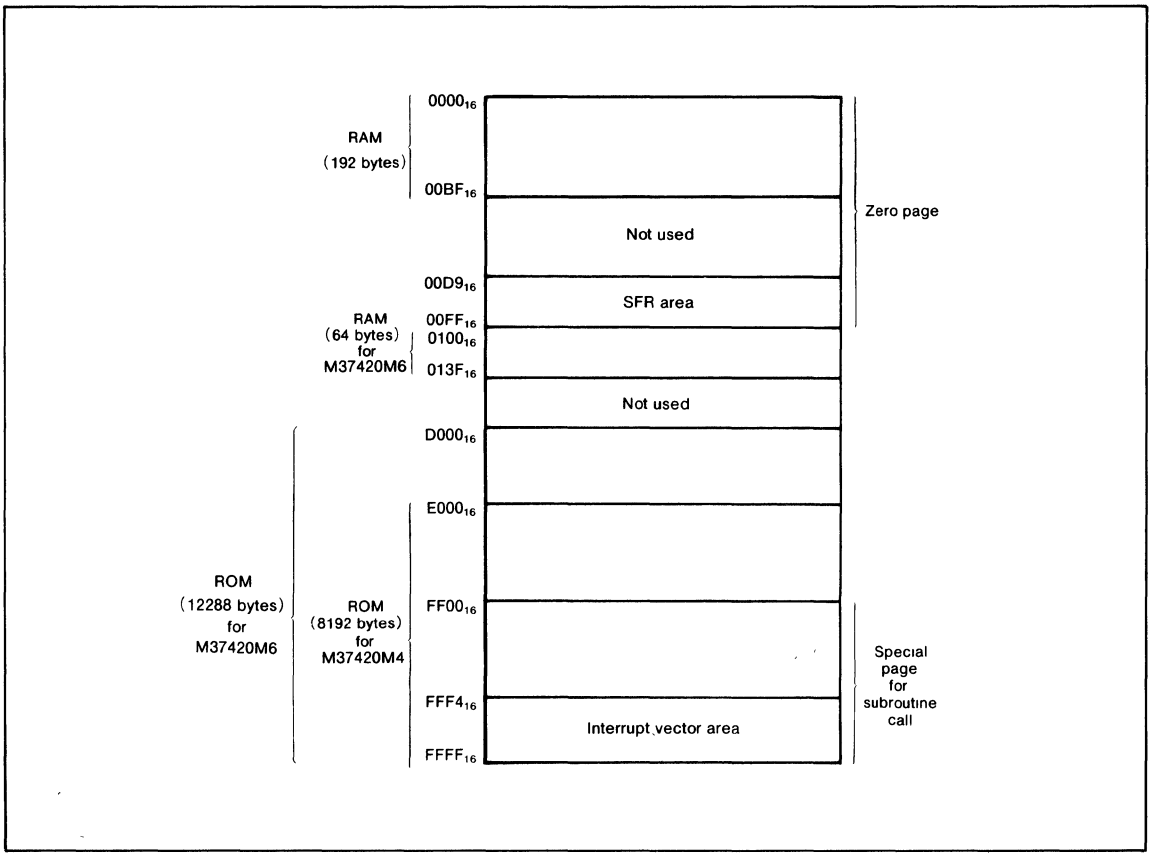


Fig.2 Memory map

$00D9_{16}$	D-A conversion register 1
$00DA_{16}$	D-A conversion register 2
$00DB_{16}$	V pulse preset value P
$00DC_{16}$	V pulse preset value N
$00DD_{16}$	V pulse register
$00DE_{16}$	Serial I/O register L
$00DF_{16}$	Serial I/O register H
$00E0_{16}$	Port P0
$00E1_{16}$	Port P0 directional register
$00E2_{16}$	Port P1
$00E3_{16}$	Port P1 directional register
$00E4_{16}$	Port P2
$00E5_{16}$	Port P2 directional register
$00E6_{16}$	
$00E7_{16}$	
$00E8_{16}$	Port P3
$00E9_{16}$	Port P3 directional register
$00EA_{16}$	Port P4
$00EB_{16}$	Port P4 directional register

$00EC_{16}$	Port P5
$00ED_{16}$	Port P5 latch/directional register
$00EE_{16}$	Port P6
$00EF_{16}$	Port P6 directional register
$00F0_{16}$	Pulse width modulation register H
$00F1_{16}$	Pulse width modulation register L
$00F2_{16}$	Successive approximation register
$00F3_{16}$	A-D control register
$00F4_{16}$	Watchdog timer
$00F5_{16}$	Serial I/O mode register
$00F6_{16}$	Special function selection register
$00F7_{16}$	Timer 3 prescaler
$00F8_{16}$	Timer 3
$00F9_{16}$	Timer 1,2 prescaler
$00FA_{16}$	Timer 1
$00FB_{16}$	Timer 2
$00FC_{16}$	Timer X prescaler
$00FD_{16}$	Timer X
$00FE_{16}$	Interrupt control register
$00FF_{16}$	Timer control register

Fig. 3 SFR (Special Function Register) memory map

INTERRUPT

The M37420M6-XXXSP can be interrupted from seven sources; INT_1, timer X, timer 1, timer 2/serial I/O, or INT_2/BRK instruction.

However, the INT_1 pin is used with port $P3_0$ and the INT_2 pin is used with port $P3_1$ and the corresponding directional register bit should be set to "0" when each port used as an interrupt input pin.

The value of bit 2 and bit 3 of the serial I/O mode register (address $00F5_{16}$) determine whether the interrupt is from timer 2 or from serial I/O. When the value of bit 2 and bit 3 is [00], the interrupt is from timer 2, and the value of bit 2 and bit 3 is [01], the interrupt is from serial I/O. Also, when the value of bit 2 and bit 3 is [01], parts of port P3 are used for serial I/O. These interrupts are vectored and their priorities are shown in Table 1. Reset is included in this table since it has the same functions as the interrupts.

When an interrupt is accepted, the contents of certain registers are pushed into specified locations, the interrupt disable flag I is set, the program jumps to the address specified by the interrupt vector, and the interrupt request bit is cleared automatically. The reset interrupt is the highest priority interrupt and can never be inhibited. Except for the reset interrupt, all interrupt are inhibited when the interrupt disable flag I is set to "1". All of the other interrupts can further be controlled individually via the interrupt control register shown in Figure 4. An interrupt is accepted when the interrupt enable bit and the interrupt request bit are both "1" and the interrupt disable flag is "0".

The interrupt request bits are set when the following conditions occur:

(1) When the level of INT_1 or INT_2 pin changes
(2) When the contents of timer X, timer 1, timer 2 (or the serial I/O counter) go to "0"

Table 1. Interrupt vector address and priority

Interrupt	Priority	Vector address
$\overline{RESET}$	1	$FFFF_{16}$, $FFFE_{16}$
$\overline{INT_1}$	2	$FFFD_{16}$, $FFFC_{16}$
Timer X	3	$FFFB_{16}$, $FFFA_{16}$
Timer 1	4	$FFF9_{16}$, $FFF8_{16}$
Timer 2 or serial I/O	5	$FFF7_{16}$, $FFF6_{16}$
$\overline{INT_2}$ (BRK)	6	$FFF5_{16}$, $FFF4_{16}$

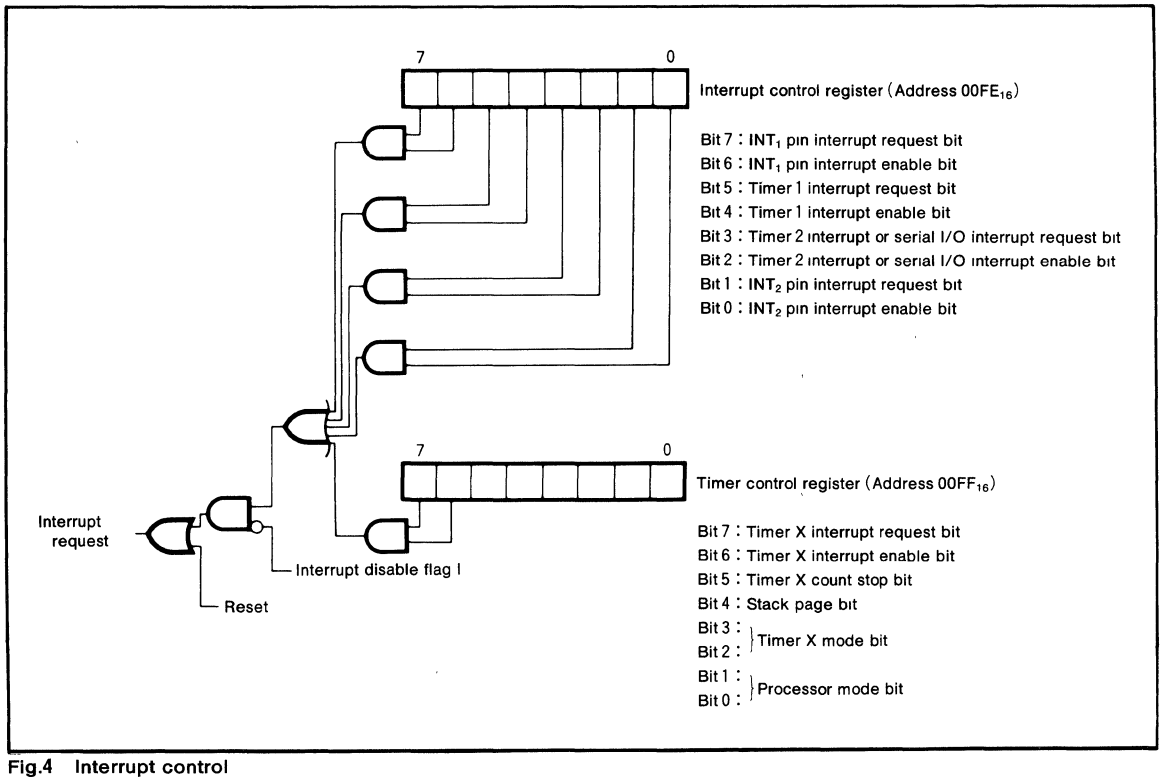


Fig.4 Interrupt control

The change in level at which the INT pins generate a interrupt varies according to the content of bits 4 and 5 of the special function selection register (address $00F6_{16}$). When these bits are "0", the interrupt request is generated when INT changes from high-level to low-level. When these bits are "1", the interrupt request is generated when INT changes from low-level to high-level. Bits 4 and 5 correspond to INT_1 and INT_2 respectively.

These request bits can be reset by the program but can not be set by the program. However, the interrupt enable bit can be set and reset by the program.

Since the BRK instruction and the INT_2 interrupt have the same vectored address, the contents of the B flag must be checked to determine if the BRK instruction caused the interrupt or if INT_2 generated the interrupt.

TIMER

The M37420M6-XXXSP has four timers; timer X, timer 1, timer 2 and timer 3. Since P3 (in serial I/O mode) and timer 2 use some of the same architecture, they cannot be used at the same time (see serial I/O section) Timer X has four modes which can be selected by bit 2 and 3 of the timer control register. When the timer X count stop bit (bit 5) is set to "1", the timer X will stop regardless of which mode it is in. A block diagram of timer X, timer 1, timer 2 and timer 3 is shown in Figure 5.

The $P3_3$/CNTR pin cannot be used as CNTR when $P3_3$ is being used in the normal I/O mode.

Timer 1 and timer 2 share with a prescaler. This prescaler has an 8-bit programmable latch used as a frequency divider. The division ratio is defined as $1/(n+1)$, where n is the decimal contents of the prescaler latch. All four timers are down-count timers which are reloaded from the timer latch following the zero cycle of the timer (i.e. the cycle after the timer counts to zero).

The timer interrupt request bit is set to "1" during the next clock pulse after the timer reaches zero for timer 1, timer 2 and timer X. The interrupt and timer control registers are located at addresses $00FE_{16}$ and $00FF_{16}$, respectively (see Interrupt section). The prescaler latch and timer latch can be loaded with any number.

The four modes of timer X as follows:

(1) Timer mode [00]
In this mode the clock is driven by the oscillator frequency divided by 16. When the timer down-counts to zero, the timer interrupt request bit is set to "1" and the contents of the timer's latch is reloaded into the timer and the counting begins again.

(2) Pulse output mode [01]
In this mode, the polarity of the CNTR signal is reversed each time the timer down-counts to zero.

(3) Event counter mode [10]
This mode operates in the same manner as the timer mode except, the clock source is input to the CNTR pin. This mode will allow an interrupt to be generated whenever a specified number of external events have been generated. The timer down-counts every rising edge of the clock source.

(4) Pulse width measurement mode [11]
This mode measures the pulse width (between lows) input to the CNTR pin. The timer, driven by the oscillator frequency divided by 16, continues counting during the low cycle of the CNTR pin. When the timer contents reaches "0", the interrupt request bit is set to "1", the timer's reload latch is reloaded and the counting resumes.

The structure of the timer control register is shown in Figure 6.

When the STP instruction is executed, or after reset, the prescaler and timer latch are set to FF_{16} and 01_{16}, respectively. Also, when the STP instruction is executed, the oscillator's frequency (divided by 16) will become the counting source, regardless of the timer X mode setting. This state will be released when the timer X interrupt request bit is set to "1", or after a reset. Timer X will then enter the mode specified by its mode bits. For more details on the STP instruction, refer to the oscillation circuit section.

The function of timer 3 is as same as that of timer 1 and timer 2, with the exception that the detection of its overflow is known by the overflow bit (bit 3 of address $00EF_{16}$). When the timer down-counts to zero, the overflow bit is set to "1" and the contents of the timer's latch is reloaded into the timer.

The reset of the overflow bit is made by;

a) hard ware reset
b) write "0" to overflow bit
c) write instruction to timer 3

The structure of special function selection register is shown in Figure 7.

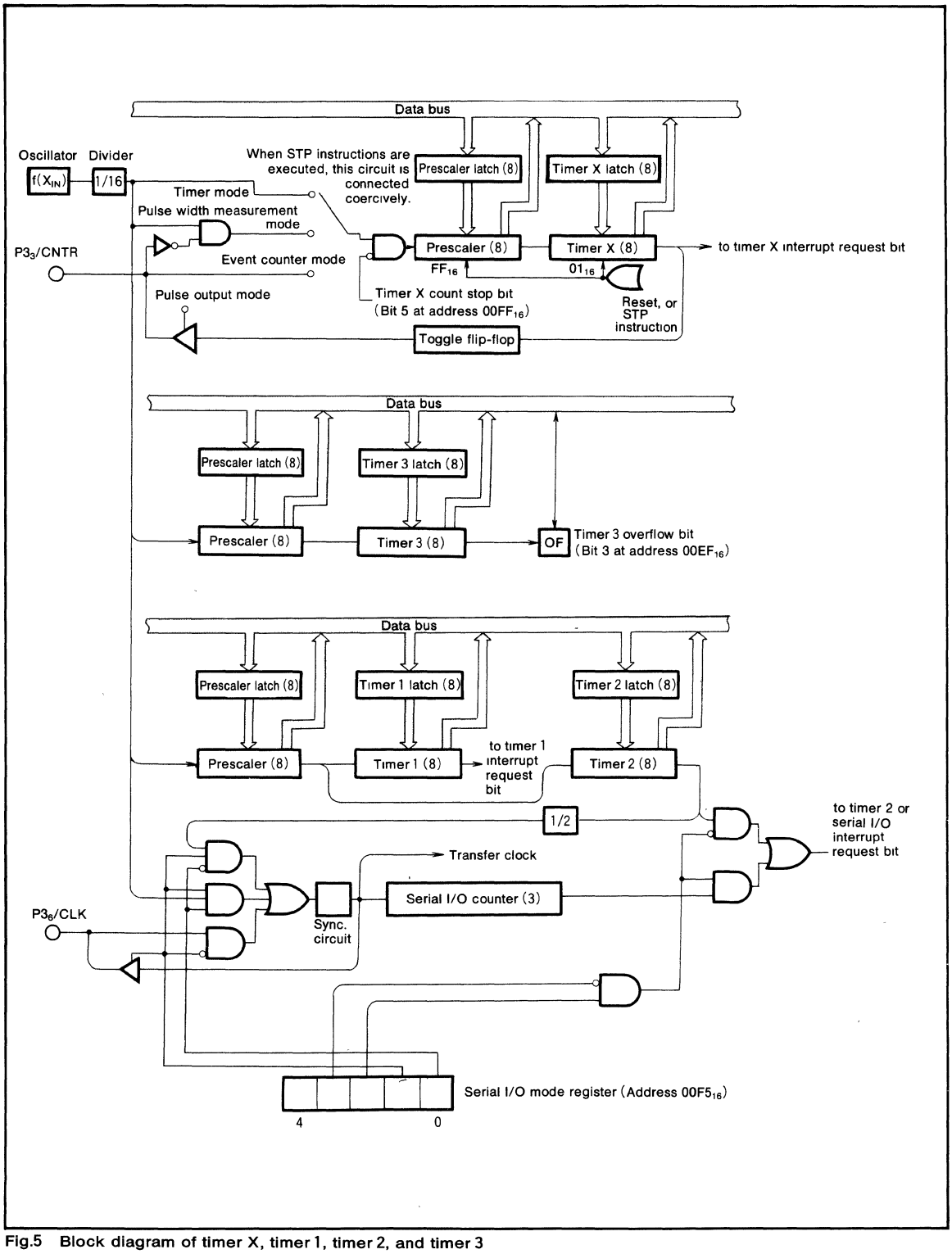


Fig.5 Block diagram of timer X, timer 1, timer 2, and timer 3

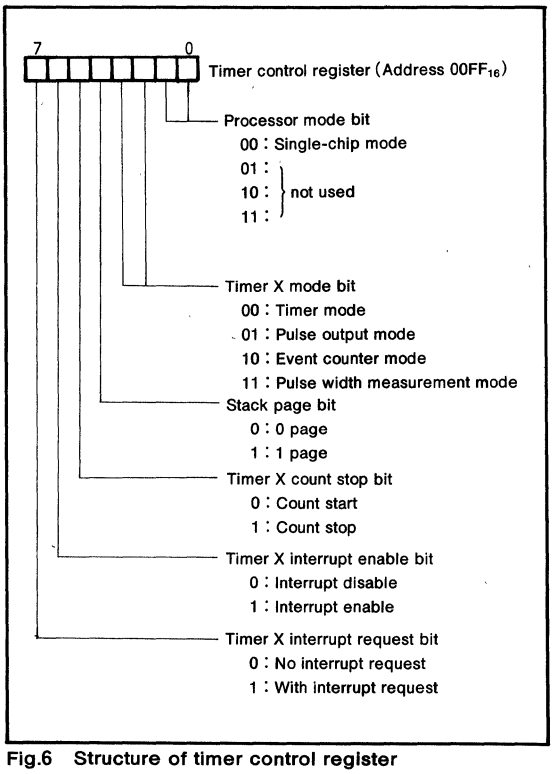


Fig.6 Structure of timer control register

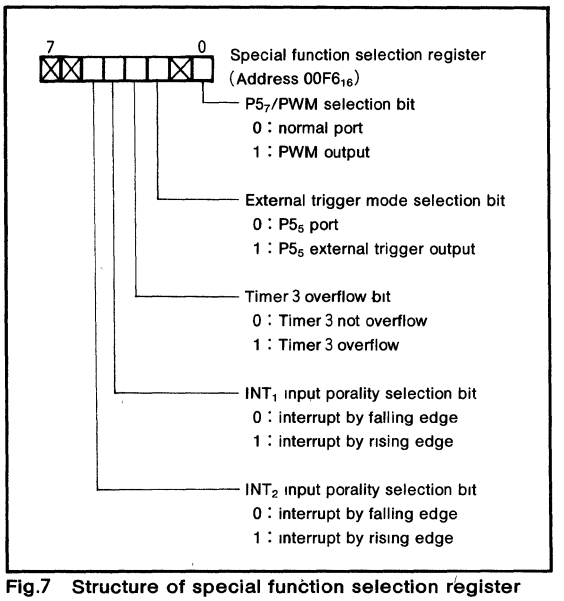


Fig.7 Structure of special function selection register

SERIAL I/O

A block diagram of the serial I/O is shown in Figure 8.

In the serial I/O mode the receive ready signal ($\overline{S_{RDY}}$), synchronous input /output clock (CLK), and the serial I/O pins (S_{OUT}, S_{IN}) are used as $P3_7$, $P3_6$, $P3_5$, and $P3_4$, respectively. The serial I/O mode register (address $00F5_{16}$) is a 6-bit register. Bits 1 and 0 of this register is used to select a synchronous clock source.

When these bits are [00] or [01], an external clock from $P3_6$ is selected. When these bits are [10], the overflow signal from timer 2, divided by two, becomes the synchronous clock. Therefore, changing the timer period will change the transfer speed. When the bits are [11], the oscillator frequency divided by 16, becomes the clock.

Bit 2 to 4 decide whether parts of P3 will be used as a serial I/O or not. When bit 3 is "0" and bit 2 is "1", $P3_6$ becomes an I/O pin of the synchronous clock. When an internal synchronous clock is selected, the clock is output from $P3_6$. If an external synchronous clock is selected, the clock is input to $P3_6$ and $P3_5$ will be a serial output and $P3_4$ will be a serial input. To use $P3_4$ as a serial input, set the directional register bit which corresponds to $P3_4$ to "0". For more information on the directional register, refer to the I/O pin section.

To use the serial I/O, bit 3 and bit 2 need to be set to "01", if they are "00" $P3_6$ will function as a normal I/O. Interrupts will be generated from the serial I/O counter instead of timer 2. Bit 4 determines if $P3_7$ is used as an output pin for the receive data ready signal (bit 4=1, $\overline{S_{RDY}}$) or used as normal I/O pin (bit 4=0). Bit 5 determines the serial I/O mode. If this bit is "0", serial I/O becomes 8-bit mode and this bit is "1", serial I/O becomes 16-bit mode. The serial I/O function is discussed below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.

Internal clock—The $\overline{S_{RDY}}$ signal becomes "H" during transmission or while dummy data is stored in the serial I/O register (address $00F7_{16}$). Data is stored only to the serial I/O register L (address $00DE_{16}$) in 8-bit mode, and stored high-order 8-bit to serial I/O register H (address $00DF_{16}$) at first, then low order 8-bit to serial I/O register L (address $00DE_{16}$) in 16-bit mode. After the falling edge of the write signal, the $\overline{S_{RDY}}$ signal becomes low signaling that the M37420M6-XXXSP is ready to receive the external serial data. The $\overline{S_{RDY}}$ signal goes "H" at the next falling edge of the transfer clock. The serial I/O counter is set to 7 in 8-bit mode and 15 in 16-bit mode when data is stored in the serial I/O register. At each falling edge of the transfer

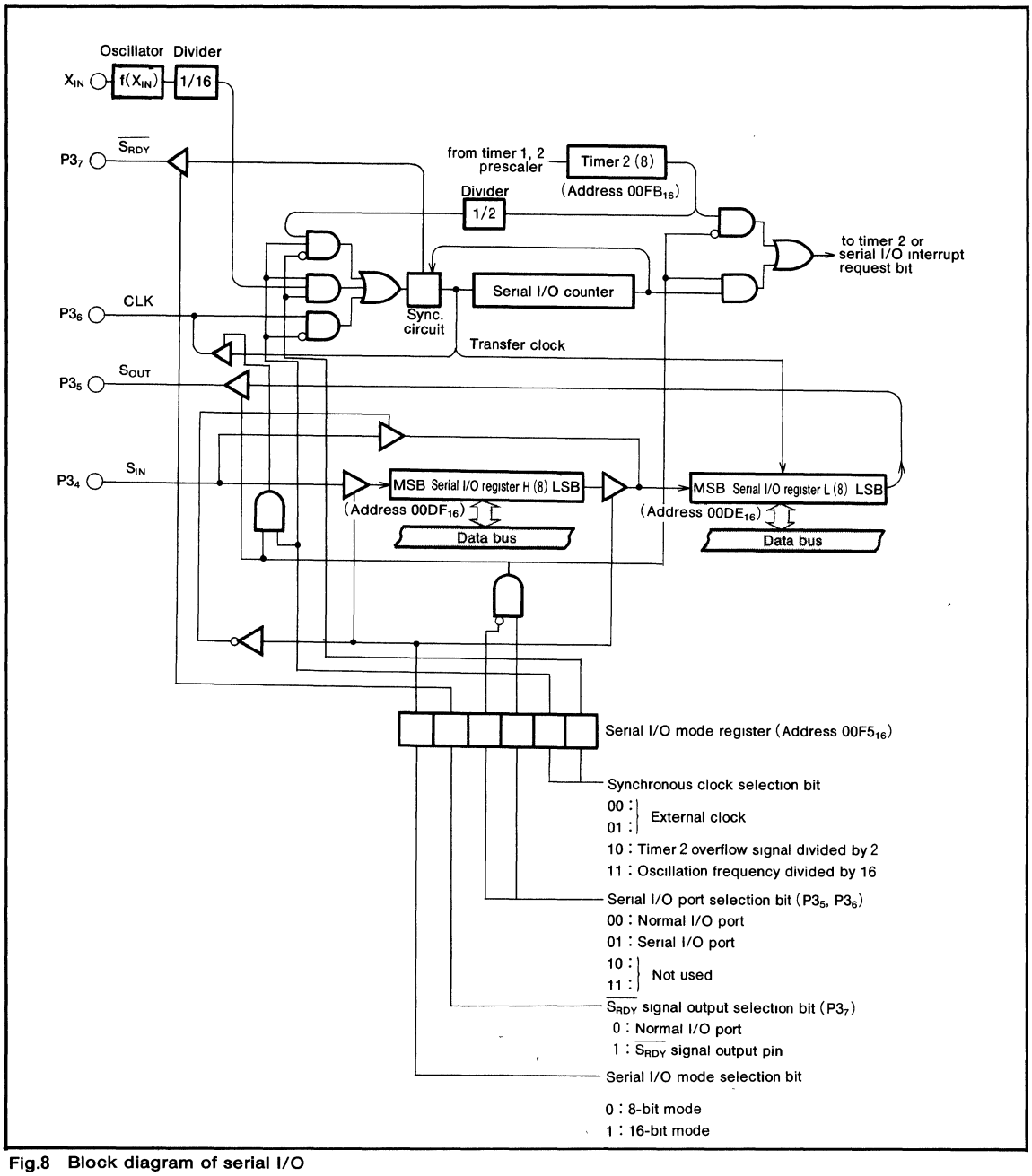


Fig.8 Block diagram of serial I/O

clock, serial data is output to $P3_5$. During the rising edge of this clock, data can be input from $P3_4$ and the data in the serial I/O register will be shifted 1 bit.

Data is output starting with the LSB. After the transfer clock has counted 8 or 16 times, the serial I/O register will be empty and the transfer clock will remain at a high level. At this time the interupt request bit will be set.

External clock—If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 250kHz at a duty cycle of 50%. The timing diagram is shown in Figure 9. An example of communication between two M37420M6-XXXSPs is shown in Figure 10.

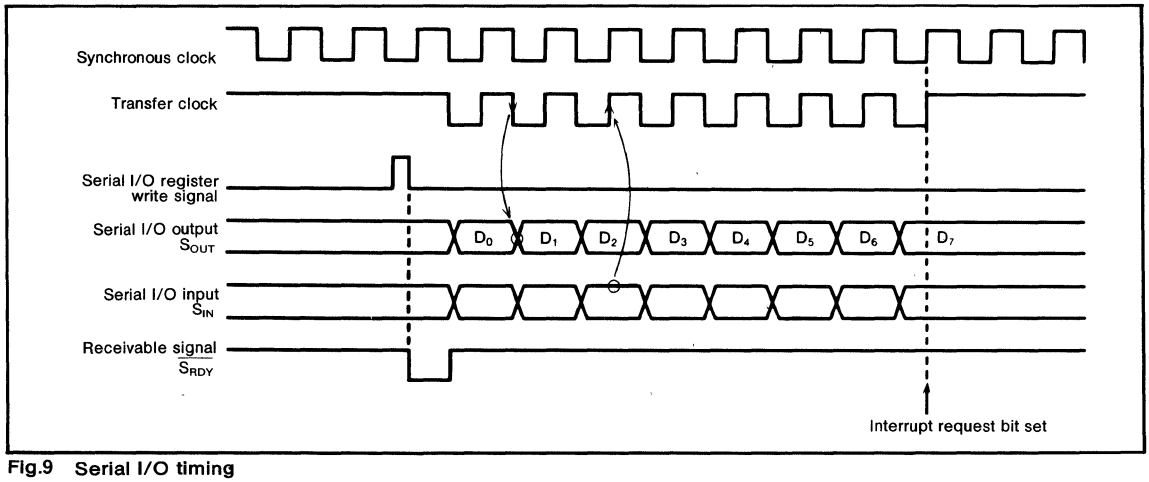


Fig.9 Serial I/O timing

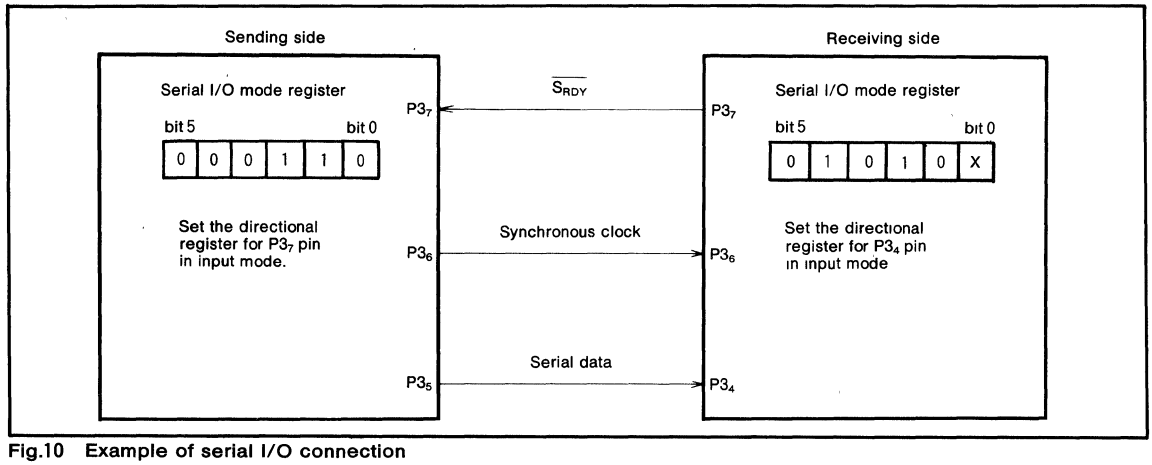


Fig.10 Example of serial I/O connection

A-D CONVERTER

An 8-bit successive approximation method of A-D conversion is employed providing a precision of ±3LSB. A block diagram of the A-D converter is shown in Figure 11. Conversion is automatic once it is started with the program.

The four analog inputs are used in common with pins $P4_7$, $P4_6$, $P4_5$ and $P4_4$ of port 4. Bits 2, 1 and 0 of the A-D control register (address $00F3_{16}$) are used to select which pins are used for A-D conversion. The input condition is accomplished by setting to "0" the bit in the directional register that corresponds to the pin where A-D conversion is to take place. Bit 4 of the A-D control register is the A-D conversion end bit. During A-D conversion, this bit is "0", and upon completion becomes "1". Thus, it can be ascertained whether or not A-D conversion has been completed or not by inspecting this bit. The relation between the contents of the A-D control register and the selection of input pins are shown in Figure 12.

The results of the conversion can be found be reading the contents of the successive approximation register address $00F2_{16}$ which stores the results of the conversion The procedure for executing A-D conversion is next explained. Firstly, the pin that is to be used for the A-D conversion is selected by setting bit 2, bit 1 and bit 0 of the A-D control register. Next, the successive approximation is written to upon which the A-D conversion starts Since actual data is not written to the successive approximation, any type of may be written. Simultaneous with its being written, the A-D conversion end bit (bit 4 of address $00F3_{16}$) is cleared to "0" signifying that A-D conversion operations are being conducted. A-D conversion completes after 198 clock cycles upon which the A-D conversion end bit is set to "1" and the results of the conversion can be found in the successive approximation register. Since the comparator consists of the capacitive coupled configuration, f (X_{IN}) is needed larger than 1MHz during A-D conversion. When A-D conversion is not required, power consumption can be saved by setting bit 5 of the A-D control register to "0". To carry out A-D conversion, set bit 5 to "1", and connect the resistor ladder.

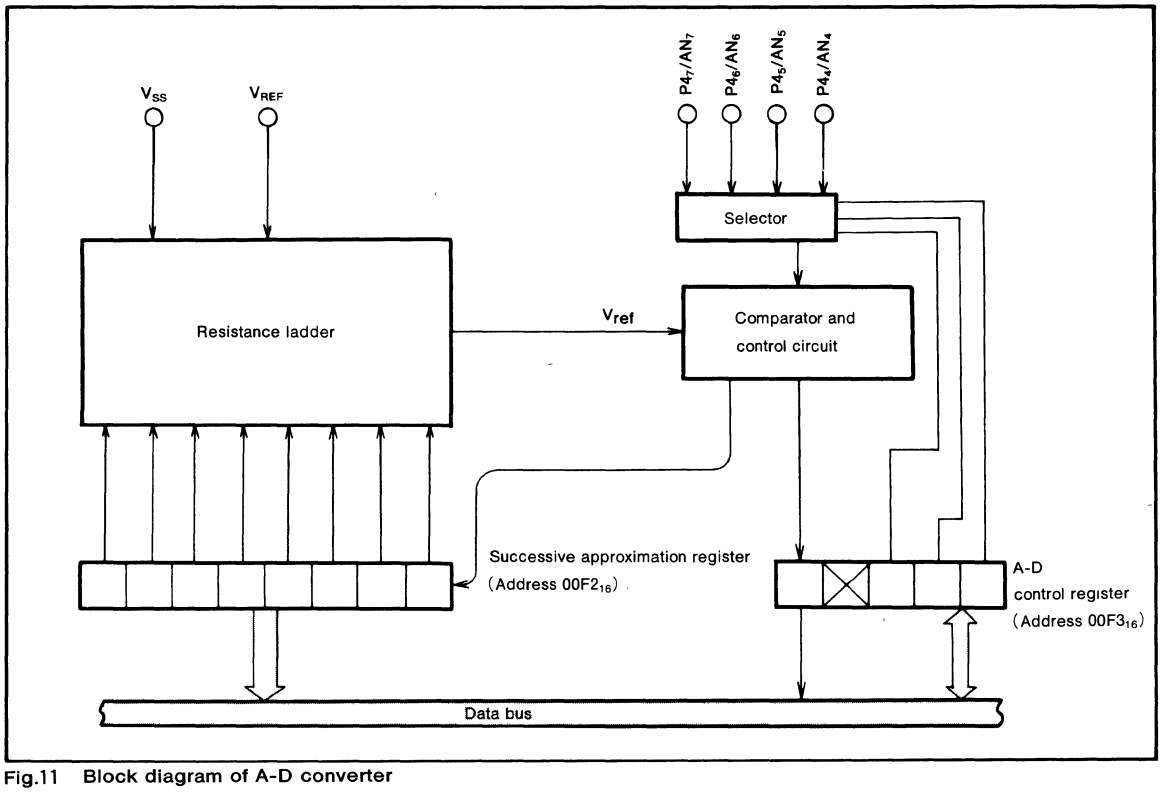


Fig.11 Block diagram of A-D converter

D-A CONVERTER

The M37420M6-XXXSP has two R-2R method D-A converters. D-A conversion starts by setting value to D-A conversion register (address $00D9_{16}$ and $00DA_{16}$).

The output port of D-A conversion result DA_1 or DA_2 is common with $P6_0$ and $P6_1$ respectively. The value of bit 7 or bit 6 of A-D control register (address $00F3_{16}$) determines whether this port is used as D-A output or normal port. When this bit is "1" this port becomes D-A output, and is "0" this port becomes normal port.

Bit 6 or bit 7 corresponds to $P6_0/DA_1$ or $P6_1/DA_2$ respectively. When using each port as D-A output, its directional register must be set to "0".

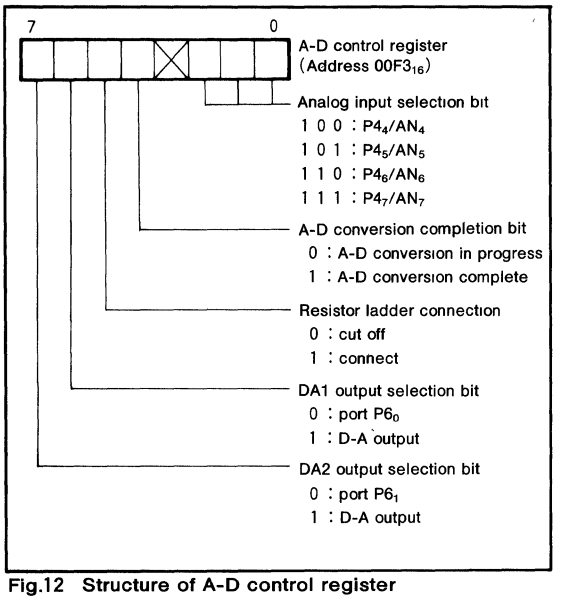


Fig.12 Structure of A-D control register

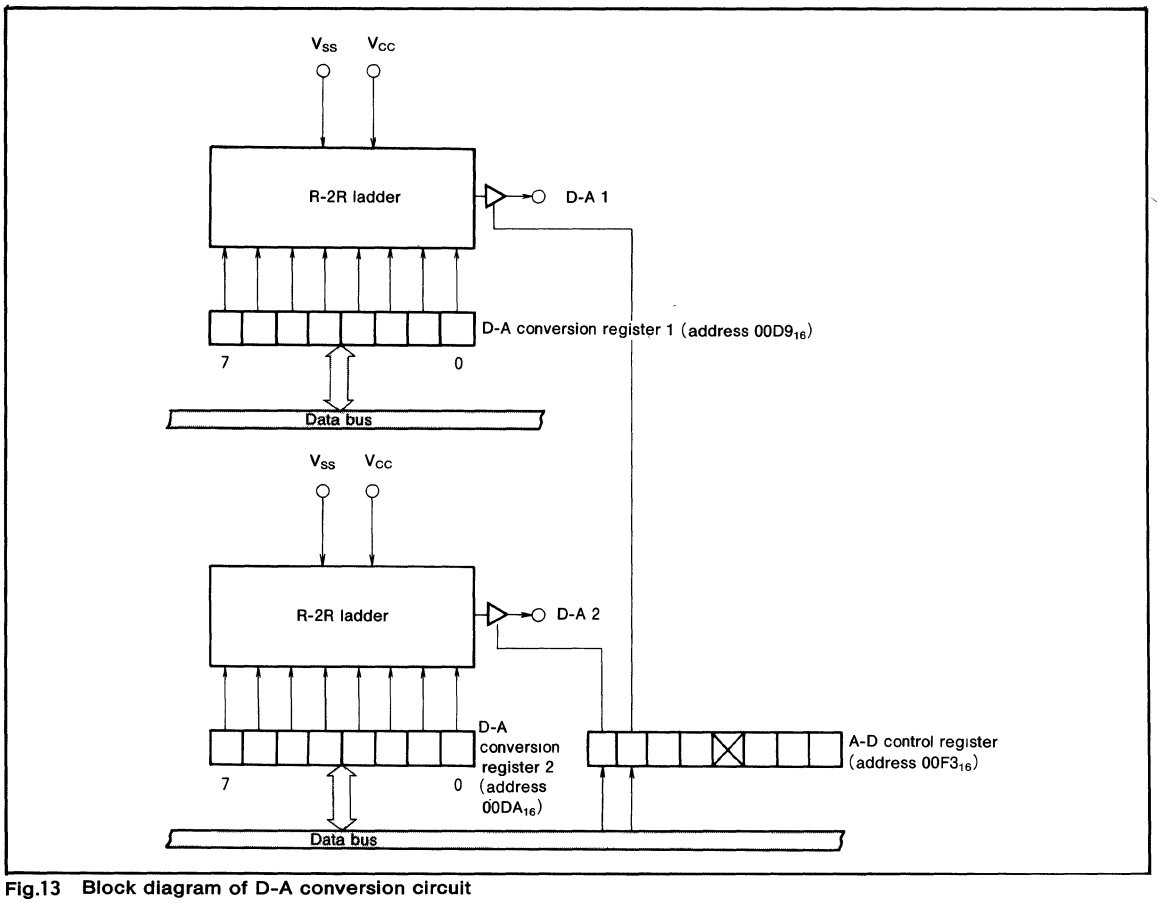


Fig.13 Block diagram of D-A conversion circuit

PWM OUTPUT CIRCUIT

(1) Introduction

The M37420M6-XXXSP is equipped with 14-bit PWM. The 14-bit resolution gives PWM the minimum resolution bit width of 0.25μs (for X_{IN}=8MHz) and a repeat period of 4096μs.

Block diagram of the PWM is shown in Figure 14.

The PWM timing generator section applies control signals to PWM, using clock input X_{IN} divided by 2 as a reference signal.

(2) Data setting

The output pin PWM is in common with pin $P5_7$ (i.e. for PWM output, bit 0 of the special function selection register). When PWM is used for output, first set the higher 8-bit of the PWM1-H register (address $00F0_{16}$), then the lower 6-bit of the PWM1-L register (address $00F1_{16}$). Note that the higher 2 bits of these 8-bit registers are ignored when used 6-bit register.

(3) Transferring data from registers to latches

The data written to the PWM registers is transferred to the PWM latches at the repetition of the PWM period The signals output to the PWM pins correspond to the contents of these latches. When data at addresses $00F0_{16}$ and $00F1_{16}$ are read, data in these latches has already been read allowing the data output by the PWM to be confirmed. When the 6-bit latch is being read, the upper 2 bits of the register becomes undefined. However, bit 7 of the PWM1-L register indicated the completion of the data transfer from the PWM1 register to the PWM1 latch. If bit 7 is "0", the transfer has been completed, if bit 7 is "1", the transfer has not yet begun.

(4) 14-bit PWM operation

The timing diagram of the 14-bit PWM1 is shown in Figure 15. The 14-bit PWM divides the data within the PWM latch into the lower 6 bits and higher 8 bits.

A high-level area within a length N times τ is output every short area of t=256 τ =64μs as determined by data N of the higher 8 bits. (Refer to PWM output ② in the lower part of Figure 15.)

Thus, the time for the high-level area is equal to the time set by the lower 8 bits or that plus τ As a result, the short-area period t(=64μs, approx. 15.6kHz) becomes an approximately repetitive period.

(5) Output after reset

At reset the output of port $P5_7$ is in the high impedance state and the contents of the PWM register and latch are undefined. Note that after setting the PWM register, its data is transferred to the latch.

Table 2. Relation between the 6 lower-order bits of data and the space set by the ADD bit

6 lower-order bits of data	Area longer by τ than that of other t_m (m = 0 ~ 63)
0 0 0 0 0 0 (LSB)	Nothing
0 0 0 0 0 1	m=32
0 0 0 0 1 0	m=16, 48
0 0 0 1 0 0	m= 8, 24, 40, 56
0 0 1 0 0 0	m= 4, 12, 20, 28, 36, 44, 52, 60
0 1 0 0 0 0	m= 2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62
1 0 0 0 0 0	m= 1, 3, 5, 7, ····· ····· ·57, 59, 61, 63

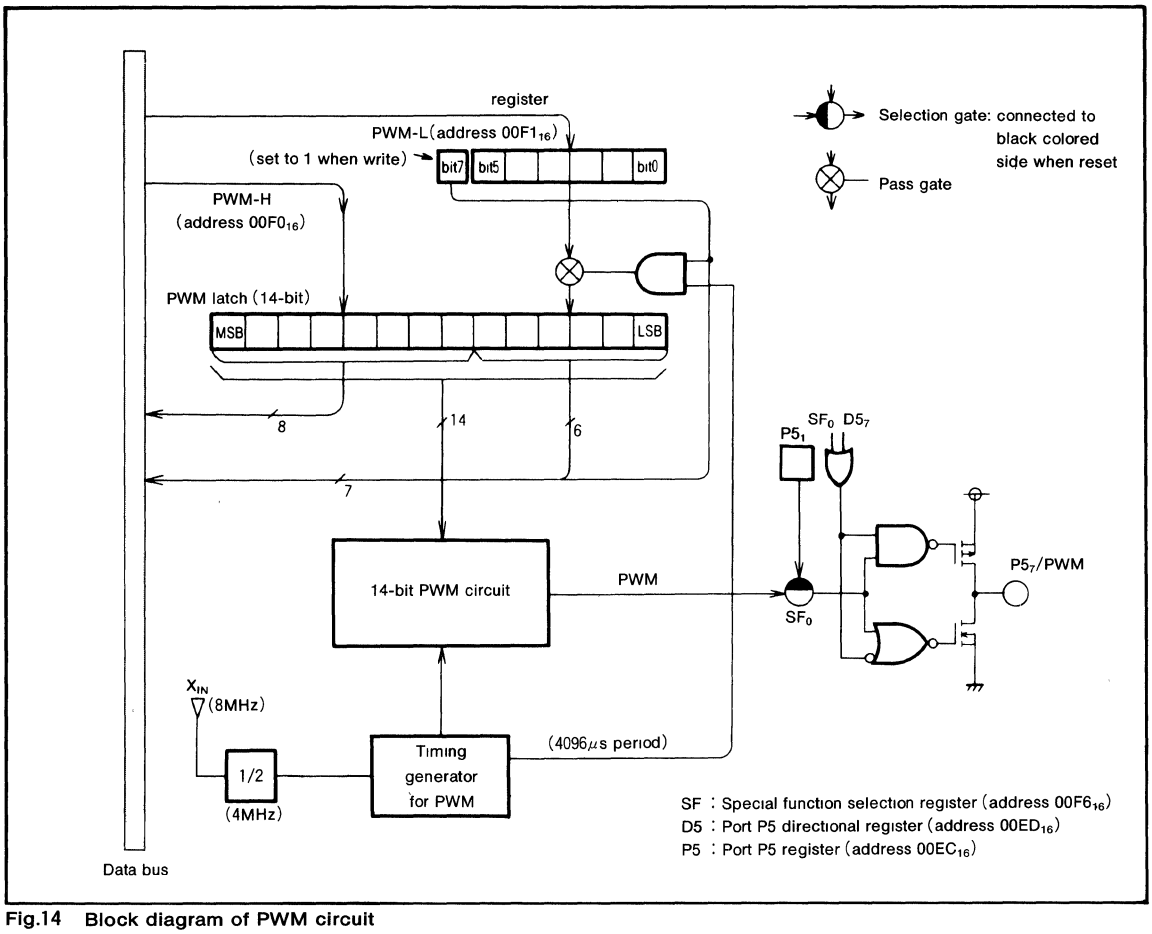


Fig.14 Block diagram of PWM circuit

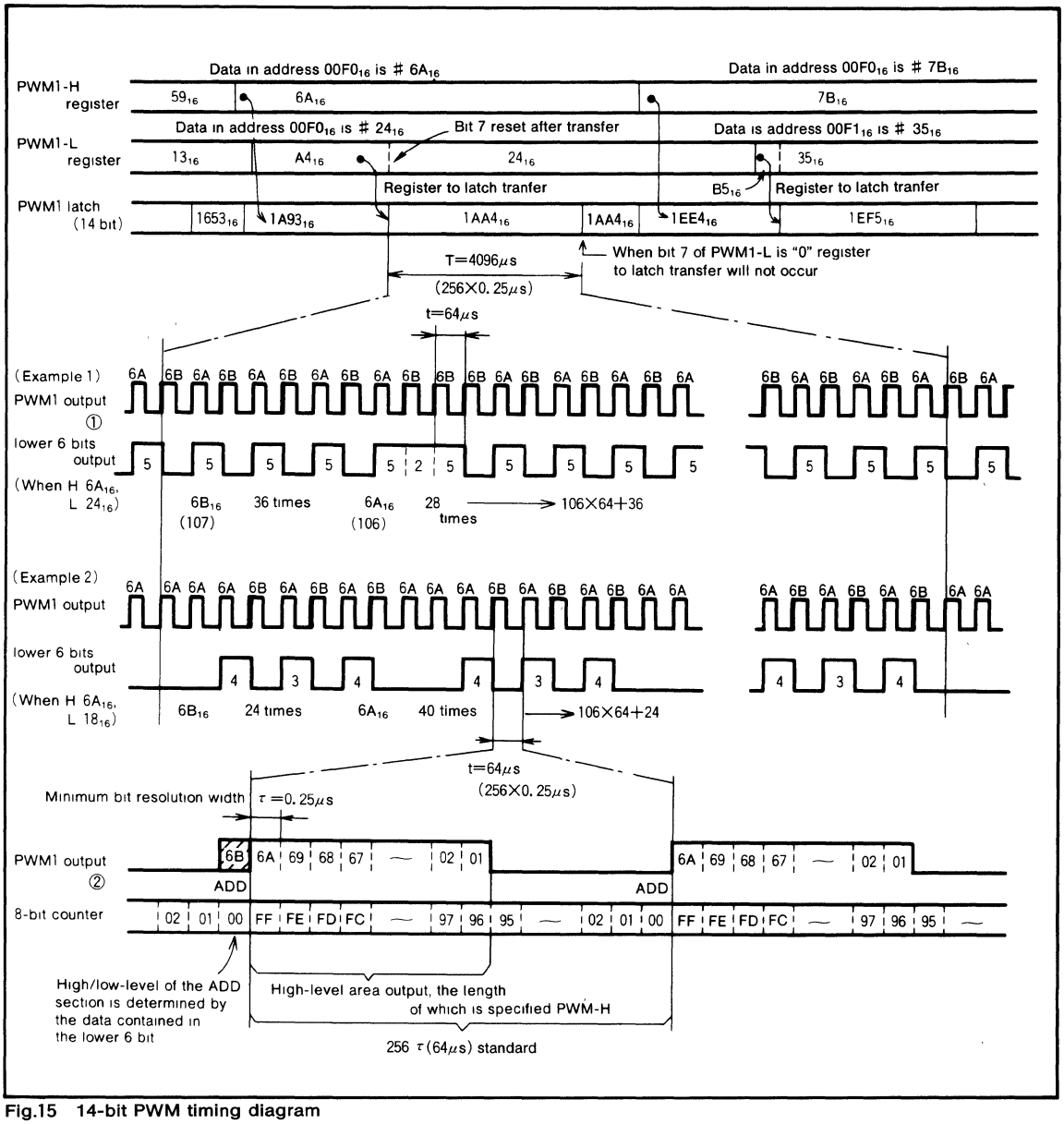


Fig.15 14-bit PWM timing diagram

V pulse and Y pulse generator

Pin 5_4 operates as the VPLS pin to output the V pulse and pin 5_3 operates as the T pin to which the trigger clock is input. These pins can be used as the V pulse output by setting bit 5 of the V pulse register ($00DD_{16}$) to "1". Pin $P5_6$ operates as the YPLS pin which outputs the Y pulse. It can be used as the Y pulse (VPF signal) output by setting bit 6 of the V pulse register to "1". Figure 17 shows the block diagram of the V pulse, Y pulse generator. Figure 18 shows the timing chart of the V pulse and Y pulse.

At the falling or rising edge of T, the VPP counter starts. By the overflow signal of the VPP counter, VPLS goes "H". By the overflow signal of VPP counter, the VPN counter starts. By the overflow signal of the VPN counter, VPLS goes "L". When the VPP counter or the VPN counter is counting, bit 4 of the V pulse register is "1".

The preset value of the VPP counter can be set by the 9-bit register with bit 1 of the V pulse register being the most significant bit and the V pulse preset value P ($00DB_{16}$) being the low-order eight bits. The preset value of the VPN counter can be set by the 9-bit register with bit 0 of the V pulse register being the least significant bit and the V pulse preset value N ($00DB_{16}$) being the low-order eight bits.

Note that values of bits 0 and 1 of the V pulse register are the current counting values in the VPP counter and the VPN counter, not the preset values of the counters.

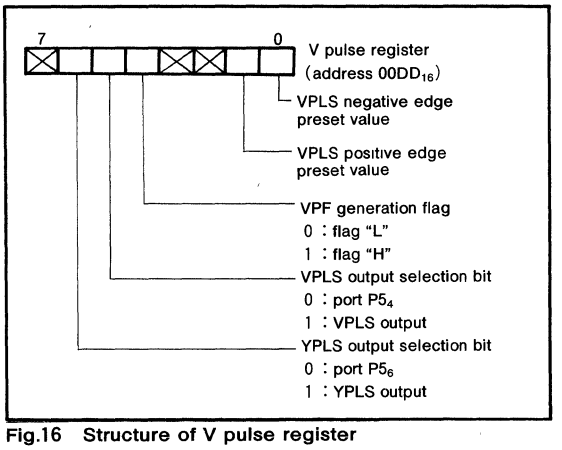


Fig.16 Structure of V pulse register

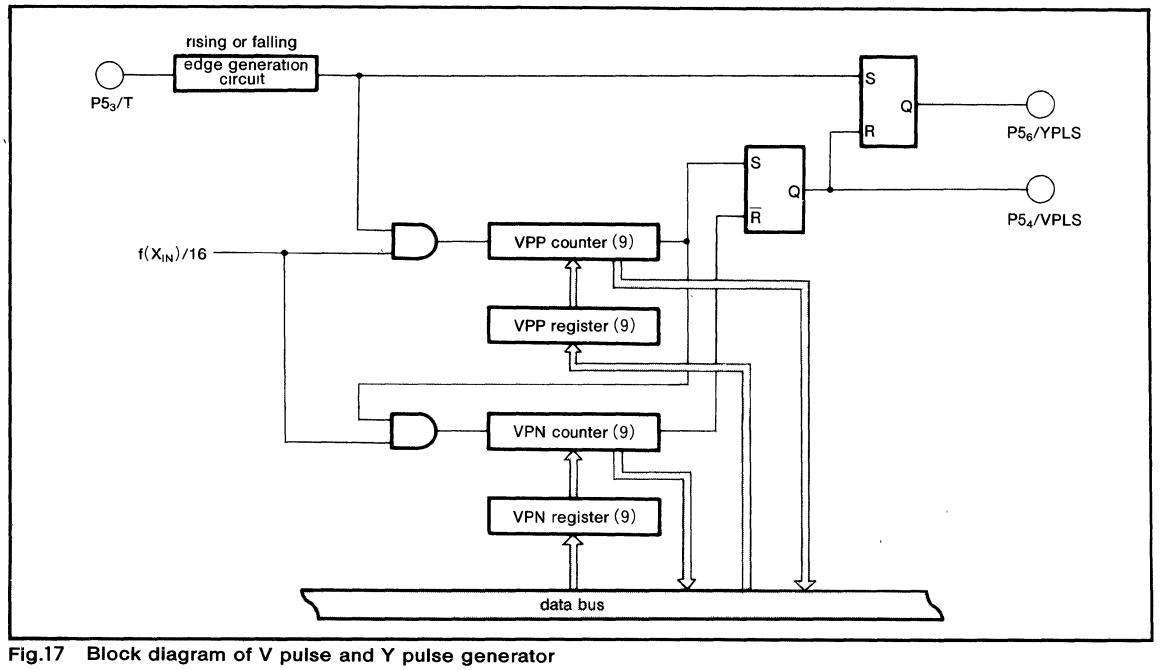


Fig.17 Block diagram of V pulse and Y pulse generator

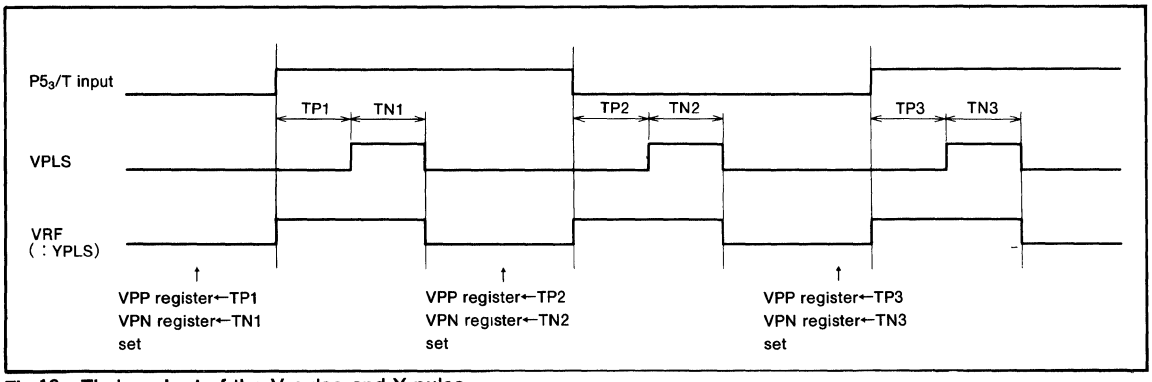


Fig.18 Timing chart of the V pulse and Y pulse

Edge sense input

Ports $P5_0 \sim P5_3$ are the input ports having the edge sense function. To use these ports as edge sense inputs, read data from address $00ED_{16}$. Address $00ED_{16}$ has a latch. $P5_0 \sim P5_2$ are set to "1" when the input changes from "H" to "L". $P5_3$ is set to "1" when the input changes from "H" to "L" and from "L" to "H". For the input pulse width, seven or more clock cycles are necessary. This latch is cleared by writing "0" at address $00ED_{16}$ by the LDM or CLB instruction. When data is read from address $00ED_{16}$, the high-order four bits are always "0's". At reset, the content of this latch is "0". When a read operation is performed from address $00EC_{16}$, the normal level sense input will result.

External trigger output

Pin $P5_5$ operates as the pin Q which outputs the external trigger signal. Pin $P5_3$ operates as the pin T which inputs the trigger clock. By setting bit 5 of the special function selection register (address $00F6_{16}$) to "1", these pins can be used as the external trigger outputs.

In the external trigger mode, every time the falling edge and rising edge of T are detected, the contents of $P5_5$ port output latch and the $P5_5$ direction register latch are output from the port. Depending on the combination of the port output latch and the directional register latch, the output to port $P5_5$ becomes as shown in Table 3. At reset, the content of this bit is "0".

Table 3. External trigger output

output latch / directional register	0	1
0	high-impedance	high-impedance
1	L	H

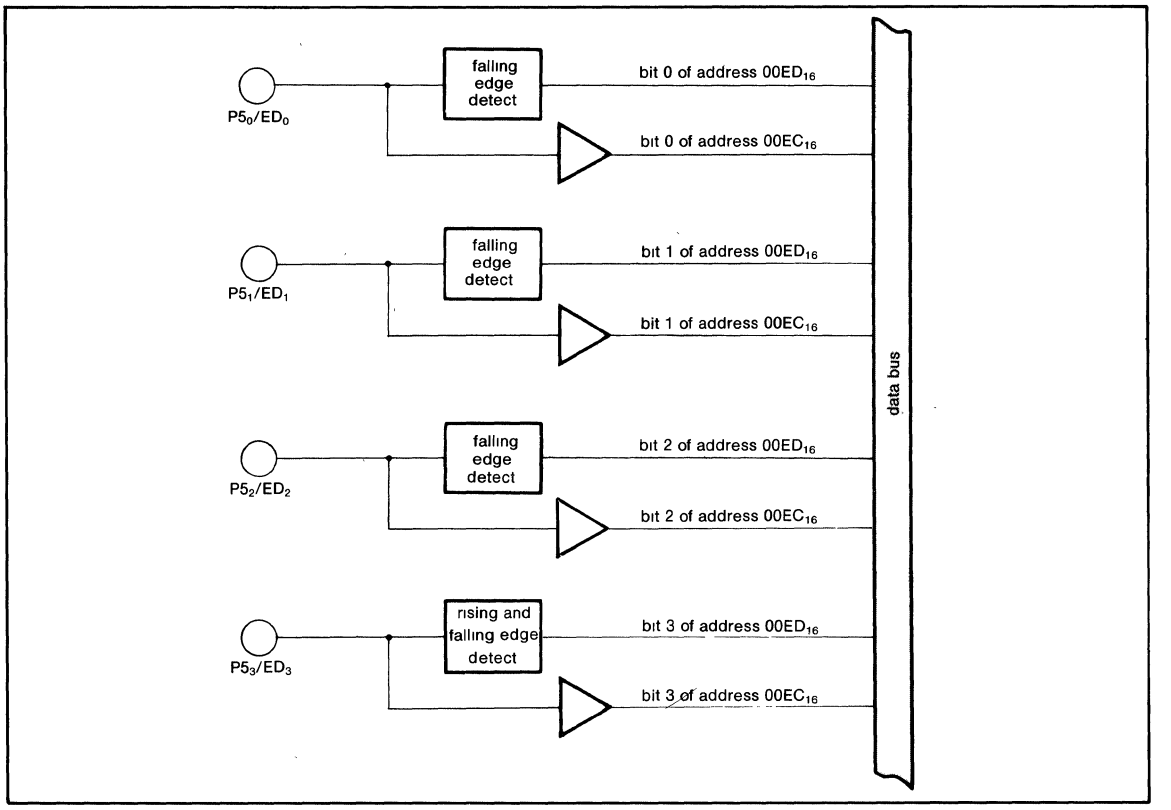


Fig.19 Block diagram of edge sence input

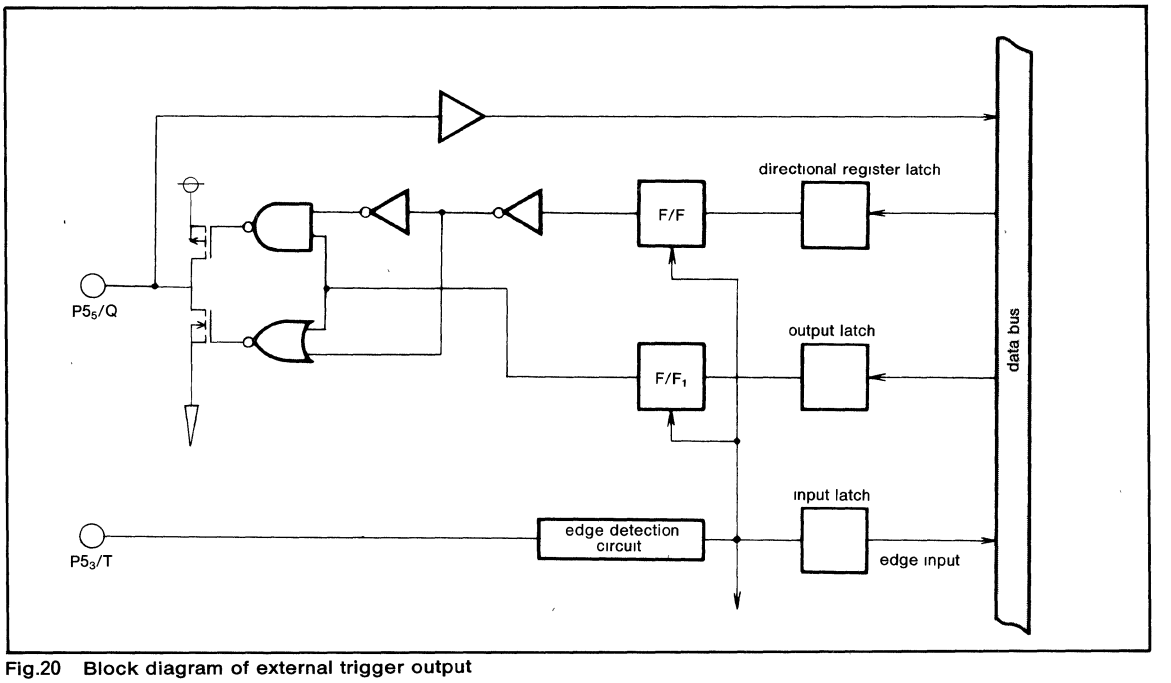


Fig.20 Block diagram of external trigger output

MITSUBISHI ELECTRIC

WATCHDOG TIMER

The watchdog timer provides the means to return to a reset condition when a program runs wild and the program will not run the normal loops.

The watchdog timer (address $00F4_{16}$) is a 15-bit counter. The watchdog timer counts 1/16th the output frequency of the oscillator. The watchdog timer is set to $7FFF_{16}$ when a reset is accomplished a write operation has been made to it. As well as any of the instructions that generate a write signal, such as STA, LDM, and CLB, can be used to write data to the watchdog timer. An output of the most significant bits of the watchdog timer is input to the reset circuit. When 262144 clock cycles have been counted, the most significant bit becomes "0" and reset is carried out. When reset is carried out, the watchdog timer is set to $7FFF_{16}$ and reset is released. The program then begins again from reset vector address. Normally, the program is written so that a writing operation is made to the watchdog timer prior to the most significant bit's becoming "0"

Since execution of the STP instruction causes both the clock and the watchdog timer to stop, an option is offered where the STP instruction can be disabled.

RESET CIRCUIT

The M37420M6-XXXSP is reset according to the sequence shown in Figure 21. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for more than 2μs while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 22.

An example of the reset circuit is shown in Figure 23.

When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

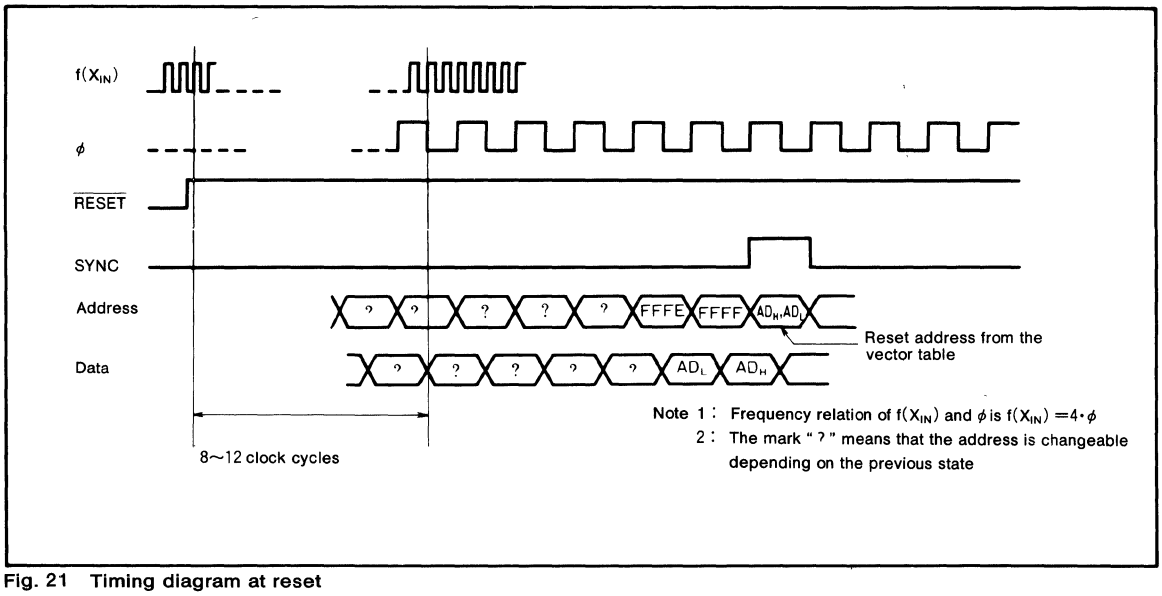


Fig. 21 Timing diagram at reset

		address	
(1)	D-A conversion register 1	($D9_{16}$)	00_{16}
(2)	D-A conversion register 2	(DA_{16})	00_{16}
(3)	Port P0 directional register	($E1_{16}$)	00_{16}
(4)	Port P1 directional register	($E3_{16}$)	00_{16}
(5)	Port P2 directional register	($E5_{16}$)	00_{16}
(6)	Port P3 directional register	($E9_{16}$)	00_{16}
(7)	Port P4 directional register	(EB_{16})	00_{16}
(8)	Port P5 latch/directional register	(ED_{16})	00_{16}
(9)	Port P6 directional register	(EF_{16})	00_{16}
(10)	A-D control register	($F3_{16}$)	0 0
(11)	Watchdog timer	($F4_{16}$)	$7FFF_{16}$
(12)	Serial I/O mode register	($F5_{16}$)	0 0 0 0 0 0 0 0
(13)	Special function selection register	($F6_{16}$)	0 0 0 0 0 0
(14)	Prescaler X	(FC_{16})	FF_{16}
(15)	Timer X	(FD_{16})	01_{16}
(16)	Interrupt control register	(FE_{16})	00_{16}
(17)	Timer control register	(FF_{16})	00_{16}
(18)	Interrupt disable flag on processor status register	(PS)	1
(19)	Program counter	(PC_H)	Contents of address $FFFF_{16}$
		(PC_L)	Contents of address $FFFE_{16}$

Note 1 : Port P6 is the high-impedance state during reset
After return from reset, it is "FF_{16}".

Fig.22 Internal state of microcomputer at reset

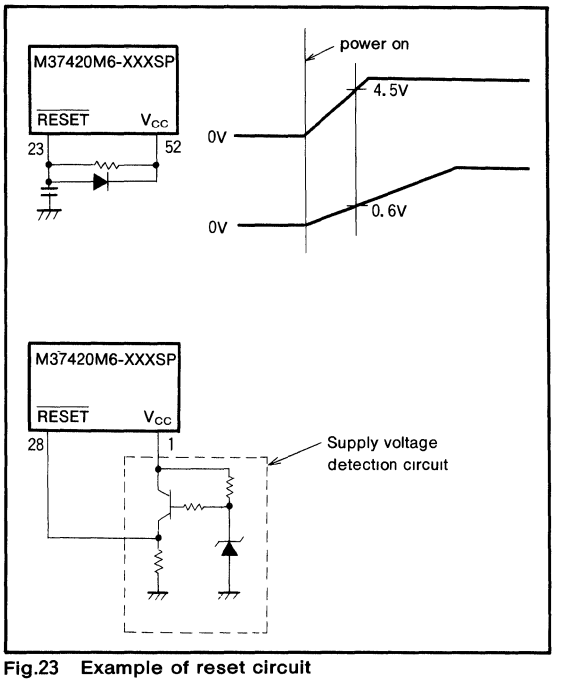


Fig.23 Example of reset circuit

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with N-channel open drain output.

As shown in the memory map (Figure 2), port P0 can be accessed at zero page memory address $00E0_{16}$. Port P0 has a directional register (address $00E1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

(2) Port P1

Port P1 is a 6-bit I/O port and has the same function as Port P0.

(3) Port P2

Port P2 has the same function as Port P0, but it has CMOS output.

(4) Port P3

Port P3 has the same function as port P0. Port P3 can also be used as serial I/O, $\overline{INT_1}$, $\overline{INT_2}$ and I/O pins for timer X.

(5) Port P4

Port P4 is a 4-bit I/O port and has the same function as port P0. But $P4_7$ through $P4_4$ can also be used as analog input pins AN_7 through AN_4.

(6) Port P5

Port $P5_3 \sim P5_0$ is an input port and can also be used as edge sence inputs. In such a case, reading is begun from $00ED_{16}$.

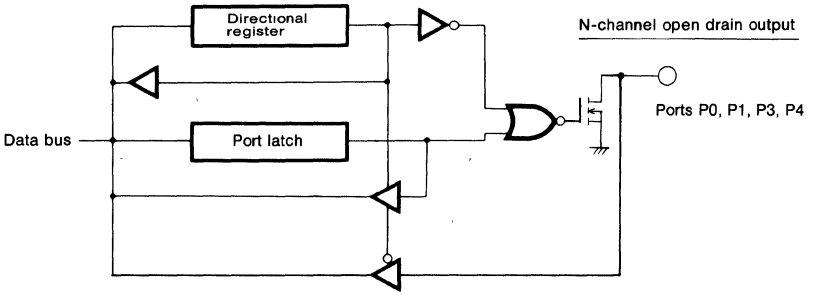
When port P5 is used as level sense input, read the contents of the address $00EC_{16}$.

$P5_7 \sim P5_4$ have the same function as port P0 except that they are I/O ports and double-functioning. The PWM output pin operates as $P5_7$, the Y pulse output pin as $P5_6$, and the V pulse output pin as $P5_4$. These ports are used by selecting the function through the special function selection register and the V pulse register. For details, see the descriptions of the PWM and the V pulse, Y pulse generator. The external trigger output pin operates as $P5_5$. The external trigger output mode can be selected by setting bit 2 of the special function select register to "1". At reset, all of $P5_7 \sim P5_4$ are in the state where the nomal I/O port function is selected. The output is the CMOS output.

(7) Port P6

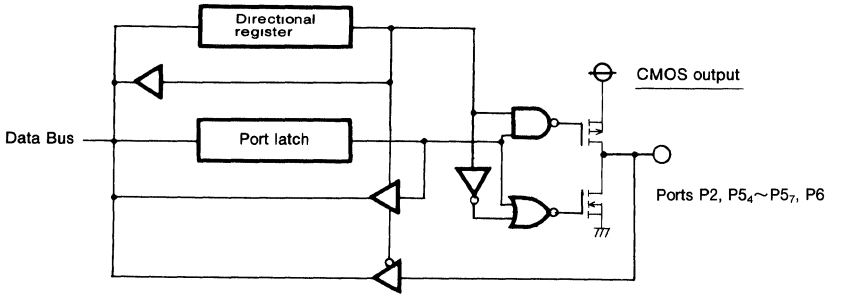
Port P6 is a 4-bit I/O port and has the same function as P0 except that $P6_0$ and $P6_1$ can be used as D-A output pin.

Ports P0, P1, P3, P4



Note 1 : Port P3 can be also used as I/O pin of serial I/O, timer I/O, and interrupt input
Port P4 can be also used as analog input

Ports P2, $P5_4$~$P5_7$, P6



Note 2 : Port $P5_4$~$P5_7$ can be also used as the PWM output, Y pulse output, external trigger output (Q) and V pulse output Port P6 can be also used as D-A output

Ports $P5_0$~$P5_3$

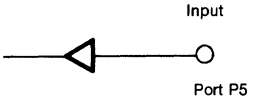


Fig.24 Block diagram of ports P0~P6

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 27.

When the STP instruction is executed, the oscillation of internal clock ϕ is stopped in the "H" state.

Also, the prescaler X and timer X are loaded with FF_{16} and 01_{16}, respectively. The oscillator (dividing by 16) is then connected to the prescaler input. This connection is cleared when timer X overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the internal clock ϕ keeps its "H" level until timer X overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 25.

The constant capacitance will differ depending on which oscillator is used; and should be set to the manufactures suggested value.

The example of external clock usage is shown in Figure 26. X_{IN} is the input, and X_{OUT} is open.

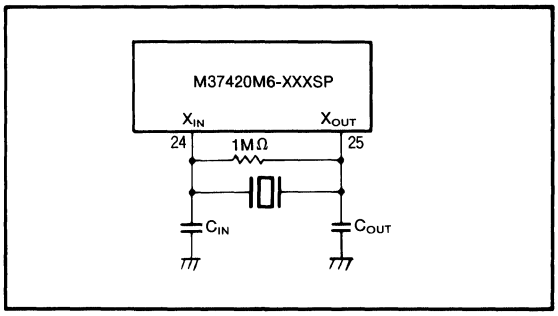


Fig.25 External ceramic resonator circuit

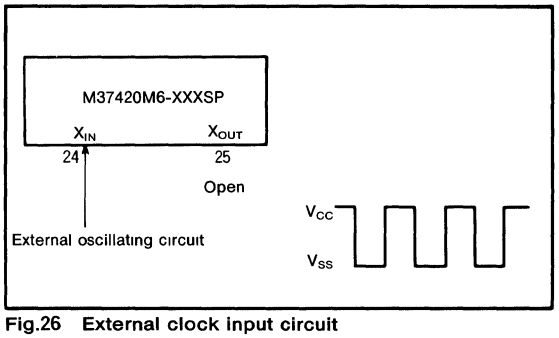


Fig.26 External clock input circuit

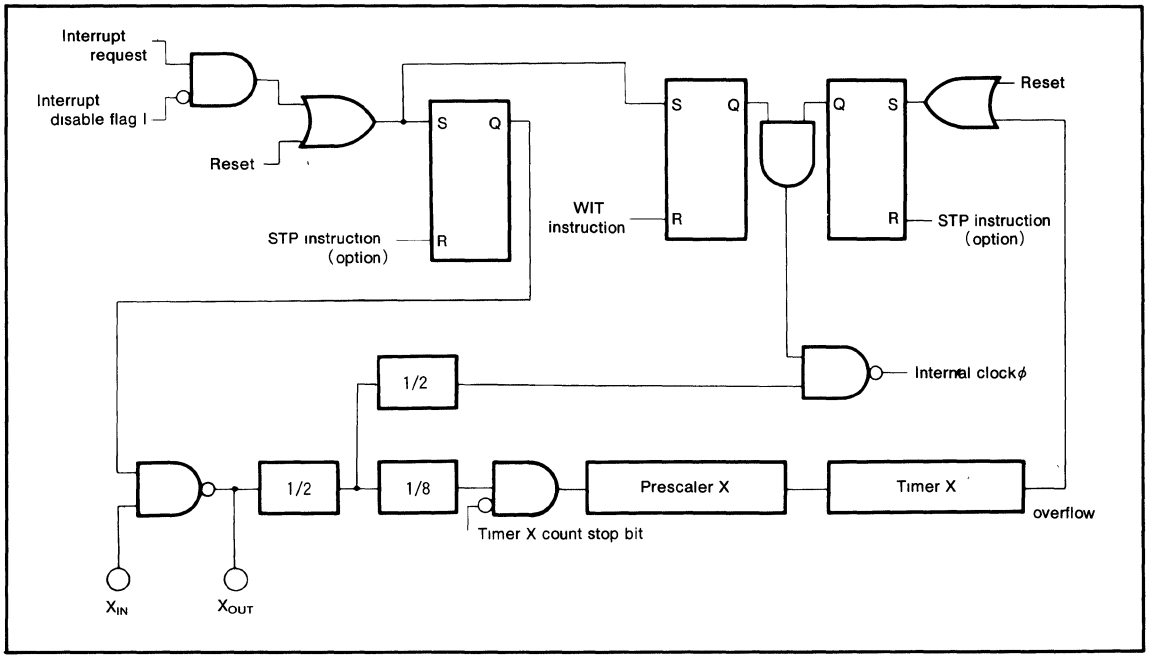


Fig.27 Block diagram of the clock generating circuit

PROGRAMMING NOTES

(1) The frequency ratio of the timer and the prescaler is 1/(n+1).

(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) Reading the timer and prescaler must be avoided while the input to the prescaler is changing.

(4) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.

(5) A NOP instruction must be used after the execution of a PLP instruction.

(6) Since the comparator consists of the capacitive coupled configuration, $f(X_{IN})$ is needed larger than 1MHz during A-D conversion. And during A-D conversion, don't use STP or WIT instruction.

(7) Values of bits 0 and 1 of the V pulse register are the current counting values in the VPP counter and the VPN counter, not the preset values.
Therefore, if the read values of bits 0 and 1 are written as they are when other bits in the V pulse register is to be set, the preset values may be changed.
This must be kept in mind before executing the SEB or CLB instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

(1) mask ROM confirmation form

(2) mark specification form

(3) ROM data ..... EPROM 3sets

Write the following option on the mask ROM confirmation form

- STP instruction option
- Reset option for watchdog timer

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors cut-off	−0.3~7	V
V_I	Input voltage X_{IN}		−0.3~7	V
V_I	Input voltage $P2_0$~$P2_7$, $P4_2$~$P4_7$, $P5_4$~$P5_7$, $P6_0$~$P6_3$		−0.3~V_{CC}+0.3	V
V_I	Input voltage $P0_0$~$P0_7$, $P1_0$~$P1_5$, $P3_0$~$P3_7$, $P4_0$, $P4_1$, $P5_0$~$P5_7$		−0.3~13	V
V_I	Input voltage CNV_{SS}, $\overline{RESET}$		−0.3~13	V
V_O	Output voltage $P2_0$~$P2_7$, $P4_2$~$P4_7$, $P5_4$~$P5_7$, $P6_0$~$P6_3$		−0.3~V_{CC}+0.3	V
V_O	Output voltage $P0_0$~$P0_7$, $P1_0$~$P1_5$, $P3_0$~$P3_7$		−0.3~13	V
P_d	Power dissipation	T_a=25℃	1000	mW
T_{opr}	Operating temperature		−10~70	℃
T_{stg}	Storage temperature		−40~125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{REF}	Reference voltage	4		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$~$P0_7$, $P1_0$~$P1_5$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $\overline{RESET}$, X_{IN}, $P6_0$~$P6_3$	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, CNV_{SS}, $P6_0$~$P6_3$	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$~$P0_7$, $P1_0$~$P1_5$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$ (Note 2)			10	mA
$I_{OL(peak)}$	"L" peak output current $P6_0$~$P6_3$ (Note 2)			10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$~$P0_7$, $P1_0$~$P1_5$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, (Note 1)			5	mA
$I_{OL(avg)}$	"L" average output current $P6_0$~$P6_3$ (Note 1)			5	mA
$I_{OH(peak)}$	"H" peak output current $P2_0$~$P2_7$, $P5_4$~$P5_7$, $P6_0$~$P6_3$ (Note 2)			−10	mA
$I_{OH(avg)}$	"H" average output current $P2_0$~$P2_7$, $P5_4$~$P5_7$, $P6_0$~$P6_3$ (Note 1)			−5	mA
$f(X_{IN})$	Internal clock oscillating frequency			8	MHz

Note 1 : Average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms
2 : Total of "L" output current I_{OL}, of ports P0, P1, P2, P3, P4, P6, and PWM is 80mA max
Total of "H" output current I_{OH}, of port P2 is 50mA max

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, T_a=−10~70℃, f(X_{IN})=8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	"H" output voltage $P2_0$~$P2_7$, $P5_4$~$P5_7$, $P6_0$~$P6_3$	I_{OH}=−10mA	3			V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_5$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_4$~$P5_7$, $P6_0$~$P6_3$	I_{OL}=10mA			2	V
$V_{T+}-V_{T-}$	Hysteresis $P3_0$, $P3_1$	When used as INT input	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $P3_6$	When used as $\overline{CLK_2}$ input	0.3	0.8		V
$V_{T+}-V_{T-}$	Hysteresis $P3_3$	When used as CNTR input	0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis $P5_3$	When used as T input	0.5	1		V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$			0.5	0.7	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_5$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_3$, PWM	V_I=0V			−5	μA
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}	V_I=0V			−5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_5$, $P3_0$~$P3_7$, $P5_0$~$P5_3$	V_I=12V			12	μA
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}, $P2_0$~$P2_7$, $P4_4$~$P4_7$, $P5_4$~$P5_7$, $P6_0$~$P6_3$	V_I=5V			5	μA
V_{RAM}	RAM retention voltage	At clock stop	2			V
I_{CC}	Supply current	φ, X_{OUT}, and D-A pins opened, other pins at V_{SS}, and A-D converter in the finished condition f(X_{IN})=8MHz Square wave		3	6	mA

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=AV_{SS}=0V, T_a=−10~70℃, f(X_{IN})=8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	V_{REF}=V_{CC}			8	Bits
—	Absolute accuracy	V_{REF}=V_{CC}			±3	LSB
R_{LADDER}	Ladder resistance value	V_{REF}=V_{CC}	2		10	kΩ
t_{CONV}	Conversion time				25	μs
V_{IA}	Analog input voltage		0		V_{CC}	V

D-A CONVERTER CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=AV_{SS}=0V, T_a=−10~70℃, f(X_{IN})=8MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	V_{REF}=V_{CC}			8	Bits
—	Error in full scale range	V_{REF}=V_{CC}			±2	%
t_{SU}	Setup time	V_{REF}=V_{CC}			3	μs
R_O	Output resistance	V_{REF}=V_{CC}	1	2	4	kΩ