M37421P-000SS
M37421P-001SS

PIGGYBACK for M37421M6-XXXSP

DESCRIPTION

The M37421P-000SS and the M37421P-001SS are EPROM mounted-type microcomputers which utilizes CMOS technology, and is designed for developing programs for single-chip 8-bit microcomputer the M37421M6-XXXSP. It is housed in a piggyback-type 64-pin shrink DIP.

There is a 28-pin socket on the package for the M5L27128K or the M5L27256K EPROM.

The M37421P-000SS and the M37421P-001SS simplify the development of programs for the M37421M6-XXXSP and is excellent for making prototypes.

FEATURES

- Differences with the M37421M6 are:

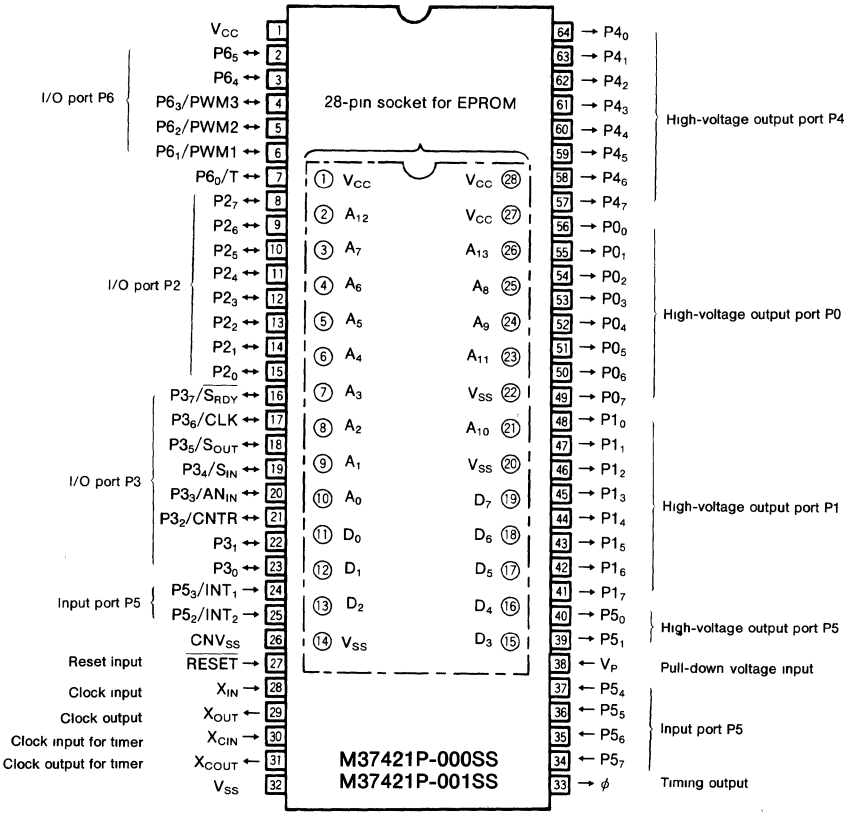
(1) ROMless, EPROM is attached externally.

(2) Suitable EPROM is the M5L27128K or the M5L27256K.

APPLICATION

Development of programs for VCR, tuners, and audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



Outline 64S1M

The symbol "○" indicates sockets for EPROM

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PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±5% to V_{CC}, and 0V to V_{SS}
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}
V_P	Pull-down voltage	Input	This is the input voltage pin for the pull-down transistor of ports P0, P1, P4, $P5_0$ and $P5_1$
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin ϕ=2MHz (when X_{IN}=4MHz)
X_{CIN}	Clock input for clock function	Input	This is the I/O pins of the clock generating circuit for the clock function To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{CIN} and X_{COUT} pins If an external clock is used, the clock source should be connected to the X_{CIN} pin, and the X_{COUT} pin should be left open This clock can be used as a program controlled the system clock
X_{COUT}	Clock output for clock function	Output	
$P0_0$~$P0_7$	Output port P0	Output	Port P0 is an 8-bit output port Output structure is high-voltage P-channel open drain A pull-down transistor is built in between the V_P pin and this port At reset, this port is set to a "L" level
$P1_0$~$P1_7$	Output port P1	Output	Port P1 is an 8-bit output port and has basically the same functions as port P0
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output At reset, this port is set to input mode. The output structure is N-channel open drain
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P2 When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$ CLK, S_{OUT}, and S_{IN} pins, respectively
$P4_0$~$P4_7$	Output port P4	Output	Port P4 is an 8-bit output port and has basically the same functions as port P0
$P5_0$, $P5_1$	Output port P5	Output	Bit 0 and 1 of port P5 are 2-bit output port and has basically the same functions as port P0
$P5_2/INT_2$, $P5_3/INT_1$	Input port P5	Input	Bit 2 and 3 of port P5 are 2-bit input port and are in common with interrupt inputs
$P5_4$~$P5_7$		Input	Bit 4~7 of port P5 are 4-bit input port
$P6_0$~$P6_5$	I/O port P6	I/O	Port P6 is a 6-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output The output structure is CMOS tri-state output $P6_0$, $P6_1$, $P6_2$, $P6_3$ can be programmed to function as timer output pin (T), PWM output pins (PWM1, PWM2, and PWM3), respectively
A_0~A_{14}	Output port A	Output	These are for addresses to an EPROM mounted on the package
D_0~D_7	Input port D	Input	These are for input data from an EPROM mounted on the package

EXPLANATION OF FUNCTION BLOCK OPERATION

The differences between the M37421P-000SS, the M37421P-001SS and the M37421M6-XXXSP are noted below. The following explanations apply to the M37421P-000SS and the M37421P-001SS.

Specification variations for other chips are noted accordingly.

MEMORY

The M37421P-000SS and the M37421P-001SS are mounted an EPROM instead of an internal ROM.

RAM size is 512 bytes, and addresses 0100_{16} to $023F_{16}$ are used for the stack.

The address of an EPROM is $8000_{16} \sim FFFF_{16}$, and this memory size is 32K bytes. Other than these, the M37421P-000SS and the M37421P-001SS have the same functions as the M37421M6-XXXSP has.

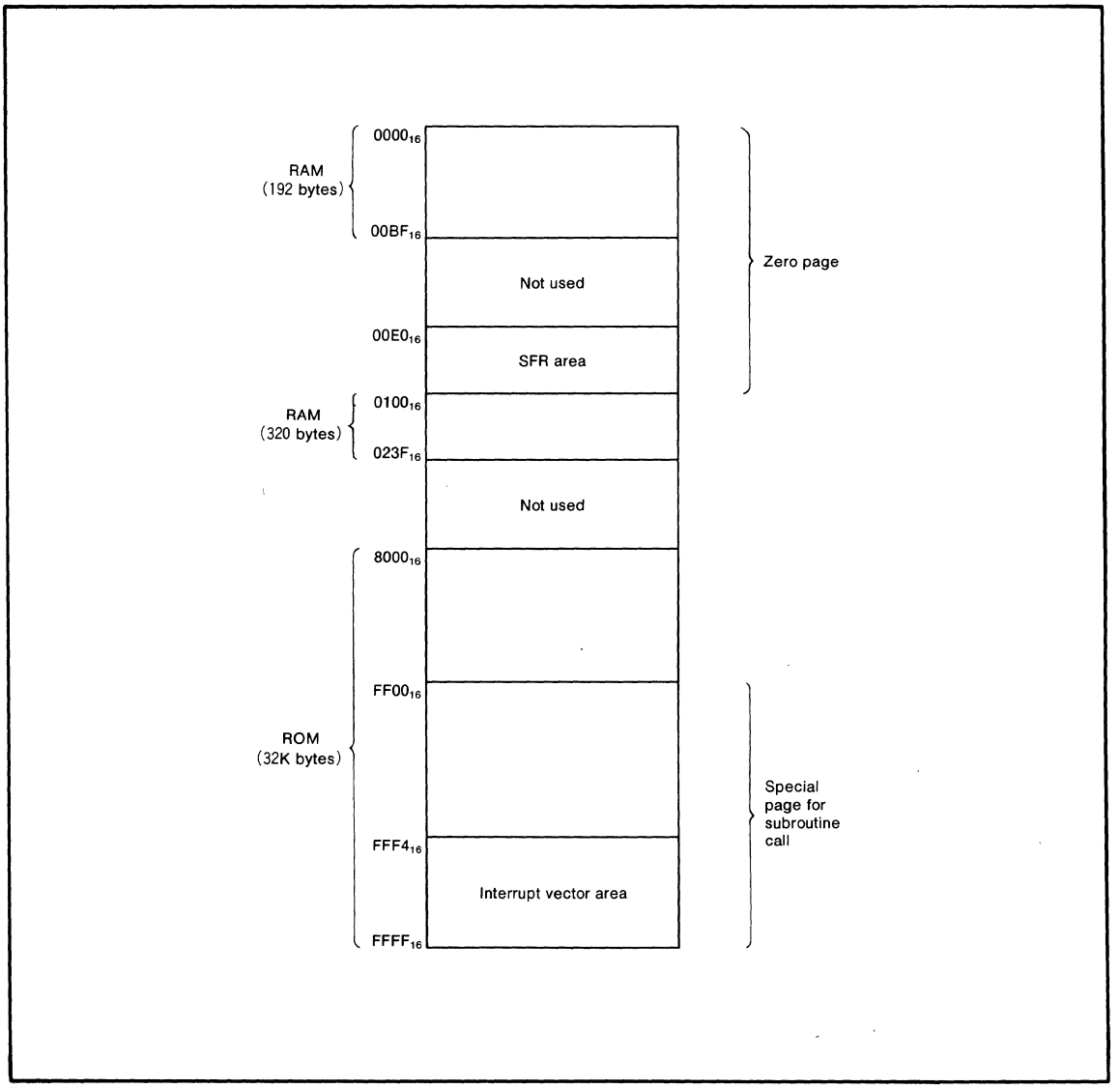

Fig.1 Memory map

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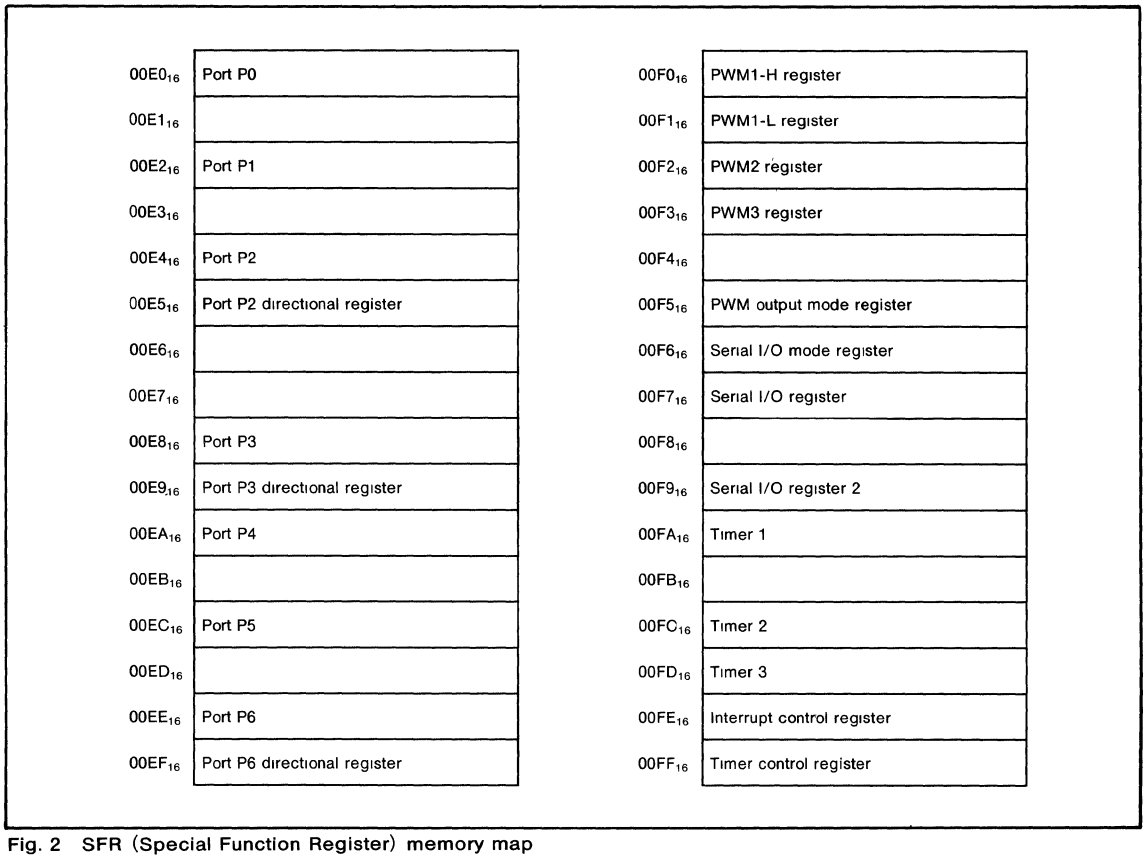

$00E0_{16}$	Port P0	$00F0_{16}$	PWM1-H register
$00E1_{16}$		$00F1_{16}$	PWM1-L register
$00E2_{16}$	Port P1	$00F2_{16}$	PWM2 register
$00E3_{16}$		$00F3_{16}$	PWM3 register
$00E4_{16}$	Port P2	$00F4_{16}$	
$00E5_{16}$	Port P2 directional register	$00F5_{16}$	PWM output mode register
$00E6_{16}$		$00F6_{16}$	Serial I/O mode register
$00E7_{16}$		$00F7_{16}$	Serial I/O register
$00E8_{16}$	Port P3	$00F8_{16}$	
$00E9_{16}$	Port P3 directional register	$00F9_{16}$	Serial I/O register 2
$00EA_{16}$	Port P4	$00FA_{16}$	Timer 1
$00EB_{16}$		$00FB_{16}$	
$00EC_{16}$	Port P5	$00FC_{16}$	Timer 2
$00ED_{16}$		$00FD_{16}$	Timer 3
$00EE_{16}$	Port P6	$00FE_{16}$	Interrupt control register
$00EF_{16}$	Port P6 directional register	$00FF_{16}$	Timer control register

Fig. 2 SFR (Special Function Register) memory map

RESET MODE

With the M37421M6-XXXSP, one of the two modes can be selected: the normal operation start mode which executes reset by normal operation ($f(X_{IN}) = 4.2MHz$) and the low-speed operation start mode which executes reset by low-speed operation ($f(X_{CIN}) = 3.2kHz$).

Therefore, two types of piggybacks are provided:

(1) M37421P-000SS
With this piggyback, pin ϕ is set to the internal reset signal output and the reset mode option to the normal operation start mode.

(2) M37421P-001SS
With this piggyback, pin ϕ is set to the internal reset signal output and the reset mode option to the low-speed operation start mode.

PRECAUTION FOR USE

(1) In case of the M5L27128K or the M5L27256K EPROM use the following areas (refer to Figure 1):
- For the M37421M6-XXXSP, usable ROM area are $D000_{16}$~$FFFF_{16}$.

M5L27128K ····· addresses 1000_{16}~$3FFF_{16}$
M5L27256K ····· addresses 5000_{16}~$7FFF_{16}$

(2) In case of the development of programs by the M37421P-000SS or M37421P-001SS, RAM area for the stack:
M37421M6-XXXSP ····· addresses 0100_{16}~$017F_{16}$
M37421P-000SS or
M37421P-001SS ····· addresses 0100_{16}~$023F_{16}$

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors cut-off	−0.3~7	V
V_P	Pulldown input voltage		V_{CC}−40~V_{CC}+0.3	V
V_I	Input voltage, $P2_0$~$P2_7$, $P3_0$~$P3_2$, $P3_4$~$P3_7$, CNV_{SS}, $P5_2/INT_2$, $P5_3/INT_1$		−0.3~13	V
V_I	Input voltage, $\overline{RESET}$, X_{IN}, X_{CIN}		−0.3~7	V
V_I	Input voltage, $P3_3$, $P6_0$~$P6_5$		−0.3~V_{CC}+0.3	V
V_I	Input voltage, $P5_4$~$P5_7$		−0.3~13	V
V_O	Output voltage, $P2_0$~$P2_7$, $P3_0$~$P3_2$, $P3_4$~$P3_7$		−0.3~13	V
V_O	Output voltage, $P6_0$~$P6_5$, X_{OUT}, X_{COUT}, ϕ, $P3_3$		−0.3~V_{CC}+0.3	V
V_O	Output voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P4_0$~$P4_7$, $P5_0$, $P5_1$		V_{CC}−40~V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000	mW
Topr	Operating temperature		−10~70	℃
Tstg	Storage temperature		−40~125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±5%, T_a=−10~70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_P	Pull-down supply voltage	V_{CC}−3.8		V_{CC}	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $P2_0$~$P2_7$, $P3_0$~$P3_7$, CNV_{SS}(Note 1) $P5_2/INT_2$, $P5_3/INT_1$, $P6_0$~$P6_5$	0.75V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, X_{CIN}	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P5_4$~$P5_7$	0.4V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P2_0$~$P2_7$, $P3_0$~$P3_7$, CNV_{SS}, $P5_2/INT_2$, $P5_3/INT_1$, $P6_0$~$P6_5$	0		0.25V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}, X_{CIN}	0		0.16V_{CC}	V
V_{IL}	"L" input voltage $P5_4$~$P5_7$	0		0.12V_{CC}	V
$I_{OH(sum)}$	"H" sum output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P4_0$~$P4_7$, $P5_0$, $P5_1$			−120	mA
$I_{OH(sum)}$	"H" sum output current $P6_0$~$P6_5$			−5	mA
$I_{OL(sum)}$	"L" sum output current $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P6_0$~$P6_5$			50	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$~$P0_4$			−40	mA
$I_{OH(peak)}$	"H" peak output current $P0_5$~$P0_7$, $P1_0$~$P1_7$			−30	mA
$I_{OH(peak)}$	"H" peak output current $P4_0$~$P4_7$, $P5_0$, $P5_1$			−24	mA
$I_{OH(peak)}$	"H" peak output current $P6_0$~$P6_5$			−3	mA
$I_{OL(peak)}$	"L" peak output current $P2_0$~$P2_7$, $P3_0$~$P3_7$			15	mA
$I_{OL(peak)}$	"L" peak output current $P6_0$~$P6_5$			3	mA
$I_{OH(avg)}$	"H" average output current $P0_0$~$P0_7$, $P1_0$~$P1_7$			−18	mA
$I_{OH(avg)}$	"H" average output current $P4_0$~$P4_7$, $P5_0$, $P5_1$			−12	mA
$I_{OH(avg)}$	"H" average output current $P6_0$~$P6_5$			−1.5	mA
$I_{OL(avg)}$	"L" average output current $P2_0$~$P2_7$, $P3_0$~$P3_7$			10	mA
$I_{OL(avg)}$	"L" average output current $P6_0$~$P6_5$			1.5	mA
$f_{(P3_2/CNTR)}$	Timer 3 counter clock input oscillation frequency (Note 2) $f(X_{IN})$=4.2MHz			250	kHz
	$f(X_{CIN})$=32kHz			50	
$f(X_{IN})$	Clock input oscillating frequency (Note 2, 3, 5)			4.2	MHz
$f(X_{CIN})$	Clock oscillating frequency for clock function		32.768	50	kHz

Note 1 : High-level input voltage of up to +12V may be applied to permissible for ports $P2_0$~$P2_7$, $P3_0$~$P3_2$, $P3_4$~$P3_7$, CNV_{SS}, and $P5_2$~$P5_7$

2 : Oscillation frequency is at 50% duty cycle

3 : When used in the low-speed mode, the timer clock input frequency should be $f(X_{IN}) < f(X_{IN})/3$

4 : When external clock input is used, the timer clock input frequency should be $f(X_{CIN}) \leqq 50kHz$

5 : The average output current $I_{OL(avg)}$ and $I_{OH(avg)}$ are in period of 100ms.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±5%, V_{SS} = 0V, T_a = 25℃, f(X_{IN}) = 4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max.	
V_{OH}	"H" output voltage $P6_0$~$P6_5$	I_{OH}=−0.5mA	V_{CC}−0.4			V
V_{OH}	"H" output voltage ϕ	I_{OH}=−2.5mA	V_{CC}−2			V
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$	I_{OH}=−18mA	V_{CC}−2			V
V_{OH}	"H" output voltage $P4_0$~$P4_7$, $P5_0$, $P5_1$	I_{OL}=−12mA	V_{CC}−2			V
V_{OL}	"L" output voltage $P2_0$~$P2_7$, $P3_0$~$P3_7$	I_{OL}=10mA			2	V
V_{OL}	"L" output voltage $P6_0$~$P6_5$	I_{OL}=0.5mA			0.4	V
V_{OL}	"L" output voltage ϕ	I_{OL}=2.5mA			2	V
V_{T+}−V_{T-}	Hysteresis $P5_2$/INT_2, $P5_3$/INT_1		0.3		1	V
V_{T+}−V_{T-}	Hysteresis $\overline{RESET}$			0.5	0.7	V
V_{T+}−V_{T-}	Hysteresis $P3_6$	When used as CLK input	0.3		1	V
V_{T+}−V_{T-}	Hysteresis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P2_0$~$P2_7$, $P3_0$~$P3_7$	V_I=0V			−5	μA
I_{IL}	"L" input current $P6_0$~$P6_5$	V_I=0V			−5	μA
I_{IL}	"L" input current $P5_4$~$P5_7$	V_I=0V			−5	μA
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}, X_{CIN}	V_I=0V			−5	μA
I_{IL}	"L" input current $P5_2$/INT_2, $P5_3$/INT_1	V_I=0V			−5	μA
I_{IH}	"H" input current $P2_0$~$P2_7$, $P3_0$~$P3_7$	V_I=5V			5	μA
	"H" input current $P2_0$~$P2_7$, $P3_0$~$P3_2$, $P3_4$~$P3_7$	V_I=12V			12	
I_{IH}	"H" input current $P6_0$~$P6_5$	V_I=5V			5	μA
I_{IH}	"H" input current $P5_4$~$P5_7$	V_I=5V			5	μA
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}, X_{CIN}	V_I=5V			5	μA
I_{IH}	"H" input current $P5_2$/INT_2, $P5_3$/INT_1	V_I=5V			5	μA
		V_I=12V			12	
I_{LOAD}	Output load current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P4_0$~$P4_7$, $P5_0$, $P5_1$	V_P=V_{CC}−36V, V_{OL}=V_{CC}	150	500	900	μA
I_{LEAK}	Output leak current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P4_0$~$P4_7$, $P5_0$, $P5_1$	V_P=V_{CC}−38V, V_{OL}=V_{CC}−38V			30	μA
V_{RAM}	RAM retention voltage	at clock stop	2		5.5	V
I_{CC}	Supply current	Output pins open (output OFF) V_P=V_{CC}, V_P=V_{SS} input and I/O pins all at V_{SS} X_{IN}=4MHz (system operation)		6	12	mA

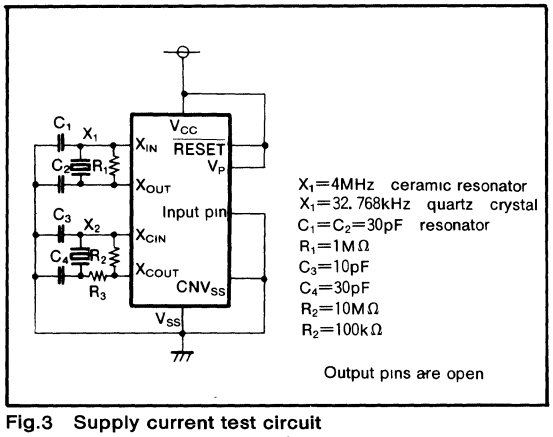

Fig.3 Supply current test circuit