M37424M8-XXXSP
M37524M4-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37424M8-XXXSP, M37524M4-XXXSP are single-chip microcomputers designed with CMOS silicon gate technology. They are housed in a 64-pin shrink plastic molded DIP.

This single-chip microcomputer is useful for business equipment and other consumer applications.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The differences between the M37424M8-XXXSP and the M37524M4-XXXSP are noted below. The following explanations apply to the M37424M8-XXXSP.

Specification variations for other chips are noted accordingly.

Type name	Port P1 output structure
M37424M8-XXXSP	CMOS
M37524M4-XXXSP	N-channel open drain

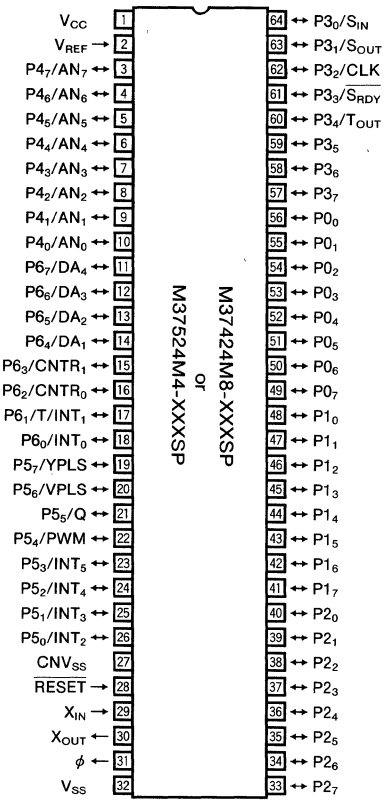
FEATURES

- Number of basic instructions 70
  68 MELPS 740 basic instructions + 2 multiply/divide instructions
- Memory size ROM ..... 16384 bytes
  RAM ..... 256 bytes
- Instruction execution time
  ..... 1 μs (minimum instructions, at 4MHz frequency)
- Single power supply ..... 5V $\pm$ 10%
- Power dissipation
  normal operation mode (at 4MHz frequency) 30mW
- Subroutine nesting ..... 96 levels (Max.)
- Interrupt ..... 16 types, 16 vectors
- 8-bit timer 4
- 16-bit timer 1
- Serial I/O (8-bit or 16-bit) 1
- PWM output (14-bit) 1
- A-D converter (8-bit resolution) 8-channel
- D-A converter (5-bit resolution) 2
- D-A converter (8-bit resolution) 2
- Watchdog timer
- External trigger output (1-bit) 1
- V pulse Y pulse generator
- Programmable I/O ports
  (Ports P0, P1, P2, P3, P4, P5, P6) 56

APPLICATION

Office automation equipment
VCR equipment

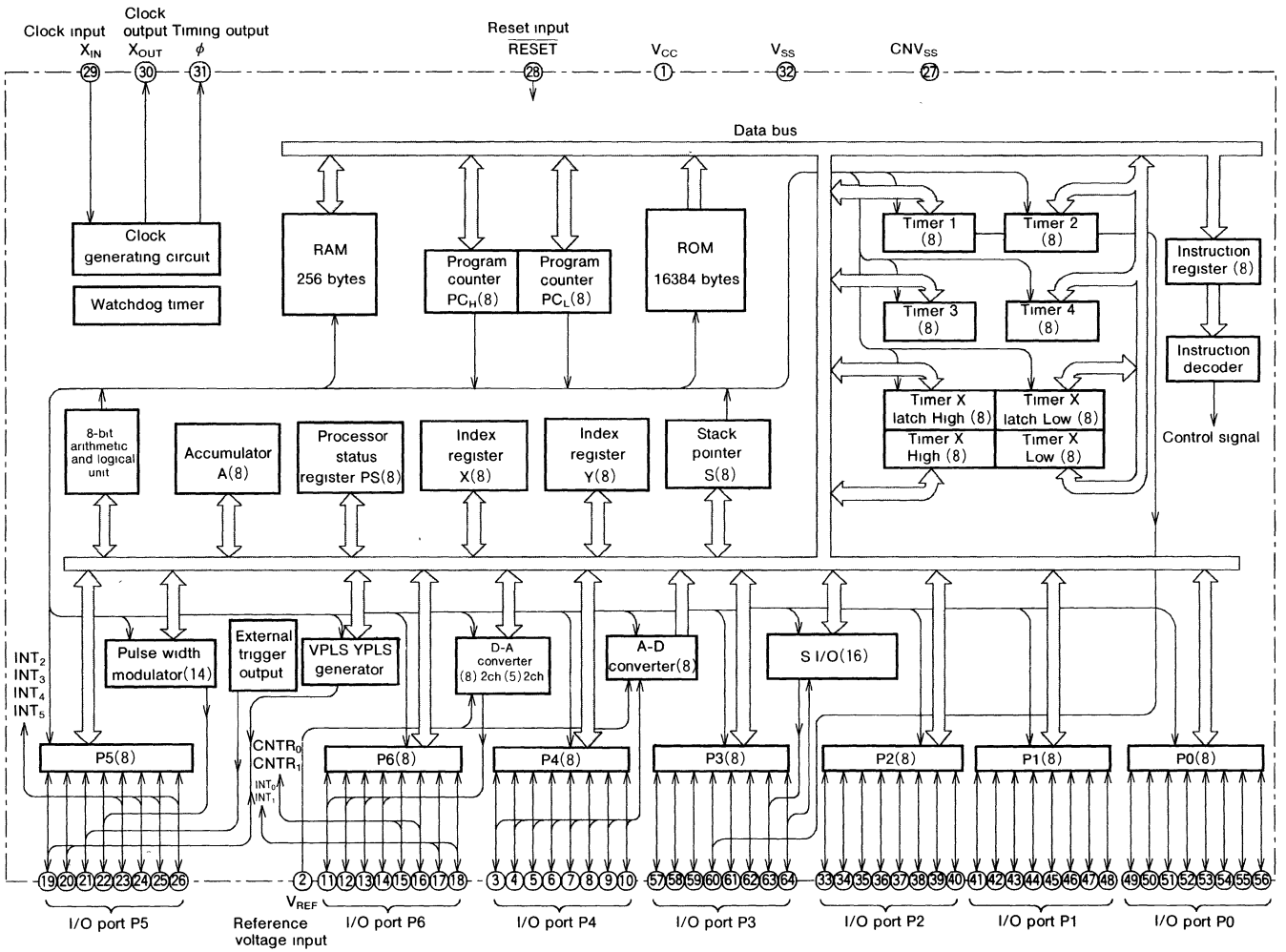
PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

MITSUBISHI ELECTRIC

M37424M8-XXXSP BLOCK DIAGRAM



FUNCTIONS OF M37424M8-XXXSP

Parameter			Functions
Number of basic instructions			70 (68 MELPS 740 basic instructions+2)
Instruction execution time			1μs (minimum instructions, at 4MHz frequency)
Clock frequency			4MHz
Memory size	ROM		16384 bytes
	RAM		256 bytes
Input/Output ports	P0, P1, P2, P3, P4, P5, P6	I/O	8-bit×7
Serial I/O			8-bit or 16-bit×1
Timers			8-bit×4, 16-bit×1
A-D conversion			8-bit×1 (8 channels)
D-A conversion			5-bit×2, 8-bit×2
Pulse width modulator			14-bit×1
Watchdog timer			15-bit×1
Subroutine nesting			96 levels (max.)
Interrupt			16 (external 8, internal 8)
Clock generating circuit			Built-in (ceramic or quartz crystal oscillator)
Supply voltage			5V±10%
Power dissipation			30mW (at 4MHz frequency)
Operating temperature range			−10~70°C
Device structure			CMOS silicon gate
Package			64-pin shrink plastic molded DIP

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}
CNV_{SS}	CNV_{SS}		This is usually connected to V_{SS}
V_{REF}	Reference voltage input	Input	Reference voltage input pin for A-D and D-A converter
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 4μs (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin
$P0_0$~$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional register allowing each I/O bit to be individually programmed as input or output At reset, this port is set to input mode The output structure is CMOS output
$P1_0$~$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0 The output structure of M37424M8-XXXSP is CMOS output and that of M37524M4-XXXSP is N-channel open drain output
$P2_0$~$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0 The output structure is CMOS output
$P3_0$~$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0 When serial I/O is used, $P3_3$, $P3_2$, $P3_1$, and $P3_0$ work as $\overline{S_{RDY}}$, CLK, S_{OUT}, and S_{IN} pins, respectively Also $P3_4$ works as T_{OUT} pin The output structure is N-channel open drain
$P4_0$~$P4_7$	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0 $P4_0$~$P4_7$ work as analog input port AN_0~AN_7
$P5_0$~$P5_7$	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same functions as port P0 $P5_7$, $P5_6$, $P5_5$, $P5_4$ and $P5_3$~$P5_0$ are in common with the YPLS output, VPLS output, Q output, PWM output and interrupt input respectively
$P6_0$~$P6_7$	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same functions as port P0 $P6_7$~$P6_4$, $P6_3$, $P6_2$, and $P6_1$, $P6_0$ are in common with the D-A output, CNTR output and interrupt input respectively

FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

The M37424, M37524 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions can be used.

The WIT instruction can be used.

The STP instruction are not provided.

CPU MODE REGISTER

The CPU mode register is allocated to address $00FB_{16}$. This register has a stack page selection bit.

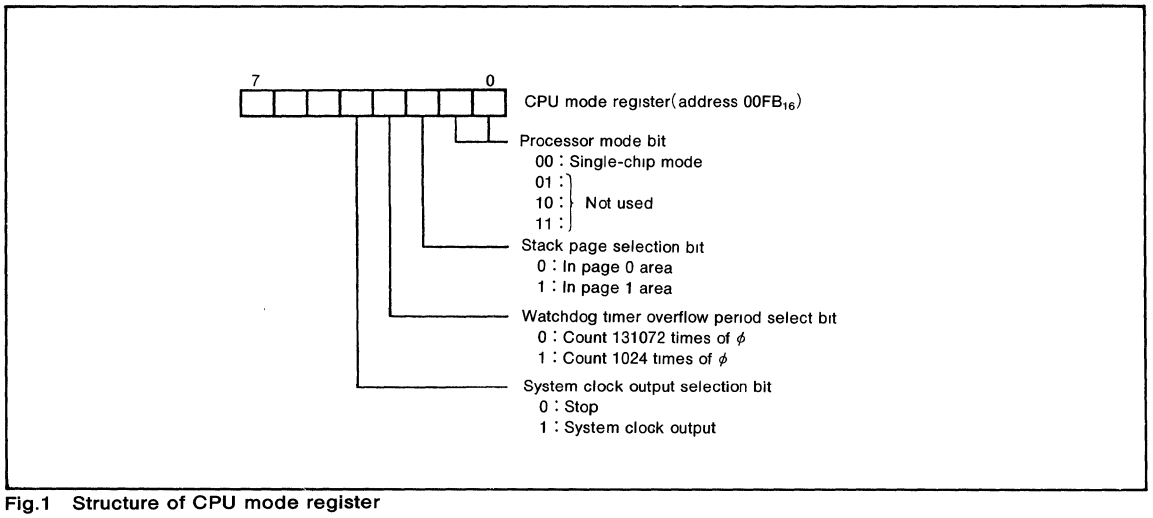


Fig.1 Structure of CPU mode register

MEMORY

- Special Function Register (SFR) Area
  The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.
- RAM
  RAM is used for data storage as well as a stack area.
- ROM
  ROM is used for storing user programs as well as the interrupt vector area.
- Interrupt Vector Area
  The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.
- Zero Page
  Zero page addressing mode is useful because it enables access to this area with fewer instruction cycles.
- Special Page
  Special page addressing mode is useful because it enables access to this area with fewer instruction cycles.

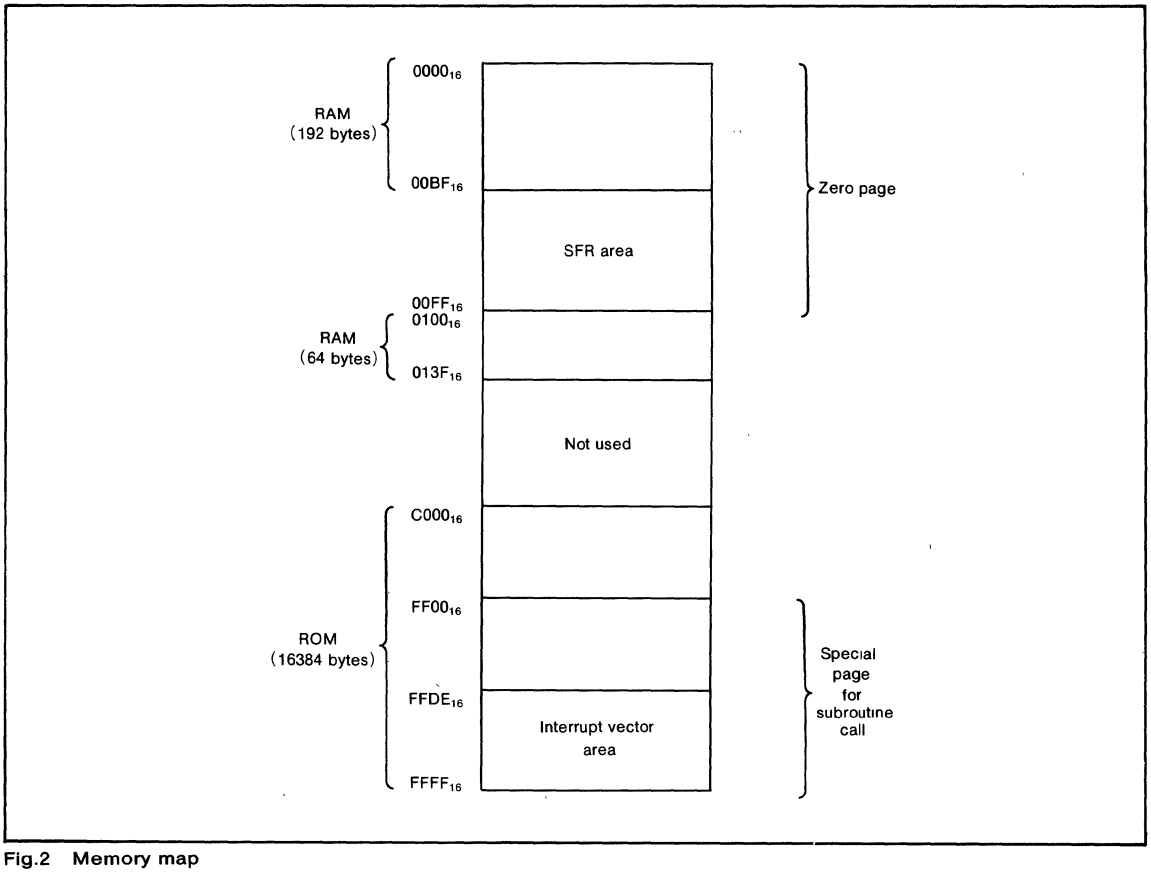


Fig.2 Memory map

$00C0_{16}$	Port P0
$00C1_{16}$	Port P0 directional register
$00C2_{16}$	Port P1
$00C3_{16}$	Port P1 directional register
$00C4_{16}$	Port P2
$00C5_{16}$	Port P2 directional register
$00C6_{16}$	Port P3
$00C7_{16}$	Port P3 directional register
$00C8_{16}$	Port P4
$00C9_{16}$	Port P4 directional register
$00CA_{16}$	Port P5
$00CB_{16}$	Port P5 directional register
$00CC_{16}$	Port P6
$00CD_{16}$	Port P6 directional register
$00CE_{16}$ to $00D0_{16}$	Reserved area
$00D1_{16}$	D-A output enable register
$00D2_{16}$	D-A3 conversion register
$00D3_{16}$	D-A4 conversion register
$00D4_{16}$	Pulse width modulation register H
$00D5_{16}$	Pulse width modulation register L
$00D6_{16}$	V pulse preset value P
$00D7_{16}$	V pulse preset value N
$00D8_{16}$	V pulse control register
$00D9_{16}$	A-D successive approximation register
$00DA_{16}$	A-D control register
$00DB_{16}$	D-A1 conversion register
$00DC_{16}$	D-A2 conversion register
$00DD_{16}$	Serial I/O mode register
$00DE_{16}$	Serial I/O register L
$00DF_{16}$	Serial I/O register H

$00E0_{16}$ to $00EC_{16}$	Reserved area
$00ED_{16}$	Interrupt polarity specification register
$00EE_{16}$	Special function selection register
$00EF_{16}$	Watchdog timer
$00F0_{16}$	Timer 1
$00F1_{16}$	Timer 2
$00F2_{16}$	Timer 3
$00F3_{16}$	Timer 4
$00F4_{16}$	Timer X (low-order)
$00F5_{16}$	Timer X (high-order)
$00F6_{16}$	Timer X latch (low-order)
$00F7_{16}$	Timer X latch (high-order)
$00F8_{16}$	Timer 1, 2 mode register
$00F9_{16}$	Timer 3, 4 mode register
$00FA_{16}$	Timer X mode register
$00FB_{16}$	CPU mode register
$00FC_{16}$	Interrupt request register 1
$00FD_{16}$	Interrupt request register 2
$00FE_{16}$	Interrupt control register 1
$00FF_{16}$	Interrupt control register 2

Fig. 3 SFR (Special Function Register) memory map

INTERRUPTS

Interrupts can be caused by 16 different events. Interrupts are vectored interrupts with prioities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed, interrupt inhibit flag I is set, and the program jumps to the address specified in the vector table. The interrupt request flag is cleared automatically. The reset and BRK instruction interrupt can never be inhibited. Other interrupt are disabled when the interrupt inhibit flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figure 5 shows the structure of the interrupt request registers 1 and 2, interrupt control registers 1 and 2 and interrupt polarity specification register.

For external interrupts (INT_0 to INT_5, $CNTR_0$, and $CNTR_1$), the polarity of each pin's interrupt input can be set. Polarity for INT_0 to INT_5 and $CNTR_1$ is set by bits 0 to 6 of the interrupt polarity specification register (address $00ED_{16}$); polarity for $CNTR_0$ is set by bit 6 of the timer X mode register (address $00FA_{16}$). If "0" is written to one of these bits, the corresponding interrupt request is falling-edge active; if "1" is written, the corresponding interrupt request is rising-edge active. INT_1 can also be set to be both rising-edge and falling-edge active by setting bit 7 of the interrupt polarity specification register to "1". The meaning of the $CNTR_0$ interrupt is different if it is used with timer X in pulse width measurement mode 1, pulse width measurement mode 2, or pulse period measurement mode. For details, see the section on timer X

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt inhibit flag is "0". The interrupt request bit can be reset with a program, but not set. The interrupt enable bit can be set and reset with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 4 shows interrupts control.

Table 1. Interrupt vector address and priority

Event	Priority	Vector addresses	Remarks
$\overline{RESET}$	1	$FFFF_{16}$, $FFFE_{16}$	Non-maskable
INT_0 interrupt	2	$FFFD_{16}$, $FFFC_{16}$	External interrupt (phase programmable)
INT_1 interrupt	3	$FFFB_{16}$, $FFFA_{16}$	External interrupt (phase programmable)
INT_2 interrupt	4	$FFF9_{16}$, $FFF8_{16}$	External interrupt (phase programmable)
Timer 4 interrupt	5	$FFF7_{16}$, $FFF6_{16}$	
Timer 1 interrupt	6	$FFF5_{16}$, $FFF4_{16}$	
INT_3 interrupt	7	$FFF3_{16}$, $FFF2_{16}$	External interrupt (phase programmable)
$CNTR_1$ interrupt	8	$FFF1_{16}$, $FFF0_{16}$	External interrupt (phase programmable)
INT_4 interrupt	9	$FFEF_{16}$, $FFEE_{16}$	External interrupt (phase programmable)
Timer X interrupt	10	$FFED_{16}$, $FFEC_{16}$	
$CNTR_0$ interrupt	11	$FFEB_{16}$, $FFEA_{16}$	External interrupt (phase programmable)
Timer 2 interrupt	12	$FFE9_{16}$, $FFE8_{16}$	
Timer 3 interrupt	13	$FFE7_{16}$, $FFE6_{16}$	
Serial I/O interrupt	14	$FFE5_{16}$, $FFE4_{16}$	
INT_5 interrupt	15	$FFE3_{16}$, $FFE2_{16}$	External interrupt (phase programmable)
A-D conversion completion interrupt	16	$FFE1_{16}$, $FFE0_{16}$	
BRK instruction interrupt	17	$FFDF_{16}$, $FFDE_{16}$	Non-maskable software interrupt

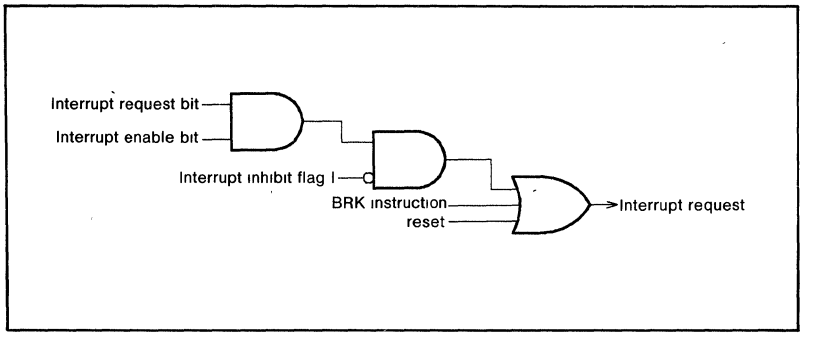


Fig.4 Interrupt control

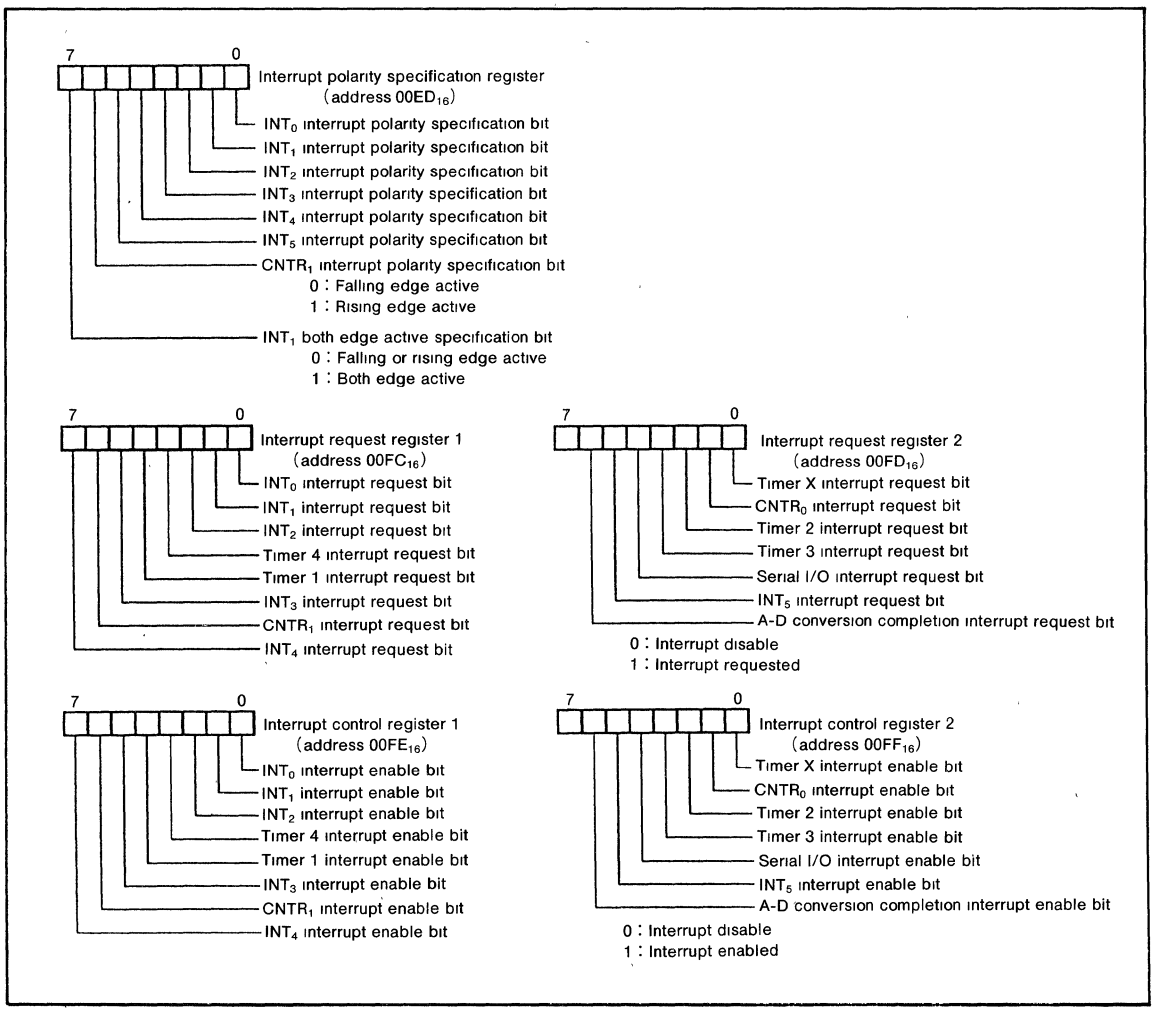


Fig.5 Structure of registers related to interrupt

TIMERS

The M37424M8-XXXSP has five timers : timer X, timer 1, timer 2, timer 3, and timer 4. A block diagram of these timers is shown in Figure 9.

Timer X is a 16-bit timer. It has an independent 16-bit timer latch and can be used in eight modes. The structure of the timer X mode register is shown in Figure 8, and the eight timer X modes are described below.

(1) 16-bit timer mode [000]

Basic mode in which timer X functions as a 16-bit reload timer and timer X generates an interrupt request when it overflows.

The count source is selected by bit 4 of the timer X mode register : if this bit is "0", the count source is the oscillation frequency divided by 2 ; if it is "1", the count source is the oscillation frequency divided by 16. This bit is "0" immediately after a reset.

The timer counts down the value which decrements by one from the value set in the latch. At the next count pulse after it reaches $FFFF_{16}$ from 0000_{16}, an timer X interrupt is generated, and at the same time the value in the timer latch is reloaded into the timer The value is not reloaded into the timer until it overflows, even if the contents of the timer latch are overwritten.

When writing to the timer directly, write the upper value first, then the lower value. The upper value is overwritten at the same time that the lower value is written. When reading the timer, read the lower value first, then the upper value. At the point at which the lower value is read, the upper value is latched. If reading the lower value always read the upper value as well. There are no restrictions on which part of the timer latch should be written to or read first.

(2) Event counter mode [001]

Mode in which timer X operates in exactly the same way as in timer mode, except that the count source is the external pulse input from the $CNTR_0$ pin The input polarity of the $CNTR_0$ pin can be selected by bit 6 of the timer X mode register : if this bit is "0", falling edges are counted ; if it is "1", rising edges are counted.

(3) Pulse width measurement mode 1 [010]

Mode in which timer X measures the width of "H" or "L" period of the external pulse input from the $CNTR_0$ pin.

The count source is selected by bit 4 of the timer X mode register : if this bit is "0", the count source is the oscillation frequency divided by 2 ; if it is "1", the count source is the oscillation frequency divided by 16. In this mode the timer counts up · at the same time that the measurement ends, the value in the timer is latched into the timer latch and a $CNTR_0$ interrupt request is generated.

Bit 6 of the timer X mode register selects whether the "H" period is measured or the "L" period. If this bit is "0", the "L" period is measured ; if it is "1", the "H" period is measured.

(4) Pulse width measurement mode 2 [011]

Mode in which timer X continuously measures the width of both "H" and "L" periods of the external pulse input from the $CNTR_0$ pin.

The count source is selected by bit 4 of the timer X mode register : if this bit is "0", the count source is the oscillation frequency divided by 2 ; if it is "1", the count source is the oscillation frequency divided by 16. The value in the timer is latched at both the rising edges and falling edges of the external pulse, and a $CNTR_0$ interrupt request is generated. Whether the measured value is the "H" period or the "L" period can be determined by checking the level of the $P6_2$/$CNTR_0$ pin. This mode can be used to measure the duty cycle of external pulses.

(5) Pulse period measurement mode [100]

Mode in which timer X measures the period of the external pulse input from the $CNTR_0$ pin.

The count source is selected by bit 4 of the timer X mode register : if this bit is "0", the count source is the oscillation frequency divided by 2 ; if it is "1", the count source is the oscillation frequency divided by 16. If bit 6 of the timer X mode register is "0", the period from one falling edge to the next falling edge is measured ; if it is "1", the period from one rising edge to the next rising edge is measured. The measured value is latched in the timer latch, and a $CNTR_0$ interrupt request is generated.

(6) Pulse output mode [101]

Mode in which an waveform of duty cycle 50% which is inverted every time timer X overflows is output to the $CNTR_0$ pin.

The count source is selected by bit 4 of the timer X mode register : if this bit is "0", the count source is the oscillation frequency divided by 2 ; if it is "1", the count source is the oscillation frequency divided by 16.

(7) Programmable waveform generation mode [110]

Mode in which the contents of the output level latch allocated to bit 5 of the timer X mode register are output to the $CNTR_0$ pin every time timer X overflows.

The count source is selected by bit 4 of the timer X mode register : if this bit is "0", the count source is the oscillation frequency divided by 2 ; if it is "1", the count source is the oscillation frequency divided by 16. Various different waveforms can be generated by updating the values in the output level latch, the timer and the timer latch, each time timer X overflows.

(8) Programmable one-shot generation mode [111]

Mode in which the active edge of an external pulse input from the $P6_0/INT_0$ pin sets the value of the timer latch into timer X, and timer X starts to count. The $CNTR_0$ pin goes "H" at the same time of the active edge of the INT_0 pin input, and goes "L" when timer X overflows.

The count source is selected by bit 4 of the timer X mode register : if this bit is "0", the count source is the oscillation frequency divided by 2 ; if it is "1", the count source is the oscillation frequency divided by 16. The active edge of the INT_0 pin is set by bit 0 of the interrupt polarity specification register, and is the same as the polarity of the INT_0 interrupt.

Note that if the $CNTR_0$ pin is used as a pulse output pin (in pulse output mode, programmable waveform generation mode, or programmable one-shot generation mode), bit 7 of the timer X mode register must be "1". If this bit switches from "0" to "1", an "L"-level signal will be output to the $CNTR_0$ pin. However, be aware that if timer X is switched to another pulse output mode while this bit is "1", the level output in the previous mode will still be held by the $CNTR_0$ pin.

Timer 1, timer 2, timer 3, and timer 4 are all 8-bit timers with 8-bit timer latches. Writing to a timer latch sets the corresponding timer at the same time, except that, if the value written to the latch is n, the value actually set in the timer is $(n-1)$. The timer has a count-down operation : at the next count pulse after it reaches FF_{16} from 00_{16}, the value in the timer latch is reloaded into the timer. If the value in the timer latch is n, the divide ratio is $1/(n+1)$. At the same time, the interrupt request bit corresponding to that timer is set to "1". Set the count source for each timer by the timer 1, 2 mode register (address $00F8_{16}$) or the timer 3, 4 mode register (address $00F9_{16}$).

If an external clock is selected as the count source for timer 2, timer counts the $P6_3/CNTR_1$ pin input. An inverting waveform every time timer 2 overflows can be output to the $P3_4/T_{OUT}$ pin, by setting bit 7 of the timer 1, 2 mode register to "1". The structure of the timer 1, 2 mode register is shown in Figure 6 and the structure of the timer 3, 4 mode register is shown in Figure 7

At reset, timer 3 is set to FF_{16} and timer 4 is set to 07_{16}.

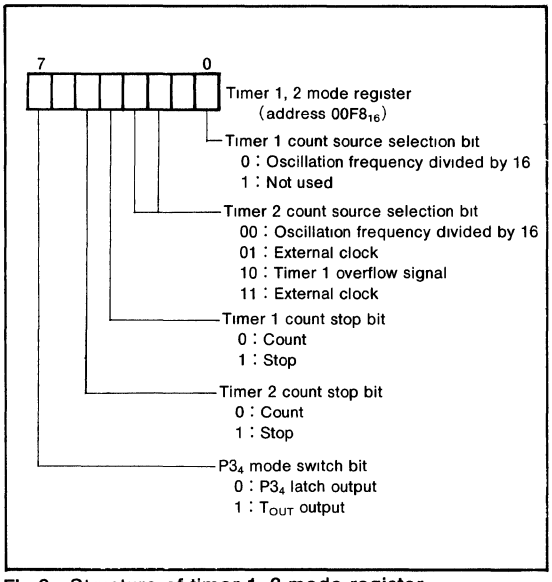


Fig.6 Structure of timer 1, 2 mode register

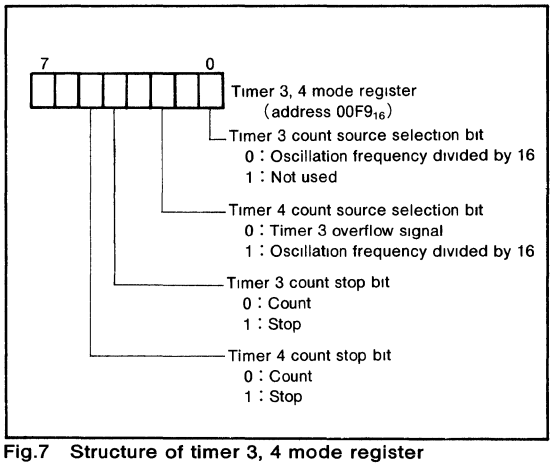


Fig.7 Structure of timer 3, 4 mode register

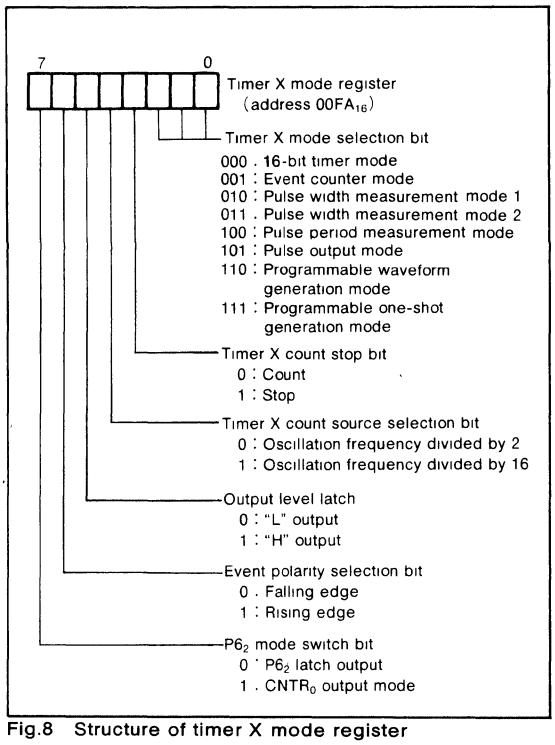


Fig.8 Structure of timer X mode register

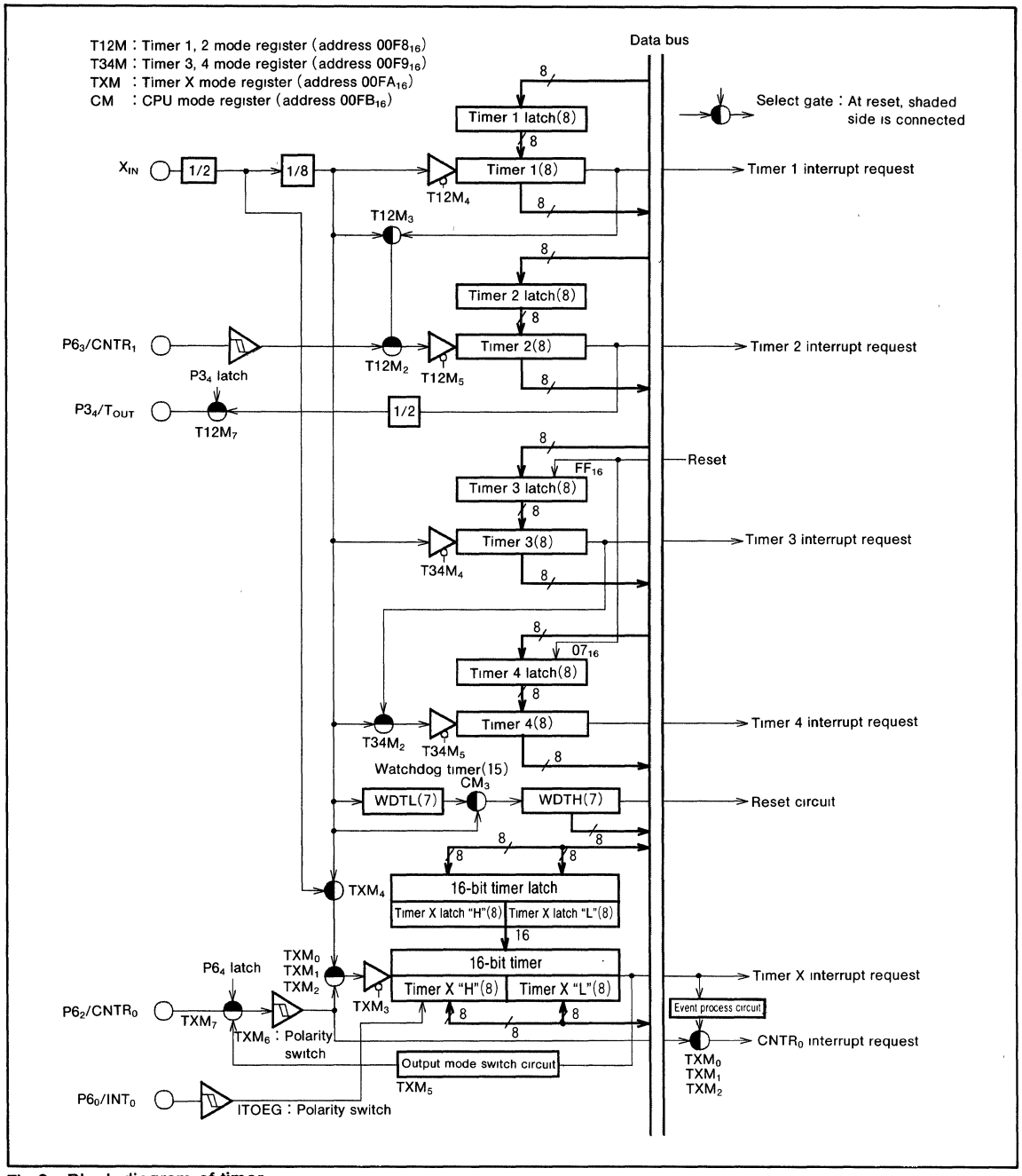


Fig.9 Block diagram of timer

SERIAL I/O

A block diagram of the serial I/O function is shown in Figure 11. The serial I/O receive enabled signal pin ($\overline{S_{RDY}}$), synchronous clock I/O pin (CLK), and data I/O pins (S_{OUT}, S_{IN}) also function as the $P3_3$, $P3_2$, $P3_1$, and $P3_0$ of the port P3.

The serial I/O mode register has an 8-bit structure. Bits 1 and 0 select the synchronous clock : the oscillation frequency is divided by 8 if they are [00], by 16 if they are [01], by 128 if they are [10], or by 512 if they are [11]. Bit 2 selects an external clock.

Bits 3 and 4 are used to select whether part of port P3 is used for serial I/O. If bit 3 is "1", the $P3_2$ is the I/O pin for the synchronous clock .

The $P3_1$ is the serial data output pin and the $P3_0$ is the serial data input pin. If using the $P3_0$ as the serial data input pin, set the bit in the directional register corresponding to $P3_0$ to "0" to set input mode. If serial I/O is being used, bit 3 must be set to "1". When bit 3 is "0", the $P3_2$ functions as an ordinary I/O pin.

Bit 4 selects whether the $P3_3$ is used as the output pin for the receive enabled signal $\overline{S_{RDY}}$. If this bit is "1", the $\overline{S_{RDY}}$ signal is output ; if it is "0", the $P3_3$ is an ordinary I/O pin.

Serial I/O register H and serial I/O register L are 8-bit registers for data transfer that can be used in both transmission and reception. For 8-bit transfer, serial I/O register L

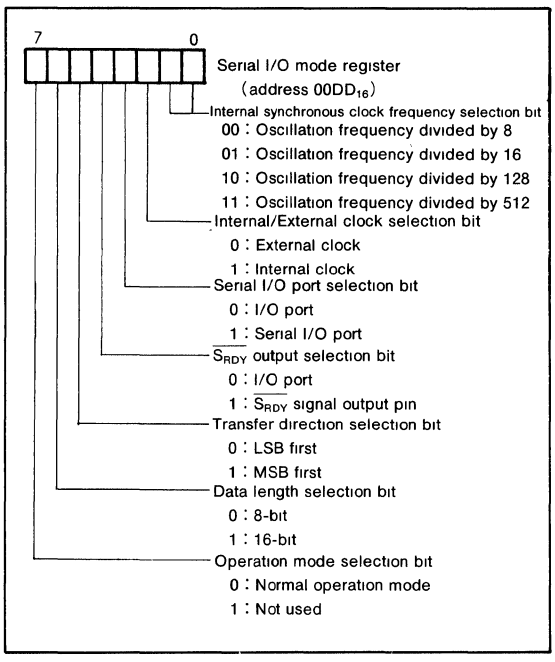


Fig.10 Structure of serial I/O mode register

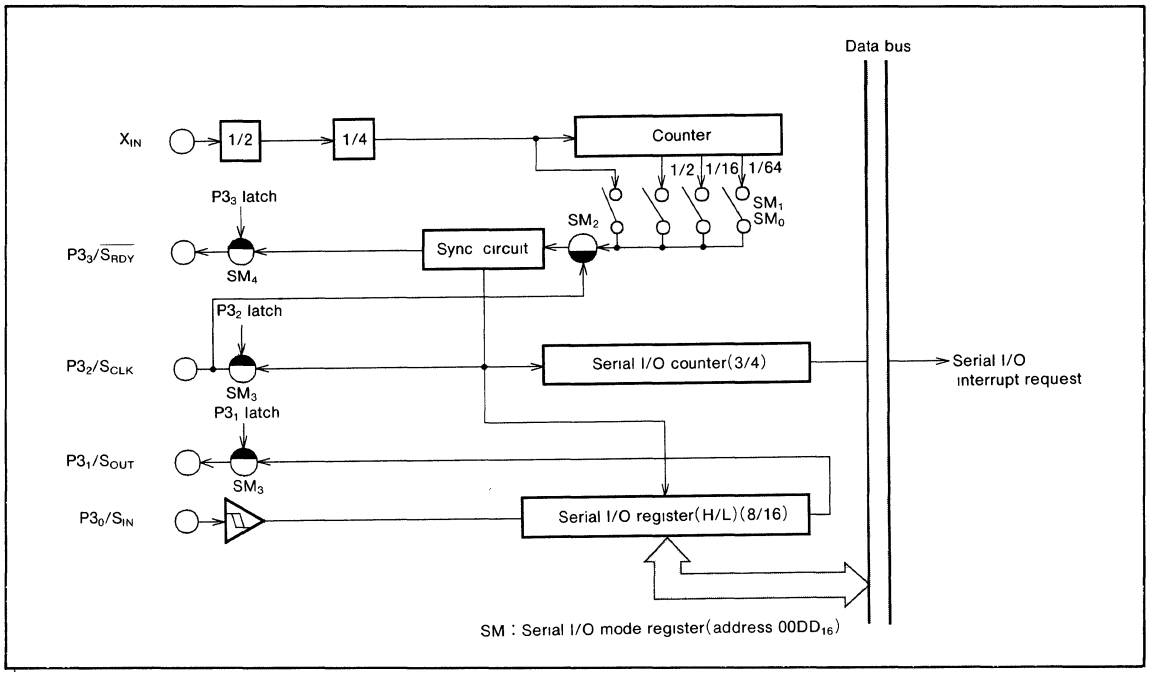


Fig.11 Block diagram of serial I/O

(address $00DE_{16}$) is used ; for 16-bit transfer, serial I/O register H (address $00DF_{16}$) is used for the upper byte and serial I/O register L for the lower byte. The data length to be transferred can be selected either 8 bits or 16 bits by setting bit 6 of the serial I/O mode register. Whether data transfer is MSB first or LSB first can be selected by setting bit 5 of the serial I/O mode register.

The operation of the serial I/O function will now be described. The operation differs depending on whether the internal clock or an external clock is selected as the synchronous clock. Use with the internal clock will be described first.

If the serial I/O register L is written to, the $\overline{S_{RDY}}$ signal is at "H" during the write cycle ; it then goes "L" when the write cycle ends to indicate reception enabled status. If the serial I/O register's transfer clock goes "L" even once, the $\overline{S_{RDY}}$ signal goes "H". During the write cycle to the serial I/O register, "7" is set in the serial I/O counter for 8-bit transfer or "15" for 16-bit transfer, and the serial I/O register's transfer clock is forced to "H". After the write cycle ends, data is output to the $P3_1$ pin each time the transfer clock goes from "H" to "L". Data is input from the $P3_0$ pin each time the transfer clock goes from "L" to "H" and, at the same time, the contents of the serial I/O register are shifted one bit. If bit 5 of the serial I/O mode register is "0", the data enters from the MSB and shifts to the right , if it is "1", the data enters from the LSB and shifts to the left.

When the serial I/O counter reaches "0" after counting either 8 or 16 transfer clocks, the transfer clock stops at "H" and the corresponding interrupt request bit is set.

If an external clock is selected as the synchronous clock, it must be controlled externally because, although the interrupt request bit is set, the transfer clock does not stop. Use a clock of no more that 500kHz with a duty cycle of 50% as the external clock.

The timing at which 8-bit data is transferred LSB-first is shown in Figure 12. If an external clock is used for the transfer, the external clock must be "H" when the serial I/O counter is initialized. Make sure that the serial I/O counter is initialized after the transfer clock switches. Initialize by writing to the serial I/O register H.

A connection example for transferring data from one M37424M8-XXXSP to another is shown in Figure 13.

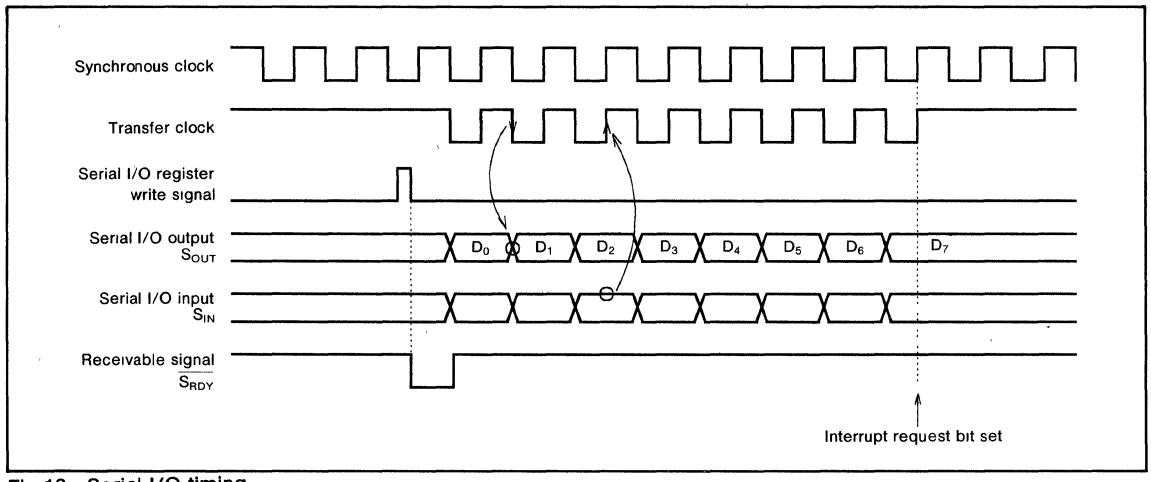


Fig.12 Serial I/O timing

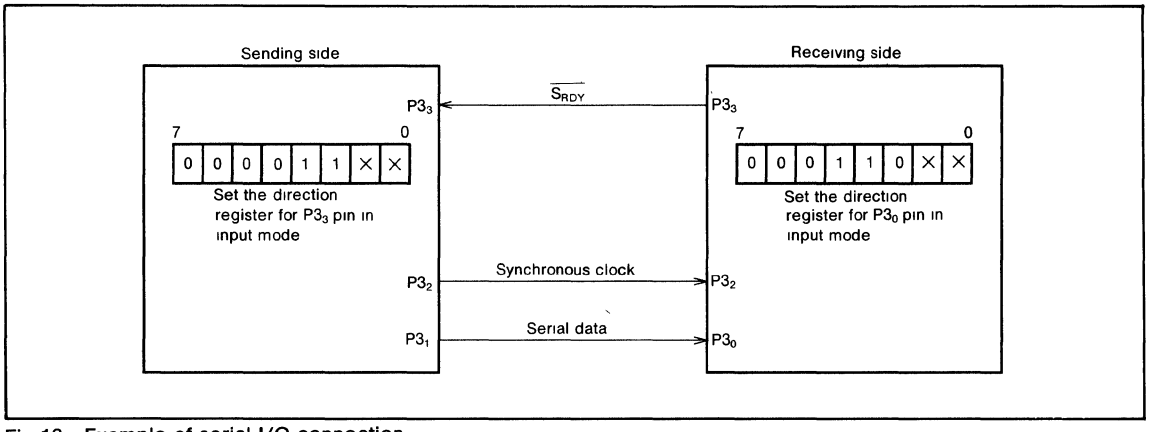


Fig.13 Example of serial I/O connection

PWM OUTPUT CIRCUIT

The M37424M8-XXXSP has a PWM function with a 14-bit resolution, a repeat period of 8192μs when the oscillation frequency X_{IN} is 4MHz (the explanation in the rest is based on the assumption that X_{IN}=4MHz), and a minimum bit resolution width of 500ns. If data is set in the lower 6 bits of the pulse width modulation register L (PWM-L : address $00D5_{16}$) and the pulse width modulation register H (PWM-H : address $00D4_{16}$), and the port $P5_4$ function selection bit (bit 0 of the special function selection register) is set to "1", a PWM waveform is output from port $P5_4$.

The period of 8192μs is resolved into 16,384 minimum pulse widths (500ns), and the pulse width can be modulated in 500ns units in accordance with the 14 bits of data written into PWM-H and PWM-L. By dividing the 8192μs repeat period into 64 short-area periods, pulses of approximately equal width can be output at a 128μs period. A block diagram of the PWM circuit is shown in Figure 14.

The data written to the PWM register is transferred to the PWM latch at the repetition of the PWM period. The signals output to the PWM pin correspond to the contents of this latch. When data of PWM-L register is read, data in this latch has already been read allowing the data output by the PWM to be confirmed. In this case, the upper 2 bits of the 8-bit register becomes undefined. However, bit 7 of the PWM-L register indicated the completion of the data transfer from the PWM-L register to the PWM latch. If bit 7 is "0", the transfer has been completed, if bit 7 is "1", the transfer has not yet begun.

The timing diagram of the 14-bit PWM is shown in Figure 15. The 14-bit PWM divides the data within the PWM latch into the lower 6 bits and higher 8 bits.

A high-level area with a length N times τ is output every short area of t=256$\times\tau$=128μs as determined by data N of the higher 8 bits. (Refer to PWM output ② in the lower part of Figure 15.)

The contents of the lower 6 bits of data enable the lengthening of the high signal by τ.

Thus, the time for the high-level area is equal to the time set by the higher 8 bits or that plus τ. As a result, the short-area period t(=128μs, approx. 7.8kHz) becomes an approximately repetitive period.

At reset the output of port $P5_4$ is in the high impedance state and the contents of the PWM register and latch are undefined. Note that after setting the PWM register, its data is transferred to the latch.

Table 2. Relation between the 6 lower-order bits of data and the space set by the ADD bit

6 lower-order bits of data (LSB)	Area longer by τ than that of other t_m ($m = 0 \sim 63$)
0 0 0 0 0 0	Nothing
0 0 0 0 0 1	m=32
0 0 0 0 1 0	m=16, 48
0 0 0 1 0 0	m=8, 24, 40, 56
0 0 1 0 0 0	m=4, 12, 20, 28, 36, 44, 52, 60
0 1 0 0 0 0	m=2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62
1 0 0 0 0 0	m=1, 3, 5, 7, ····· ·····57, 59, 61, 63

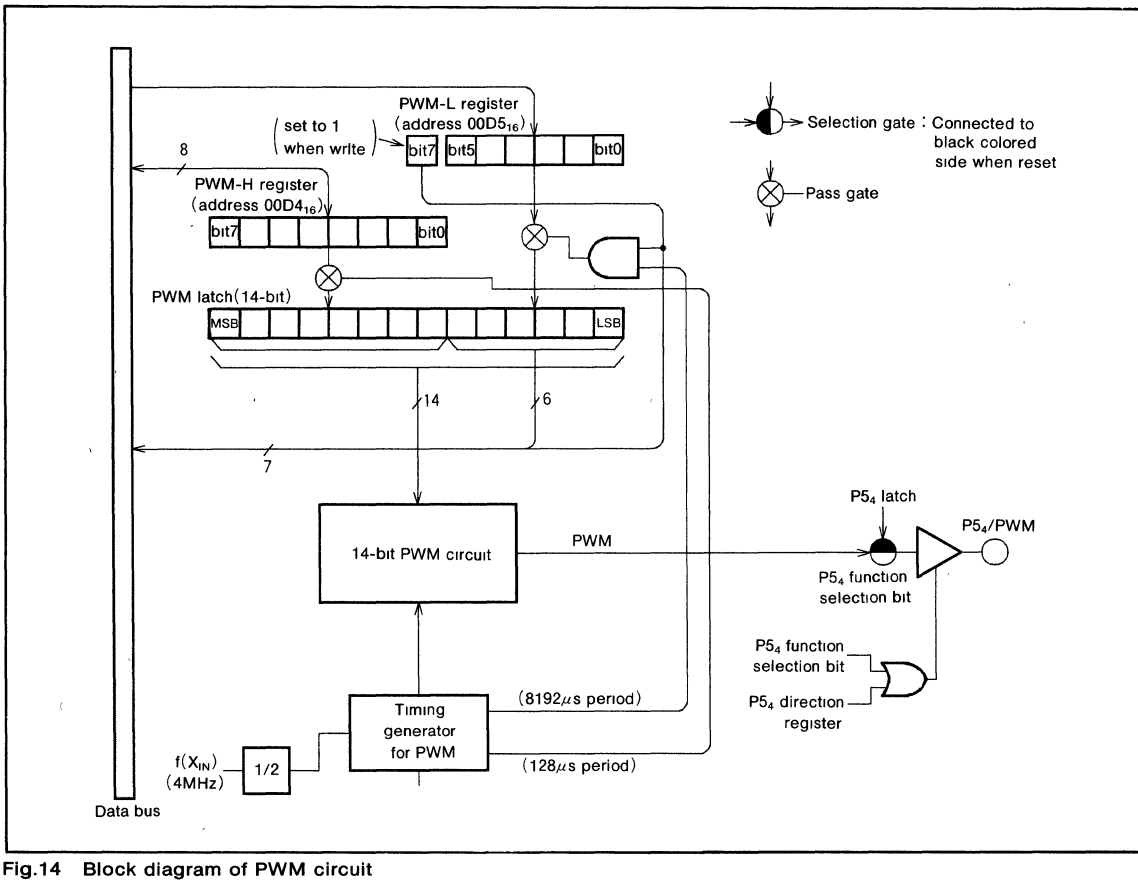


Fig.14 Block diagram of PWM circuit

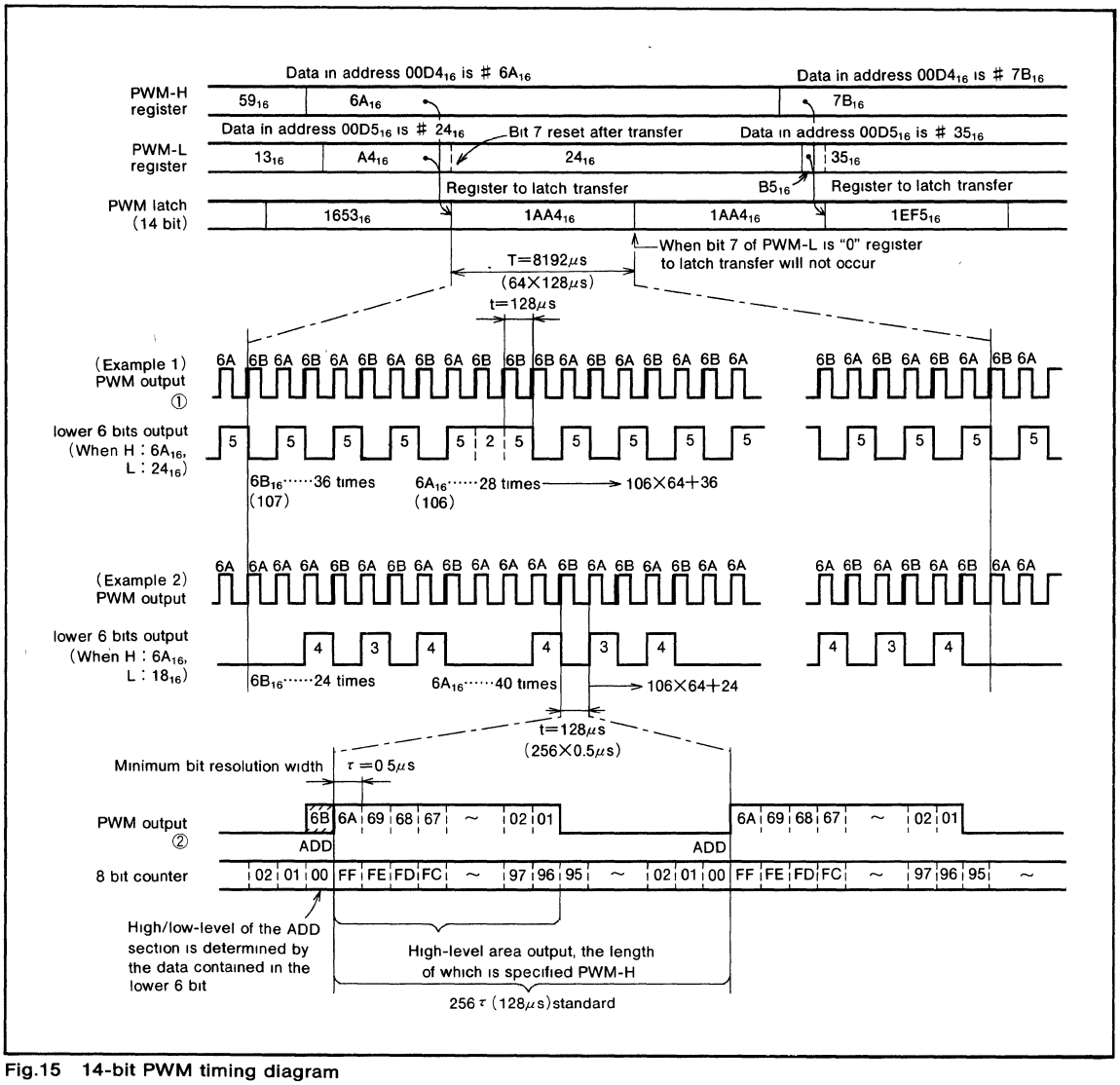


Fig.15 14-bit PWM timing diagram

A-D CONVERTER

An 8-bit successive approximation method of A-D conversion is employed providing a precision of ±3LSB. A block diagram of the A-D converter is shown in Figure 16. Conversion is automatic once it is started with the program.

The analog inputs are used in common with port P4. Bits 2, 1 and 0 of the A-D control register (address $00DA_{16}$) are used to select which pins are used for A-D conversion. The input condition is accomplished by setting to "0" the bit in the directional register that corresponds to the pin where A-D conversion is to take place. Bit 3 of the A-D control register is the A-D conversion end bit. During A-D conversion, this bit is "0", and upon completion becomes "1". Thus, it can be ascertained whether A-D conversion has been completed or not by inspecting this bit. The relation between the contents of the A-D control register and the selection of input pins are shown in Figure 17.

The results of the conversion can be found be reading the contents of the successive approximation register address $00D9_{16}$ which stores the results of the conversion.

The procedure for executing A-D conversion is next explained. Firstly, the pin that is to be used for the A-D conversion is selected by setting bit 2, bit 1 and bit 0 of the A-D control register.

Next, clear the A-D conversion end bit to "0".

When the above is done, A-D conversion is started. A-D conversion completes after 49 clock cycles upon which the A-D conversion end bit is set to "1" and the results of the conversion can be found in the successive approximation register. Since the comparator consists of the capacitive coupled configuration, $f(X_{IN})$ is needed larger than 1MHz during A-D conversion.

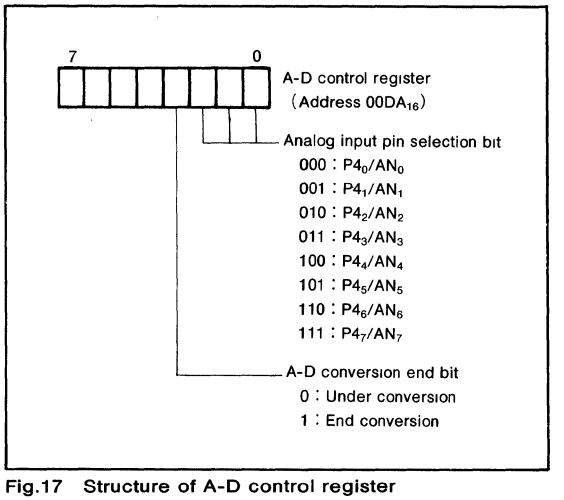


Fig.17 Structure of A-D control register

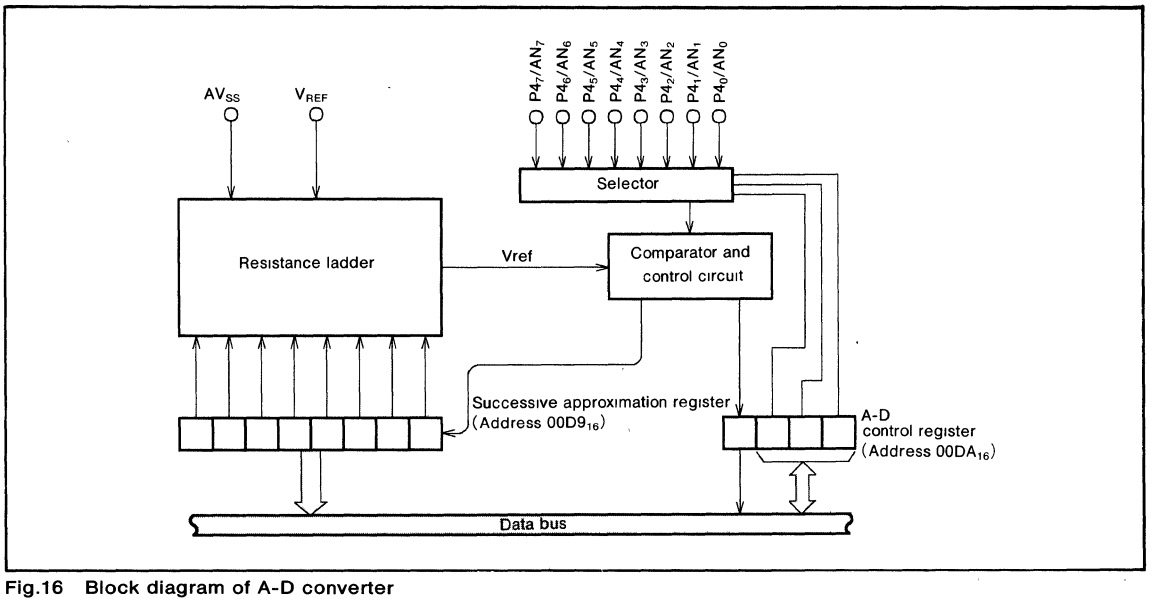


Fig.16 Block diagram of A-D converter

D-A CONVERTER

The M37424M8-XXXSP has two 8-bit resolution, R-2R method D-A converters and two 5-bit resolution D-A converters. A block diagram of the D-A converters is shown in Figure 19.

If a value is written into one of the D-A conversion registers corresponding to these D-A converters, an analog voltage equivalent to that digital value is generated by the ladder resistors. If the corresponding D-A output enable bit (bit 0 to bit 3 of the D-A output enable register) is set to "1", that value is output to the corresponding output pin $P6_4/DA_1$ to $P6_7/DA_4$. In this case, the directional register of that pin must be set to "0" to set input mode.

The relationship between analog voltage and digital value is as follows :

$V=V_{REF}\times n/256$(n=0 to 255) : DA_1 and DA_2
$V=V_{REF}\times n/32$(n=0 to 31) : DA_3 and DA_4

Where V is the output voltage, V_{REF} is the reference voltage, and n is the value in the D-A conversion register.

At reset, the $P6_4/DA_1$ to $P6_7/DA_4$ pins go to high impedance. D-A output does not have a built-in buffer, so if connecting a low-impedance load, connect an external buffer as well.

The structure of the D-A output enable register is shown in Figure. 18.

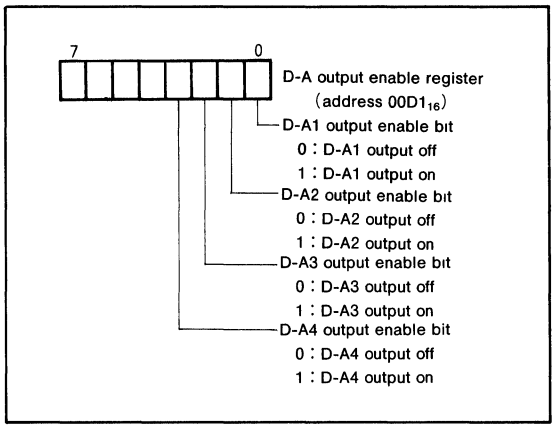


Fig.18 D-A output enable register

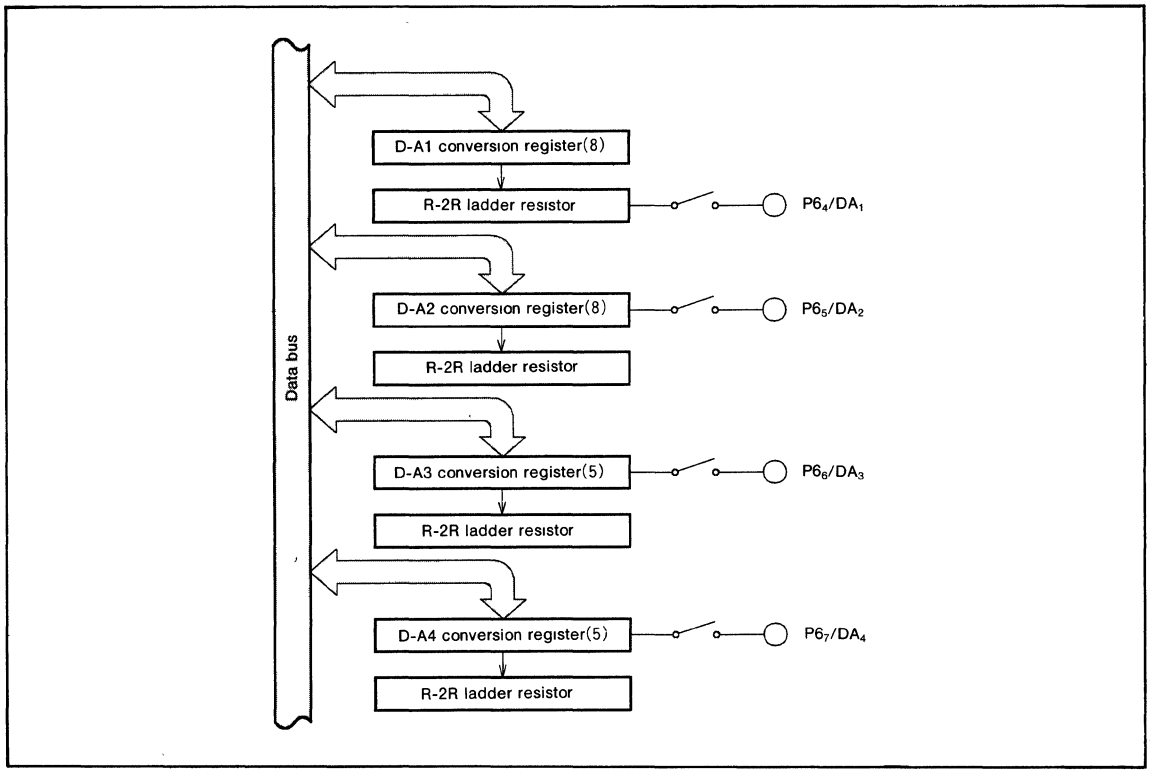


Fig.19 Block diagram of D-A converter

EXTERNAL TRIGGER OUTPUT

Port $P5_5$ operates as the pin Q which outputs the external trigger signal. Port $P6_1$ operates as the pin T which inputs the trigger clock. By setting bit 1 of the special function selection register (address $00EE_{16}$) to "1", the $P6_1/T/INT_1$ pin functions a trigger input pin and $P6_1$, $P5_5$ can be used as the external trigger function pins.

In external trigger mode, the value set by the external trigger output data bit is output to port $P5_5$ each time the active edge specified by bits 1 and 7 of the interrupt polarity specification register. Combinations of bits 3 and 4 of the special function selection register set port $P5_5$ to output mode as shown in Table 3. If using external trigger output, set the $P5_5$ directional bit to "0". At reset, this bit is cleared to "0".

Table 3. External trigger output

External trigger output direction specify bit \ External trigger output data bit	0	1
0	High-impedance	High-impedance
1	L	H

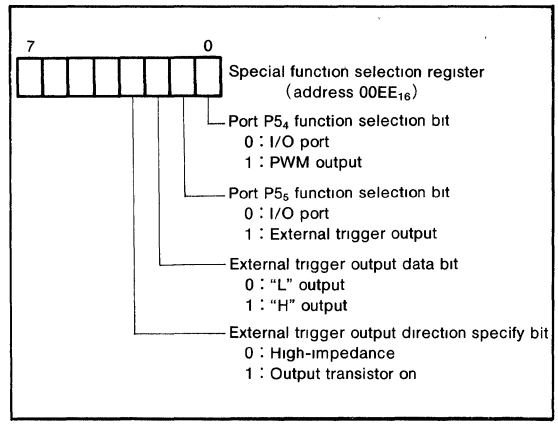


Fig.20 Structure of special function selection register

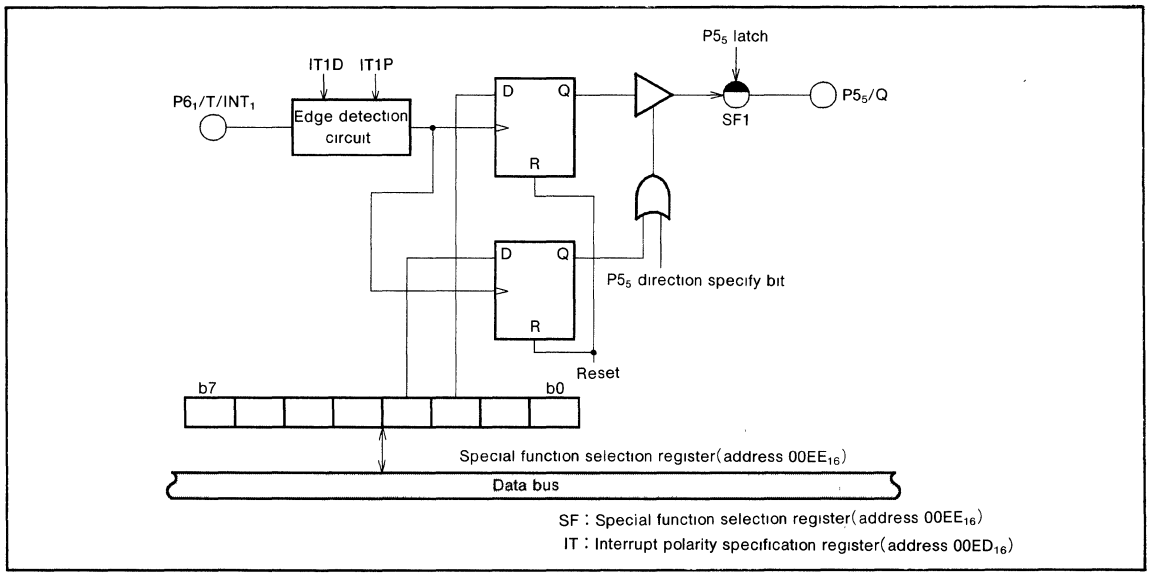


Fig.21 Block diagram of external trigger output

V PULSE AND Y PULSE GENERATOR

Port $P5_6$ operates as the VPLS pin to output the V pulse and port $P6_1$ operates as the T pin to input the trigger clock. $P5_6$ can be used as the V pulse output by setting bit 5 of the V pulse control register ($00D8_{16}$) to "1". Port $P5_7$ operates as the YPLS pin which outputs the Y pulse. It can be used as the Y pulse (VPF signal) output by setting bit 6 of the V pulse control register to "1". Effective edge of trigger input can be selected by setting bits 2 and 3 of V pulse control register. Figure 22 shows the block diagram of the V pulse, Y pulse generator. Figure 23 shows the timing diagram of the V pulse and Y pulse.

At the falling or rising edge of T, the VPP counter starts. By the overflow signal of the VPP counter, VPLS goes "H". By the overflow signal of VPP counter, the VPN counter starts. By the overflow signal of the VPN counter, VPLS goes "L". When the VPP counter or the VPN counter is counting, bit 4 of the V pulse control register is "1".

The preset value of the VPP conter can be set by the 9-bit register with bit 1 of the V pulse control register being the most significant bit and the V pulse preset value P ($00D6_{16}$) being the low-order eight bits. The preset value of the VPN counter can be set by the 9-bit register with bit 0 of the V pulse control register being the most significant bit and the V pulse preset value N ($00D7_{16}$) being the low-order eight bits.

Note that values of bits 0 and 1 of the V pulse control register are the current counting values in the VPP counter and the VPN counter, not the preset values of the counters.

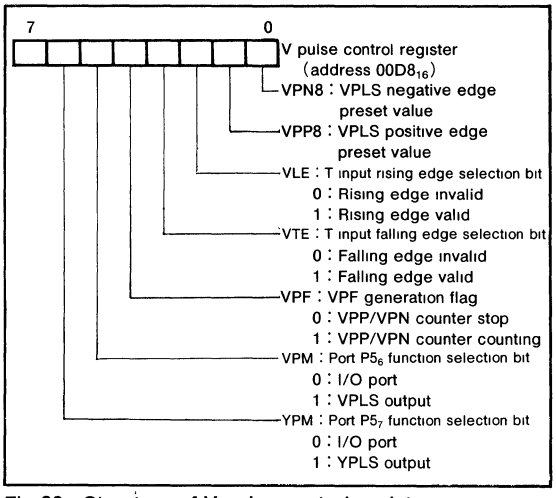


Fig.22 Structure of V pulse control register

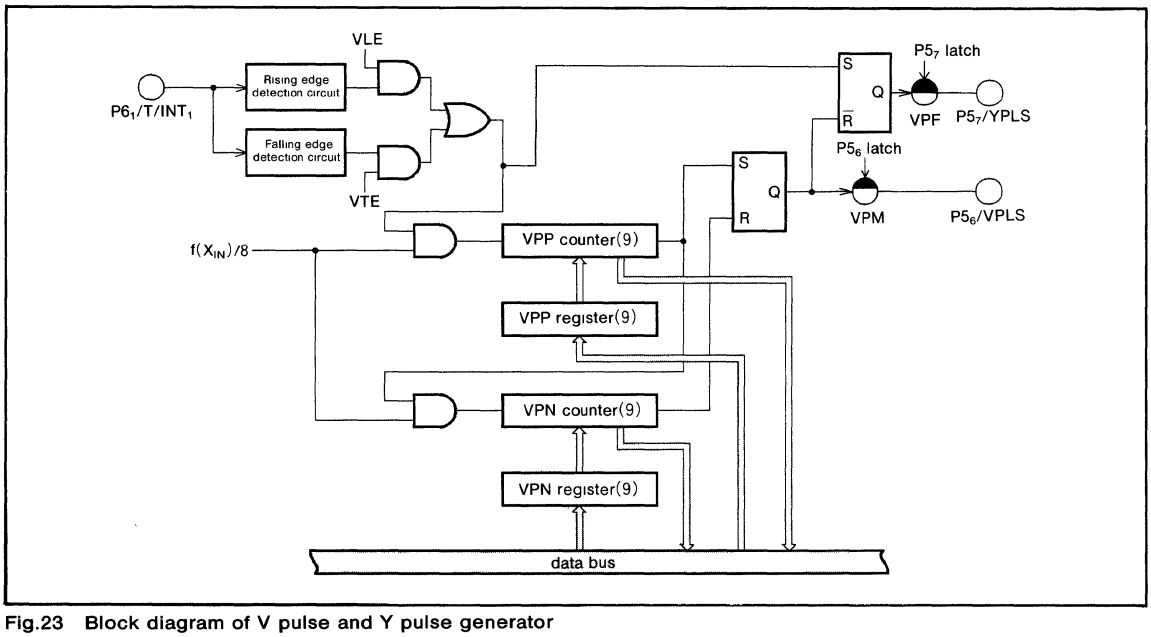


Fig.23 Block diagram of V pulse and Y pulse generator

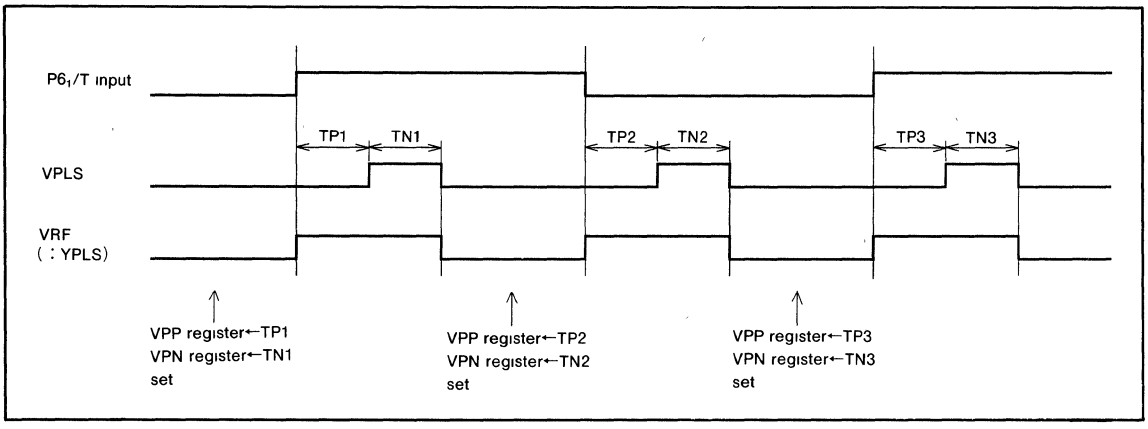


Fig.24 Timing diagram of the V pulse and Y pulse

WATCHDOG TIMER

The watchdog timer provides a method of returning to reset status if a runaway or other cause prevents a program from running a loop normally.

The watchdog timer is a 15-bit counter consisting of a lower seven bits and an upper eight bits (address $00EF_{16}$). At reset or after the watchdog timer is written to, $7FFF_{16}$ is set in this timer and it starts to count.

When the MSB reaches "0", an internal reset is generated. Therefore programs should normally be written to ensure that the watchdog timer is written to before this bit reaches "0". If address $00EF_{16}$ is read, the value in the upper eight bits of the counter is read. Directly after a reset, the watchdog timer is stopped. After reset is released, the first write to address $00EF_{16}$ validates the watchdog timer function.

The count source of the lower seven bits is a signal that is the system clock ϕ divided by eight. The count source of the upper eight bits can be selected as either the overflow signal from the 7-bit counter or a signal that is the system clock ϕ divided by eight, depending on the value of bit 3 of the CPU mode register (address $00FB_{16}$).

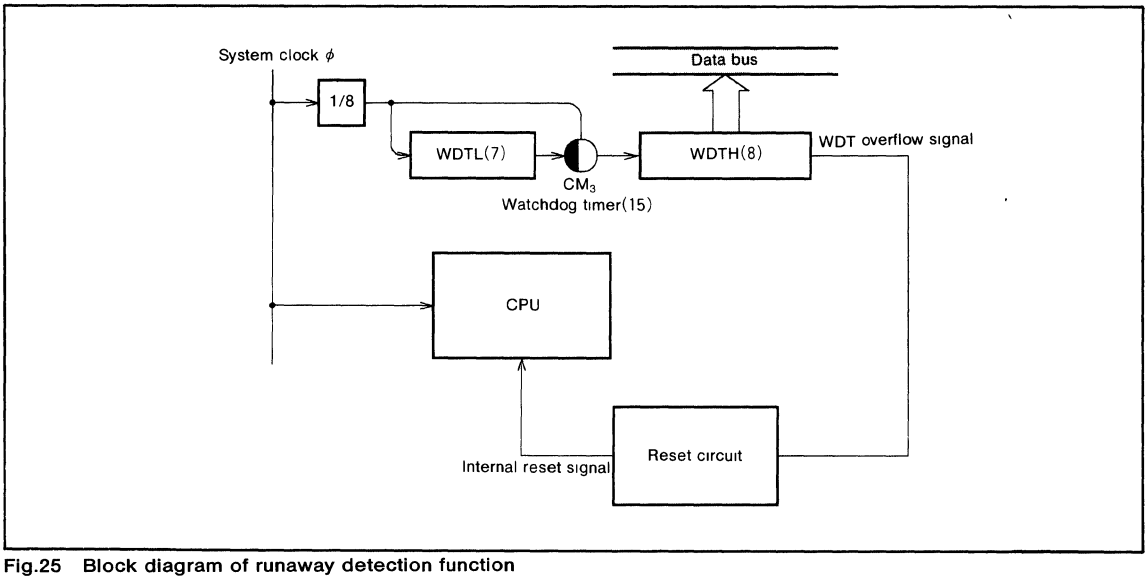


Fig.25 Block diagram of runaway detection function

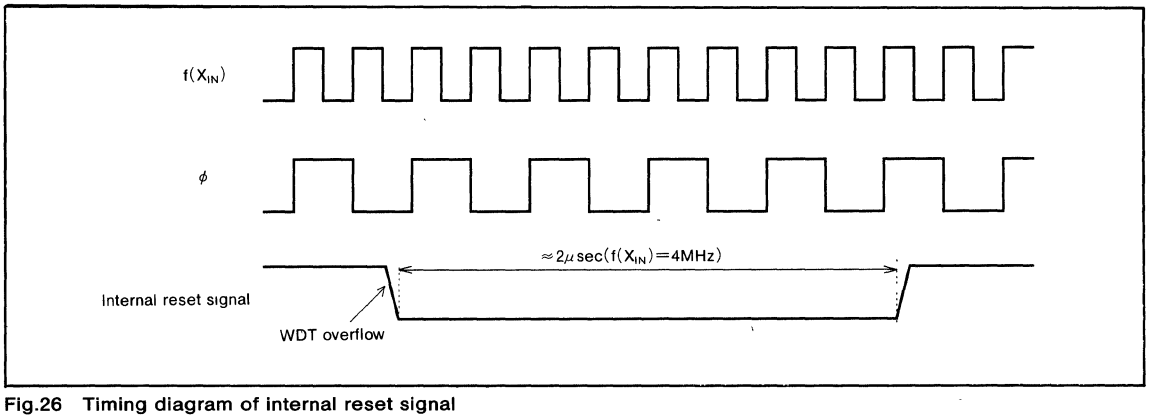


Fig.26 Timing diagram of internal reset signal

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS output.

As shown in the memory map (Figure 1), port P0 can be accessed at zero page memory address $00C0_{16}$. Port P0 has a directional register (address $00C1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

(2) Port P1

Port P1 has the same function as Port P0. The output structure of M37424M8-XXXSP is CMOS output. The output structure of M37524M4-XXXSP is N-channel open drain output.

(3) Port P2

Port P2 has the same function as Port P0.

(4) Port P3

Port P3 has the same function as port P0, but it has N-channel open drain output. Port P3 can also be used as serial I/O and timer output pins.

(5) Port P4

Port P4 has the same function as port P0. $P4_7$ through $P4_0$ can also be used as analog input pins AN_7 through AN_0.

(6) Port P5

Port P5 has the same function as port P0. Port P5 can also be used as INT_2~INT_5, PWM output, external trigger output Q and V pulse, Y pulse output pins.

(7) Port P6

Port P6 has the same function as port P0. Port P6 can also be used as INT_0, INT_1, trigger clock input T, timer I/O and D-A output pins.

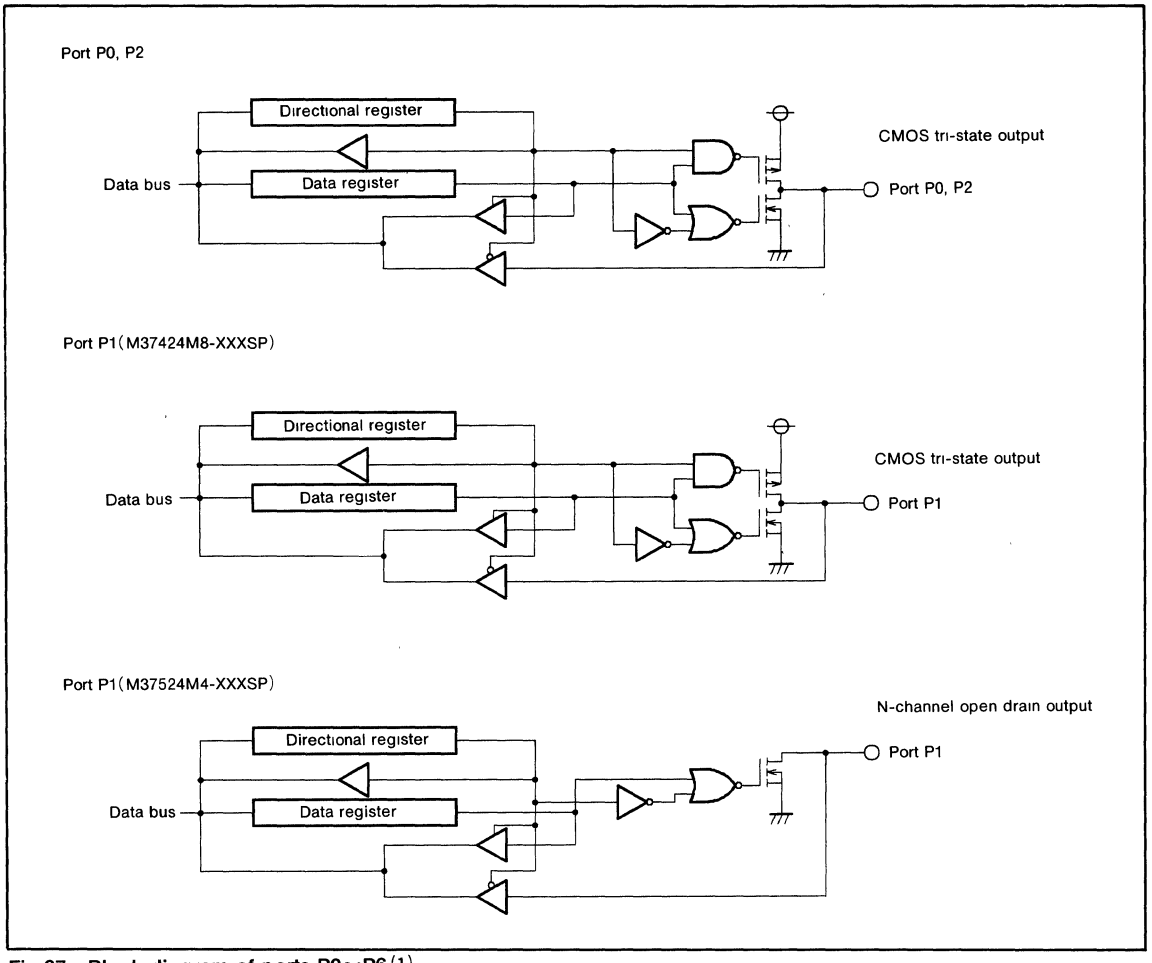


Fig.27 Block diagram of ports P0~P6(1)

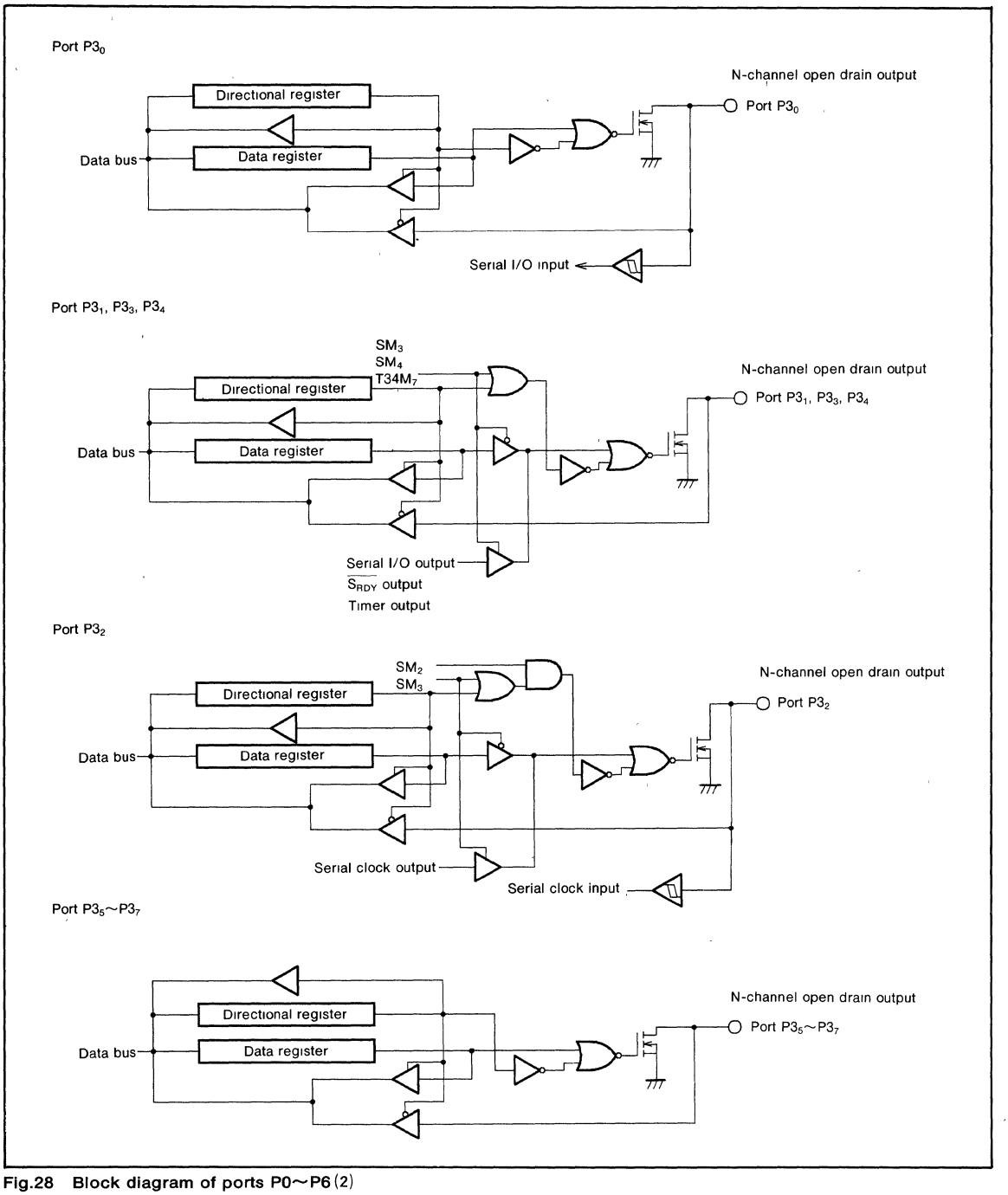


Fig.28 Block diagram of ports P0~P6 (2)

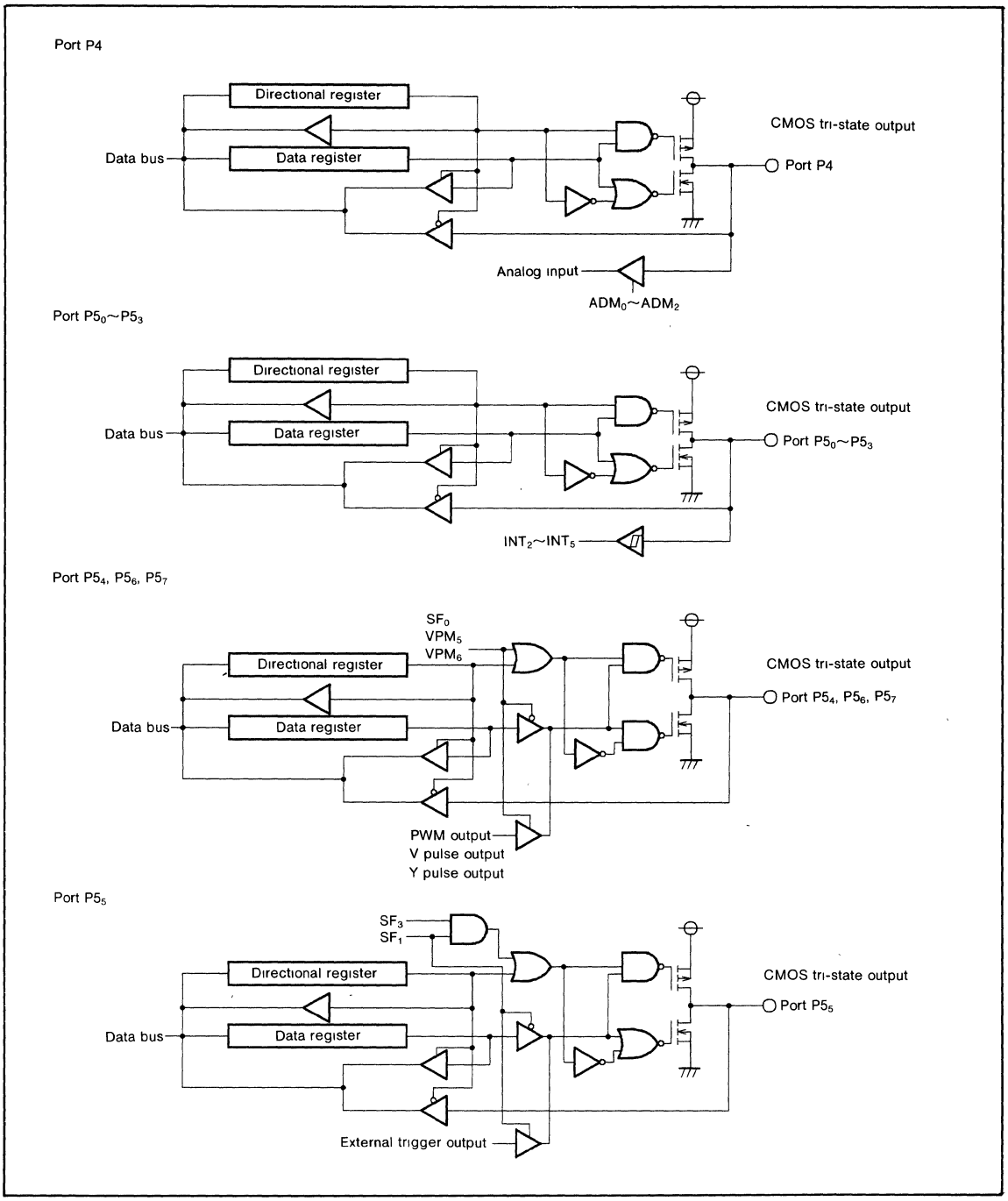


Fig.29 Block diagram of ports P0~P6 (3)

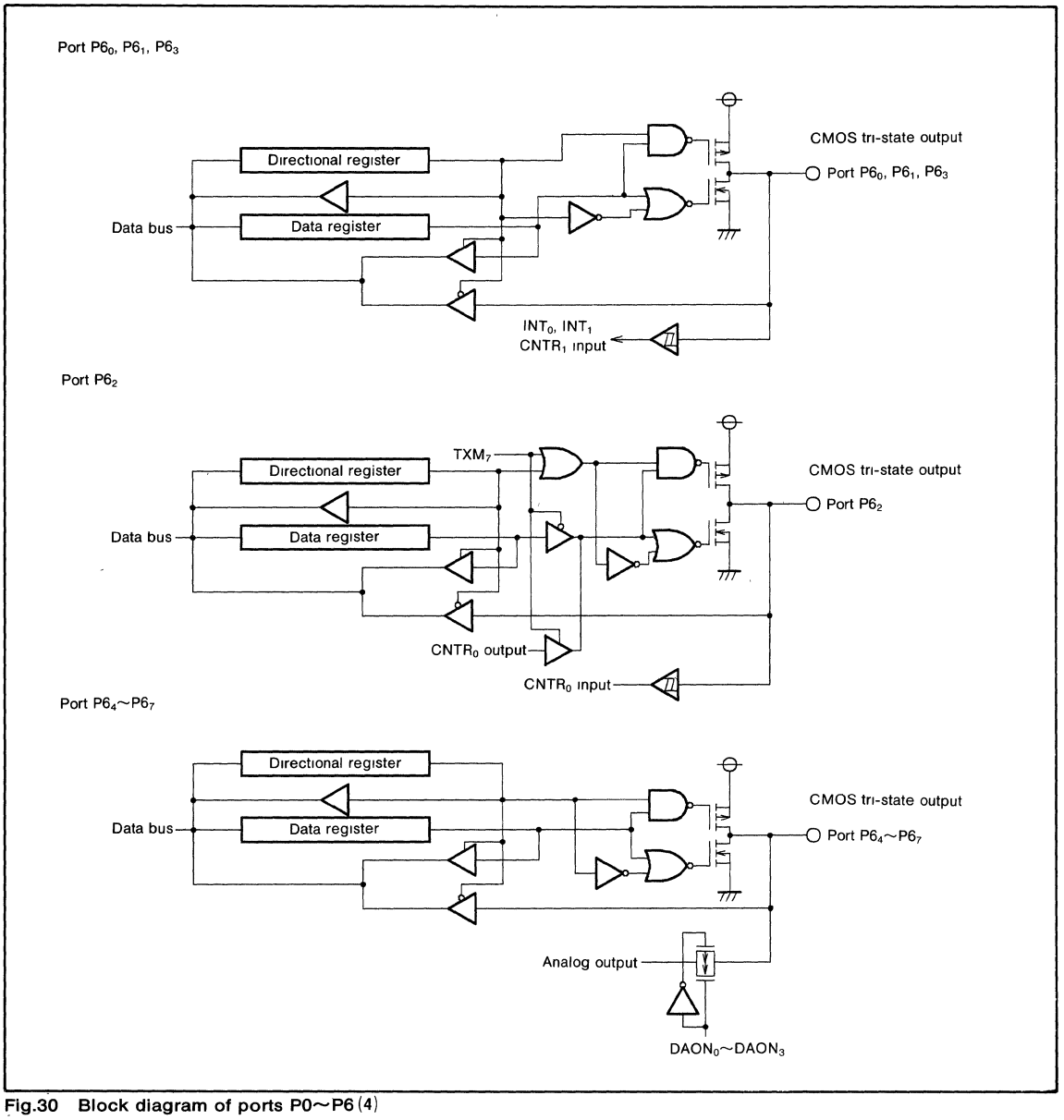


Fig.30 Block diagram of ports P0~P6 (4)

RESET CIRCUIT

The M37424M8-XXXSP is reset according to the sequence shown in Figure 31. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for more than 2μs while the power voltage is in the recommended operating condition and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 33. An example of the reset circuit is shown in Figure 32.

When the power on reset is used, the $\overline{RESET}$ pin must be held "L" until the oscillation of X_{IN}-X_{OUT} becomes stable.

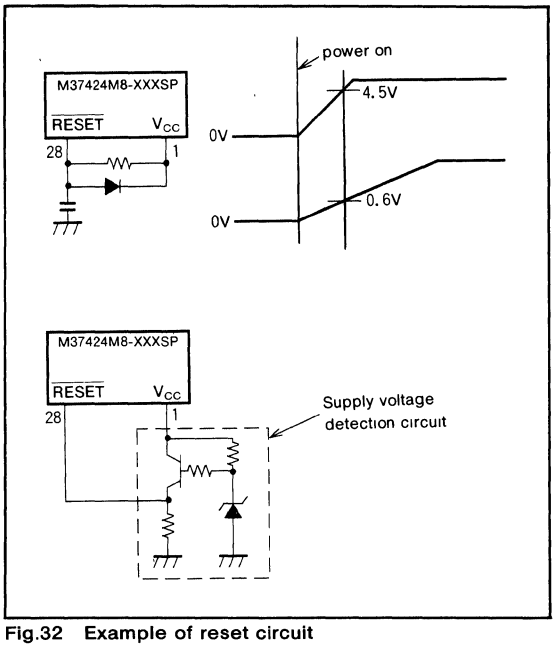


Fig.32 Example of reset circuit

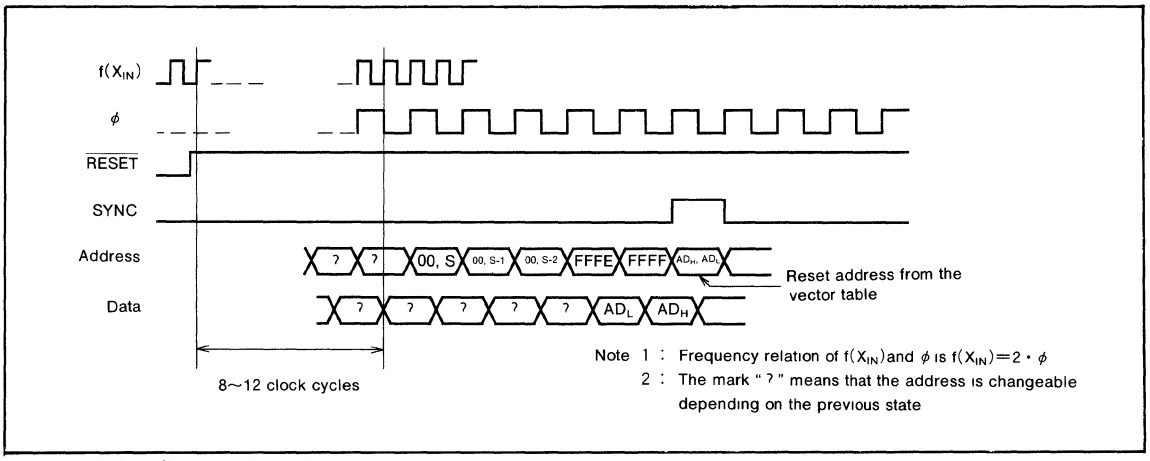


Fig.31 Timing diagram at reset

		address	
(1)	Port P0 directional register	($C1_{16}$)	00_{16}
(2)	Port P1 directional register	($C3_{16}$)	00_{16}
(3)	Port P2 directional register	($C5_{16}$)	00_{16}
(4)	Port P3 directional register	($C7_{16}$)	00_{16}
(5)	Port P4 directional register	($C9_{16}$)	00_{16}
(6)	Port P5 directional register	(CB_{16})	00_{16}
(7)	Port P6 directional register	(CD_{16})	00_{16}
(8)	D-A output enable register	($D1_{16}$)	0 0 0 0
(9)	D-A3 conversion register	($D2_{16}$)	00_{16}
(10)	D-A4 conversion register	($D3_{16}$)	00_{16}
(11)	V pulse control register	($D8_{16}$)	0 0 0 0
(12)	A-D control register	(DA_{16})	0 0 0 0
(13)	D-A1 conversion register	(DB_{16})	00_{16}
(14)	D-A2 conversion register	(DC_{16})	00_{16}
(15)	Serial I/O mode register	(DD_{16})	00_{16}
(16)	Interrupt polarity specification register	(ED_{16})	00_{16}
(17)	Special function selection register	(EE_{16})	0 0 0 0
(18)	Watchdog timer	(EF_{16})	$7FFF_{16}$
(19)	Timer 3	($F2_{16}$)	FF_{16}
(20)	Timer 4	($F3_{16}$)	07_{16}
(21)	Timer 1, 2 mode register	($F8_{16}$)	0 0 0 0 0 0
(22)	Timer 3, 4 mode register	($F9_{16}$)	0 0 0 0
(23)	Timer X mode register	(FA_{16})	00_{16}
(24)	CPU mode register	(FB_{16})	1 0 1 0 0
(25)	Interrupt request register 1	(FC_{16})	00_{16}
(26)	Interrupt request register 2	(FD_{16})	00_{16}
(27)	Interrupt control register 1	(FE_{16})	00_{16}
(28)	Interrupt control register 2	(FF_{16})	00_{16}
(29)	Processor status register	(PS)	1
(30)	Program counter	(PC_H)	Contents of address $FFFF_{16}$
		(PC_L)	Contents of address $FFFE_{16}$

Fig. 33 Internal state of microcomputer at reset

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 36.
When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once. To return from the wait status, the interrupt enable bit must be set to "1" before executing WIT instruction.
Since the M37424M8-XXXSP does not have STP instruction, the oscillation can not be stopped.
The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 34.
The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.
The example of external clock usage is shown in Figure 35. X_{IN} is the input, and X_{OUT} is open.

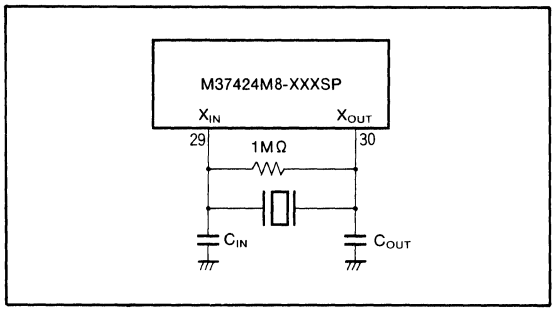


Fig.34 External ceramic resonator circuit

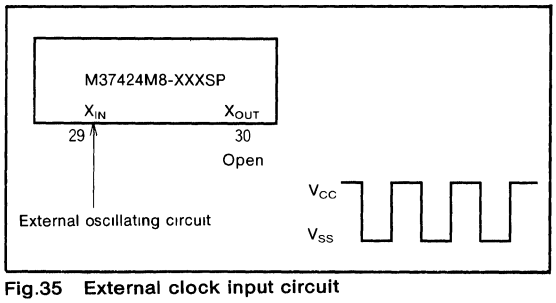


Fig.35 External clock input circuit

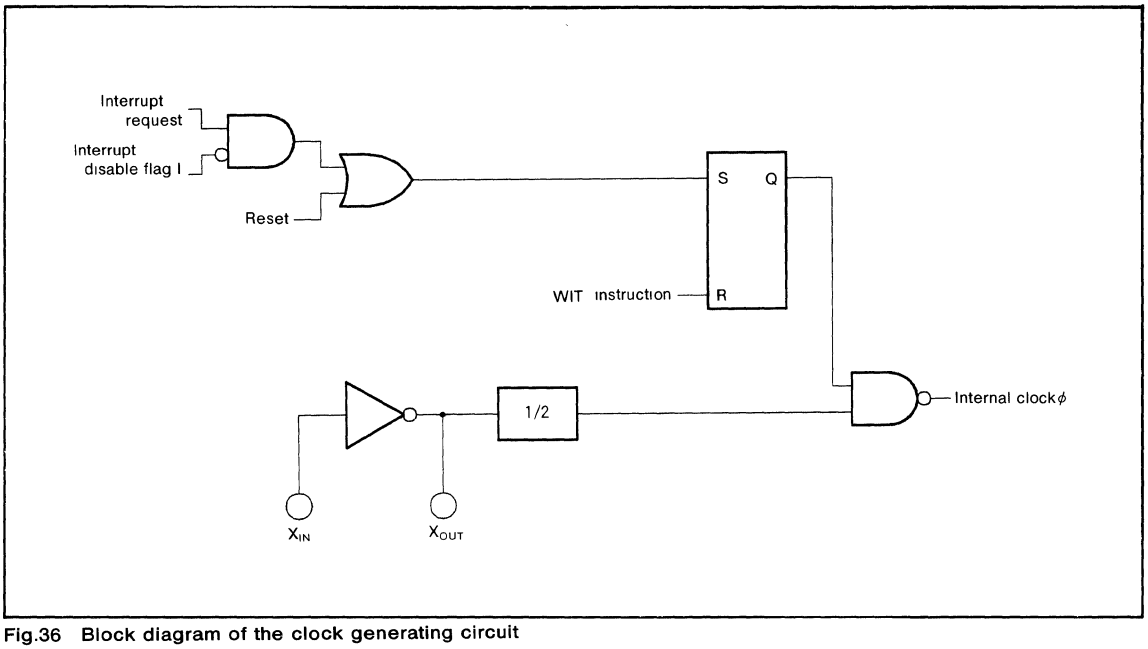


Fig.36 Block diagram of the clock generating circuit

PROGRAMMING NOTES

(1) The frequency ratio of the timer is 1/(n+1).
(2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
(3) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
(4) A NOP instruction must be used after the execution of a PLP instruction.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.
(1) mask ROM confirmation form
(2) mark specification form
(3) ROM data ..... EPROM 3sets

M37424M8-XXXSP
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state	−0.3∼7	V
V_{SS}	Supply voltage		0	V
V_{REF}	Reference voltage		−0.3∼V_{CC}+0.3	V
V_I	Input voltage X_{IN}, $\overline{RESET}$, $P3_0$∼$P3_7$, CNV_{SS}		−0.3∼7	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$		−0.3∼V_{CC}+0.3	V
V_O	Output voltage $P3_0$∼$P3_7$		0.3∼7	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, X_{OUT}, ϕ		−0.3∼V_{CC}+0.3	V
P_d	Power dissipation	T_a=25℃	1000	mW
Topr	Operating temperature		−10∼70	℃
Tstg	Storage temperature		−40∼125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=−10∼70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, INT_0∼INT_5, $CNTR_0$, $CNTR_1$, T, $\overline{RESET}$, X_{IN}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, INT_0∼INT_5, $CNTR_0$, $CNTR_1$, T	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OH(peak)}$	"H" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (Note 1)			−10	mA
$I_{OH(avg)}$	"H" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (Note 1)			−5	mA
$I_{OL(peak)}$	"L" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (Note 2)			10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (Note 2)			5	mA
$f(X_{IN})$	Clock oscillating frequency			4	MHz

Note 1. The total of "H" peak output current of port P0, P1, P2, P4, P5 and P6 is less than 65mA
2. The total of "L" peak output current of port P0, P1, P2, P3, P4, P5 and P6 is less than 65mA

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	I_{OH}=−10mA	3			V
V_{OH}	"H" output voltage ϕ	I_{OH}=−2.5mA	3			V
V_{OL}	"L" output voltage $P3_0$~$P3_7$	I_{OL}=10mA			2	V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	I_{OL}=10mA			2	V
V_{OL}	"L" output voltage ϕ	I_{OL}=2.5mA			2	V
V_+−V_-	Hysteresis X_{IN}		0.1		0.5	V
V_+−V_-	Hysteresis $\overline{RESET}$			0.5	0.7	V
V_+−V_-	Hysteresis INT_0~INT_5, $CNTR_0$, $CNTR_1$, T	Use as INT_0~INT_5, $CNTR_0$, $CNTR_1$, T input	0.3		1.0	V
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}	V_{IH}=5V			5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	V_{IH}=5V			5	μA
I_{IH}	"H" input current $P3_0$~$P3_7$	V_{IH}=5V			5	μA
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}	V_{IL}=0V	−5			μA
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	V_{IL}=0V	−5			μA
I_{IL}	"L" input current $P3_0$~$P3_7$	V_{IL}=0V	−5			μA
I_{CC}	Supply current	f(X_{IN}) = 4MHz, output pins opened, input pins at V_{SS} or V_{CC}, and A-D converter in the finished condition		6	12	mA

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	V_{REF}=V_{CC}			8	bits
—	Absolute accuracy	V_{REF}=V_{CC}			±3	LSB
R_{LADDER}	Ladder resistor	V_{REF}=V_{CC}	20			kΩ
t_{CONV}	Conversion time				25	μs
V_{REF}	Reference voltage		4		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

D-A CONVERTER 1, 2 CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	V_{REF}=V_{CC}			8	bits
—	Absolute accuracy	V_{REF}=V_{CC}			±2	%
R_O	Ladder resistor	V_{REF}=V_{CC}			4	kΩ
t_{SU}	Setup time	V_{REF}=V_{CC}			3	μs
V_{REF}	Reference voltage		4		V_{CC}	V

D-A CONVERTER 3, 4 CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	V_{REF}=V_{CC}			5	bits
—	Absolute accuracy	V_{REF}=V_{CC}			±2	%
R_O	Ladder resistor	V_{REF}=V_{CC}			4	kΩ
t_{SU}	Setup time	V_{REF}=V_{CC}			3	μs
V_{REF}	Reference voltage		4		V_{CC}	V

M37524M4-XXXSP
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state	−0.3∼7	V
V_{SS}	Supply voltage		0	V
V_{REF}	Reference voltage		−0.3∼V_{CC}+0.3	V
V_I	Input voltage X_{IN}, $\overline{RESET}$, CNV_{SS}		−0.3∼7	V
V_I	Input voltage $P1_0$∼$P1_7$, $P3_0$∼$P3_7$		−0.3∼13	V
V_I	Input voltage $P0_0$∼$P0_7$, $P2_0$∼$P2_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$		−0.3∼V_{CC}+0.3	V
V_O	Output voltage $P1_0$∼$P1_7$, $P3_0$∼$P3_7$		−0.3∼13	V
V_O	Output voltage $P0_0$∼$P0_7$, $P2_0$∼$P2_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, X_{OUT}, ϕ		−0.3∼V_{CC}+0.3	V
Pd	Power dissipation	T_a=25℃	1000	mW
Topr	Operating temperature		−10∼70	℃
Tstg	Storage temperature		−40∼125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=−10∼70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, INT_0∼INT_5, $CNTR_0$, $CNTR_1$, T, $\overline{RESET}$, X_{IN}	0.8V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, INT_0∼INT_5, $CNTR_0$, $CNTR_1$, T	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OH(peak)}$	"H" peak output current $P0_0$∼$P0_7$, $P2_0$∼$P2_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (Note 1)			−10	mA
$I_{OH(avg)}$	"H" average output current $P0_0$∼$P0_7$, $P2_0$∼$P2_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (Note 1)			−5	mA
$I_{OL(peak)}$	"L" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (Note 2)			10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_7$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$ (Note 2)			5	mA
$f(X_{IN})$	Clock oscillating frequency			4	MHz

Note 1. The total of "H" peak output current of port P0, P2, P4, P5 and P6 is less than 65mA.
2. The total of "L" peak output current of port P0, P1, P2, P3, P4, P5 and P6 is less than 65mA

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P2_0$~$P2_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	I_{OH}=−10mA	3			V
V_{OH}	"H" output voltage ϕ	I_{OH}=−2.5mA	3			V
V_{OL}	"L" output voltage $P1_0$~$P1_7$, $P3_0$~$P3_7$	I_{OL}=10mA			2	V
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P2_0$~$P2_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	I_{OL}=10mA			2	V
V_{OL}	"L" output voltage ϕ	I_{OL}=2.5mA			2	V
V_+−V_-	Hysteresis X_{IN}		0.1		0.5	V
V_+−V_-	Hysteresis $\overline{RESET}$			0.5	0.7	V
V_+−V_-	Hysteresis INT_0~INT_5, $CNTR_0$, $CNTR_1$, T	Use as INT_0~INT_5, $CNTR_0$, $CNTR_1$, T input	0.3		1.0	V
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}	V_{IH}=5V			5	μA
I_{IH}	"H" input current $P0_0$~$P0_7$, $P2_0$~$P2_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	V_{IH}=5V			5	μA
I_{IH}	"H" input current $P1_0$~$P1_7$, $P3_0$~$P3_7$	V_{IH}=12V			12	μA
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}	V_{IL}=0V	−5			μA
I_{IL}	"L" input current $P0_0$~$P0_7$, $P2_0$~$P2_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$	V_{IL}=0V	−5			μA
I_{IL}	"L" input current $P1_0$~$P1_7$, $P3_0$~$P3_7$	V_{IL}=0V	−5			μA
I_{CC}	Supply current	f(X_{IN}) = 4MHz, output pins opened, input pins at V_{SS} or V_{CC}, and A-D converter in the finished condition		6	12	mA

A-D CONVERTER CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	V_{REF}=V_{CC}			8	bits
—	Absolute accuracy	V_{REF}=V_{CC}			±3	LSB
R_{LADDER}	Ladder resistor	V_{REF}=V_{CC}	20			kΩ
t_{CONV}	Conversion time				25	μs
V_{REF}	Reference voltage		4		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

D-A CONVERTER 1, 2 CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	V_{REF}=V_{CC}			8	bits
—	Absolute accuracy	V_{REF}=V_{CC}			±2	%
R_O	Ladder resistor	V_{REF}=V_{CC}			4	kΩ
t_{SU}	Setup time	V_{REF}=V_{CC}			3	μs
V_{REF}	Reference voltage		4		V_{CC}	V

D-A CONVERTER 3, 4 CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution	V_{REF}=V_{CC}			5	bits
—	Absolute accuracy	V_{REF}=V_{CC}			±2	%
R_O	Ladder resistor	V_{REF}=V_{CC}			4	kΩ
t_{SU}	Setup time	V_{REF}=V_{CC}			3	μs
V_{REF}	Reference voltage		4		V_{CC}	V