M37450M4TXXXSP/J

EXTENDED OPERATING TEMPERATURE VERSION of M37450M4-XXXSP

DESCRIPTION

The M37450M4TXXXSP/J is a single-chip microcomputer designed with CMOS sillicon gate technology. It is housed in a 64-pin shrink plastic molded DIP or an 84-pin plastic molded QFJ (PLCC).

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

It is suited for office automation equipment and control devices The low power consumption made by the use of a CMOS process makes it especially suitable for battery powered devices requiring low power consumption. It also has a unique feature that enables it to be used as a slave microcomputer.

The differences between the M37450M4TXXXSP/J and the M37450M4-XXXSP/FP are some electrical characteristics, the expansion of operating temperature range, and the package.

The number of analog input pins for the 84-pin PLCC (J version) is different from the 64-pin model (SP version). In addition, the 84-pin model has special pins for $\overline{RD}$, $\overline{WR}$, $RESET_{OUT}$, DAV_{REF}, ADV_{REF}, AV_{CC} and the 64-pin model has a special V_{REF} pin.

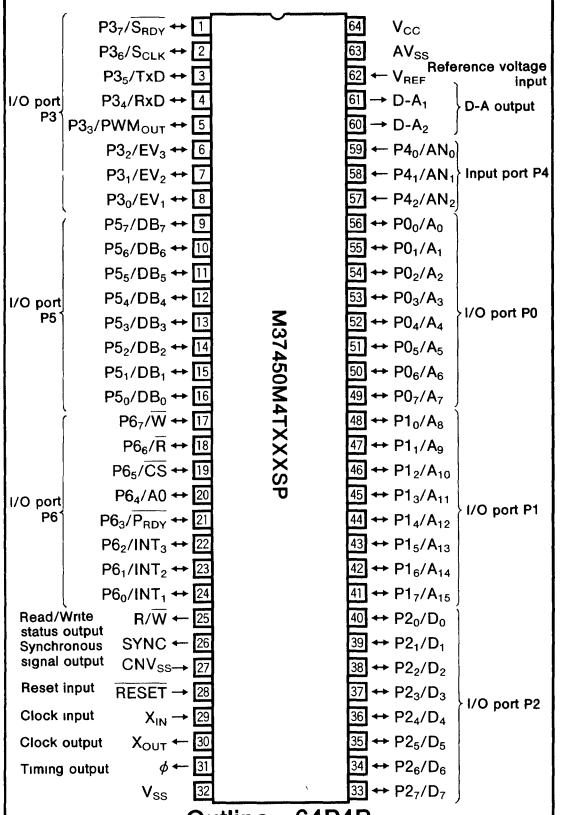
FEATURES

- Number of basic instructions 71
  69 MELPS 740 basic instructions+2 multiply/divide instructions
- Memory size
  ROM ..... 8192 bytes
  RAM ..... 256 bytes
- Instruction execution time
  (minimum instructions at 10MHz frequency) 0.8μs
- Single power supply ..... 5V$\pm$10%
- Power dissipation normal operation mode
  (at 10MHz frequency) 30mW
- Subroutine nesting ..... 96 levels max
- Interrupt ..... 15 events
- Master CPU interface ..... 1 byte
- 16-bit timer 3
- 8-bit timer (Serial I/O use) 1
- Serial I/O (UART or clock synchronous) 1
- A-D converter (8-bit resolution) ..... 3 channels (DIP)
  8 channels (QFJ)
- D-A converter (8-bit resolution) ..... 2 channels
- PWM output (8 bit or 16 bit) 1
- Programmable I/O ports
  (Ports P0, P1, P2, P3, P5, P6) 48
- Input port (Port P4) ..... 3(DIP), 8(QFJ)
- Output ports (Ports $D\text{-}A_1$, $D\text{-}A_2$) 2

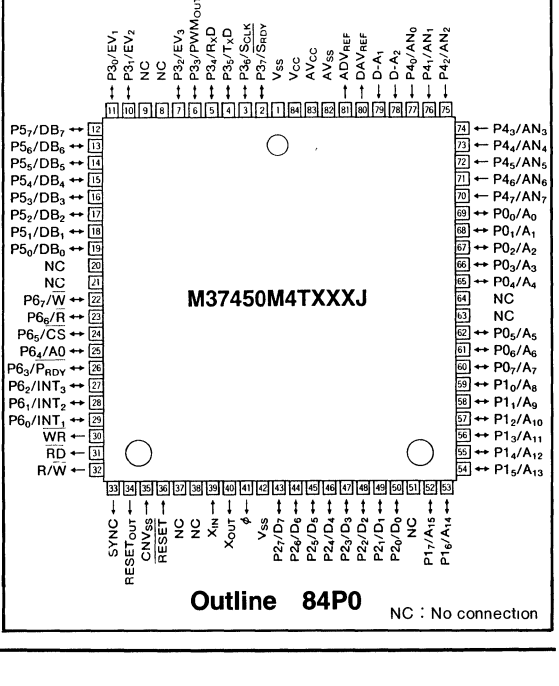
APPLICATION

Slave controller for PPCs, facsimiles, and page printers.
HDD, optical disk, inverter, and industrial motor controllers.
Industrial robots and machines.

PIN CONFIGURATION (TOP VIEW)



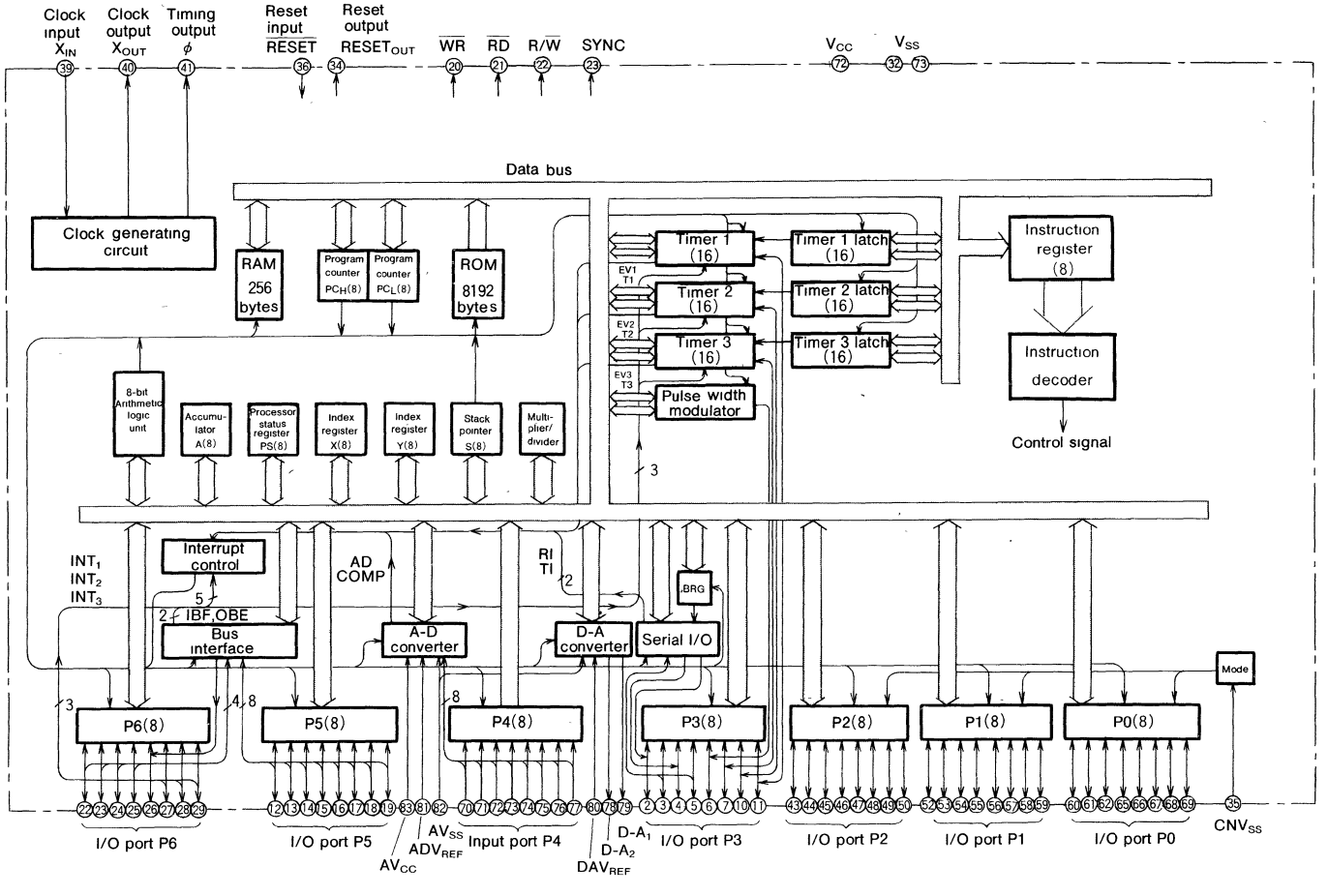
Outline 64P4B



Outline 84P0

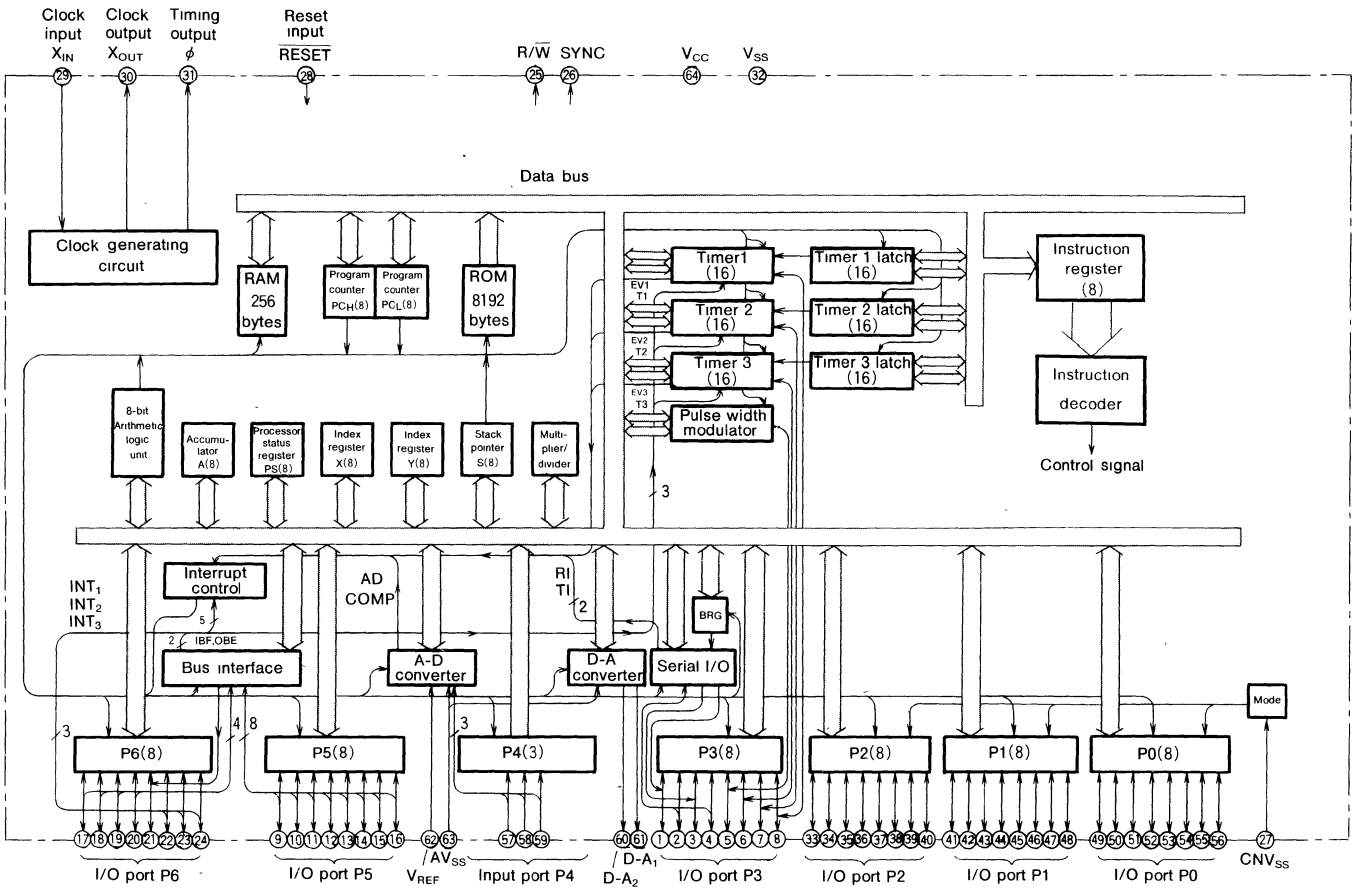
NC : No connection

M37450M4TXXXJ BLOCK DIAGRAM



MITSUBISHI ELECTRIC

M37450M4TXXXSP BLOCK DIAGRAM



FUNCTIONS OF M37450M4TXXXSP/J

Parameter			Functions
Number of basic instructions			71(69 MELPS 740 basic instructions+2)
Instruction execution time			0.8μs (minimum instructions, at 10MHz of frequency)
Clock frequency			10MHz (max.)
Memory size	ROM		8192 bytes
	RAM		256 bytes
Input/Output ports	P0-P3, P5, P6	I/O	8-bit×6
	P4	Input	3-bit×1 (8-bit×1 for 84-pin model)
	D-A	Output	2-bit×1
Serial I/O			UART or clock synchronous
Timers			16-bit timer×3, 8-bit timer (serial I/O baud rate generator)×1
A-D converter			8-bit×3 channels (8 channels for 84-pin model)
D-A converter			8-bit×2 channels
Pulse width modulator			8-bit or 16-bit×1
Data bus buffer			1-byte input and output each
Subroutine nesting			96-levels (max.)
Interrupt			6 external interrupts, 8 internal interrupts 1 software interrupt
Clock generating circuit			Built-in (ceramic or quarts crystal oscillator)
Supply voltage			5V±10%
Power dissipation			30mW (at 10MHz frequency)
Input/Output characters	Input/Output voltage		5V
	Output current		±5mA (max.)
Memory expansion			Possible
Operating temperature range			−40 to 85℃
Device structure			CMOS silicon gate
Package	M37450M4TXXXSP		64-pin shrink plastic molded DIP
	M37450M4TXXXJ		84-pin plastic molded QFJ (PLCC)

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}
CNV_{SS}	CNV_{SS}		Controls the processor mode of the chip Normally connected to V_{SS} or V_{CC}
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 8 clock cycles (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	Outputs signal consisting of oscillating frequency divided by four
SYNC	Synchronous signal output	Output	This signal is output "H" during operation code fetch and is used to control single stepping of programs
R/$\overline{W}$	Read/Write status output	Output	This signal determines the direction of the data bus It is "H" during read and "L" during write
$P0_0$-$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output The output structure is CMOS output The low-order bits of the address are output except in single-chip mode
$P1_0$-$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0 The high-order bits of the address are output except in single-chip mode
$P2_0$-$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0 Used as data bus except in single-chip mode
$P3_0$-$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0 Serial I/O, PWM output, or event I/O function can be selected with a program
$P4_0$-$P4_2$ ($P4_0$-$P4_7$)	Input port P4	Input	Analog input pin for the A-D converter The 64-pin model has three pins and the 84-pin model has eight pins They may also be used as digital input pins
$P5_0$-$P5_7$	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same functions as port P0 This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program
$P6_0$-$P6_7$	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same function as port P0 Pins $P6_3$ to $P6_7$ change to a control bus for the master CPU when slave mode is selected with a program Pins $P6_0$ to $P6_2$ may be programmed as external interrupt input pins
$D\text{-}A_1$, $D\text{-}A_2$	D-A output	Output	Analog signal from D-A converter is output
V_{REF}	Reference voltage input	Input	Reference voltage input pin for A-D and D-A converter This pin is for 64-pin model only
ADV_{REF}	A-D reference voltage input	Input	Reference voltage input pin for A-D converter This pin is for 84-pin model only
DAV_{REF}	D-A reference voltage input	Input	Reference voltage input pin for D-A converter This pin is for 84-pin model only
AV_{SS}	Analog power supply		Ground level input pin for A-D and D-A converter Same voltage as V_{SS} is applied
AV_{CC}	Analog power supply		Power supply input pin for A-D converter This pin is for 84-pin model only Same voltage as V_{CC} is applied In the case of the 64-pin model, AV_{CC} is connected to V_{CC} internally
$\overline{RD}$	Read signal output	Output	Control signal output as active "L" when valid data is read from data bus This pin is for 84-pin model only
$\overline{WR}$	Write signal output	Output	Control signal output as active "L" when writing data from data bus to external component This pin is for 84-pin model only
$RESET_{OUT}$	Reset output	Output	Control signal output as active "H" during reset It is used as a reset output signal for peripheral components This pin is for 84-pin model only

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "off" state	−0.3 to 7	V
V_I	Input voltage X_{IN}, $\overline{RESET}$		−0.3 to 7	V
V_I	Input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, ADV_{REF}, DAV_{REF}, V_{REF}, AV_{CC}		−0.3 to V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3 to 13	V
V_O	Output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, X_{OUT}, ϕ, R/$\overline{W}$, $\overline{RD}$, $\overline{WR}$, SYNC, $RESET_{OUT}$		−0.3 to V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000	mW
Topr	Operating temperature		−40 to 85	℃
Tstg	Storage temperature		−65 to 150	℃

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=−40 to 85℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, CNV_{SS} (Note 1)	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (expect Note 1)	2.0		V_{CC}	V
V_{IL}	"L" input voltage CNV_{SS} (Note 1)	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (expect Note 1)	0		0.8	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note 2)			5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			−10	mA
$I_{OH(avg)}$	"H" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note 2)			−5	mA
$f(X_{IN})$	Internal clock oscillating frequency	1		10	MHz

Note 1 : Ports operating as special function pins INT_1-INT_3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_XD($P3_4$), S_{CLK}($P3_6$)

2 : $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average current in 100ms.

3 : The total of I_{OL} of Port P0, P1 and P2 should be 40mA (max)
The total of I_{OL} of Port P3, P5, P6, R/$\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ should be 40mA (max)
The total of I_{OH} of Port P0, P1, and P2 should be 40mA (max)
The total of I_{OH} of Port P3, P5, P6, R/$\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$, and ϕ should be 40mA (max)

EXTENDED OPERATING TEMPERATURE VERSION of M37450M4-XXXSP

ELECTRIC CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}= 0 V, T_a=−40 to 85℃, f(X_{IN})=10MHz)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max.	
V_{OH}	"H" output voltage $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	I_{OH} = − 2 mA	V_{CC}−1			V
V_{OH}	"H" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	I_{OH} = − 5 mA	V_{CC}−1			V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	I_{OL} =2 mA			0.45	V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	I_{OL} =5 mA			1	V
$V_{T+}-V_{T-}$	Hysteresis INT_1-INT_3($P6_0$-$P3_2$), EV_1-EV_3($P3_0$-$P3_2$), R_XD($P3_4$), S_{CLK}($P3_6$)	Function input level	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$				0.7	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	V_I =V_{SS}	−5		5	μA
I_{IH}	"H" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	V_I =V_{CC}	−5		5	μA
V_{RAM}	RAM retention voltage	At stop mode	2			V
I_{CC}	Supply current	f(X_{IN})=10MHz At system operation		6	15	mA
		At stop mode (Note 1)		1	10	μA

Note 1 : The terminals $\overline{RD}$, $\overline{WR}$, SYNC, R/$\overline{W}$, $RESET_{OUT}$, ϕ, D-A_1 and D-A_2 are all open The other ports, which are in the input mode, are connected to V_{SS} A-D converter is in the A-D completion state The current through ADV_{REF} and DAV_{REF} is not included (Fig 4)

A-D CONVERTER CHARACTERISTICS

(V_{CC}=AV_{CC}= 5 V±10%, V_{SS}=AV_{SS}= 0 V, T_a =−40 to 85℃, f(X_{IN})=10MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=AV_{CC}=ADV_{REF}=5V±10%		±1.5	±3	LSB
t_{CONV}	Conversion time				49	$t_{c(\phi)}$
V_{IA}	Analog input voltage		AV_{SS}		AV_{CC}	V
V_{ADVREF}	Reference input voltage		2		V_{CC}	V
R_{LADDER}	Ladder resistance value	ADV_{REF}= 5 V	2	7.5	10	kΩ
$I_{IADVREF}$	Reference input current	ADV_{REF}= 5 V	0.5	0.7	2.5	mA
V_{AVCC}	Analog power supply input voltage			V_{CC}		V
V_{AVSS}	Analog power supply input voltage			0		V

D-A CONVERTER CHARACTERISTICS (V_{CC}= 5 V±10%, V_{SS}=AV_{SS}= 0 V, T_a =−40 to 85℃ unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Full scale deviation	V_{CC}=DAV_{REF}=5V			1.0	%
t_{SU}	Set time				3	μs
R_O	Output resistance		1	2	4	kΩ
V_{AVSS}	Analog power supply input voltage			0		V
V_{DAVREF}	Reference input voltage		4		V_{CC}	V
I_{DAVREF}	Reference power input current (Each pin)		0	2.5	5	mA

TIMING REQUIREMENTS

Port/single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ	Max.	
$t_{su(P0D-\phi)}$	Port P0 input setup time	Fig.1	200			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time		200			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time		200			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time		200			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time		200			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time		200			ns
$t_{su(P6D-\phi)}$	Port P6 input setup time		200			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		40			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		40			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		40			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		40			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		40			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time		40			ns
$t_{h(\phi-P6D)}$	Port P6 input hold time		40			ns
$t_C(X_{IN})$	External clock input cycle time		100		1000	ns
$t_W(X_{IN}L)$	External clock input "L" pulse width		30			ns
$t_W(X_{IN}H)$	External clock input "H" pulse width		30			ns
$t_r(X_{IN})$	External clock rising edge time				20	ns
$t_f(X_{IN})$	External clock falling edge time				20	ns

Master CPU bus interface timing ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ	Max	
$t_{su(CS-R)}$	$\overline{CS}$ setup time	Fig 2	0			ns
$t_{su(CS-W)}$	$\overline{CS}$ setup time		0			ns
$t_{h(R-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{h(W-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-R)}$	A0 setup time		40			ns
$t_{su(A-W)}$	A0 setup time		40			ns
$t_{h(R-A)}$	A0 hold time		10			ns
$t_{h(W-A)}$	A0 hold time		10			ns
$t_{W(R)}$	Read pulse width		160			ns
$t_{W(W)}$	Write pulse width		160			ns
$t_{su(D-W)}$	Date input setup time before write		100			ns
$t_{h(W-D)}$	Date input hold time after write		10			ns

Master CPU bus interface timing (R/$\overline{W}$ type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{su(CS-E)}$	$\overline{CS}$ setup time	Fig 2	0			ns
$t_{h(E-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-E)}$	A0 setup time		40			ns
$t_{h(E-A)}$	A0 hold time		10			ns
$t_{su(RW-E)}$	R/$\overline{W}$ setup time		40			ns
$t_{h(E-RW)}$	R/$\overline{W}$ hold time		10			ns
$t_{W(EL)}$	Enable clock "L" pulse width		160			ns
$t_{W(EH)}$	Enable clock "H" pulse width		160			ns
$t_{r(E)}$	Enable clock rising edge time				25	ns
$t_{f(E)}$	Enable clock falling edge time				25	ns
$t_{su(D-E)}$	Data input setup time before write		100			ns
$t_{h(E-D)}$	Data input hold time after write		10			ns

Local bus/memory expansion mode, microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ.	Max	
$t_{SU(D-\phi)}$	Data input setup time	Fig 3	130			ns
$t_{h(\phi-D)}$	Data input hold time		0			ns
$t_{SU(D-RD)}$	Data input setup time		130			ns
$t_{h(RD-D)}$	Data input hold time		0			ns

SWITCHING CHARACTERISTICS

Port/single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig.3			200	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				200	ns
$t_{d(\phi-P5Q)}$	Port P5 data output delay time				200	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				200	ns
$t_{C(\phi)}$	Cycle time		400		4000	ns
$t_{W(\phi H)}$	ϕ clock pulse width ("H" level)		190			ns
$t_{W(\phi L)}$	ϕ clock pulse width ("L" level)		170			ns
$t_{r(\phi)}$	ϕ clock rising edge time				20	ns
$t_{f(\phi)}$	ϕ clock falling edge time				20	ns

Master CPU bus interface ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{a(R-D)}$	Data output enable time after read	Fig.4			120	ns
$t_{V(R-D)}$	Data output disable time after read		10		85	ns
$t_{PLH(R-PR)}$	$\overline{P_{RDY}}$ output transmission time after read				150	ns
$t_{PLH(W-PR)}$	$\overline{P_{RDY}}$ output transmission time after write				150	ns

Master CPU bus interface (R/$\overline{W}$ type mode) (V_{CC}=5V±10%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{a(E-D)}$	Data output enable time after read	Fig 4			120	ns
$t_{V(E-D)}$	Data output disable time after read		10		85	ns
$t_{PLH(E-PR)}$	$\overline{P_{RDY}}$ output transmission time after E clock				150	ns

Local bus/memory expansion mode, microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−40 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ.	Max	
$t_{d(\phi-A)}$	Address delay time after ϕ	Fig.40			150	ns
$t_{V(\phi-A)}$	Address effective time after ϕ		10			ns
$t_{V(RD-A)}$	Address effective time after $\overline{RD}$		10			ns
$t_{V(WR-A)}$	Address effective time after $\overline{WR}$		10			ns
$t_{d(\phi-D)}$	Data output delay time after ϕ				160	ns
$t_{d(WR-D)}$	Data output delay time after $\overline{WR}$				160	ns
$t_{V(\phi-D)}$	Data output effective time after ϕ		20			ns
$t_{V(WR-D)}$	Data output effective time after $\overline{WR}$		20			ns
$t_{d(\phi-RW)}$	R/$\overline{W}$ delay time after ϕ				150	ns
$t_{d(\phi-SYNC)}$	SYNC delay time after ϕ				150	ns
$t_{W(RD)}$	$\overline{RD}$ pulse width		170			ns
$t_{W(WR)}$	$\overline{WR}$ pulse width		170			ns

TEST CONDITION

Input voltage level : V_{IH} 2.4V
V_{IL} 0.45V
Output test level : V_{OH} 2.0V
V_{OL} 0.8V

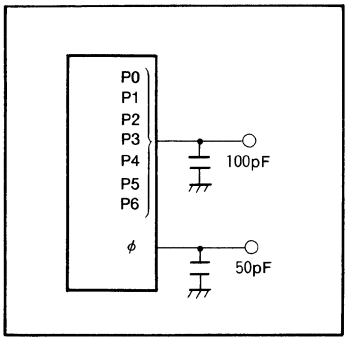


Fig. 1 Test circuit in single-chip mode

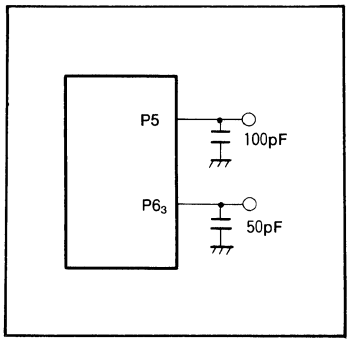


Fig. 2 Master CPU bus interface test circuit

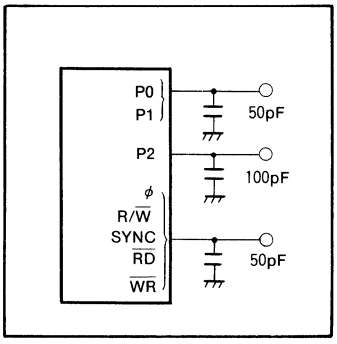


Fig. 3 Local bus test circuit

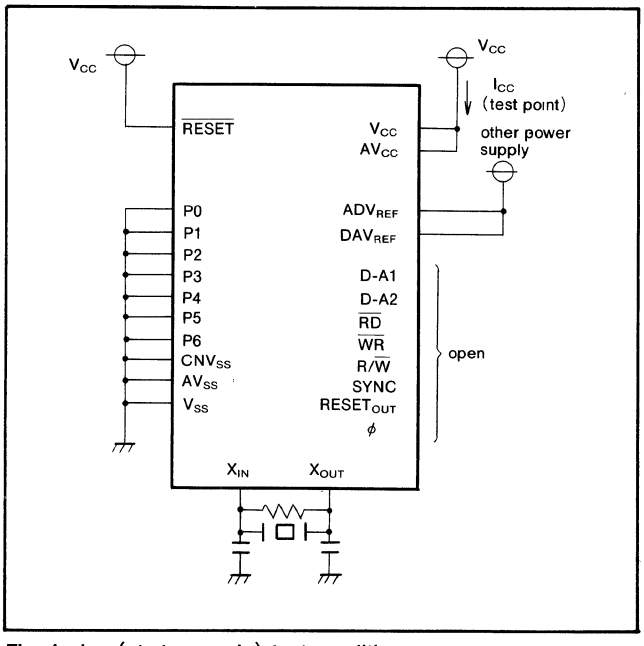
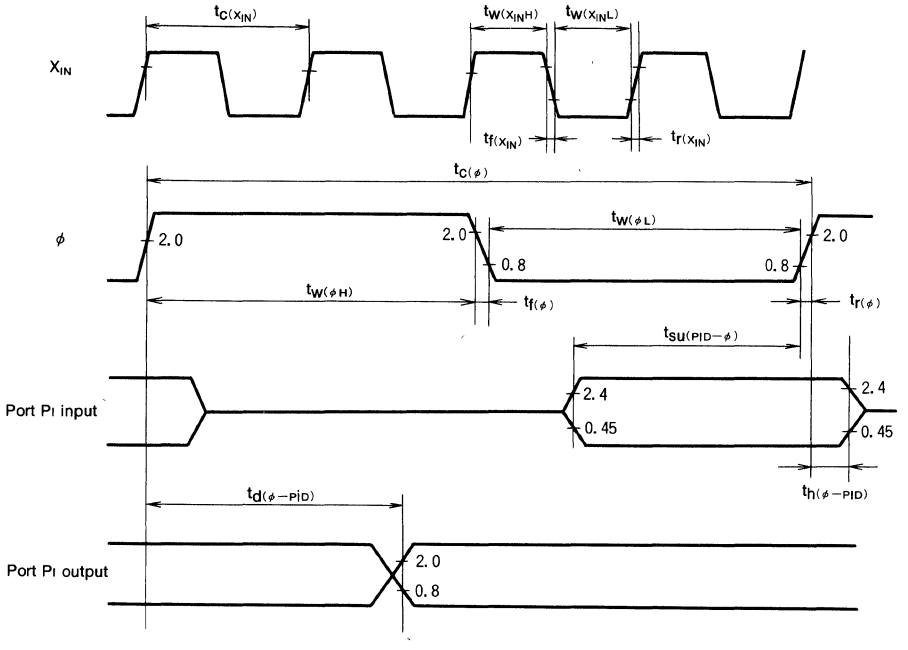


Fig. 4 I_{CC} (at stop mode) test condition

TIMING DIAGRAM

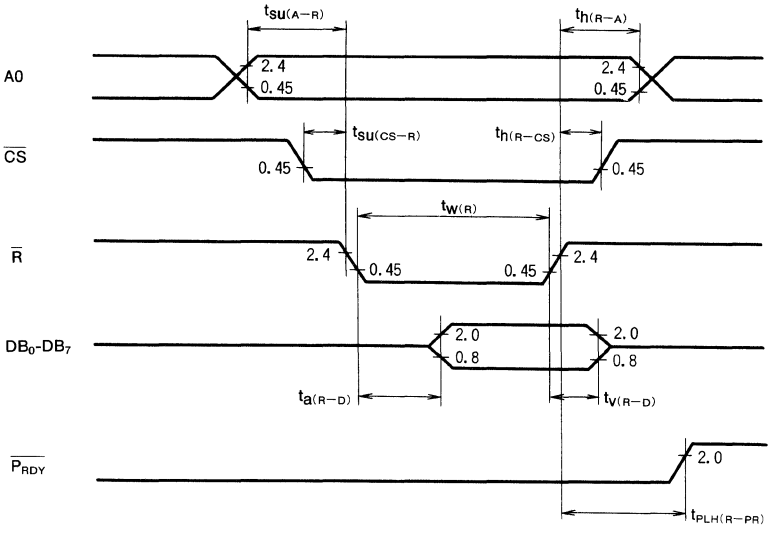
Port/single-chip mode timing diagram



Note : V_{IH}=0.8V_{CC}, V_{IL}=0.16V_{CC} of X_{IN}

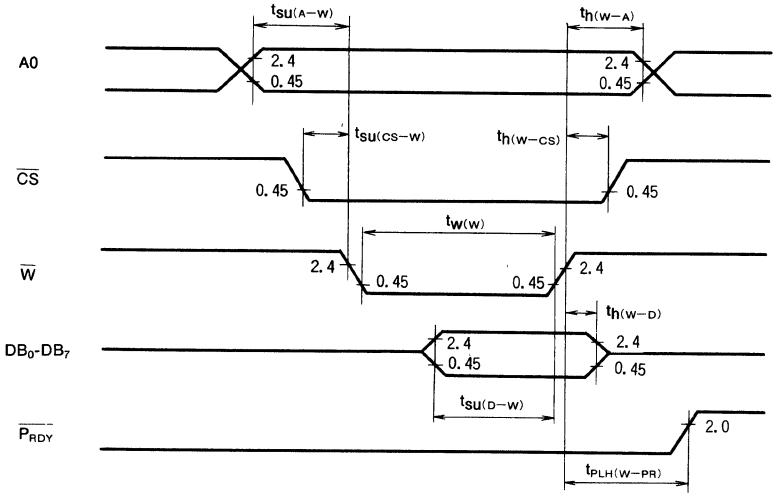
Master CPU bus interface/ $\overline{R}$ and $\overline{W}$ separation type timing diagram

Read

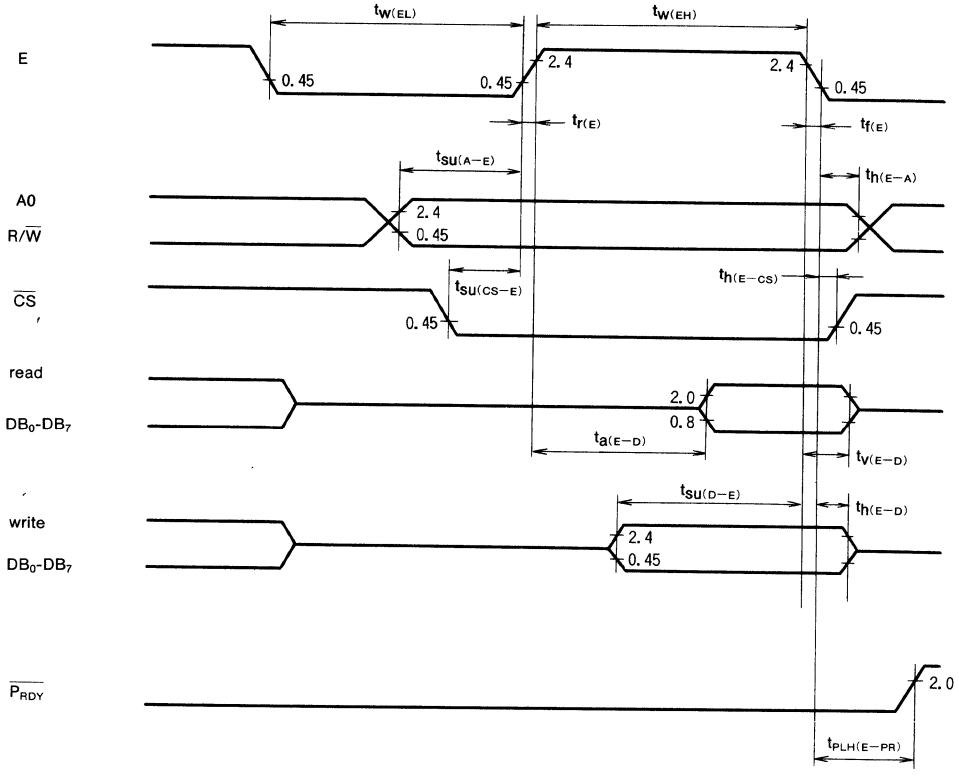


MITSUBISHI ELECTRIC

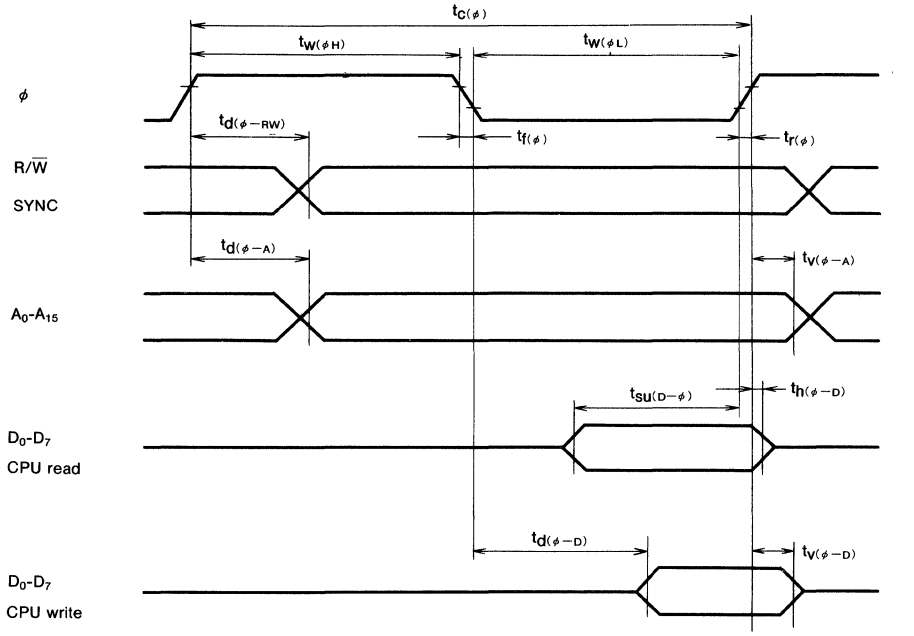
Write

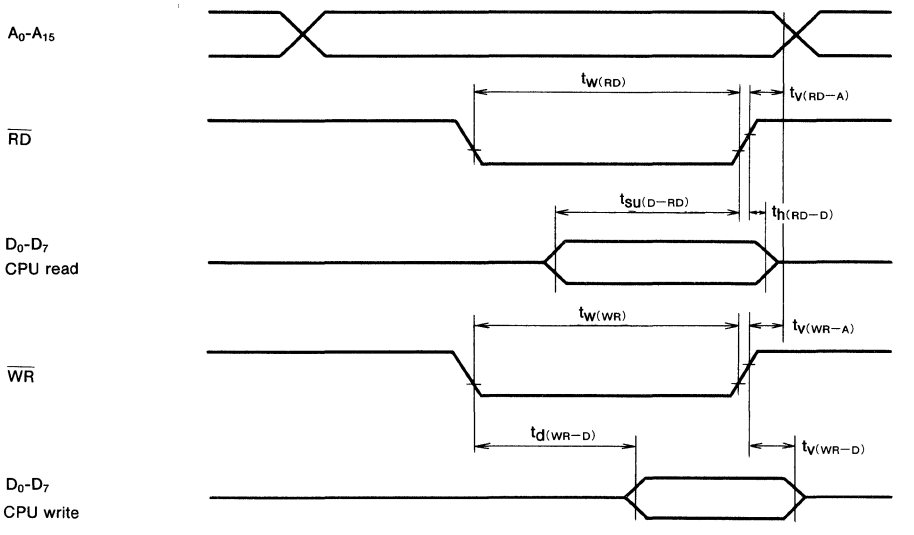


Master CPU interface/ R/$\overline{W}$ type timing diagram



Local bus timing diagram





MITSUBISHI ELECTRIC