M37450PFS

PIGGYBACK for M37450M2-XXXFP,M37450M4-XXXFP,M37450M8-XXXFP

DESCRIPTION

The M37450PFS is an EPROM mounted-type microcomputer employing a silicon gate CMOS process and was designed for developing programs for single-chip, 8-bit microcomputers M37450M2-XXXFP, M37450M4-XXXFP and M37450M8-XXXFP. The M37450PFS, being housed in a piggyback-type 80-pin plastic QFP is compatible with the M37450M2-XXXFP, M37450M4-XXXFP and M37450M8-XXXFP.

There is a 32-pin socket on the upper surface so that the outline is LCC-32C-A01 and 27C256 EPROM may be used.

The M37450PSS simplifies the development of programs for the M37450M2-XXXFP, M37450M4-XXXFP and M37450 M8-XXXFP and is excellent for making prototypes.

FEATURES

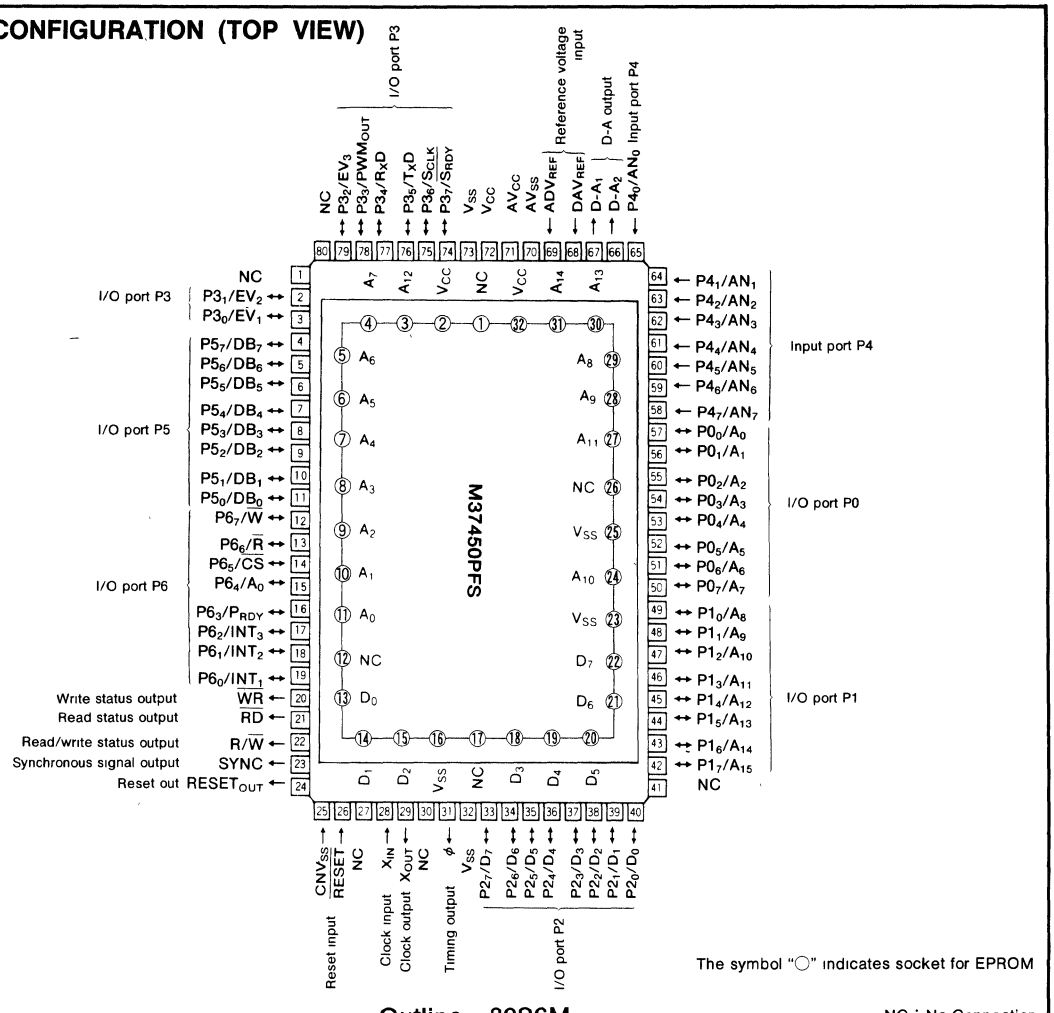
- Difference with the M37450M2-XXXFP, M37450M4-XXXFP and M37450M8-XXXFP is:
  (1) ROMless, EPROM is attached externally.
  (2) Suitable EPROM is that the outline is LCC-32C-A01 and 27C256

APPLICATION

Development of programs for the following systems:

- Slave controller for PPCs, facsimiles, and page printers
- HDD, optical disk, inverter, and industrial motor controllers
- Industrial robots and machines

PIN CONFIGURATION (TOP VIEW)



The symbol "○" indicates socket for EPROM

Outline 80S6M

NC : No Connection

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PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC} and 0V to V_{SS}
CNV_{SS}	CNV_{SS}		Controls the processor mode of the chip Normally connected to V_{SS} or V_{CC}
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 8 clock cycles (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit for main clock To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	Outputs signal consisting of oscillating frequency divided by four
SYNC	Synchronous signal output	Output	This signal is output "H" during operation code fetch and is used to control single stepping of programs
R/$\overline{W}$	Read/Write status output	Output	This signal determines the direction of the data bus It is "H" during read and "L" during write
$P0_0$-$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programed as input or output The output structure is CMOS output The low-order bits of the address are output except in single-chip mode
$P1_0$-$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same function as port P0 The high-order bits of the address are output except in single-chip mode
$P2_0$-$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same function as P0 Used as data bus except in single-chip mode
$P3_0$-$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same function as P0 Serial I/O, PWM output, or even I/O function can be selected with a program
$P4_0$-$P4_7$	Input port P4	Input	Analog input pin for the A-D converter They may also be used as digital input pins
$P5_0$-$P5_7$	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same function as P0 This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program
$P6_0$-$P6_7$	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same function as P0 Pins $P6_3$ to $P6_7$ change to control bus for the master CPU when slave mode is selected with a program Pins $P6_0$ to $P6_2$ may be programed as external interrupt input pins
$D\text{-}A_1$, $D\text{-}A_2$	D-A output	Output	Analog signal from D-A converter is output
ADV_{REF}	A-D refference voltage input	Input	Reference voltage input pin for A-D converter
DAV_{REF}	D-A refference voltage input	Input	Reference voltage input pin for D-A converter
AV_{SS}	Analog power supply		Ground level input pin for A-D and D-A converter
AV_{CC}	Analog power supply		Power supply input pin for A-D converter
$\overline{RD}$	Read signal output	Output	Control signal output as active "L" when vailed data is read from data bus
$\overline{WR}$	Write signal output	Output	Control signal output as active "L" when writing data from data bus to external component
$RESET_{OUT}$	Reset output	Output	Control signal output as active "H" during reset It is used as a reset output signal for perpheral components
A_0-A_{14}	Output port A	Output	Port A outputs the adresses to the EPROM mounted on the top of the package
D_0-D_7	Input port D	Input	Port D takes the input data from the EPROM mounted on the top of the package

EXPLANATION OF FUNCTION BLOCK OPERATION

The differences between the M37450PFS and the M37450M2-XXXFP, M37450M4-XXXFP and M37450M8-XXXFP are explained below. As all other points are the same, only the differences are explained.

MEMORY

Instead of an internal ROM, an EPROM is mounted. The addresses of EPROM are 8000_{16} to $FFFF_{16}$, having 32K bytes. Internal RAMs are provided from 0000_{16} to $00BF_{16}$ (192 bytes) and from 0100_{16} to $01FF_{16}$ (256 bytes) for a total of 448 bytes. However, the 64-byte area from $01C0_{16}$ to $01FF_{16}$ cannot be used when creating masked ROM. The rest of the functions are equivalent to the M37450M2-XXXFP, M37450M4-XXXFP and M37450M8-XXXFP.

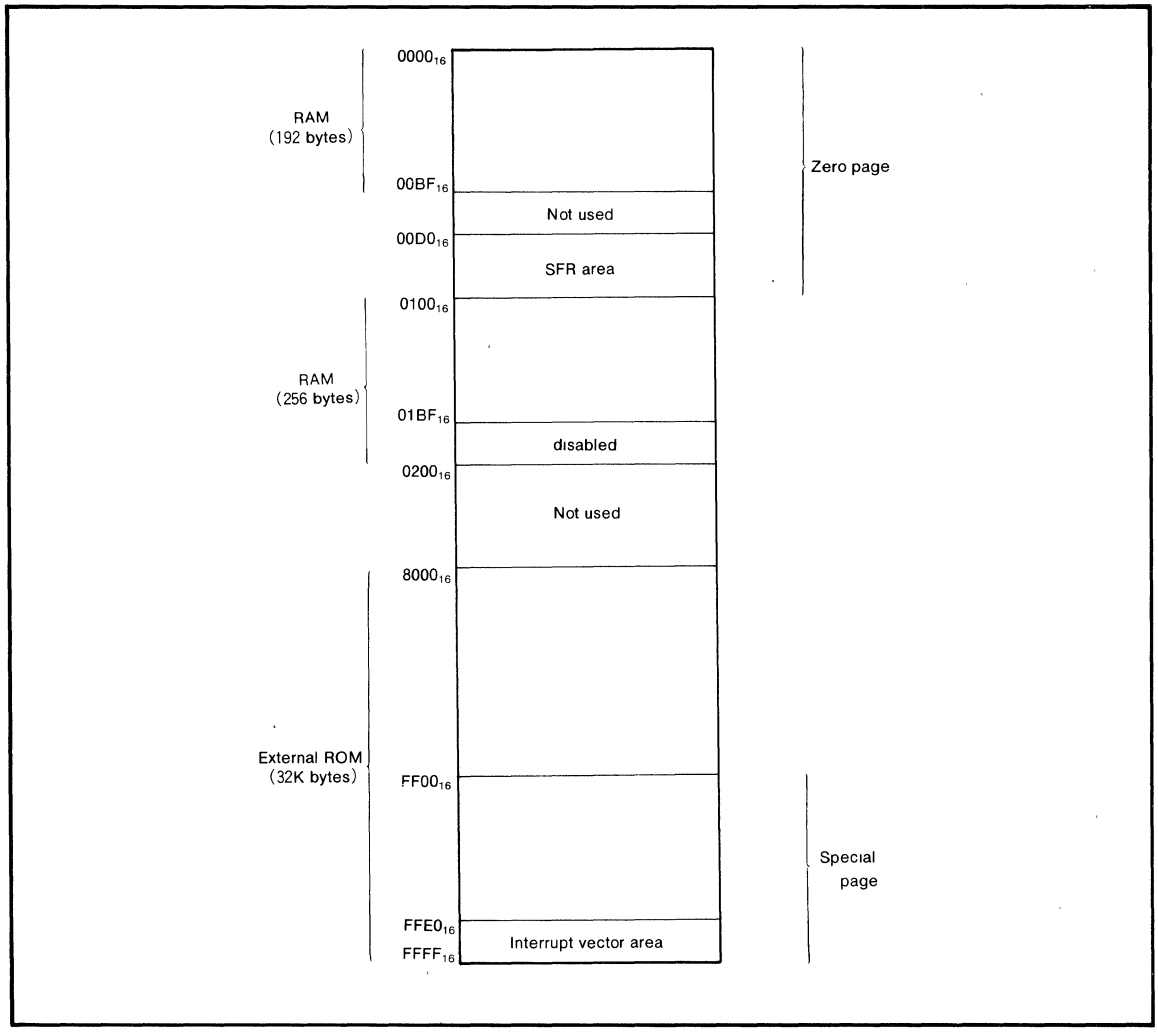

Fig. 1 Memory map

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$00D0_{16}$	Port P0 register
$00D1_{16}$	Port P0 directional register
$00D2_{16}$	Port P1 register
$00D3_{16}$	Port P1 directional register
$00D4_{16}$	Port P2 register
$00D5_{16}$	Port P2 directional register
$00D6_{16}$	Port P3 register
$00D7_{16}$	Port P3 directional register
$00D8_{16}$	Port P4 register
$00D9_{16}$	Reserved
$00DA_{16}$	Port P5 register
$00DB_{16}$	Port P5 directional register
$00DC_{16}$	Port P6 register
$00DD_{16}$	Port P6 directional register
$00DE_{16}$	MISRG1
$00DF_{16}$	MISRG2
$00E0_{16}$	D-A1 register
$00E1_{16}$	D-A2 register
$00E2_{16}$	A-D register
$00E3_{16}$	A-D control register
$00E4_{16}$	Data bus buffer register
$00E5_{16}$	Data bus buffer status register
$00E6_{16}$	Receive/transfer buffer register
$00E7_{16}$	Serial I/O status register

$00E8_{16}$	Serial I/O control register
$00E9_{16}$	UART control register
$00EA_{16}$	Baud rate generator
$00EB_{16}$	PWM register (lower-byte)
$00EC_{16}$	PWM register (higher-byte)
$00ED_{16}$	Timer 1 control register
$00EE_{16}$	Timer 2 control register
$00EF_{16}$	Timer 3 control register
$00F0_{16}$	Timer 1 register (lower-byte)
$00F1_{16}$	Timer 1 register (higher-byte)
$00F2_{16}$	Timer 1 latch (lower-byte)
$00F3_{16}$	Timer 1 latch (higher-byte)
$00F4_{16}$	Timer 2 register (lower-byte)
$00F5_{16}$	Timer 2 register (higher-byte)
$00F6_{16}$	Timer 2 latch (lower-byte)
$00F7_{16}$	Timer 2 latch (higher-byte)
$00F8_{16}$	Timer 3 register (lower-byte)
$00F9_{16}$	Timer 3 register (higher-byte)
$00FA_{16}$	Timer 3 latch (lower-byte)
$00FB_{16}$	Timer 3 latch (higher-byte)
$00FC_{16}$	Interrupt request register 1
$00FD_{16}$	Interrupt request register 2
$00FE_{16}$	Interrupt control register 1
$00FF_{16}$	Interrupt control register 2

Fig. 2 SFR (Special Function Register) memory map

PROCESSOR MODE

External memory area differs from the M37450M2-XXXFP, M37450M4-XXXFP and M37450M8-XXXFP.

Figure 3 shows the external memory area when the M37450PFS is in the memory expanding mode and Figure 4 shows the external memory area when the M37450PFS is in the microprocessor mode.

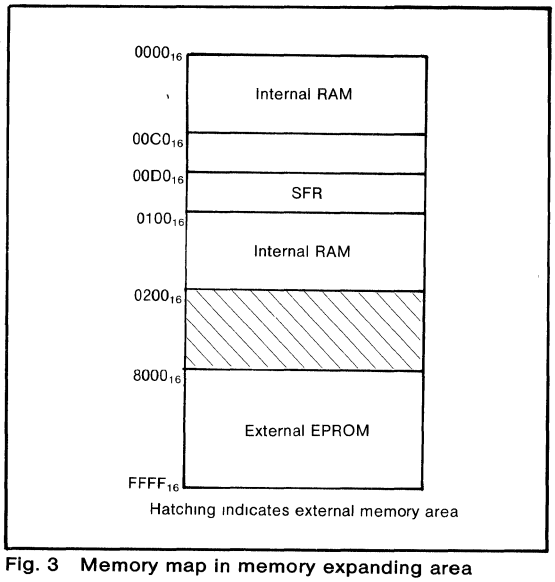

Fig. 3 Memory map in memory expanding area

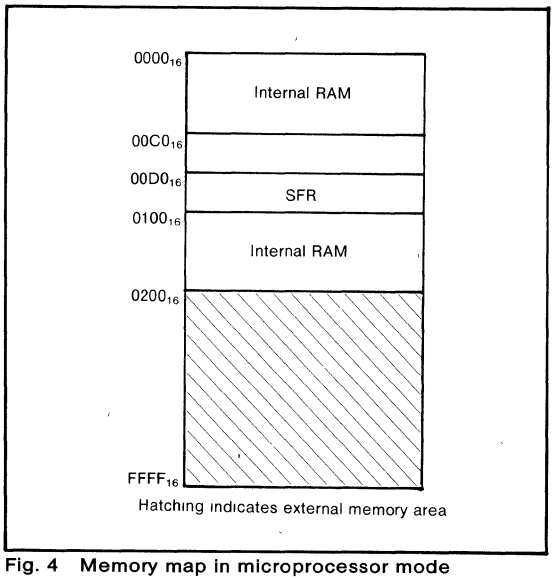

Fig. 4 Memory map in microprocessor mode

PRECAUTION FOR USE

(1) Program area

When developing programs on the M37450PFS, the ROM and sizes of the M37450M2-XXXFP, M37450M4-XXXFP, and M37450M8-XXXFP must be considered.

For the M37450M2-XXXFP, use the M37450PFS ROM program area from $F000_{16}$ to $FFFF_{16}$. (Write the program from 7000_{16} to $7FFF_{16}$ on the EPROM.)

Also, when creating masked ROMs, note that the RAM area for the M37450M2-XXXFP is 128 bytes from 0000_{16} to $0007F_{16}$.

For the M37450M4-XXXFP, use the M37450PFS ROM program area from $E000_{16}$ to $FFFF_{16}$. (Write the program from 6000_{16} to $7FFF_{16}$ on the EPROM.)

Also, when creating masked ROMs, note that the RAM area for the M37450M4-XXXFP is 192 bytes from 0000_{16} to $00BF_{16}$ and 64 bytes from 0100_{16} to $013F_{16}$ for a total of 256 bytes.

For the M37450M8-XXXFP, use the M37450PFS ROM program area from $C000_{16}$ to $FFFF_{16}$. (Write the program from 4000_{16} to $7FFF_{16}$ on the EPROM.)

Also, when creating masked ROMs, note that the RAM area for the M37450M8-XXXFP is 192 bytes from 0000_{16} to $00BF_{16}$ and 192 bytes from 0100_{16} to $01BF_{16}$ for a total of 384 bytes.

The 64 byte area from $01C0_{16}$ to $01FF_{16}$ can also be used as internal RAM. However, it cannot be used when creating masked ROMs because there is no corresponding device.

(2) External memory

When developing programs, note that the external memory area of the M37450PFS is as described in the previous section.

(3) EPROM orientation

Figure 5 shows the orientation when mountting the LCC type EPROM on the M37450PFS. Insert the EPROM firmly until it hits bottom.

PIGGYBACK for M37450M2-XXXFP,M37450M4-XXXFP,M37450M8-XXXFP

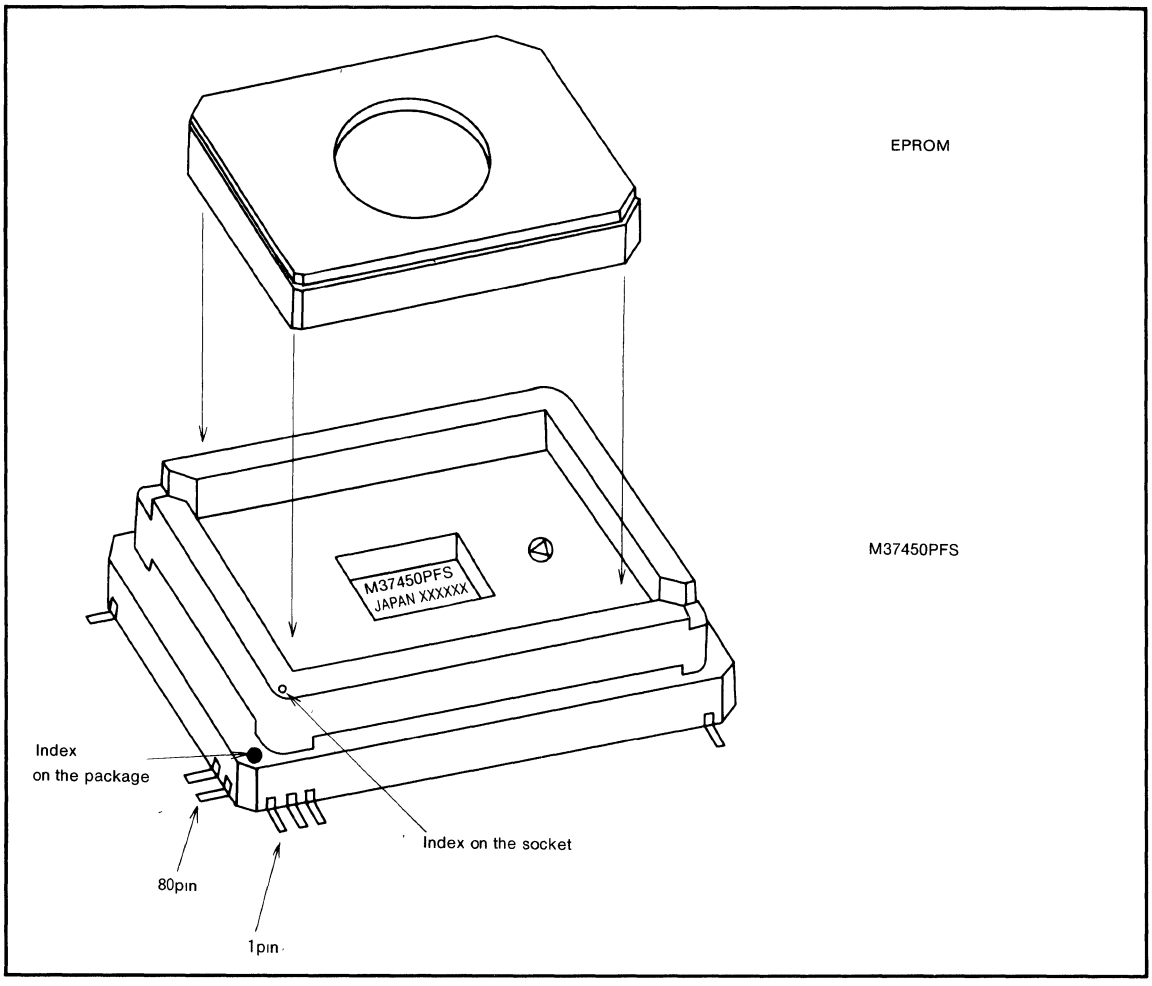

Fig. 5 EPROM orientation

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state	−0.3 to 7	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0.3 to 7	V
V_I	Input voltage, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, ADV_{RFF}, DAV_{RFF}, AV_{CC}		−0.3 to V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3 to 13	V
V_O	Output voltage, $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, X_{OUT}, ϕ, $\overline{RD}$, $\overline{WR}$, $RESET_{OUT}$, SYNC		−0.3 to V_{CC}+0.3	V
Pd	Power dissipation	T_a=25℃	500	mW
T_{opr}	Operating temperature		−10 to 70	℃
T_{stg}	Storage temperature		−40 to 125	℃

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 5V±10%, T_a = −10 to 70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, CNV_{SS} (Note1)	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (except Note1)	2.0		V_{CC}	V
V_{IL}	"L" input voltage CNV_{SS} (Note1)	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (except Note1)	0		0.8	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note2)			5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			−10	mA
$I_{OH(avg)}$	"H" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note2)			−5	mA
$f(X_{IN})$	Clock oscillating frequency	1		10	MHz

Note 1 : Ports operate as INT_1-INT_3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_XD($P3_4$)and S_{CLK}($P3_6$)
2 : The average output current $I_{OH(avg)}$ and $I_{OL(avg)}$ are the average value during a 100ms
3 : The total of "L" output $I_{OL(peak)}$ of port P0, P1 and P2 is 40mA max
The total of "H" output $I_{OH(peak)}$ of port P0, P1 and P2 is 40mA max.
The total of "L" output $I_{OL(peak)}$ of port P3, P5, P6, R/$\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is 40mA max.
The total of "H" output $I_{OH(peak)}$ of port P3, P5, P6, R/$\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is 40mA max

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = −10 to 70℃, f(X_{IN}) = 10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	"H" output $\overline{RD}$, $\overline{WR}$, SYNC, $RESET_{OUT}$, ϕ	I_{OH}=−2mA	V_{CC}−1			V
V_{OH}	"H" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	I_{OH}=−5mA	V_{CC}−1			V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, R/$\overline{W}$, $\overline{RD}$, $\overline{WR}$, SYNC, $RESET_{OUT}$, ϕ	I_{OL}=2mA			0.45	V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	I_{OL}=5mA			1	V
$V_{T+}-V_{T-}$	Hysterisis INT_1-INT_3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_XD($P3_4$), S_{CLK}($P3_6$)	Function input level	0.3		1	V
$V_{T+}-V_{T-}$	Hysterisis $\overline{RESET}$				0.7	V
$V_{T+}-V_{T-}$	Hysterisis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	V_I=V_{SS}	−5		5	μA
I_{IH}	"H" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	V_I=V_{CC}	−5		5	μA
V_{RAM}	RAM retention voltage	At stop mode	2			V
I_{CC}	Supply current	At system operation f(X_{IN})=10MHz(Note 1)		6	10	mA

Note 1 : Only for M37450PFS (not contact in EPROM dissipation current)

A-D CONVERTER CHARACTERISTICS (V_{CC}=AV_{CC}=5V, V_{SS}=AV_{SS}=0V, T_a=25℃, f(X_{IN})=10MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=AV_{CC}=ADV_{REF}=5.12V		±1.5	±3	LSB
t_{CONV}	Conversion time				49	$t_C(\phi)$
V_{IA}	Analog input voltage		AV_{SS}		AV_{CC}	V
V_{ADVREF}	Reference analog input voltage		2		V_{CC}	V
R_{LADDER}	Ladder resistance value	ADV_{REF}=5V	2	7.5	10	kΩ
$I_{IADVREF}$	Reference analog input current	ADV_{REF}=5V	0.5	0.7	2.5	mA
V_{AVCC}	Analog power input			V_{CC}		V
V_{AVSS}	Analog power input			0		V

D-A CONVERTER CHARACTERISTICS (V_{CC} = 5V, V_{SS} = AV_{SS} = 0V, T_a = 25℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=DAV_{REF}=5.12V			1.0	%
t_{SU}	Setup time				3	μs
R_O	Output resistance		1	2	4	kΩ
V_{AVSS}	Analog power input			0		V
V_{DAVREF}	Analog power input		4		V_{CC}	V
I_{DAVREF}	Reference power input current (Each pin)		0	2.5	5	mA