M37451M4-XXXSP/FP/GP
M37451M8-XXXSP/FP/GP
M37451MC-XXXSP/FP/GP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37451M4-XXXSP/FP/GP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP or a 0.8mm-pitch or 0.65mm-pitch 80-pin plastic molded QFP.

In addition to its simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

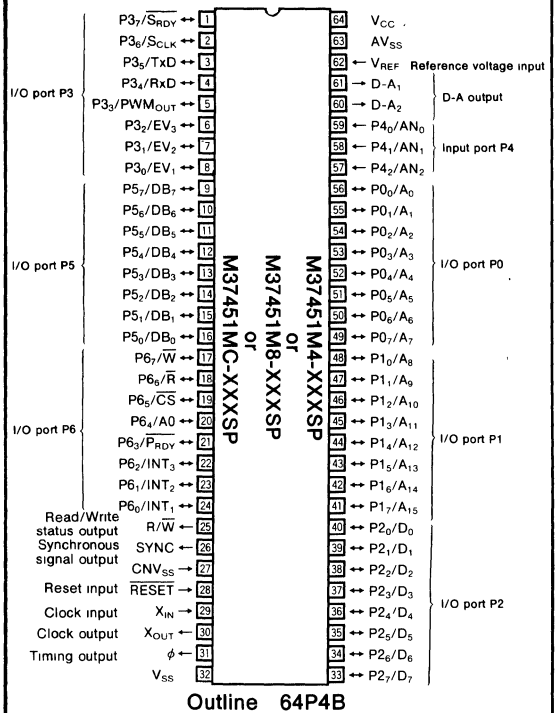
It is suited for office automation equipment and control devices The low power consumption made by the use of a CMOS process makes it especially suitable for battery powered devices requiring low power consumption. It also has a unique feature that enables it to be used as a slave microcomputer.

The differences among M37451M4-XXXSP/FP/GP, M37451M8-XXXSP/FP/GP and M37451MC-XXXSP/FP/GP are as shown below. The descriptions that follow describe the M37451M4-XXXSP/FP/GP (abbreviated as M37451) unless otherwise noted.

Type name	ROM size	RAM size
M37451M4-XXXSP/FP/GP	8192 bytes	256 bytes
M37451M8-XXXSP/FP/GP	16384 bytes	384 bytes
M37451MC-XXXSP/FP/GP	24576 bytes	512 bytes

The number of analog input pins for the 80-pin model (FP, GP version) is different from the 64-pin model (SP version). In addition, the 80-pin model has special pins for $\overline{RD}$, $\overline{WR}$, $RESET_{OUT}$, DAV_{REF}, ADV_{REF}, AV_{CC} and the 64-pin model has a special V_{REF} pin.

PIN CONFIGURATION (TOP VIEW)



Outline 64P4B

FEATURES

- Number of basic instructions 71
  69 MELPS 740 basic instructions+2 multiply/divide instructions
- Instruction execution time
  (minimum instructions at 12.5MHz frequency) 0.64μs
- Single power supply ..... 5V±10%
- Power dissipation normal operation mode
  (at 12.5MHz frequency) 40mW
- Subroutine nesting ..... 96 levels max.(M37451M4)
  96 levels max.(M37451M8)
  128 levels max.(M37451MC)
- Interrupt ..... 15 events
- Master CPU bus interface ..... 1 byte
- 16-bit timer 3
- 8-bit timer (Serial I/O use) 1
- Serial I/O (UART or clock synchronous) 1
- A-D converter (8-bit resolution) ..... 3 channels (DIP)
  8 channels (QFP)
- D-A converter (8-bit resolution) ..... 2 channels
- PWM output with 8-bit prescaler
  (Either resolution 8 bit or 16 bit is software selectable) 1
- Programmable I/O ports
  (Ports P0, P1, P2, P3, P5, P6) 48
- Input port (Port P4) ..... 3(DIP), 8(QFP)
- Output ports (Ports $D\text{-}A_1$, $D\text{-}A_2$) 2

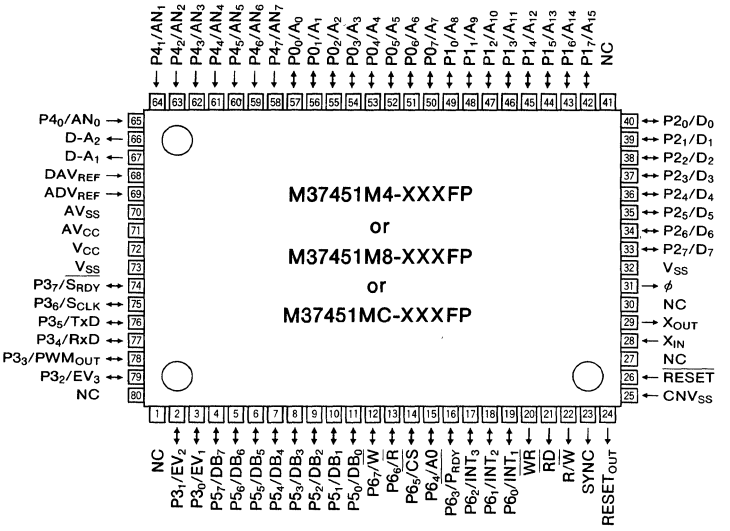
APPLICATION

Slave controller for PPCs, facsimiles, and page printers. HDD, optical disk, inverter, and industrial motor controllers. Industrial robots and machines.

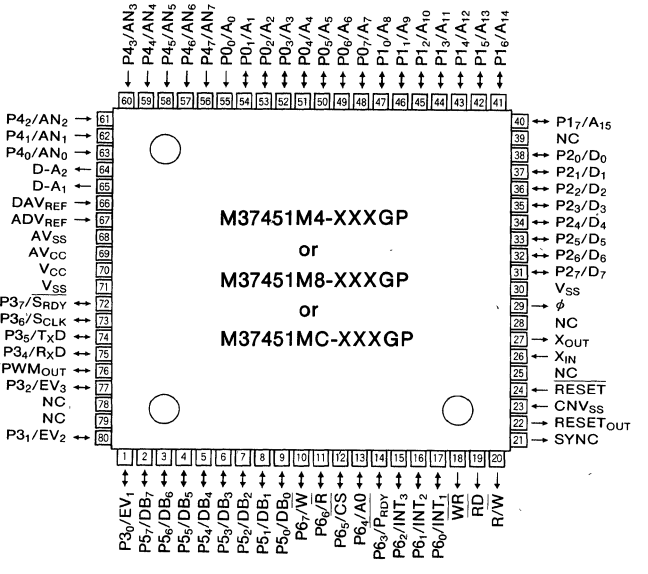
M37451M4-XXXSP/FP/GP, M37451M8-XXXSP/FP/GP M37451MC-XXXSP/FP/GP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

PIN CONFIGURATION (TOP VIEW)



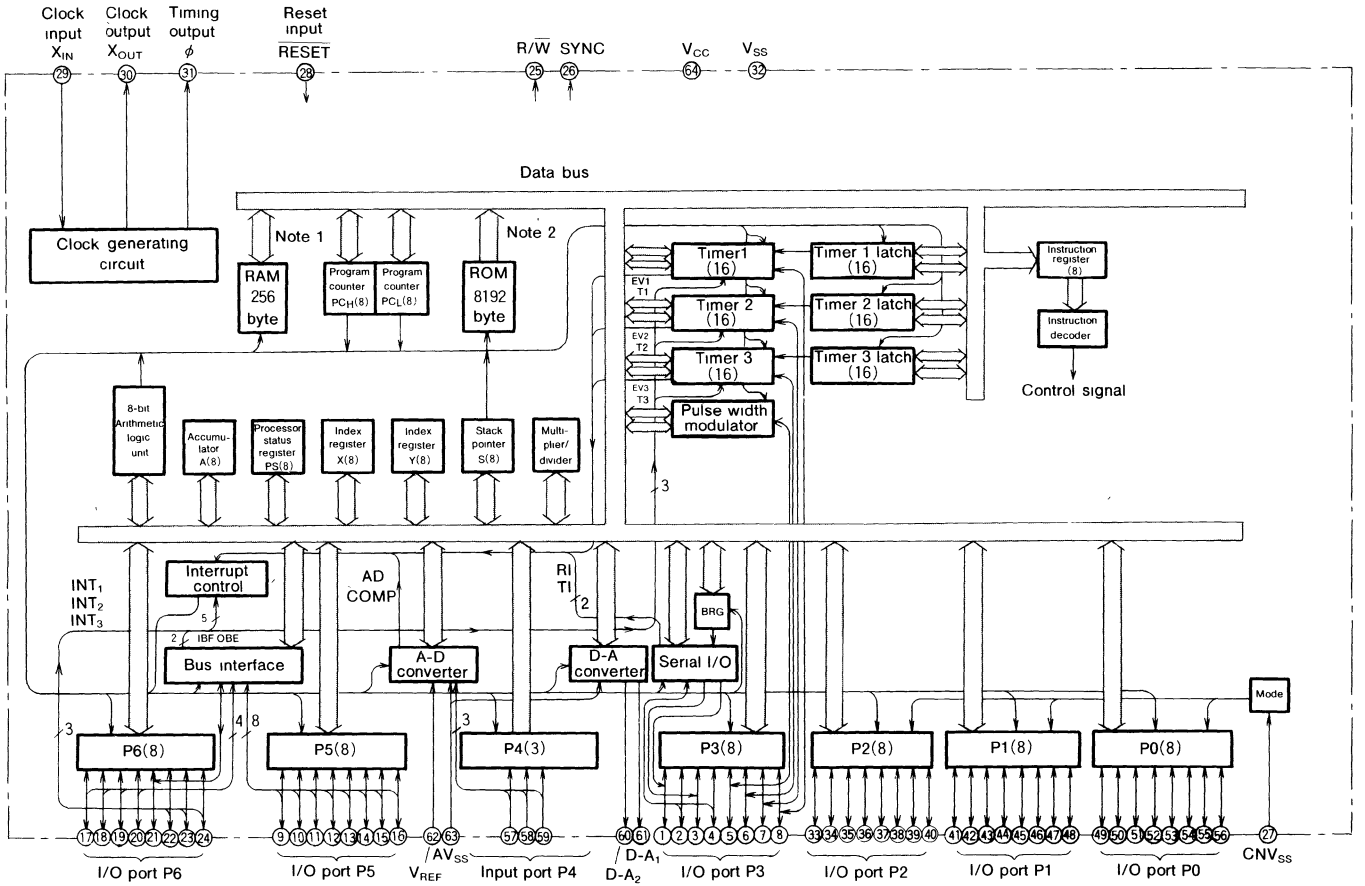
Outline 80P6N



Outline 80P6S

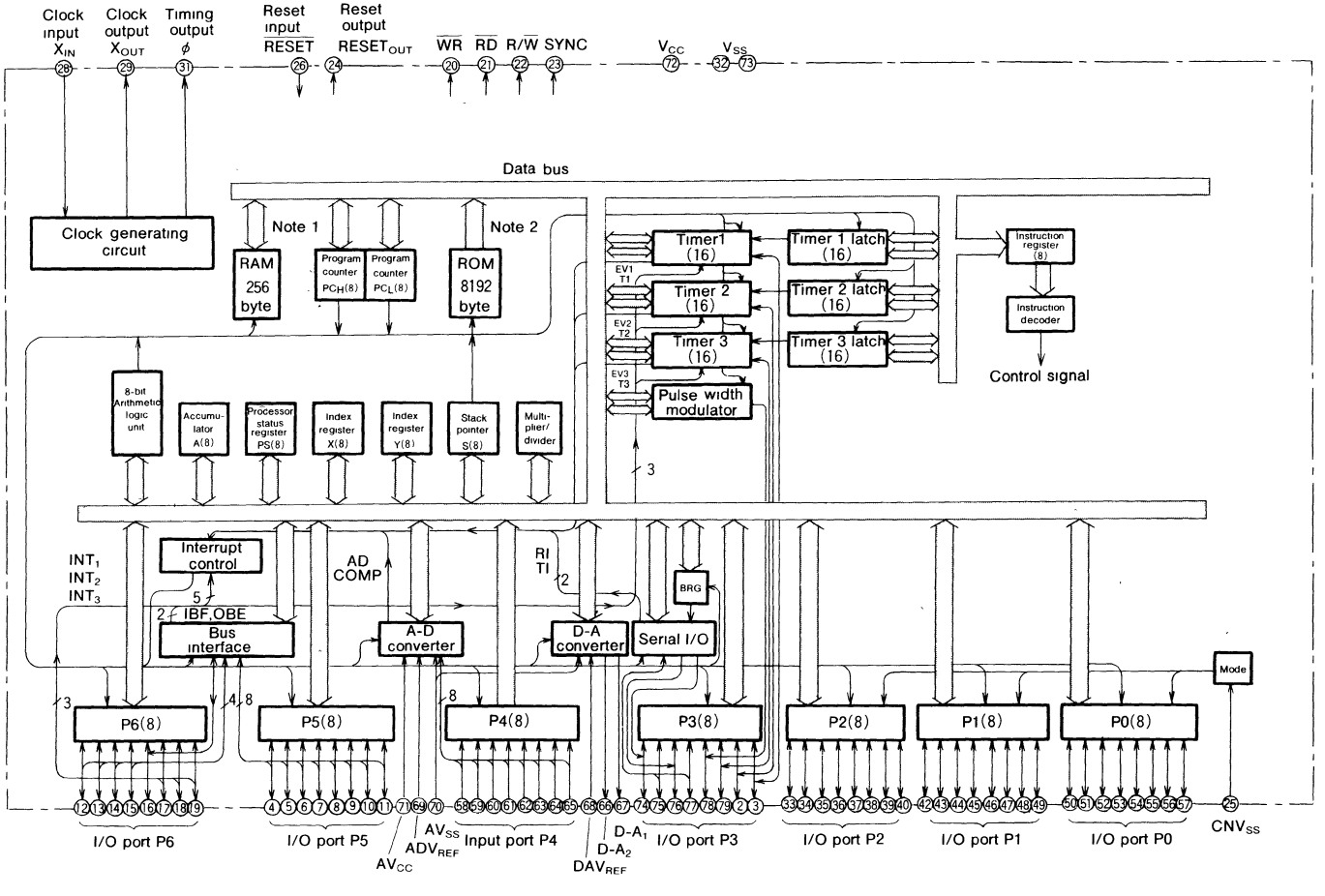
NC : No connection

M37451M4-XXXSP BLOCK DIAGRAM



Note 1 : 384 bytes for M37451M8-XXXSP and 512 bytes for M37451MC-XXXSP
2 : 16384 bytes for M37451M8-XXXSP and 24576 bytes for M37451MC-XXXSP

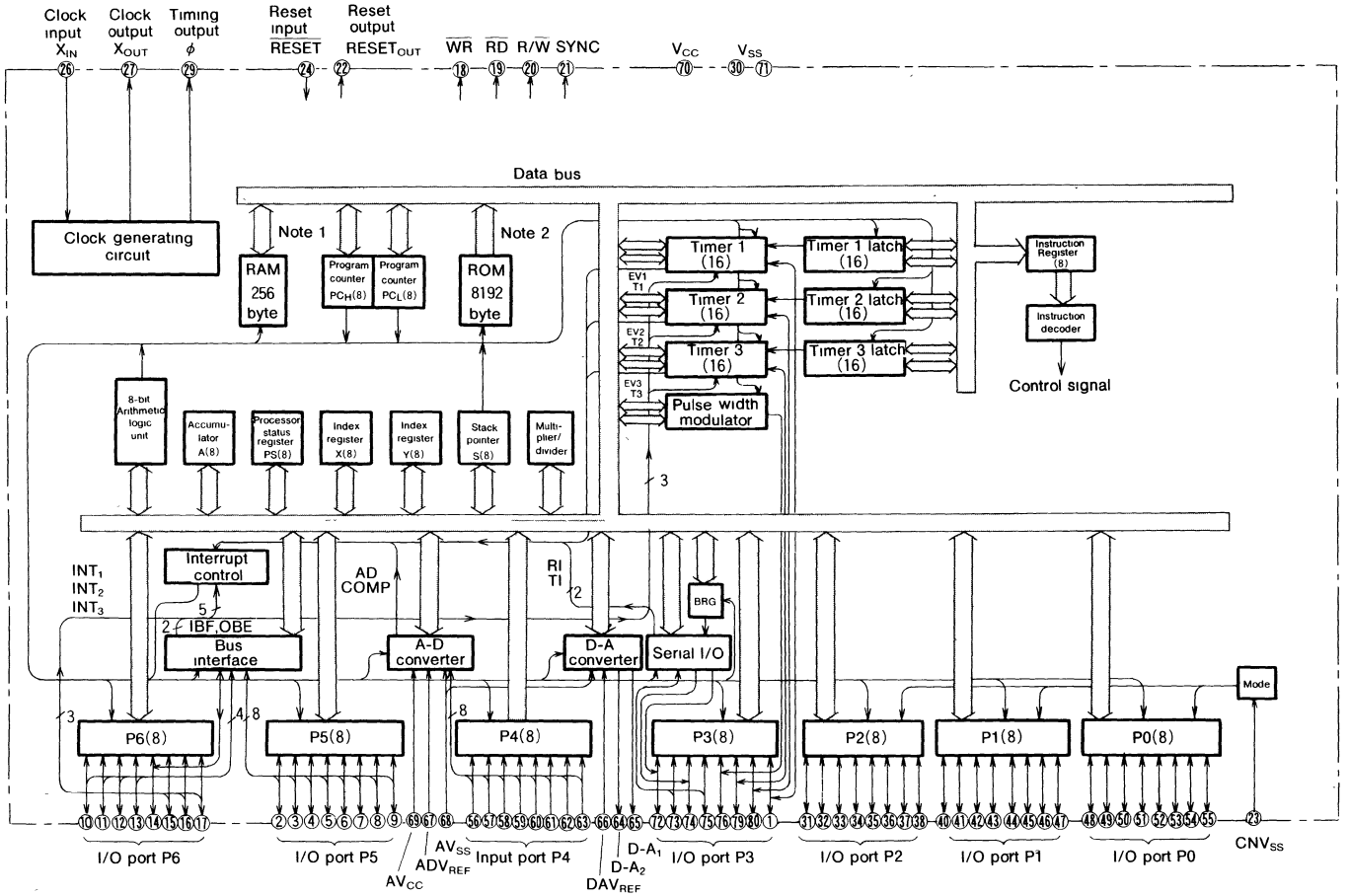
M37451M4-XXXFP BLOCK DIAGRAM



Note 1 : 384 bytes for M37451M8-XXXFP and 512 bytes for M37451MC-XXXFP
2 : 16384 bytes for M37451M8-XXXFP and 24576 bytes for M37451MC-XXXFP

MITSUBISHI ELECTRIC

M37451M4-XXXGP BLOCK DIAGRAM



Note 1 : 384 bytes for M37451M8-XXXGP and 512 bytes for M37451MC-XXXGP
2 : 16384 bytes for M37451M8-XXXGP and 24576 bytes for M37451MC-XXXGP

MITSUBISHI ELECTRIC

FUNCTIONS OF M37451M4-XXXSP/FP/GP, M37451M8-XXXSP/FP/GP, M37451MC-XXXSP/FP/GP

Parameter			Functions
Number of basic instructions			71 (69 MELPS 740 basic instructions+2)
Instruction execution time			0.64μs (minimum instructions, at 12.5MHz frequency)
Clock frequency			12.5MHz (max.)
Memory size	M37451M4-XXXSP/FP/GP	ROM	8192 bytes
		RAM	256 bytes
	M37451M8-XXXSP/FP/GP	ROM	16384 bytes
		RAM	384 bytes
	M37451MC-XXXSP/FP/GP	ROM	24576 bytes
		RAM	512 bytes
Input/Output ports	P0-P3, P5, P6	I/O	8-bit×6
	P4	Input	3-bit×1 (8-bit×1 for 80-pin model)
	D-A	Output	2-bit×1
Serial I/O			UART or clock synchronous
Timers			16-bit timer×3, 8-bit timer (serial I/O baud rate generator)×1
A-D converter			8-bit×3 channels (8 channels for 80-pin model)
D-A converter			8-bit×2 channels
Pulse width modulator with 8-bit prescaler			8-bit or 16-bit×1
Data bus buffer			1-byte input and output each
Subroutine nesting			96-levels (max. for M37451M4, M37451M8)
			128-levels (max. for M37451MC)
Interrupt			6 external interrupts, 8 internal interrupts 1 software interrupt
Clock generating circuit			Built-in (ceramic or quarts crystal oscillator)
Supply voltage			5V±10%
Power dissipation			40mW (at 12.5MHz frequency)
Input/Output characters	Input/Output voltage		5V
	Output current		±5mA (max.)
Memory expansion			Possible (64K bytes max.)
Operating temperature range			−20 to 85°C
Device structure			CMOS silicon gate
Package	M37451M4-XXXSP		64-pin shrink plastic molded DIP
	M37451M8-XXXSP		
	M37451MC-XXXSP		
	M37451M4-XXXFP		80-pin plastic molded QFP (0.8mm-pitch)
	M37451M8-XXXFP		
	M37451MC-XXXFP		
	M37451M4-XXXGP		80-pin plastic molded QFP (0.65mm-pitch)
	M37451M8-XXXGP		
	M37451MC-XXXGP		

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}
CNV_{SS}	CNV_{SS}	Input	Controls the processor mode of the chip Normally connected to V_{SS} or V_{CC}
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 8 clock cycles (under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	Normally outputs signal consisting of oscillating frequency divided by four
SYNC	Synchronous signal output	Output	This signal is output "H" during operation code fetch and is used to control single stepping of programs
R/$\overline{W}$	Read/Write status output	Output	This signal determines the direction of the data bus It is "H" during read and "L" during write
$P0_0$-$P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output The output structure is CMOS output The low-order bits of the address are output except in single-chip mode
$P1_0$-$P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0 The high-order bits of the address are output except in single-chip mode
$P2_0$-$P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0 Used as data bus except in single-chip mode
$P3_0$-$P3_7$	I/O port P3	I/O	Port P3 is an 8-bit I/O port and has basically the same functions as port P0 Serial I/O, PWM output, or event I/O function can be selected with a program
$P4_0$-$P4_2$ ($P4_0$-$P4_7$)	Input port P4	Input	Analog input pin for the A-D converter The 64-pin model has three pins and the 80-pin model has eight pins They may also be used as digital input pins
$P5_0$-$P5_7$	I/O port P5	I/O	Port P5 is an 8-bit I/O port and has basically the same functions as port P0 This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program
$P6_0$-$P6_7$	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same function as port P0 Pins $P6_3$-$P6_7$ change to a control bus for the master CPU when slave mode is selected with a program Pins $P6_0$-$P6_2$ may be programmed as external interrupt input pins
D-A_1, D-A_2	D-A output	Output	Analog signal from D-A converter is output
V_{REF}	Reference voltage input	Input	Reference voltage input pin for A-D and D-A converter This pin is for 64-pin model only
ADV_{REF}	A-D reference voltage input	Input	Reference voltage input pin for A-D converter This pin is for 80-pin model only
DAV_{REF}	D-A reference voltage input	Input	Reference voltage input pin for D-A converter This pin is for 80-pin model only
AV_{SS}	Analog power supply		Ground level input pin for A-D and D-A converter Same voltage as V_{SS} is applied
AV_{CC}	Analog power supply		Power supply input pin for A-D converter This pin is for 80-pin model only Same voltage as V_{CC} is applied. In the case of the 64-pin model, AV_{CC} is connected to V_{CC} internally
$\overline{RD}$	Read signal output	Output	Control signal output as active "L" when valid data is read from data bus This pin is for 80-pin model only.
$\overline{WR}$	Write signal output	Output	Control signal output as active "L" when writing data from data bus to external component This pin is for 80-pin model only
$RESET_{OUT}$	Reset output	Output	Control signal output as active "H" during reset It is used as a reset output signal for peripheral components This pin is for 80-pin model only

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The M37451 microcomputers use the standard MELPS 740 instruction set. For details of instructions, refer to the MELPS 740 CPU core basic functions, or the MELPS 740 Software Manual.

Machine-resident instructions are as follows:

The FST and SLW instructions are not provided.

The MUL and DIV instructions can be used.

The WIT instruction can be used.

The STP instruction can be used.

MISRG2 Register

The MISRG2 register is allocated to address $00DF_{16}$. Bits 0 and 1 of this register are processor mode bits. This register also has a stack page selection bit.

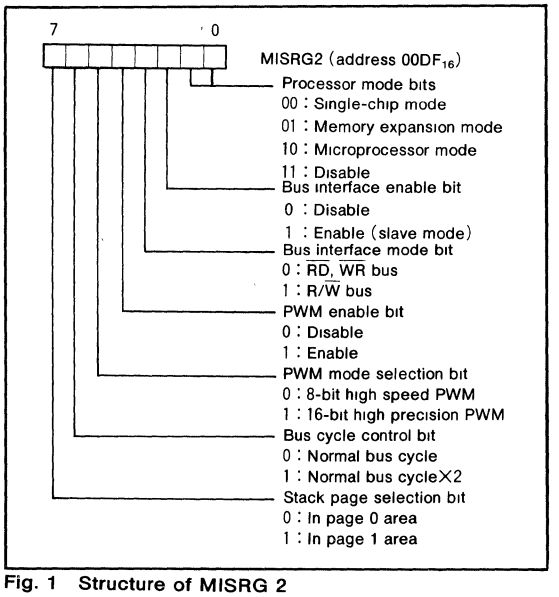


Fig. 1 Structure of MISRG 2

MEMORY

• Special Function Register (SFR) Area

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• RAM

RAM is used for data storage as well as a stack area.

• ROM

ROM is used for storing user programs as well as the interrupt vector area.

• Interrupt Vector Area

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated.

• Zero Page

Zero page addressing mode is useful because it enables access to this area with only 2 bytes.

• Special Page

Special page addressing mode is useful because it enables access to this area with only 2 bytes.

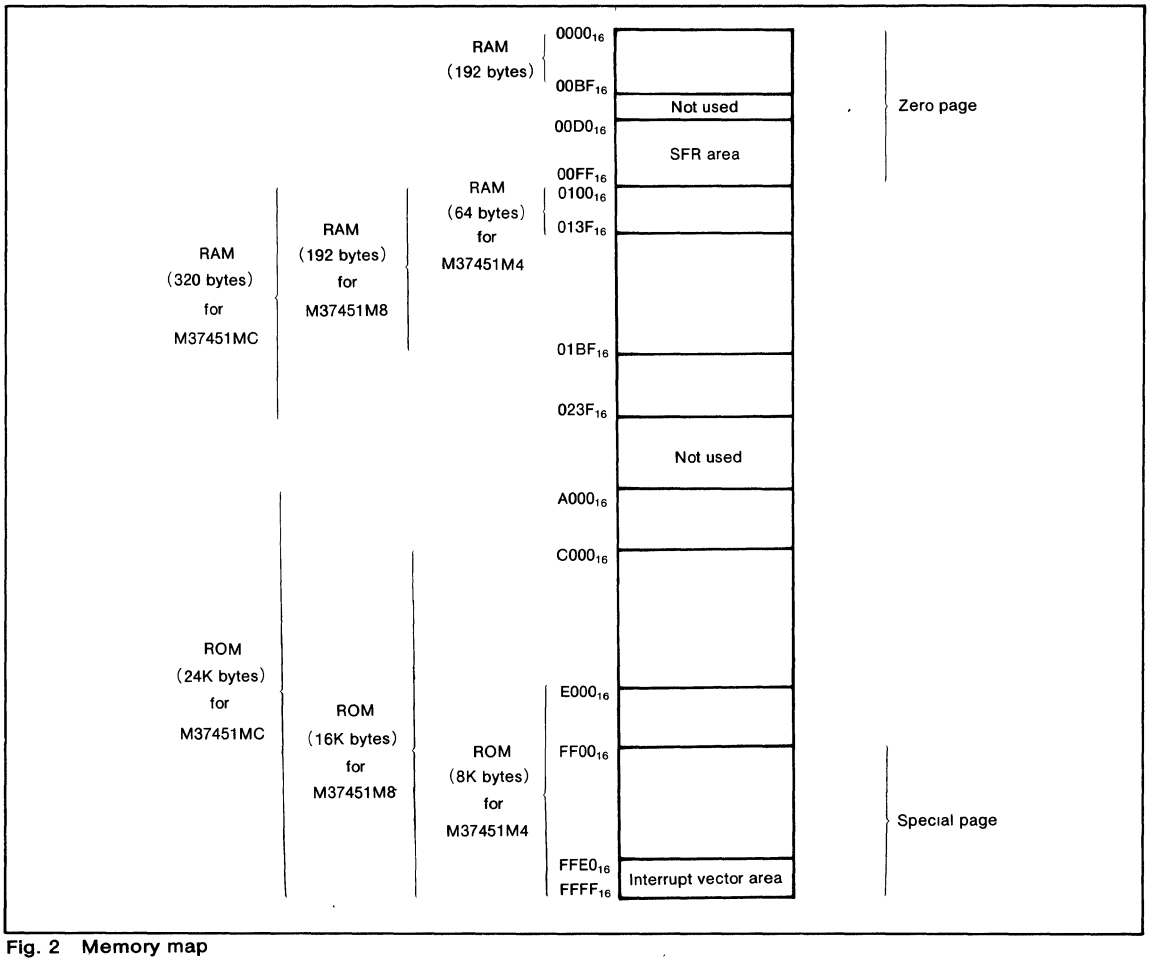


Fig. 2 Memory map

$00D0_{16}$	P0 register
$00D1_{16}$	P0 directional register
$00D2_{16}$	P1 register
$00D3_{16}$	P1 directional register
$00D4_{16}$	P2 register
$00D5_{16}$	P2 directional register
$00D6_{16}$	P3 register
$00D7_{16}$	P3 directional register
$00D8_{16}$	P4 register/PWM prescaler latch
$00D9_{16}$	Additional function register
$00DA_{16}$	P5 register
$00DB_{16}$	P5 directional register
$00DC_{16}$	P6 register
$00DD_{16}$	P6 directional register
$00DE_{16}$	MISRG1
$00DF_{16}$	MISRG2
$00E0_{16}$	D-A1 register
$00E1_{16}$	D-A2 register
$00E2_{16}$	A-D register
$00E3_{16}$	A-D control register
$00E4_{16}$	Data bus buffer register
$00E5_{16}$	Data bus buffer status register
$00E6_{16}$	Receive/Transmit buffer register
$00E7_{16}$	Serial I/O status register
$00E8_{16}$	Serial I/O control register
$00E9_{16}$	UART control register
$00EA_{16}$	Baud rate generator

$00EB_{16}$	PWM register (low-order)
$00EC_{16}$	PWM register (high-order)
$00ED_{16}$	Timer 1 control register
$00EE_{16}$	Timer 2 control register
$00EF_{16}$	Timer 3 control register
$00F0_{16}$	Timer 1 register (low-order)
$00F1_{16}$	Timer 1 register (high-order)
$00F2_{16}$	Timer 1 latch (low-order)
$00F3_{16}$	Timer 1 latch (high-order)
$00F4_{16}$	Timer 2 register (low-order)
$00F5_{16}$	Timer 2 register (high-order)
$00F6_{16}$	Timer 2 latch (low-order)
$00F7_{16}$	Timer 2 latch (high-order)
$00F8_{16}$	Timer 3 register (low-order)
$00F9_{16}$	Timer 3 register (high-order)
$00FA_{16}$	Timer 3 latch (low-order)
$00FB_{16}$	Timer 3 latch (high-order)
$00FC_{16}$	Interrupt request register 1
$00FD_{16}$	Interrupt request register 2
$00FE_{16}$	Interrupt control register 1
$00FF_{16}$	Interrupt control register 2

Fig. 3 SFR (Special Function Register) memory map

INTERRUPTS

Interrupts can be caused by 15 different events consisting of six external, eight internal, and one software events.

Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed, interrupt disable flag I is set, and the program jumps to the address specified in the vector table. The interrupt request bit is cleared automatically. The reset and BRK instruction interrupt can never be disabled. Other interrupts are disabled when the interrupt disable flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figure 4 shows the structure of the interrupt request registers 1 and 2 and interrupt control registers 1 and 2.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt disable flag is "0". The interrupt request bit can be reset with a program, but not set. The interrupt enable bit can be set and reset with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 5 shows interrupts control.

Table 1. Interrupt vector address and priority.

Event	Priority	Vector addresses	Remarks
$\overline{\text{RESET}}$	1	$FFFF_{16}$, $FFFE_{16}$	Non-maskable
Input buffer full interrupt	2	$FFFD_{16}$, $FFFC_{16}$	Valid only in slave mode
Output buffer empty interrupt	3	$FFFB_{16}$, $FFFA_{16}$	Valid only in slave mode
INT_1 interrupt	4	$FFF9_{16}$, $FFF8_{16}$	External interrupt (phase programmable)
INT_2 interrupt	5	$FFF7_{16}$, $FFF6_{16}$	External interrupt (phase programmable)
INT_3 interrupt	6	$FFF5_{16}$, $FFF4_{16}$	External interrupt (phase programmable)
Timer 1 interrupt	7	$FFF3_{16}$, $FFF2_{16}$	
Timer 2 interrupt	8	$FFF1_{16}$, $FFF0_{16}$	
Timer 3 interrupt	9	$FFEF_{16}$, $FFEE_{16}$	
EV_1 interrupt	10	$FFED_{16}$, $FFEC_{16}$	External event interrupt (phase programmable)
EV_2 interrupt	11	$FFEB_{16}$, $FFEA_{16}$	External event interrupt (phase programmable)
EV_3 interrupt	12	$FFE9_{16}$, $FFE8_{16}$	External event interrupt (phase programmable)
Serial I/O receive interrupt	13	$FFE7_{16}$, $FFE6_{16}$	Valid only when serial I/O is selected
Serial I/O transmit interrupt	14	$FFE5_{16}$, $FFE4_{16}$	Valid only when serial I/O is selected
A-D conversion completion flag	15	$FFE3_{16}$, $FFE2_{16}$	
BRK instruction interrupt	16	$FFE1_{16}$, $FFE0_{16}$	Non-maskable software interrupt

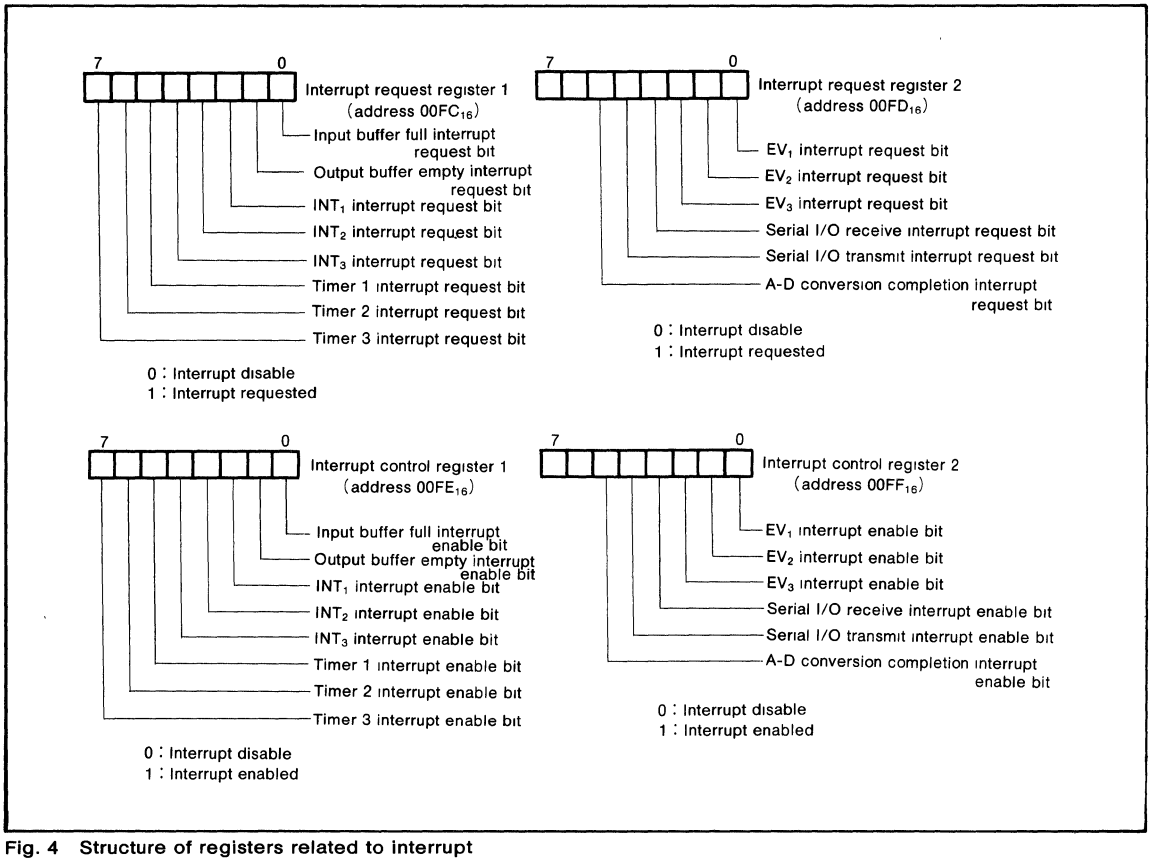


Fig. 4 Structure of registers related to interrupt

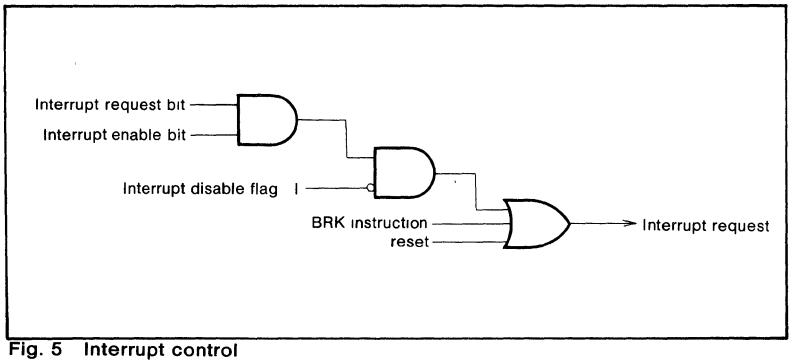


Fig. 5 Interrupt control

TIMER

The M37451 has three independent 16-bit internal timers as shown in Figure 6.

The timers are controlled by the timer i control register (i= 1, 2, 3) and MISRG1 shown in Figure 7 and 8.

The timer and the timer latch are independent of each other and a value must be written in both when setting a timer.

A write to a timer is performed in the order of T_L to T_H after setting the count enable bit to count inhibit "0".

A read from a timer is performed in the order of T_H to T_L. The value of T_L is latched in the read timer latch at the timing when T_H is read. All timers are decrement counters and are started by setting the timer i count enable bit to "1". When the value of the timer reaches 0000_{16}, and overflow occurs and the timer i interrupt request bit is set to "1" at the next count pulse.

During a reset or an STP instruction execution, the low-order byte of the timer 1 register is set to FF_{16} and the high-order byte is set to 03_{16}. Also, when an STP instruction is executed, a frequency obtained by dividing the oscillating frequency by four becomes the timer 1 input regardless of the timer 1 count source selection bit. This condition is canceled and the original count source is resumed when the timer i interrupt request bit is set to "1" or when a reset occurs. Refer to the section on the clock generator for details concerning the operation of the STP instruction.

The M37451 provides seven timer modes selectable with the timer mode selection bit in the timer i control register.

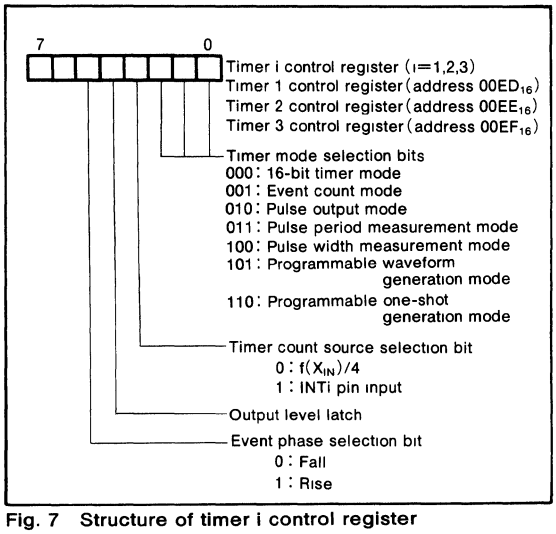


Fig. 7 Structure of timer i control register

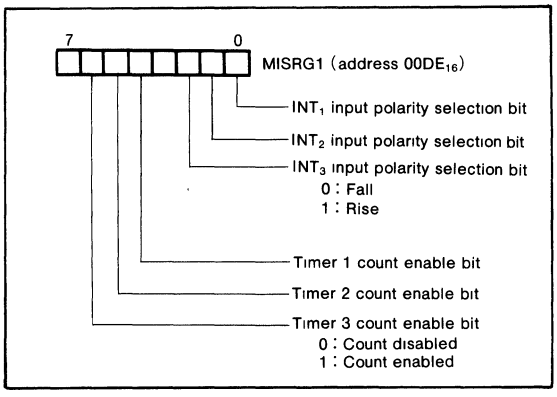


Fig. 8 Structure of MISRG1

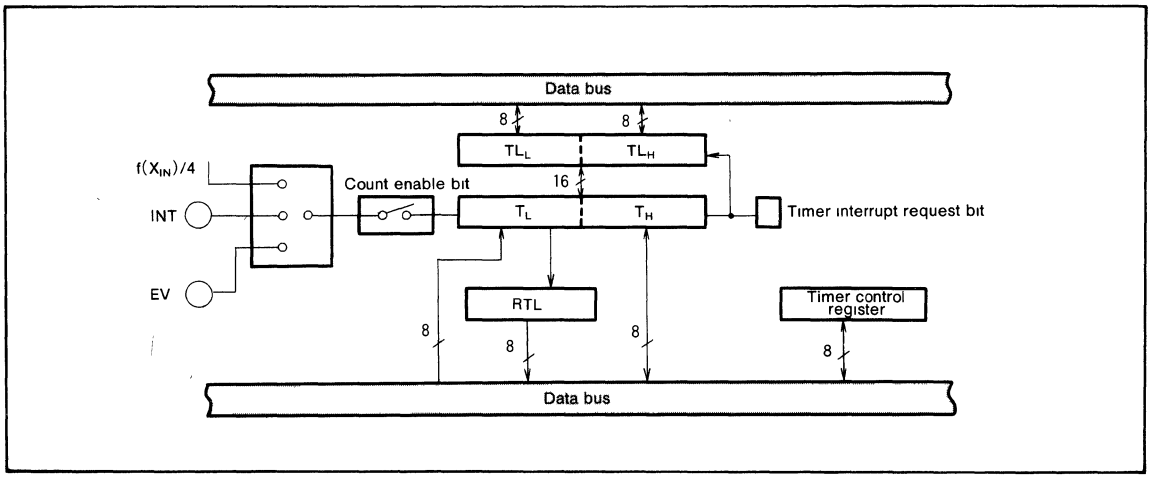


Fig. 6 Timer block diagram

(1) 16-bit Timer Mode [000]

In this mode, an interrupt request occurs and the value of the timer latch is loaded in the timer each time the timer overflows.

The timer count source is set to $f(X_{IN})$ divided by four regardless of the count sorce selection bit. Assuming that the timer latch is n, the frequency dividing ratio is $1/(n+1)$.

Figure 9 shows the timer operation during 16-bit timer mode.

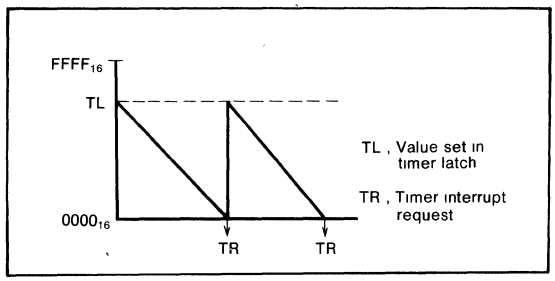


Fig. 9 16-bit timer mode operation

(2) Event Count Mode [001]

In this mode, the EVi pin input signal are counted in the direction selected by the event input polarity selection bit.

The input signal from the EVi pin is used as the count source regardless of the count source selection bit. The operation is the same as with the 16-bit timer mode except for the difference in the count source.

Both the "H" and "L" pulse width of the EVi pin input signal must be not less than $(4/f(X_{IN}))+100ns$.

Figure 10 shows the timer operation during event count mode.

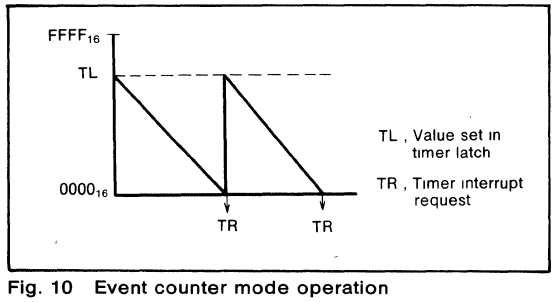


Fig. 10 Event counter mode operation

(3) Pulse Output Mode [010]

In this mode, a 50% duty pulse is output from the EVi pin.

The count source selected with the count source selection bit is counted. When it overflows, the phase of the EVi pin output level is reversed and the value of the timer latch is loaded in the timer.

When this mode is selected, the EVi pin output level is initialized to "L".

Figure 11 shows the timer operation during pulse output mode.

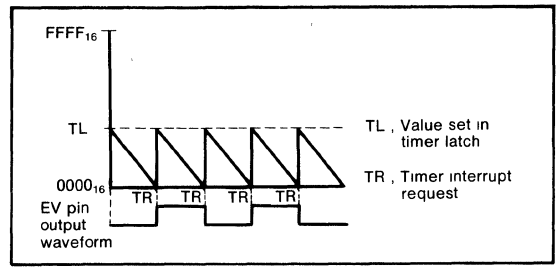


Fig. 11 Pulse output mode

(4) Pulse Period Measurement Mode [011]

This mode is used to measure the pulse period of the EVi pin input signal.

The timer counts the count source selected by the count source selection bit between the rise-to-rise or fall-to-fall interval (selected with the event input polarity selection bit in the timer i control register) of the EVi pin input signal.

At a valid edge on the EVi pin input, the 1's complement of the timer value is stored in the timer latch and the timer value is set to $FFFF_{16}$.

Figure 12 shows the timer operation during pulse frequency measurement mode.

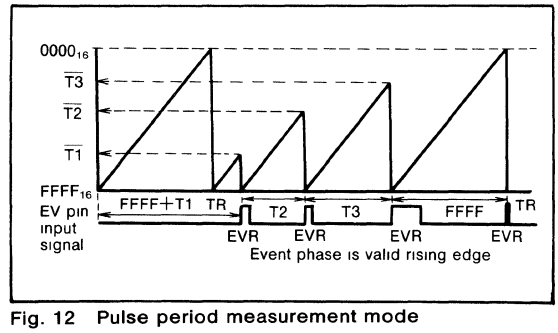


Fig. 12 Pulse period measurement mode

(5) Pulse Width Measurement Mode [100]

This mode measures the pulse width while the EVi pin input signal is "H" or "L".

Whether to measure the "H" or "L" interval is determined by the event input polarity selection bit. If this bit is "0", the count source selected with the count source selection bit is counted while the input pulse is "H". If it is "1", the count source is counted while the input pulse is "L". A 1's complement of the timer value is stored in the timer latch for a valid edge on the EVi pin input. In addition, the timer value is set to $FFFF_{16}$ for an edge (both rise and fall) on the EVi pin input. Figure 13 shows the timer operation during pulse width measurement mode.

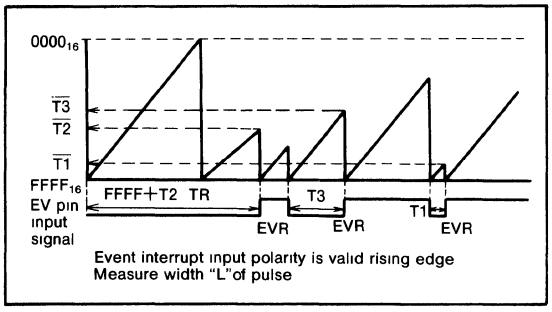


Fig. 13 Pulse width measurement mode

In pulse period measurement mode [011] and pulse width measurement mode [100], an EVi interrupt request is issued at the valid edge selected by the event phase selection bit. That is, an interrupt occurs at the end of the pulse period measurement or pulse width measurement. Also, when a timer overflow occurs, the count continues from $FFFF_{16}$ without the value of the timer latch being loaded in the timer.

Write to timer latch is inhibited in these modes. Furthermore, EVi interrupt is disabled during STP instruction execution.

(6) Programmable Waveform Generation Mode [101]

In this mode, the level set in the output level latch of the timer i control register is output to the EVi pin every time the timer overflows.

The timer counts the source selected by the count source selection bit and when it overflows, the value in the timer latch is loaded in the timer.

After it overflows, the value of the output level latch and the timer latch can be modified to generate any waveform from the EVi pin.

Figure 14 shows the timer operation during programmable waveform generation mode.

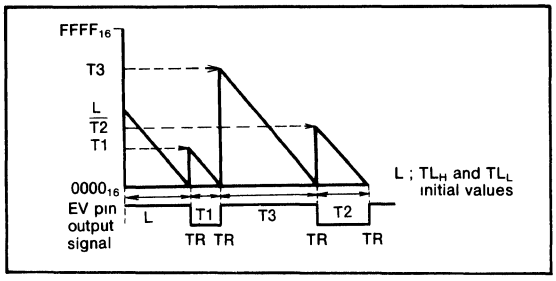


Fig. 14 Programmable waveform generation mode

(7) Programmable One-shot Generation Mode [110]

This mode uses the INTi pin input signal as a trigger and counts by writing the value of the timer latch in the timer.

The output level of the EVi pin goes "H" when the trigger is issued and goes "L" when the timer overflows.

The EVi pin level is initialized to "L" when this mode is selected.

The timer count souce is set to $f(X_{IN})$ divided by four regardless of the count source selection bit.

A valid edge of the INTi pin input trigger signal is determined by the INTi phase selection bit of MISRG1 ($00DE_{16}$).

Figure 15 shows the timer operation during programmable one-shot generation mode.

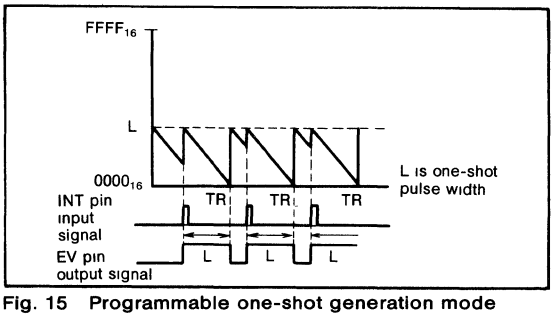


Fig. 15 Programmable one-shot generation mode

When the INTi pin input signal is selected as the count source for pulse output mode [010], pulse period measurement mode [011], pulse width measurement mode [100], and programmable waveform generation mode [101], the "H" and "L" pulse width of the input signal must not be less than $(6/f(X_{IN}))+100ns$.

SERIAL I/O

Serial I/O can operate in either clock synchronous or clock asynchronous (UART) mode. An exclusive baud rate generation timer (baud rate generator) is provided for serial I/O operation. Figure 16 shows the structure of the registers used for serial I/O.

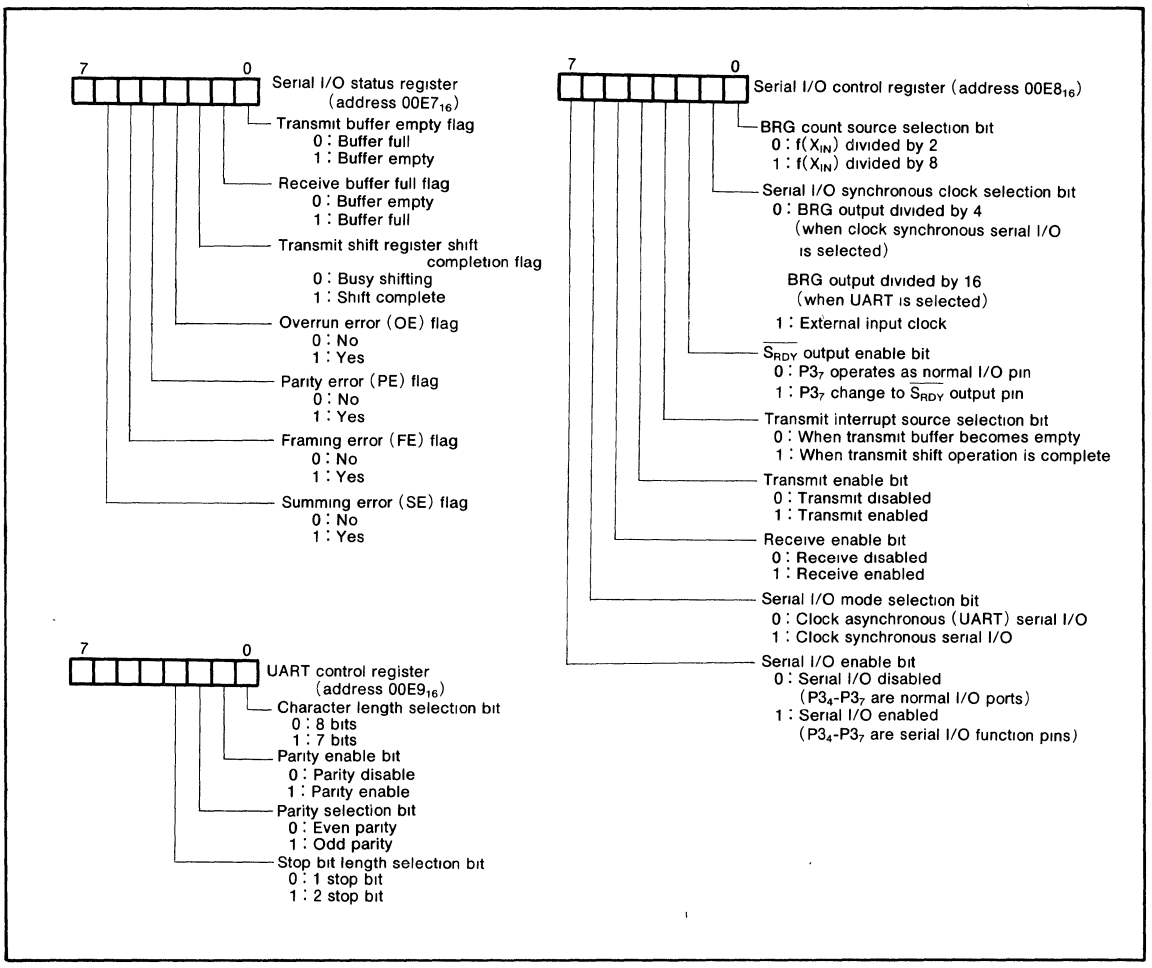


Fig. 16 Structure of registers related to serial I/O

(1) Clock Synchronous Serial I/O

Clock synchronous serial I/O is selected by setting the mode selection bit of the serial I/O control register to "1". Figure 17 shows a block diagram of clock synchronous serial I/O and Figure 18 shows its operation.

With clock synchronous serial I/O, the same clock is used as the operating clock between the transmitting and receiving microcomputers. If an internal clock is used for operating clock, transmit/receive is started by writing a signal in the transmit/receive buffer register.

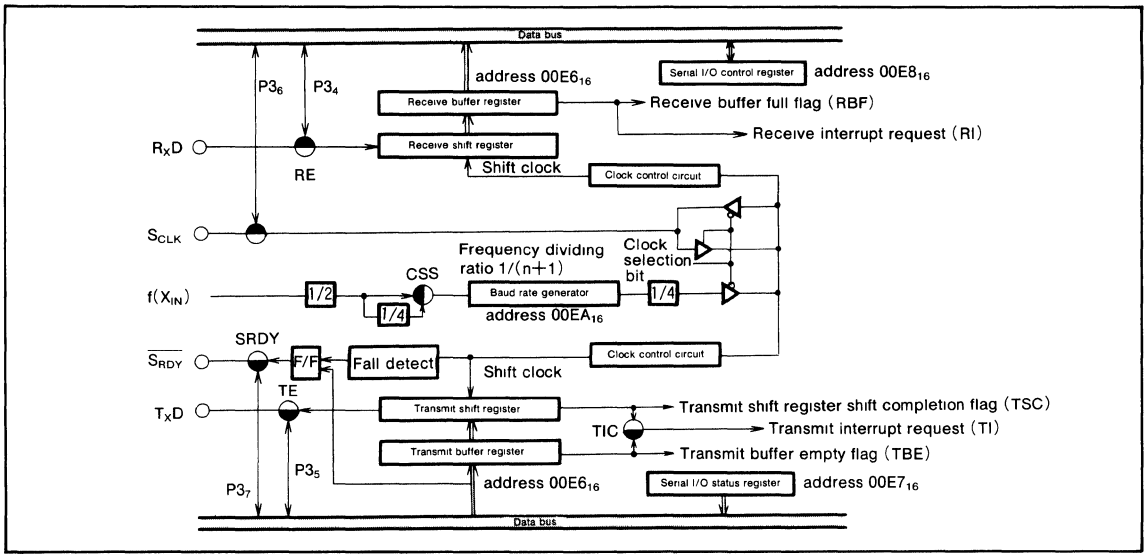
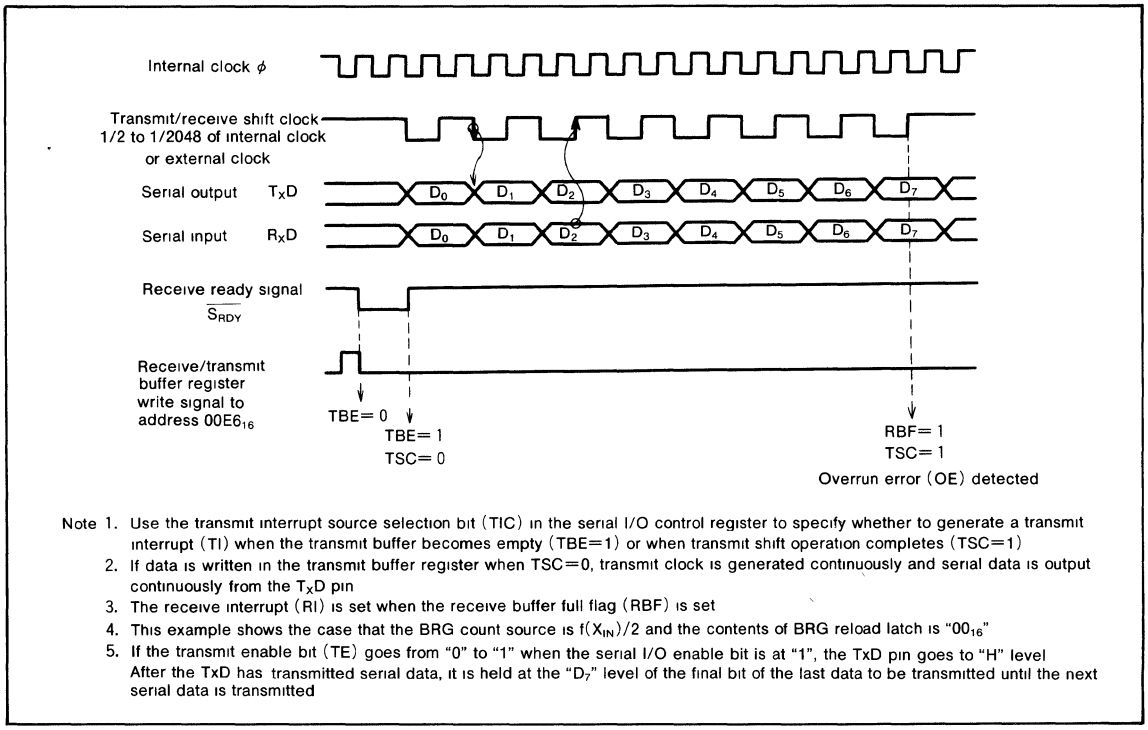


Fig. 17 Clock synchronous serial I/O block diagram



Note 1. Use the transmit interrupt source selection bit (TIC) in the serial I/O control register to specify whether to generate a transmit interrupt (TI) when the transmit buffer becomes empty (TBE=1) or when transmit shift operation completes (TSC=1)
2. If data is written in the transmit buffer register when TSC=0, transmit clock is generated continuously and serial data is output continuously from the T_XD pin
3. The receive interrupt (RI) is set when the receive buffer full flag (RBF) is set
4. This example shows the case that the BRG count source is $f(X_{IN})/2$ and the contents of BRG reload latch is "00_{16}"
5. If the transmit enable bit (TE) goes from "0" to "1" when the serial I/O enable bit is at "1", the TxD pin goes to "H" level After the TxD has transmitted serial data, it is held at the "D_7" level of the final bit of the last data to be transmitted until the next serial data is transmitted

Fig. 18 Clock synchronous serial I/O operation

(2) Clock Asynchronous Serial I/O (UART)

UART is selected by setting the mode selection bit of the serial I/O control register to "0". Figure 19 shows a block diagram of UART and Figure 20 shows its operation.

With the M37451, one of eight serial data transmission formats can be selected with the UART control register as shown in Figure 16. The transmission format must be agreed upon between the transmit side and the receive side.

The transmit shift register and the receive shift register has its buffer register respectively to perform serial data transfer (same memory addresses).

Data cannot be written or read directly to/from the shift registers. Therefore, the data to be transmitted is written to a buffer register and the received data is read from a buffer register. The buffer registers can also be used to store data to be transmitted next or to receive 2-byte data consecutively.

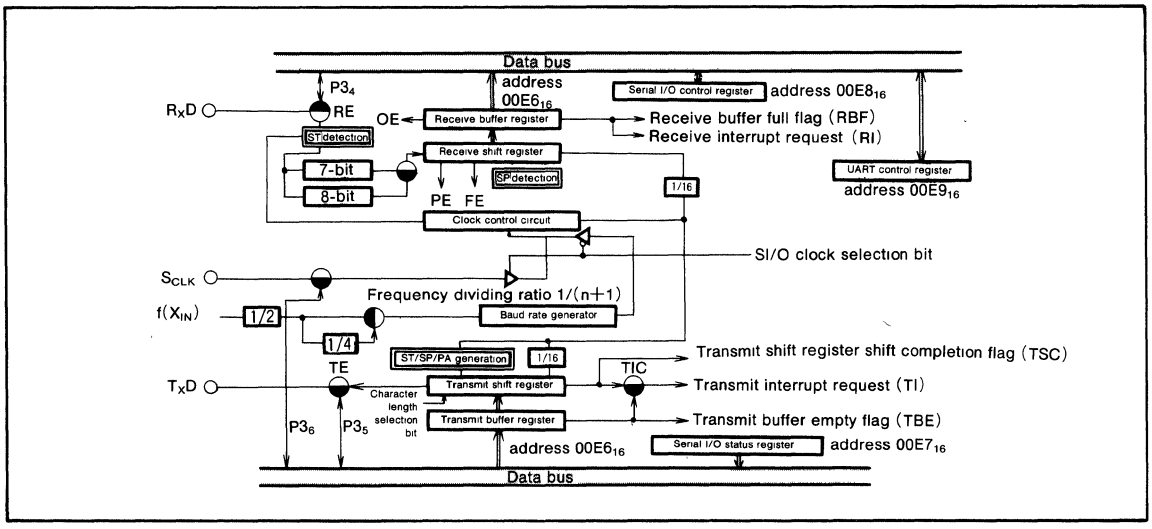
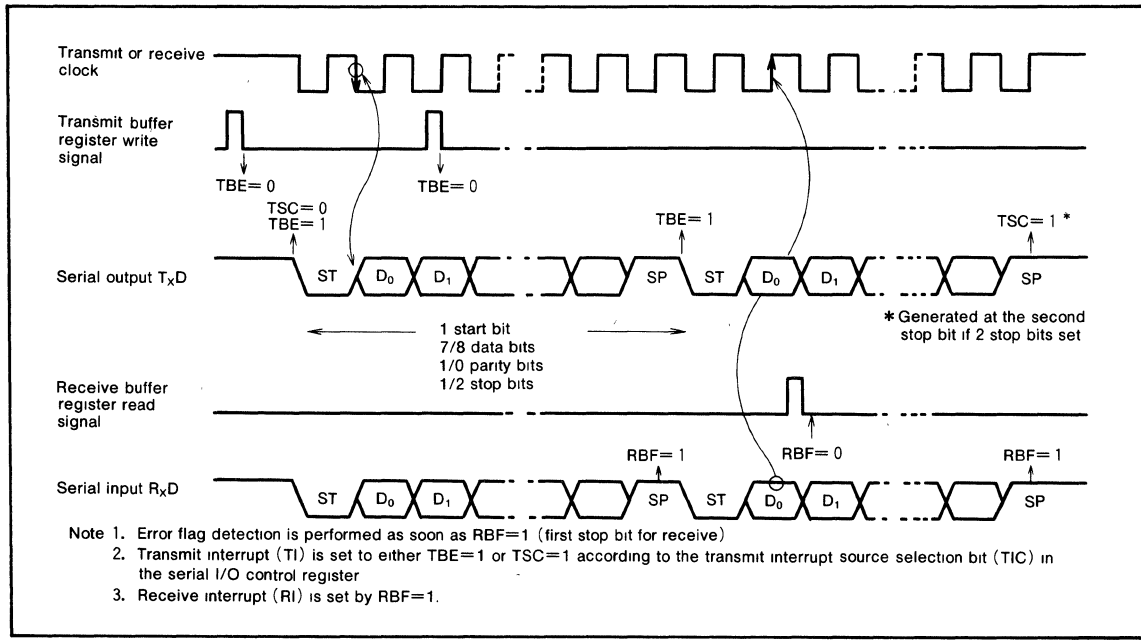


Fig. 19 UART serial I/O block diagram



Note 1. Error flag detection is performed as soon as RBF=1 (first stop bit for receive)
2. Transmit interrupt (TI) is set to either TBE=1 or TSC=1 according to the transmit interrupt source selection bit (TIC) in the serial I/O control register
3. Receive interrupt (RI) is set by RBF=1.

Fig. 20 UART serial I/O operation

[Serial I/O control register] SIOCON

The serial I/O control register is an 8-bit register consisting of selection bits for controlling the serial I/O function.

• Serial I/O enable bit SIOE

When this bit is set to "1", serial I/O is enabled and pins $P3_4$-$P3_7$ can be used as serial I/O function pins.

• Serial I/O mode selection bit SIOM

This bit is used to select the serial I/O operation mode. When this bit is "0", asynchronous serial I/O (UART), which transfers data using start and stop bits, is selected. When it is "1", clock synchronous serial I/O which performs transmission and receive using the same clock is selected.

• Receive enable bit RE

Receive operation is enabled when this bit is set to "1" and pin $P3_4$ becomes a serial data input pin.

• Transmission enable bit TE

Transmission operation is enabled when this bit is set to "1". Pin $P3_5$ becomes a serial data output pin and shift data is output.

• Transmission interrupt source selection bit TIC

This bit is used to selelct events that can cause a transmission interrupt.

• $\overline{S_{RDY}}$ output enable bit SRDY

If this bit is set to "1" when clock synchronous serial I/O is selected, pin $P3_7$ becomes an $\overline{S_{RDY}}$ signal output pin and $\overline{S_{RDY}}$ signal is output.

When an external clock is used during clock synchronous serial I/O, the $\overline{S_{RDY}}$ signal is used to notify the clock sender that it can send the serial clock signal. It goes "L" when data is written in the transmit/receive buffer register and goes "H" at the first fall of the receive clock. When using the $\overline{S_{RDY}}$ signal, the transmission enable bit must be set to "1" even when performing receive only.

• Serial I/O synchronous clock selection bit SCS

When this bit is "1", pin $P3_6$ becomes an input pin and the external clock input from the S_{CLK} pin is selected as the serial I/O synchronous clock. When this bit is "0", the baud rate generator (BRG) overflow signal is selected as the serial I/O synchronous clock. Also, when this bit is "0" during clock synchronous serial I/O, pin $P3_6$ becomes an output pin and the shift clock is output from the S_{CLK} pin.

When clock synchronous serial I/O is selected, the baud rate generator (BRG) output signal divided by four or an external clock input is used. When UART is selected, the BRG output signal divided by sixteen or an external clock input signal divided by sixteen is used.

• BRG count source selection bit CSS

The baud rate generator is an 8-bit counter with a reload register. By setting a value n in the BRG register (address $00EA_{16}$), the count source selected by the BRG count source selection bit is divided by (n+1).

[UART control register] UARTCON

The UART control regsiter is a 4-bit register consisting of control bits that are valid when UART is selected. The content of this register is used to set the data format for serial data transmission/receiving.

• Character length selection bit CHAS

This bit is used to select the transmission/receiving character length.

• Parity enable bit PARE

When this bit is set to "1", a parity bit is added next to the most significant bit (MSB) of the transmission data and parity is checked during receive.

• Parity selection bit PARS

This bit is used to specify the type of parity to be generated during transmission and checked when data is received. The number of 1's in the data is set to even or odd according to this bit.

• Stop bit length selection STPS

This bit is used to determine the number of stop bits to be used during transmission.

[Serial I/O status register] SIOSTS

The serial I/O status register is a 7-bit read only register consisting of serial I/O operation status flags and error flags. Bits 4 to 6 are valid only during UART mode.

All bits of this register are initialized to "0" at reset, and when the transmit enable bit in the serial I/O control register is set to "1", bits "0" and "2" change to "1".

• Transmission buffer empty flag TBE

This bit is cleared to "0" when transmission data is written in the transmission buffer register and set to "1" when that data is transferred to the transmit shift register. It is also cleared when TE=0.

• Receive buffer full flag RBF

When receiving serial data, data is transferred to the receive buffer register and this bit is set to "1" when the receive shift register completes receiving a data byte. This bit is cleared when the data is read. This bit is also cleared when RE=0.

• Transmit shift register shift completion flag TSC

This bit is cleared to "0" when the data in the transmission buffer register is transferred to the transmit shift register and set to "1" when data shift completes. It is also set to "1" when TE=0.

• Overrun error flag OE

When continuously receiving serial data, this bit is set when the next data fill the receive shift register before the data in the receive buffer register has been read

• Parity error flag PE

When receiving serial data with parity, this bit is set to "1 " if the parity of the received data differs from the specified parity.

· Framing error flag FE

This bit is set to "1" when there is no stop bit when transferring data from the receive shift register to the receive buffer.

· Summing error flag SE

This bit is set when either overrun, a parity, or a framing error occurs.

Tests for these errors are performed as soon as the data is transferred from the receive shift register to the receive buffer register and at the same time the receive buffer full flag is set. The error flags (OE, PE, FE, and SE) are cleared when any data is written in the serial I/O status register. Also, all status flags including error flags are cleared when SIOE=0.

Usage cautions

(1) To reset the serial I/O control register

Reset the serial I/O control register after disabling the transmit and receive enable bits that were enabled at that point and resetting the transmit and receive circuits. If the serial I/O control register is reset without resetting the other items, the settings will not operate correctly.

(2) Transmit and receive interrupt requests when transmit and receive enable bits are set.

Setting the transmit and receive enable bits to "1" sets the receive buffer empty flag and the transmit shift register shift completion flag to "1". Therefore, an interrupt request is generated and the transmit interrupt request bit is set, regardless of which timing is selected for the generation of transmit interrupts.

If interrupts of this timing are not used, first clear the transmit interrupt enable bit to "0" (disabled status), set the transmit enable bit, then clear the transmit interrupt request bit again after executing one instruction (e. g., the NOP instruction). Finally, set the transmit interrupt enable bit to "1" (enabled status).

(3) To disable transmission after one byte of data has been transmitted.

The method used in the M37451 to post the completion of data transmission is to reference the transmit shift register shift completion flag (TSC flag). The TSC flag is cleared to "0" while data is being transmitted, and it is set to "1" when the data transmission is completed. Therefore, if transmission is disabled after it has been confirmed that the TSC flag has been set, transmission can be forced to end after one byte of data is transmitted.

However, the TSC flag can also be set by enabling serial I/O, but it is not cleared by shift clock generation and transmission start (after data has been transferred from the transmit buffer to the transmit shift register, after 0.5 to 1.5 cycles of the shift clock), so if the TSC flag is referenced and transmission is disabled at this point, data will not be transmitted. Make sure that the TSC flag is referenced after transmission has started.

BUS INTERFACE

The M37451 is equipped with a bus interface that is functionally similar to the MELPS 8-41 series. Its operation can be controlled with control signals from the host CPU (slave mode).

The M37451 bus interface can be connected directly to either a R/$\overline{W}$ type CPU or separate $\overline{RD}$, $\overline{WR}$ type CPU. Figure 21 shows a block diagram of the bus interface function. Slave mode is selected with MISRG2 (address $00DF_{16}$) bit 2 and 3 as shown in Figure 22.

An input buffer full interrpt occurs when data is received from the host CPU and an output buffer empty interrupt occurs when data is read by the host CPU.

In slave mode, ports $P5_0$-$P5_7$ become a tri-state data bus used to transfer data, commands, and status to and from the host CPU.

Furthermore, ports $P6_4$-$P6_7$ become host CPU control signal input pins and $P6_3$ becomes a slave status output pin.

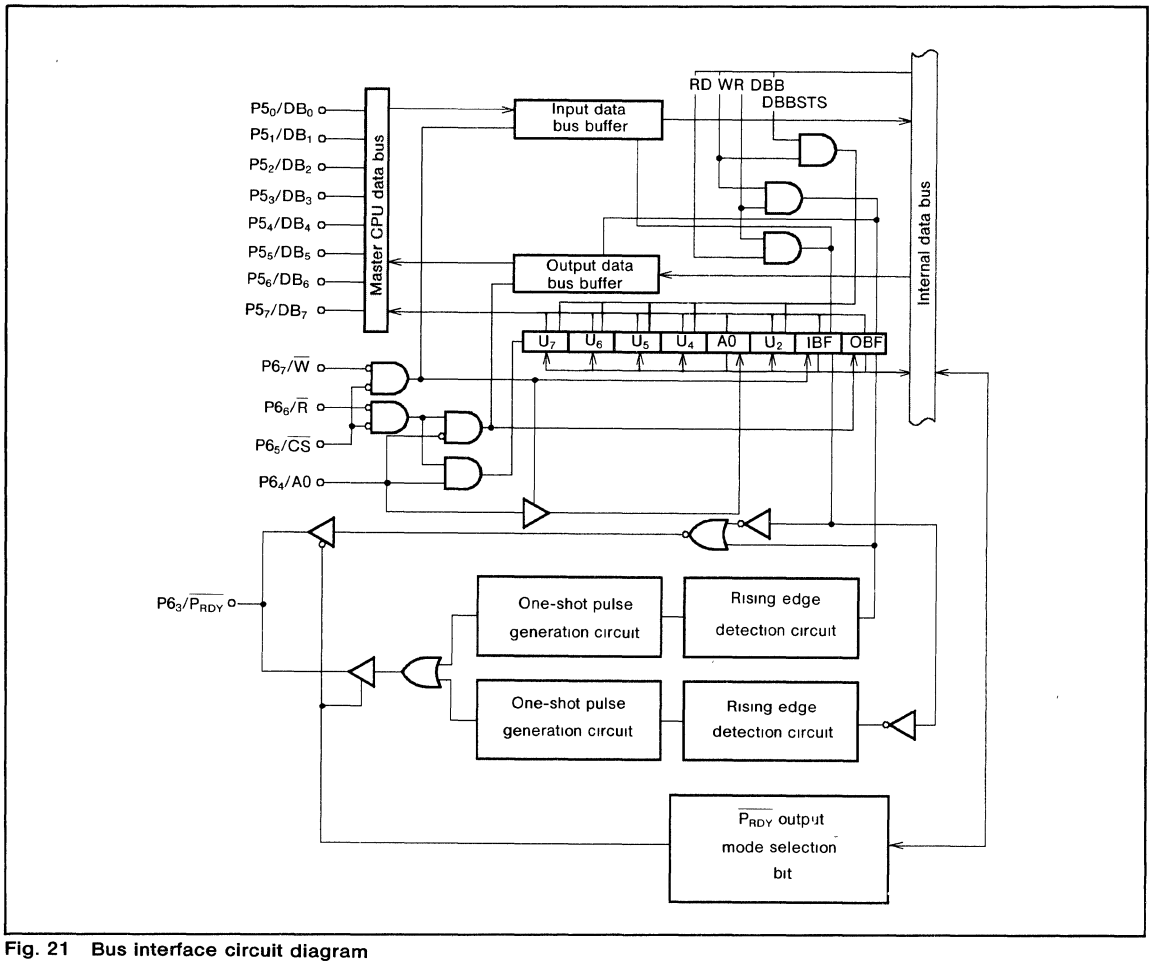


Fig. 21 Bus interface circuit diagram

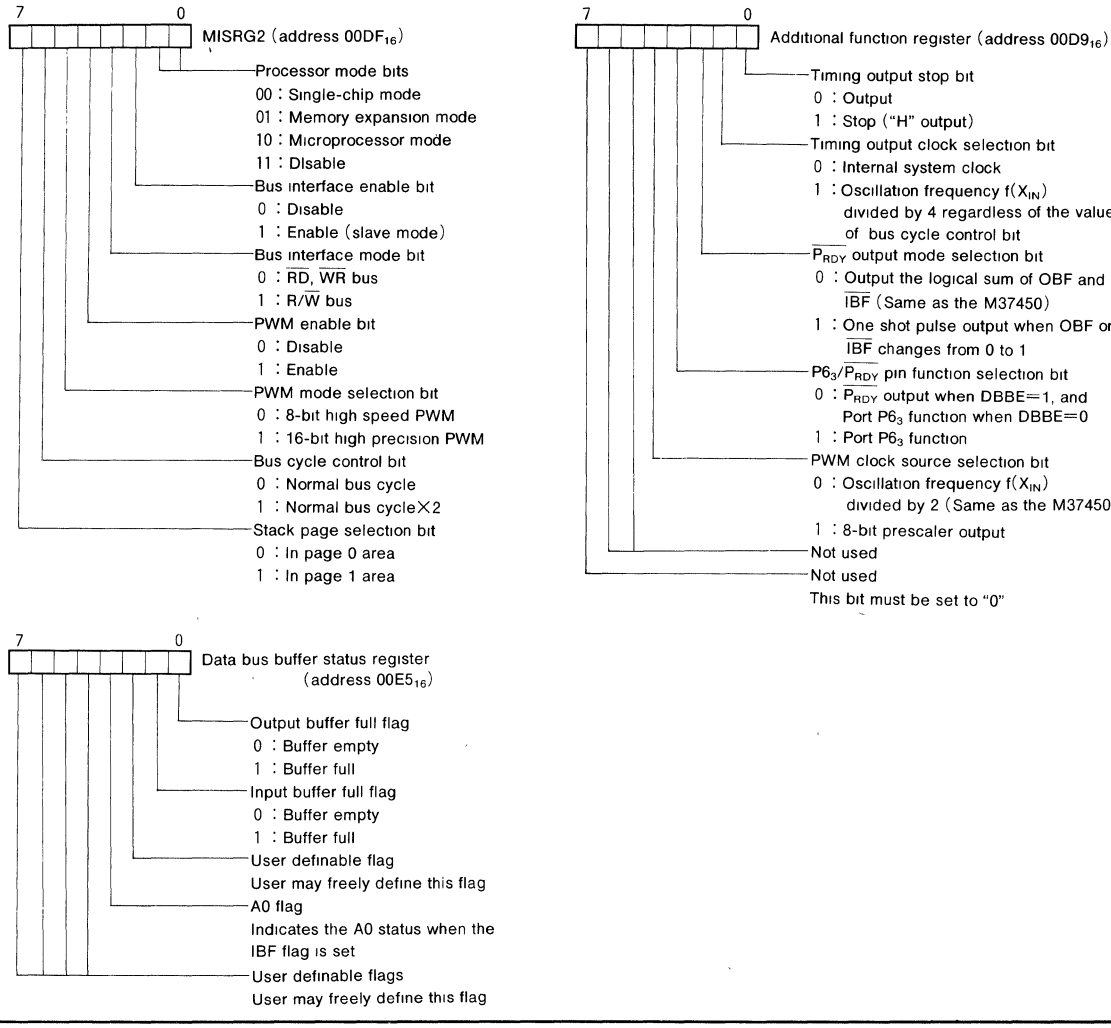


Fig. 22 Structure of bus interface relation registers

[Data bus buffer status register] DBBSTS

This is an 8-bit register. Bits 0, 1, and 3 are read-only bits indicating the status of the data bus buffer. Bits 2, 4, 5, 6, and 7 are read/write enabled user-definable flags that can be set with a program. The host CPU can only read these flags by setting the A0 pin to "H".

• Output buffer full flag OBF

This flag is set when data is written in the output data bus buffer and cleared when the host CPU reads the data in the output data bus buffer. When the $\overline{P_{RDY}}$ output mode selection bit is "0", OBF is initialized to "1" only at reset and is cleared to "0" by setting the bus interface enable bit to "1". In this case, OBF is set to "1" when the bus interface enable bit changes from "1" (enable) to "0" (disable). But when the bus interface enable bit is set to "1" again, it is set to the value directly before clearing the bus interface enable bit. When the $\overline{P_{RDY}}$ output mode selection bit is "1", OBF is initialized to "1" when the bus interface enable bit is cleared to "0" or reset.

In this case, OBF is set to "1" by clearing the bus interface enable bit and it is cleared to "0" by setting the bus interface enable bit.

• Input buffer full flag IBF

This flag is set when the host CPU writes data in the input data bus buffer and cleared when the slave CPU reads the data in the input data bus buffer. When the $\overline{P_{RDY}}$ output mode selection bit is "0", IBF is initialized to "0" only at reset.

When the $\overline{P_{RDY}}$ output mode selection bit is "1", IBF is initialized to "0" when the bus interface enable bit is cleared to "0" or reset.

A0 Flag

The level of the A0 pin is latched when the host CPU writes data in the input data bus buffer.

[Input data bus buffer] DBBIN

Data on the data bus is latched in DBBIN when there is a write request from the host CPU. The data in DBBIN can be read from the data bus buffer register (SFR address $00E4_{16}$).

[Output data bus buffer] DBBOUT

Data is written in DBBOUT by writing data in data bus buffer register (SFR address $00E4_{16}$). The data in DBBOUT is output to the data bus (P5) when the host CPU issues a read request with setting the A0 pin to "L".

Table 2. Control I/O pin functions when bus interface function is selected

Pin	Name	Bus interface mode bit	$\overline{P_{RDY}}$ output mode selection bit	$P6_3/\overline{P_{RDY}}$ pin function selection bit	Input/ Output	Function
$P6_3$	$\overline{P_{RDY}}$	—	0	0	Output	Status output The NOR of OBF and $\overline{IBF}$ is output
				1	I/O	Port $P6_3$ function
			1	0	Output	Status output Normally output "0" One shot pulse whose length is half of a period of internal system clock ϕ is output, when OBF or $\overline{IBF}$ changes from "0" to "1" (See Fig 23)
				1	I/O	Port $P6_3$ function
$P6_4$	A0	—	—	—	Input	Address input Used to select between DBBSTS and DBBOUT during host CPU read Also used to identify commands and data during write
$P6_5$	$\overline{CS}$	—	—	—	Input	Chip select input Used to select the data bus buffer Select when "L"
$P6_6$	$\overline{R}$	0	—	—	Input	Timing signal used by the host CPU to read data from the data bus buffer
	E	1	—	—	Input	Inputs a timing signal E or inverse of ϕ
$P6_7$	$\overline{W}$	0	—	—	Input	Timing signal used by the host CPU to write data to the data bus buffer
	R/$\overline{W}$	1	—	—	Input	Input R/$\overline{W}$ signal used to control the data transfer direction When this signal is "L", data bus buffer write is synchronized with the E signal When it is "H", data bus buffer read is synchronized with the E signal

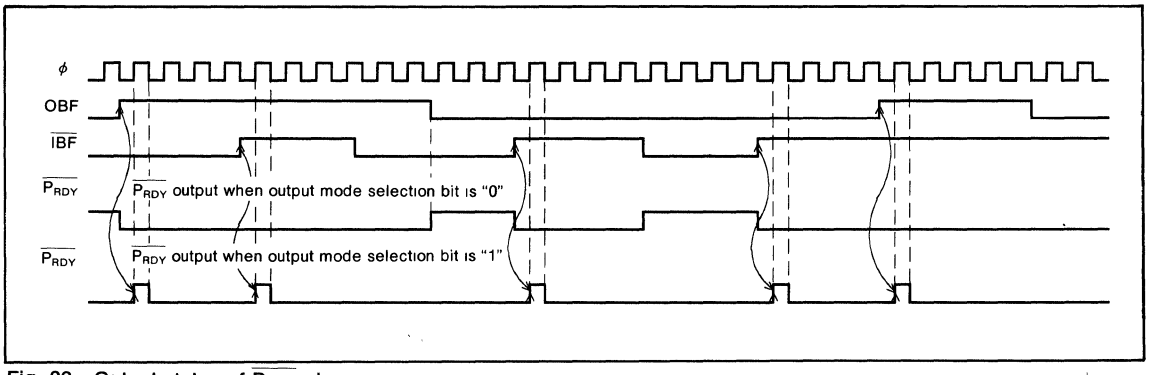


Fig. 23 Output status of $\overline{P_{RDY}}$ pin

PWM

The PWM generator has two program-selectable modes; the high-speed mode (8-bit resolution) and the high-precision mode (16-bit resolution).

Also two clocks listed below can be selected as the count clock of each PWM mode.

- Oscillation frequency f(X_{IN}) divided by 2
- 8-bit prescaler output (The count source of prescaler is oscillation frequency f(X_{IN}) divided by 2)

Figure 26 shows a block diagram of PWM.

The count clock of PWM can be selected by the PWM clock source selection bit of additional function register (address $00D9_{16}$). And the register MISRG2 (address $00DF_{16}$) is used to enable/disable the PWM and change its mode. When the PWM enable bit is set, the PWM generator starts from its initial state.

When PWM clock source selection bit is "0", as shown in Figure 24, the output period is fixed.

In high-speed mode

$(2\times255)/f(X_{IN})$ 40.8μs at $f(X_{IN})$=12.5MHz

In high-precision mode

$(2\times65535)/f(X_{IN})$ 10.4856ms at $f(X_{IN})$=12.5MHz

When PWM clock source selection bit is "1", as shown in Figure 25, the output period can be changed by setting the value to prescaler latch (address $00D8_{16}$).(Note)

In high-speed mode

$\{2(n+1)\times255\}/f(X_{IN})$ $40.8(n+1)\mu$s at $f(X_{IN})$ = 12.5MHz

In high-precision mode

$\{2(n+1)\times65535\}/f(X_{IN})$ $10.4856(n+1)$ms at $f(X_{IN})$ =12.5MHz

n : Set value to prescaler latch

The "H" width of the output pulse is determined by setting a value only in the PWM_L register for high-speed mode and in both the PWM_H and PWM_L in this order for high-precision mode.

If the value set in the PWM register is m, the "H" width of the output pulse is

(PWM period×m)/255 for high-speed mode and

(PWM period×m)/65535 for high-precision mode.

Note : Address $00D8_{16}$ functions as port P4 register (read only) when read, and functions as PWM prescaler latch (write only) when write. So the value of PWM prescaler can not be read out.

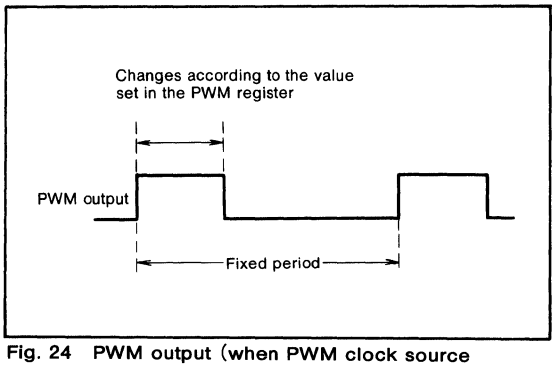


Fig. 24 PWM output (when PWM clock source selection bit is "0")

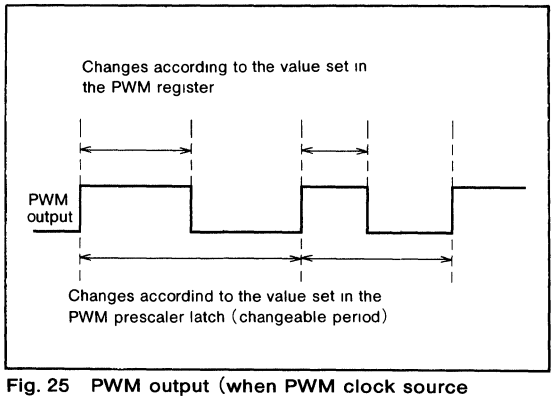


Fig. 25 PWM output (when PWM clock source selection bit is "1")

Notes on PWM start

(1) Notes on PWM start

PWM starts after the PWM enable bit is set to enable and "L" level is output from the PWM_{OUT} pin. The length of this "L"-level output is as follows:

If the PWM prescaler is not used (PWM clock source selection bit=0): 1/2 clock cycle

If the PWM prescaler is used (PWM clock source selection bit=1): (1+n)/2 clock cycle (where n is the value set in the prescaler)

(2) Notes on PWM restart (only when PWM clock source selection bit is "1")

If the PWM enable bit is set to enabled, then to disabled, then back to enabled, temporarily clear the PWM clock source selection bit to "0" then reset it to "1" to re-enable PWM.

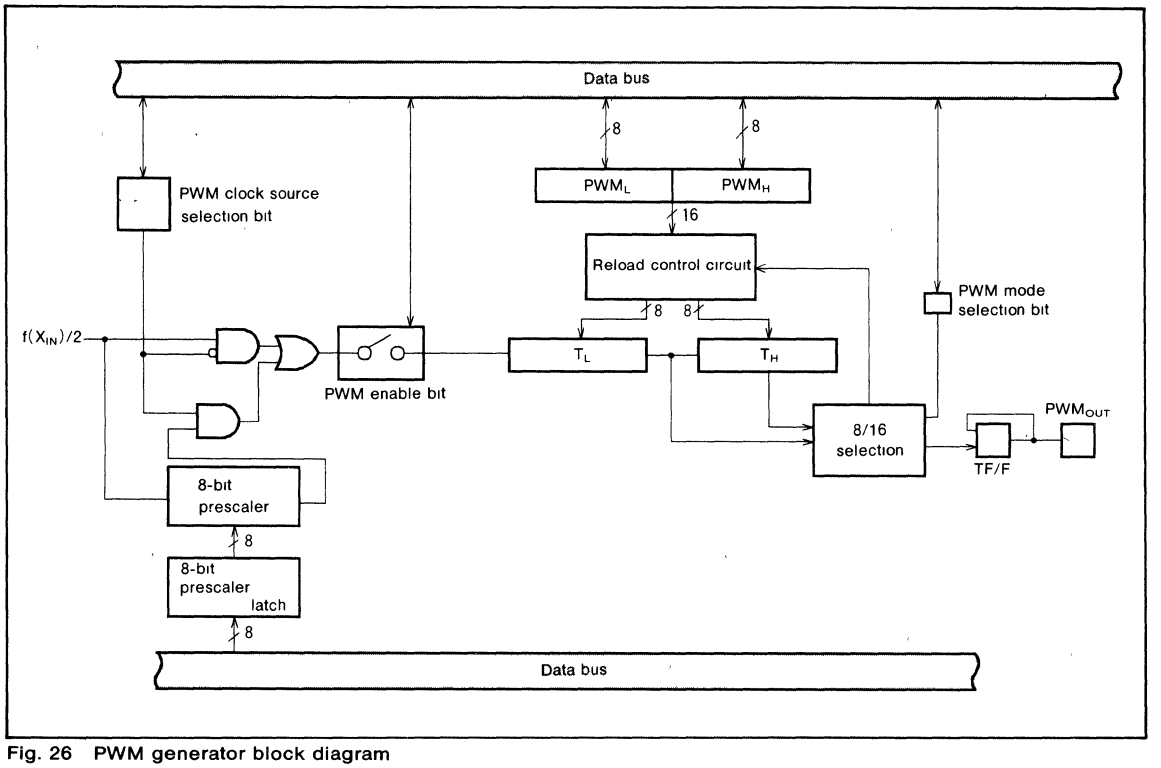


Fig. 26 PWM generator block diagram

A-D CONVERTER

An A-D converter is an 8-bit successive approximation method. Figure 28 shows a block diagram of the A-D converter.

The 64-pin model has three analog voltage input pins; the 80-pin model has eight.

A-D conversion is started by a write operation to the analog input pin selection bit of the A-D control register shown in Figure 27 and by selecting the analog voltage input pin. The A-D interrupt request bit in the interrupt request register 2 is set when A-D conversion completes. The result of A-D conversion is stored in the A-D register.

The contents of the A-D register must not be read during A-D conversion and f(X_{IN}) must be no less than 1 MHz during A-D conversion.

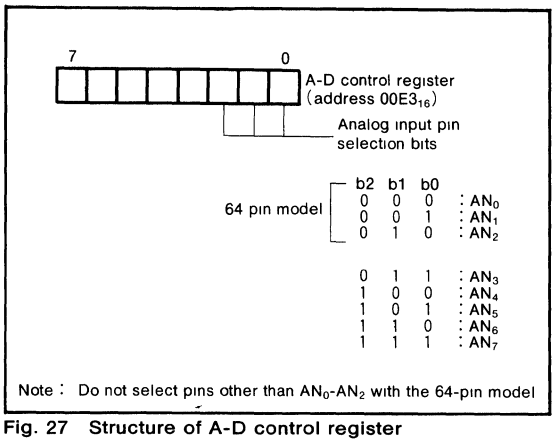


Fig. 27 Structure of A-D control register

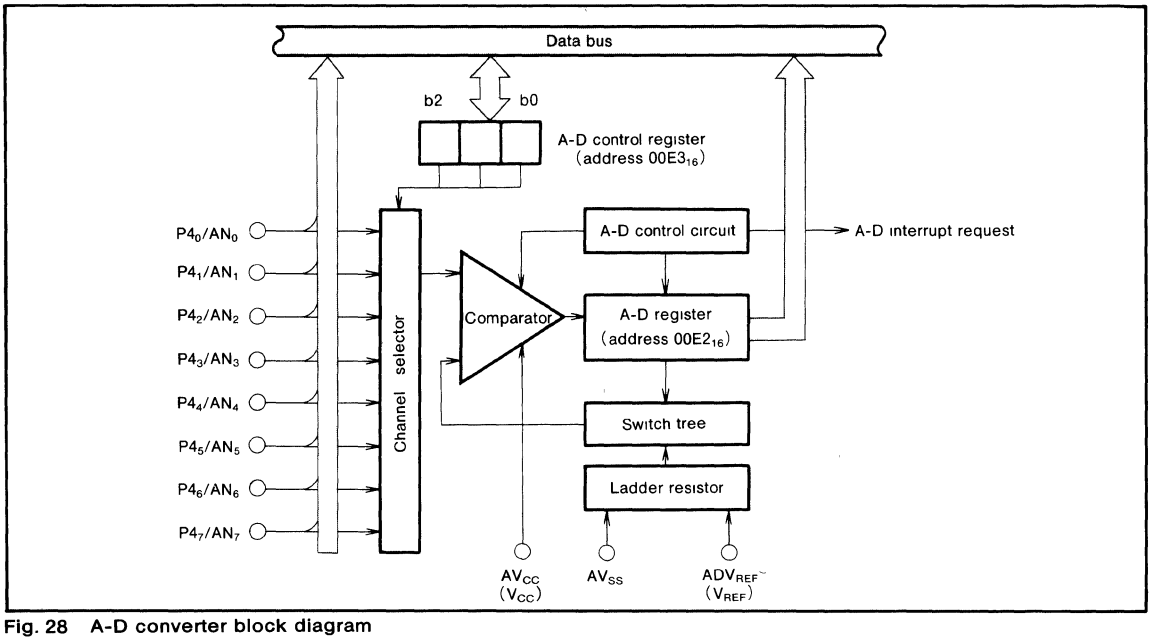


Fig. 28 A-D converter block diagram

D-A CONVERTER

Two 8-bit resolution D-A converter channels are provided. Figure 29 shows a block diagram of the D-A converter.

D-A conversion is performed by setting a value in the D-Ai register (addresses 00E0$_{16}$ and 00E1$_{16}$). The result of D-A conversion is output from the D-Ai output pin.

The output analog voltage V_{DA} is determined by the value n (decimal) set in the D-Ai register as follows:

$V_{DA}=DAV_{REF}{}^{*}\times n/256$

*V_{REF} for 64-pin model.

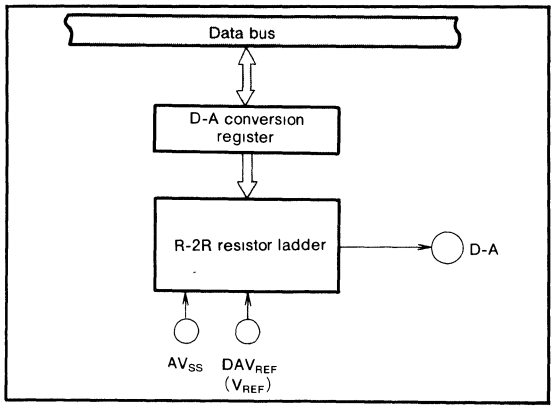


Fig. 29 D-A converter block diagram

RESET CIRCUIT

The M37451 is reset according to the sequence shown in Figure 30. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the $\overline{RESET}$ pin is held at "L" level for no less than 8 clock cycles while the power voltage is 5V±10% and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 30.

An example of the reset circuit is shown in Figure 31. The reset input voltage must be kept below 0.6V until the supply voltage surpasses 4.5V.

		address	b7	b6	b5	b4	b3	b2	b1	b0
(1)	Port P0 directional register	$00D1_{16}$	0	0	0	0	0	0	0	0
(2)	Port P1 directional register	$00D3_{16}$	0	0	0	0	0	0	0	0
(3)	Port P2 directional register	$00D5_{16}$	0	0	0	0	0	0	0	0
(4)	Port P3 directional register	$00D7_{16}$	0	0	0	0	0	0	0	0
(5)	Additional function register	$00D9_{16}$	0			0	0	0	0	0
(6)	Port P5 directional register	$00DB_{16}$	0	0	0	0	0	0	0	0
(7)	Port P6 directional register	$00DD_{16}$	0	0	0	0	0	0	0	0
(8)	MISRG1	$00DE_{16}$		0	0	0		0	0	0
(9)	MISRG2	$00DF_{16}$	0	0	0	0	0	0	CM1	0
(10)	D-A1 register	$00E0_{16}$	0	0	0	0	0	0	0	0
(11)	D-A2 register	$00E1_{16}$	0	0	0	0	0	0	0	0
(12)	Data bus buffer status register	$00E5_{16}$							0	1
(13)	Serial I/O status register	$00E7_{16}$		0	0	0	0	0	0	0
(14)	Serial I/O control register	$00E8_{16}$	0	0	0	0	0	0	0	0
(15)	UART control register	$00E9_{16}$				0	0	0	0	
(16)	Timer 1 control register	$00ED_{16}$			0	0	0	0	0	0
(17)	Timer 2 control register	$00EE_{16}$			0	0	0	0	0	0
(18)	Timer 3 control register	$00EF_{16}$			0	0	0	0	0	0
(19)	Timer 1 register (low order)	$00F0_{16}$	FF							
(20)	Timer 2 register (high order)	$00F1_{16}$	03							
(21)	Interrupt request register 1	$00FC_{16}$	0	0	0	0	0	0	0	0
(22)	Interrupt request register 2	$00FD_{16}$			0	0	0	0	0	0
(23)	Interrupt control register 1	$00FE_{16}$	0	0	0	0	0	0	0	0
(24)	Interrupt control register 2	$00FF_{16}$			0	0	0	0	0	0
(25)	Processor status register	(PS)					1			
(26)	Program counter	(PC_H)	Contents of address $FFFF_{16}$							
		(PC_L)	Contents of address $FFFE_{16}$							

Note 1 Since the contents of both registers other than those listed above (including timer 1, timer 2, timer 3, and the serial I/O register) and the RAM are undefined at reset, it is necessary to set initial values

2 The initial value of CM1 depends on the level on the CNV_{SS} pin

Fig. 30 Internal state of microcomputer at reset

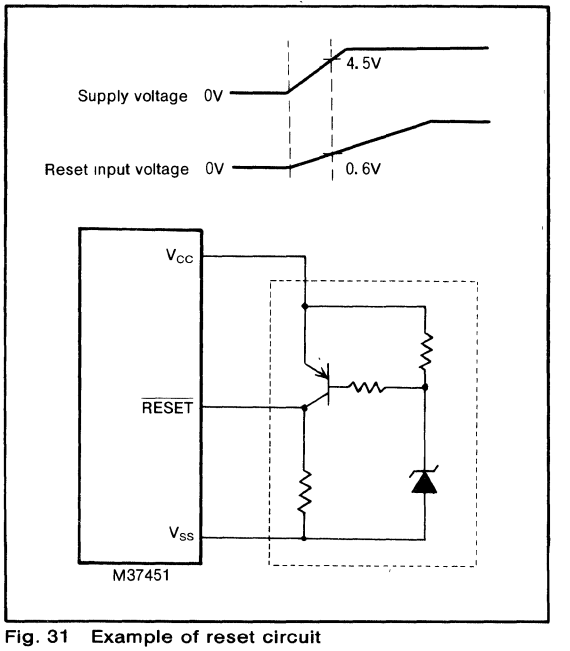


Fig. 31 Example of reset circuit

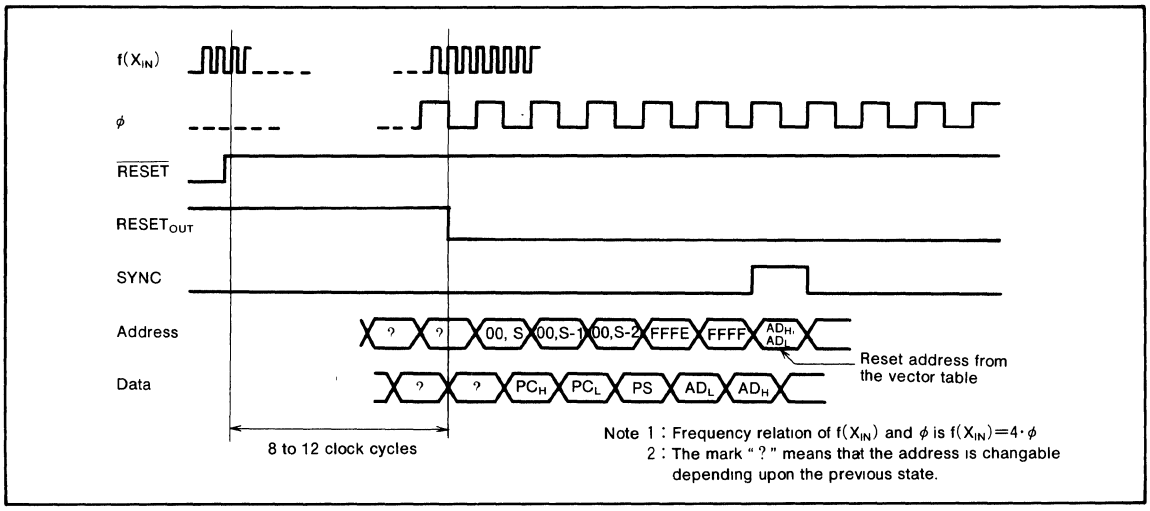


Fig. 32 Timing diagram at reset

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS output.

As shown in the memory map (Figure 3), port P0 can be accessed at zero page memory address $00D0_{16}$.

Port P0 has a directional register (address $00D1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously ouptut value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor status register (bit 0 and bit 1 at address $00DF_{16}$), three different modes can be selected; single-chip mode, memory expansion mode and microprocessor mode.

In these modes it functions as address (A_7-A_0) output port (excluding single-chip mode). For more details, see the processor mode information

(2) Port P1

In single-chip mode, port P1 has the same function as port P0. In other modes, it functions as address (A_{15}-A_8) output port.

Refer to the section on processor modes for details.

(3) Port P2

In single-chip mode, port P2 has the same function as port P0. In other modes, it functions as data (D_0-D_7) input/output port. Refer to the section on processor modes for details.

(4) Port P3

Port P3 is an 8-bit I/O port with function similar to port P0. All pins have program selectable dual functions. When a serial I/O function is selected, the input and output from pins $P3_4$-$P3_7$ are determined by the contents of the serial I/O registers.

This port is unaffected by the processor mode.

(5) Port P4

This is an input-only port and may be used as an analog voltage input port. The number of ports is different for the 64-pin model and 80-pin model The 64-pin model has three ports and the 80-pin model has eight ports.

(6) Port P5

This is an 8-bit I/O port with function similar to port P0.

When slave mode is selected with a program, all ports change to the data bus for the master CPU. In this case, port input/output is unaffected by the directional register

This port is unaffected by the processor mode register.

(7) Port P6

This is an 8-bit input/output port with function similar to port P0.

When slave mode is selected with a program, ports $P6_3$-$P6_7$ change to the control bus for the bus interface function. In this case, port input/output is unaffected by the directional register.

Ports $P6_0$-$P6_2$ are shared with the external interrupt input pins (INT_1-INT_3). The INT interrupt constantly monitors the status of this port and generates an interrupt at a valide edge. Therefore, if the INT interrupt is not used, it must be disabled and if it is used, this port must be set to input.

(8) Port D-A

Port D-A consists of two analog voltage output pins. Any analog voltage can be generated by setting a value in the D-A register.

(9) ϕ pin

The ϕ pin normally outputs the internal system clock (the oscillation frequency of the resonator connected between the X_{IN} and X_{OUT} pins, divided by four).

The timing clock output from the ϕ pin is in output mode if the timing output stop bit (bit 0 of address $00D9_{16}$) is set to "0", and in stop mode if that bit is set to "1" and the timing clock output is "H".

If the timing output clock selection bit (bit 1 of address $00D9_{16}$) is set to "0" when the timing output stop bit is "0" (timing output is being output), the internal system clock that is output from the ϕ pin is the oscillation frequency divided by four if the bus cycle control bit is "0", or the oscillation frequency divided by eight if that bit is "1". If the timing output clock selection bit is "1", the bus cycle control bit is ignored—the clock that is output is the oscillation frequency divided by four. (See Fig. 33)

(10) SYNC pin

This pin outputs a signal that is "H" during one cycle of the ϕ during operation code fetch.

(11) R/$\overline{W}$ pin

This is a control signal output pin that indicates the local bus direction in memory expansion and microprocessor modes.

(12) $\overline{RD}$, $\overline{WR}$ pins

These are local bus write and read timing signal output pins for memory expansion and microprocessor modes. A signal equivalent to the signal otuput from the R/$\overline{W}$ separated by the ϕ signal is output.

These pins are used exclusively by the 80-pin model.

(13) $RESET_{OUT}$ pin

This pin goes "H" while the microprocessor is being reset. It can be used as a reset signal output pin for peripheral devices.

This pin is used exclusively by the 80-pin model.

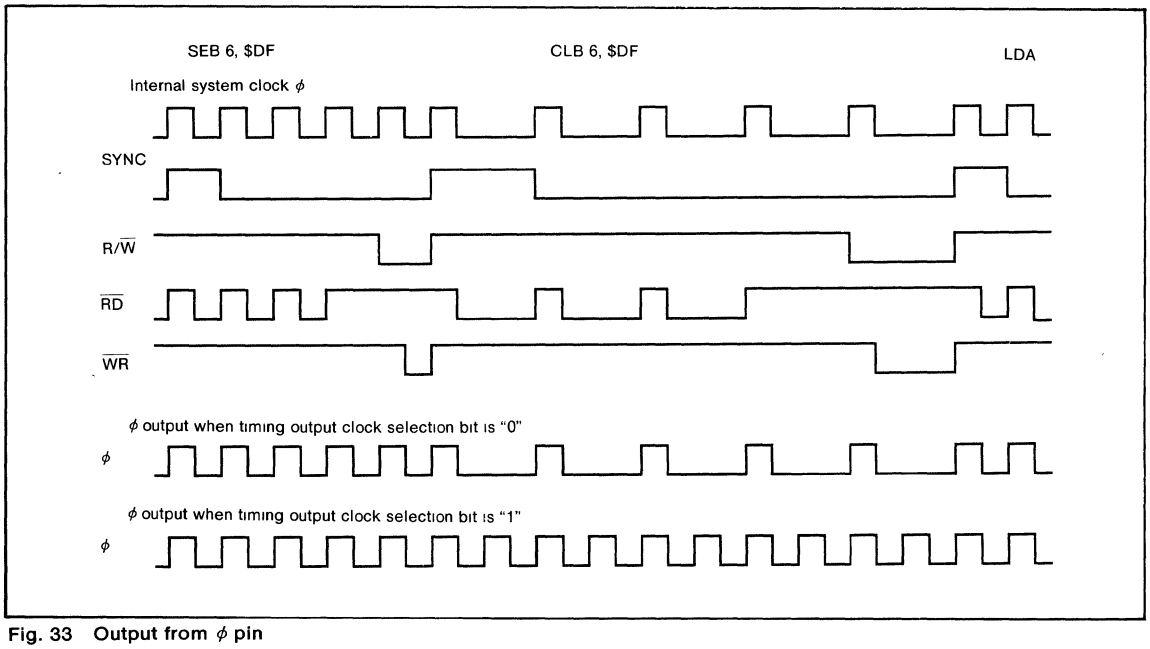


Fig. 33 Output from ϕ pin

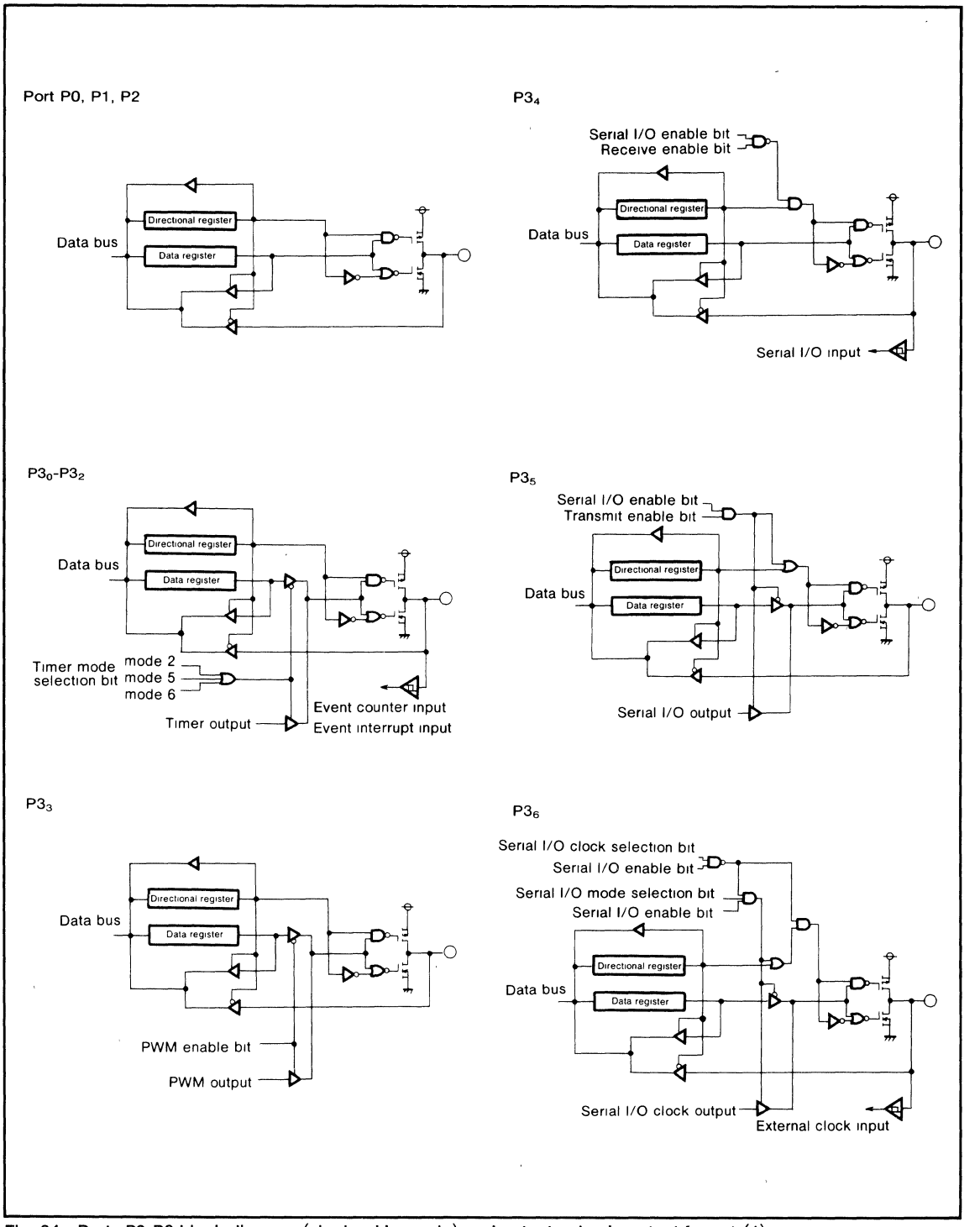


Fig. 34 Ports P0-P6 block diagram (single-chip mode) and output only pin output format (1)

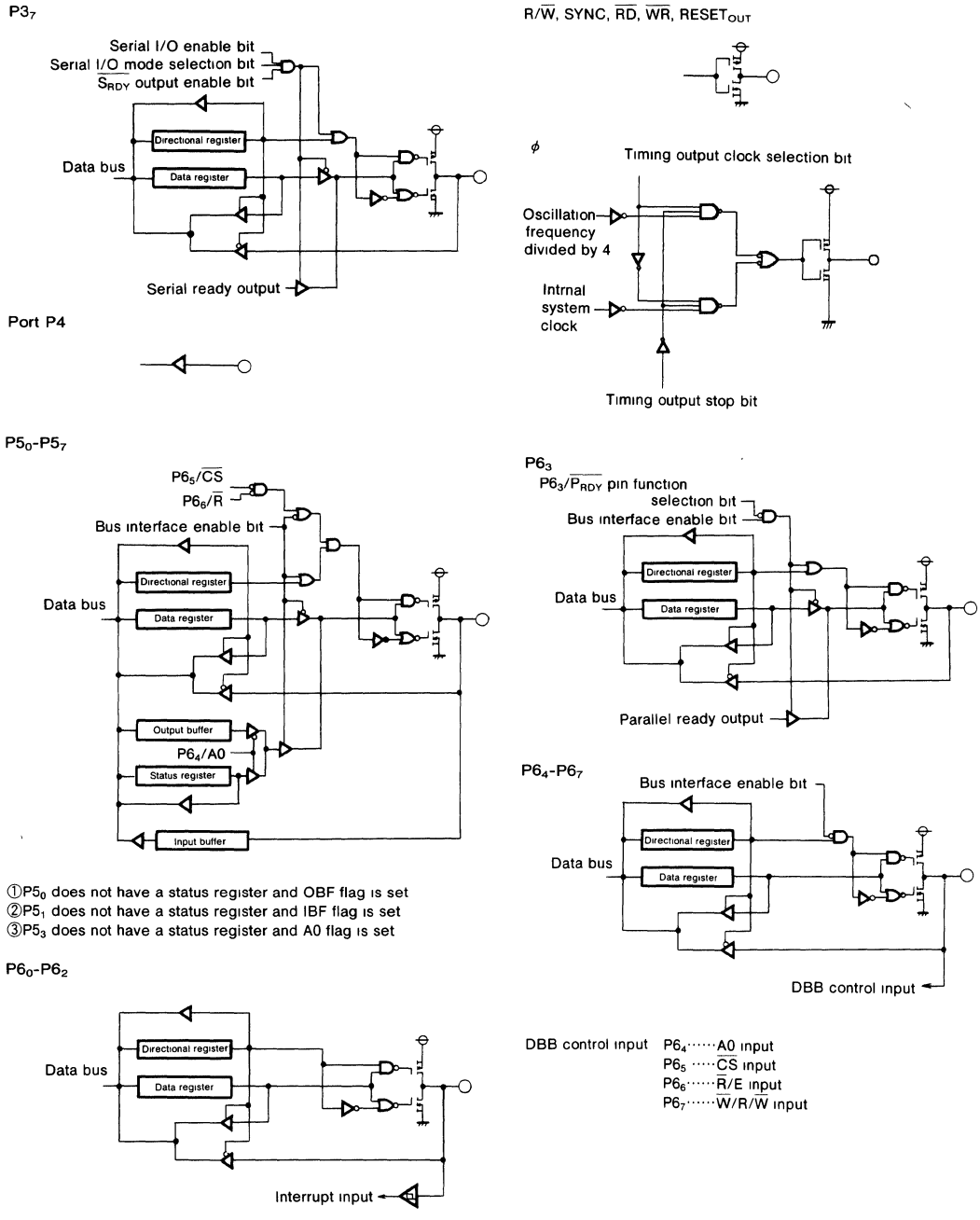


Fig. 35 Ports P0-P6 block diagram (single-chip mode) and output only pin output format (2)

PROCESSOR MODE

By changing the contents of the processor mode bits (bits 0 and 1 at address $00DF_{16}$), three different operation modes can be selected; single-chip mode, memory expansion mode, and microprocessor mode.

In the memory expansion mode and the microprocessor mode, ports P0-P2 can be used as address, and data input/output pins.

Figure 37 shows the functions of ports P0-P2

The memory map for the single-chip mode is shown in Figure 2 and for other modes, in Figure 36.

By connecting CNV_{SS} to V_{SS}, all three modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into microprocessor mode.

The three different modes are explained as follows

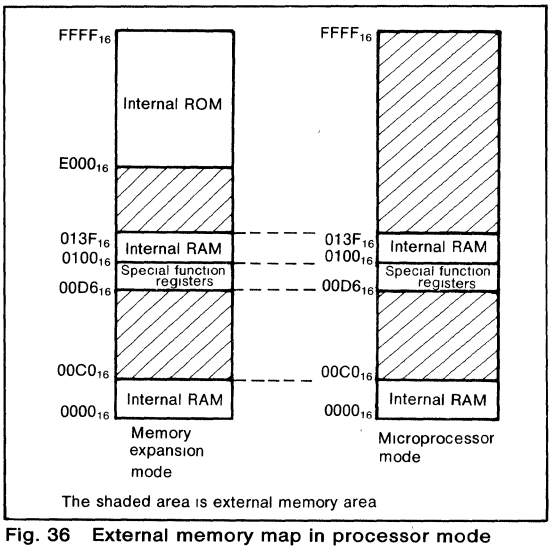


Fig. 36 External memory map in processor mode (M37451M4)

(1) Single-chip mode [00]

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0-P2 will work as original I/O ports.

(2) Memory expansion mode [01]

The microcomputer will be placed in the memory expansion mode when CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "01" This mode is used to add external memory when the internal memory is not sufficient.

In this mode, port P0 and port P1 are as a system address bus and the original I/O pin function is lost.

Port P2 becomes the data bus of D_7-D_0 (including instruction code) and loses its normal I/O functions.

(3) Microprocessor mode [10]

After connecting CNV_{SS} to V_{CC} and initiating a reset or connecting CNV_{SS} to V_{SS} and the processor mode bits are set to "10", the microcomputer will automatically default to this mode. In this mode, the internal ROM is disabled so the external memory is required. Other functions are same as the memory expansion mode. The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 3.

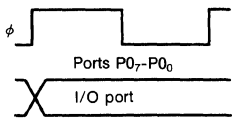
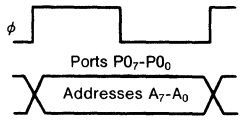
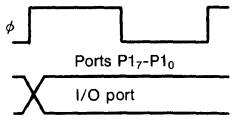
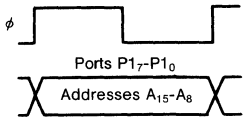
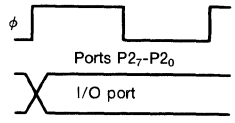
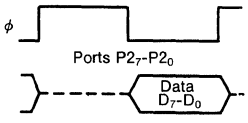
Port \ Mode	CM_1 = 0, CM_0 = 0: Single-chip mode	CM_1 = 0, CM_0 = 1: Memory expansion mode	CM_1 = 1, CM_0 = 0: Microprocessor mode
Port P0			Same as left
Port P1			Same as left
Port P2			Same as left

Fig. 37 Processor mode and function of ports P0-P2

Table 3. Relationship between CNV_{SS} pin input level and processor mode

CNV_{SS}	Mode	Explanation
V_{SS}	• Single-chip mode • Memory expansion mode • Microprocessor mode	The single-chip mode is set by the reset All modes can be selected by changing the processor mode bit with the program
V_{CC}	• Microprocessor mode	The microprocessor mode is set by the reset

CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 40.

When an STP instruction is executed, the internal clock ϕ stops oscillating at "H" level. At the same time, FF_{16} is set in the low-order byte of timer 1, 03_{16} is set in the high-order byte, and timer 1 count source is forced to $f(X_{IN})$ divided by four. This connection is cleared when timer 1 overflows or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the clock ϕ keeps its "H" level until timer 1 overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used

When the WIT instruction is executed, the clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction. Especially, to return from the stop status, the timer 1 count enable bit must be set to "1" and the timer 1 interrupt enable bit must be set to "0" before executing STP instruction.

With the M37451, the MISRG2 bit 6 shown in Figure 22 can be used to double the bus cycle. However, the timer, UART, and PWM operations are unafffected. This facilitates accessing of slow peripheral LSIs when external memory and I/O are extended in memory expansion mode or microprocessor mode. Note that this bit also affects the bus cycle in single-chip mode.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 38.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock usage is shown in Figure 39. X_{IN} is the input, and X_{OUT} is open.

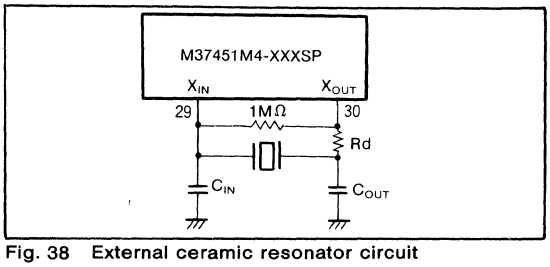


Fig. 38 External ceramic resonator circuit

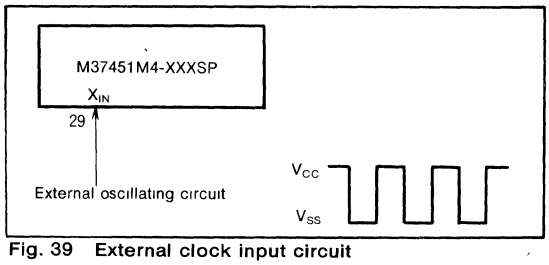


Fig. 39 External clock input circuit

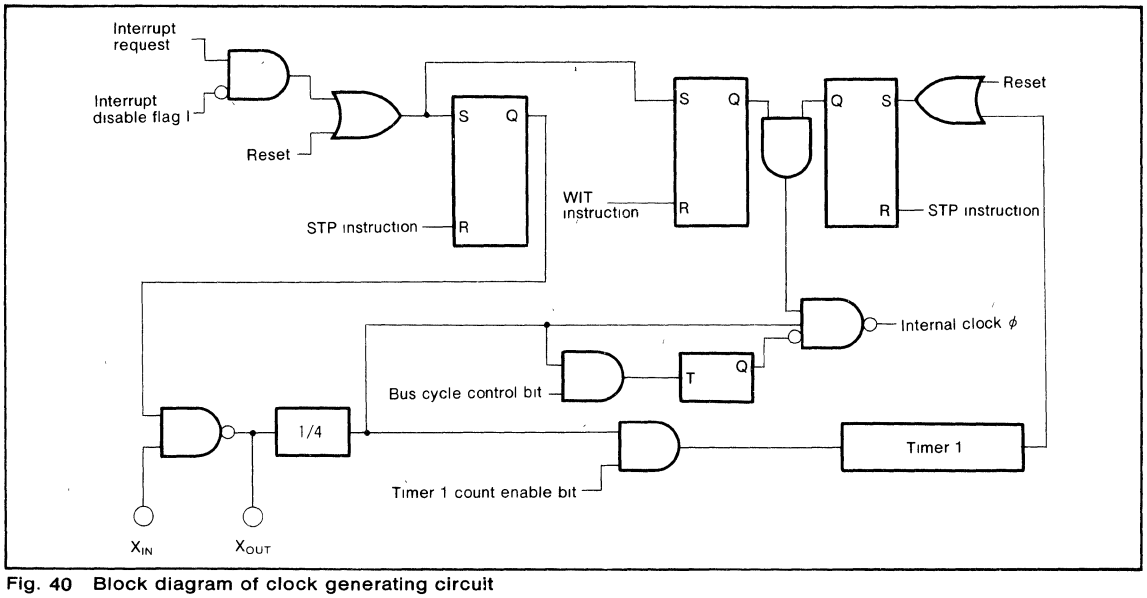


Fig. 40 Block diagram of clock generating circuit

PROGRAMMING NOTES

(1) Processor status register
1. Except for the interrupt disable flag (I) being set to "1", the content of the processor status register (PS) is unpredictable after a reset. Therefore, flags affecting program execution must be initialized.
The T flag and D flag which affect arithmetic operations, must always be initialized.
2. An NOP instruction must be used after the execution of a PLP instruction.

(2) Interrupts
Even though the BBC and BBS instructions are executed just after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as an NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.

(3) Decimal operations
1. Decimal operations are performed by setting the decimal mode flag (D) and executing the ADC or SBC instruction In this case, there must be at least one instruction following the ADC or SBC instruction before executing the SEC, CLC, or CLD instruction.
2. The N (Negative), V(Overflow), and Z(Zero) flags are ignored during decimal mode.

(4) Timers
1. The frequency dividing ratio when n (0 to 65535) is written in the timer latch is 1/(n+1).
2. When directly writing a value in the timer, set the count enable bit to count disable (0) and write in the low-order byte first and then in the high-order byte.
3. The timer value must be read from the high-order byte first.

(5) Serial I/O
In clock synchronous serial I/O mode, if the receiver is to output an $\overline{S_{RDY}}$ using an external clock, the receive enable bit, $\overline{S_{RDY}}$ output enable bit, and transmission enable bit must be set to "1"

(6) A-D conversion
The comparator consists of coupling capacitors that lose their charge when the clock frequency is low. Therefore,f(X_{IN})must be no less than 1MHz during A-D conversion. (If the bus cycle control bit is "1", the bus cycle is doubled and the A-D conversion time is also doubled, therefore, f (X_{IN}) must not be less than 2MHz.) Also, the STP and WIT instructions must not be executed during A-D conversion

(7) STP instruciton
The STP instruction must be executed after setting the timer 1 count enable bit (bit 4 at address $00DE_{16}$) to enable ("1").

(8) Multiply/Divide instructions
1. The MUL and DIV instructions are not affected by the T and D flags.
2. The contents of the processor status register are unaffected by multiply or divide instructions.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.
- mask ROM order confirmation form
- mark specification form
- ROM data·····EPROM 3 sets

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "off" state	−0.3 to 7	V
V_I	Input voltage X_{IN}, $\overline{RESET}$		−0.3 to 7	V
V_I	Input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, ADV_{REF}, DAV_{REF}, V_{REF}, AV_{CC}		−0.3 to V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3 to 13	V
V_O	Output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, X_{OUT}, ϕ, R/$\overline{W}$, $\overline{RD}$, $\overline{WR}$, SYNC, $RESET_{OUT}$		−0.3 to V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000(Note 1)	mW
Topr	Operating temperature		−20 to 85	℃
Tstg	Storage temperature		−40 to 125	℃

Note 1 : 500mW in case of the flat package

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=−20 to 85℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, CNV_{SS} (Note 1)	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (expect Note 1)	2.0		V_{CC}	V
V_{IL}	"L" input voltage CNV_{SS} (Note 1)	0		0.2V_{CC}	V
V_{IL}	"L" input voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (expect Note 1)	0		0.8	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note 2)			5	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			−10	mA
$I_{OH(avg)}$	"H" average output current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note 2)			−5	mA
$f(X_{IN})$	Internal clock oscillating frequency	1		12.5	MHz

Note 1 : Ports operating as special function pins INT_1-INT_3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_XD($P3_4$), S_{CLK}($P3_6$)

2 : $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average current in 100ms

3 : The total of I_{OL} of Port P0, P1, and P2 should be 40mA (max)
The total of I_{OL} of Port P3, P5, P6, R/$\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ should be 40mA (max)
The total of I_{OH} of Port P0, P1, and P2 should be 40mA (max)
The total of I_{OH} of Port P3, P5, P6, R/$\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$, and ϕ should be 40mA (max)

ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}= 0 V, T_a=−20 to 85℃, f(X_{IN})=12.5MHz)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	"H" output voltage $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	I_{OH} =− 2 mA	V_{CC}−1			V
V_{OH}	"H" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	I_{OH} =− 5 mA	V_{CC}−1			V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	I_{OL} =2 mA			0.45	V
V_{OL}	"L" output voltage $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	I_{OL} =5 mA			1	V
$V_{T+}-V_{T-}$	Hysteresis INT1-INT3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_XD($P3_4$), S_{CLK}($P3_6$)	Function input level	0.3		1	V
$V_{T+}-V_{T-}$	Hysteresis $\overline{RESET}$				0.7	V
$V_{T+}-V_{T-}$	Hysteresis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	V_I =V_{SS}	−5		5	μA
I_{IH}	"H" input current $P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	V_I =V_{CC}	−5		5	μA
V_{RAM}	RAM retention voltage	At stop mode	2			V
I_{CC}	Supply current	f(X_{IN})=12.5MHz At system operation		8	15	mA
		At stop mode (Note 1)		1	10	μA

Note 1 : The terminals $\overline{RD}$, $\overline{WR}$, SYNC, R/$\overline{W}$, $RESET_{OUT}$, ϕ, D-A_1 and D-A_2 are all open The other ports, which are in the input mode, are connected to V_{SS} A-D converter is in the A-D completion state The current through ADV_{REF} and DAV_{REF} is not included. (Fig 45)

A-D CONVERTER CHARACTERISTICS

(V_{CC}=AV_{CC}=5V±10%, V_{SS}=AV_{SS}= 0 V, T_a =−20 to 85℃, f(X_{IN})=12.5MHz unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=AV_{CC}=ADV_{REF}=5V±10%		±1.5	±3	LSB
t_{CONV}	Conversion time				49	$t_{c(\phi)}$
V_{IA}	Analog input voltage		AV_{SS}		AV_{CC}	V
V_{ADVREF}	Reference input voltage		2		V_{CC}	V
R_{LADDER}	Ladder resistance value	ADV_{REF}= 5 V	20	35	50	kΩ
$I_{IADVREF}$	Reference input current	ADV_{REF}= 5 V	0.1	0.14	0.25	mA
V_{AVCC}	Analog power supply input voltage			V_{CC}		V
V_{AVSS}	Analog power supply input voltage			0		V

D-A CONVERTER CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=AV_{SS}= 0 V, T_a =−20 to 85℃ unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Full scale deviation	V_{CC}=DAV_{REF}=5V±10%			1.0	%
t_{SU}	Set time				3	μs
R_O	Output resistance		1	2	4	kΩ
V_{AVSS}	Analog power supply input voltage			0		V
V_{DAVREF}	Reference input voltage		4		V_{CC}	V
I_{DAVREF}	Reference power input current		0	5	10	mA

TIMING REQUIREMENTS

Port/single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(P0D-\phi)}$	Port P0 input setup time	Fig 41	160			ns
$t_{su(P1D-\phi)}$	Port P1 input setup time		160			ns
$t_{su(P2D-\phi)}$	Port P2 input setup time		160			ns
$t_{su(P3D-\phi)}$	Port P3 input setup time		160			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time		160			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time		160			ns
$t_{su(P6D-\phi)}$	Port P6 input setup time		160			ns
$t_{h(\phi-P0D)}$	Port P0 input hold time		40			ns
$t_{h(\phi-P1D)}$	Port P1 input hold time		40			ns
$t_{h(\phi-P2D)}$	Port P2 input hold time		40			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		40			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		40			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time		40			ns
$t_{h(\phi-P6D)}$	Port P6 input hold time		40			ns
$t_C(X_{IN})$	External clock input cycle time		80		1000	ns
$t_W(X_{IN}L)$	External clock input "L" pulse width		20			ns
$t_W(X_{IN}H)$	External clock input "H" pulse width		20			ns
$t_r(X_{IN})$	External clock rising edge time				20	ns
$t_f(X_{IN})$	External clock falling edge time				20	ns

Master CPU bus interface timing ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(CS-R)}$	$\overline{CS}$ setup time	Fig 42	0			ns
$t_{su(CS-W)}$	$\overline{CS}$ setup time		0			ns
$t_{h(R-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{h(W-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-R)}$	A0 setup time		10			ns
$t_{su(A-W)}$	A0 setup time		10			ns
$t_{h(R-A)}$	A0 hold time		0			ns
$t_{h(W-A)}$	A0 hold time		0			ns
$t_{W(R)}$	Read pulse width		120			ns
$t_{W(W)}$	Write pulse width		120			ns
$t_{su(D-W)}$	Date input setup time before write		50			ns
$t_{h(W-D)}$	Date input hold time after write		0			ns

Master CPU bus interface timing (R/$\overline{W}$ type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(CS-E)}$	$\overline{CS}$ setup time	Fig 42	0			ns
$t_{h(E-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-E)}$	A0 setup time		10			ns
$t_{h(E-A)}$	A0 hold time		0			ns
$t_{su(RW-E)}$	R/$\overline{W}$ setup time		0			ns
$t_{h(E-RW)}$	R/$\overline{W}$ hold time		0			ns
$t_{W(EL)}$	Enable clock "L" pulse width		120			ns
$t_{W(EH)}$	Enable clock "H" pulse width		120			ns
$t_{r(E)}$	Enable clock rising edge time				25	ns
$t_{f(E)}$	Enable clock falling edge time				25	ns
$t_{su(D-E)}$	Data input setup time before write		50			ns
$t_{h(E-D)}$	Data input hold time after write		0			ns

Local bus/memory expansion mode, microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(D-\phi)}$	Data input setup time	Fig 43	60			ns
$t_{h(\phi-D)}$	Data input hold time		0			ns
$t_{su(D-RD)}$	Data input setup time		60			ns
$t_{h(RD-D)}$	Data input hold time		0			ns

Clock synchronous serial I/O

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(RxD-SCLK)}$	Serial input setup time	Fig. 44	160			ns
$t_{h(SCLK-RxD)}$	Serial input hold time		80			ns
$t_{r(RxD)}$	Serial input rising edge time				30	ns
$t_{f(RxD)}$	Serial input falling edge time				30	ns
$t_{r(SCLK)}$	Serial input clock rising edge time				30	ns
$t_{f(SCLK)}$	Serial input clock falling edge time				30	ns
$t_{C(SCLK)}$	Serial input clock period		640			ns
$t_{w(SCLKL)}$	Serial input clock "L" pulse width		290			ns
$t_{w(SCLKH)}$	Serial input clock "H" pulse width		290			ns

SWITCHING CHARACTERISTICS

Port/single-chip mode (V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{d(\phi-P0Q)}$	Port P0 data output delay time	Fig 41			200	ns
$t_{d(\phi-P1Q)}$	Port P1 data output delay time				200	ns
$t_{d(\phi-P2Q)}$	Port P2 data output delay time				200	ns
$t_{d(\phi-P3Q)}$	Port P3 data output delay time				200	ns
$t_{d(\phi-P5Q)}$	Port P5 data output delay time				200	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				200	ns
$t_{c(\phi)}$	Cycle time		320		4000	ns
$t_{w(\phi H)}$	ϕ clock pulse width ("H" level)		150			ns
$t_{w(\phi L)}$	ϕ clock pulse width ("L" level)		130			ns
$t_{r(\phi)}$	ϕ clock rising edge time				20	ns
$t_{f(\phi)}$	ϕ clock falling edge time				20	ns

Master CPU bus interface ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{a(R-D)}$	Data output enable time after read	Fig 42			80	ns
$t_{v(R-D)}$	Data output disable time after read		0		30	ns
$t_{PLH(R-PR)}$	P_{RDY} output transmission time after read				150	ns
$t_{PLH(W-PR)}$	$\overline{P_{RDY}}$ output transmission time after write				150	ns

Master CPU bus interface (R/$\overline{W}$ type mode) (V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{a(E-D)}$	Data output enable time after read	Fig.42			80	ns
$t_{v(E-D)}$	Data output disable time after read		0		30	ns
$t_{PLH(E-PR)}$	$\overline{P_{RDY}}$ output transmission time after E clock				150	ns

Local bus/memory expansion mode, microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{d(\phi-A)}$	Address delay time after ϕ	Fig 43			80	ns
$t_{v(\phi-A)}$	Address effective time after ϕ		10			ns
$t_{v(RD-A)}$	Address effective time after $\overline{RD}$		10			ns
$t_{v(WR-A)}$	Address effective time after $\overline{WR}$		10			ns
$t_{d(\phi-D)}$	Data output delay time after ϕ				80	ns
$t_{d(WR-D)}$	Data output delay time after $\overline{WR}$				80	ns
$t_{v(\phi-D)}$	Data output effective time after ϕ		20			ns
$t_{v(WR-D)}$	Data output effective time after $\overline{WR}$		20			ns
$t_{d(\phi-RW)}$	R/$\overline{W}$ delay time after ϕ				80	ns
$t_{d(\phi-SYNC)}$	SYNC delay time after ϕ				80	ns
$t_{w(RD)}$	$\overline{RD}$ pulse width		130			ns
$t_{w(WR)}$	$\overline{WR}$ pulse width		130			ns

Clock synchronous serial I/O (V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max.	
$t_{d(SCLK-TXD)}$	Serial output delay time	Fig 44			100	ns
$t_{r(SCLK)}$	Serial output clock rising edge time				30	ns
$t_{f(SCLK)}$	Serial output clock falling edge time				30	ns
$t_{c(SCLK)}$	Serial output clock period		640			ns
$t_{w(SCLKL)}$	Serial output clock "L" pulse width		290			ns
$t_{w(SCLKH)}$	Serial output clock "H" pulse width		290			ns

TEST CONDITION

Input voltage level : V_{IH} 2.4V
V_{IL} 0.45V
Output test level : V_{OH} 2.0V
V_{OL} 0.8V

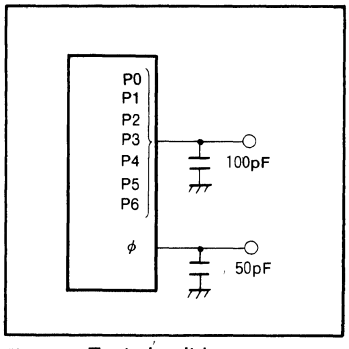


Fig. 41 Test circuit in single-chip mode

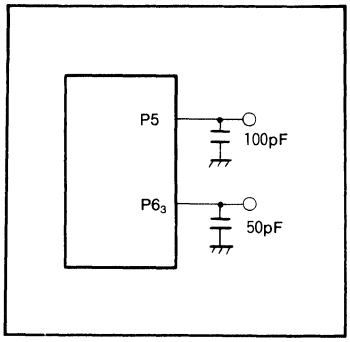


Fig. 42 Master CPU bus interface test circuit

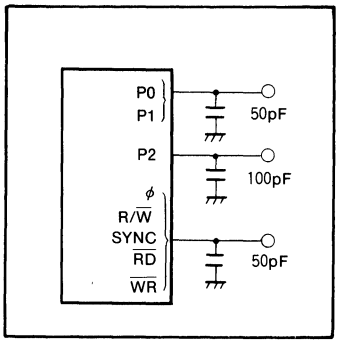


Fig. 43 Local bus test circuit

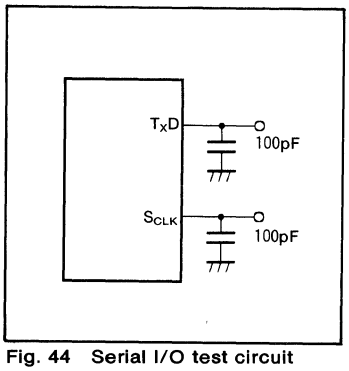


Fig. 44 Serial I/O test circuit

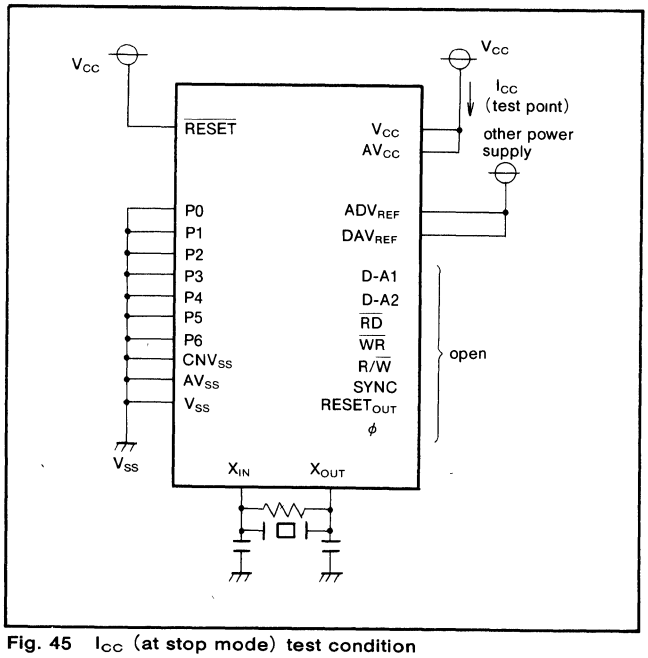
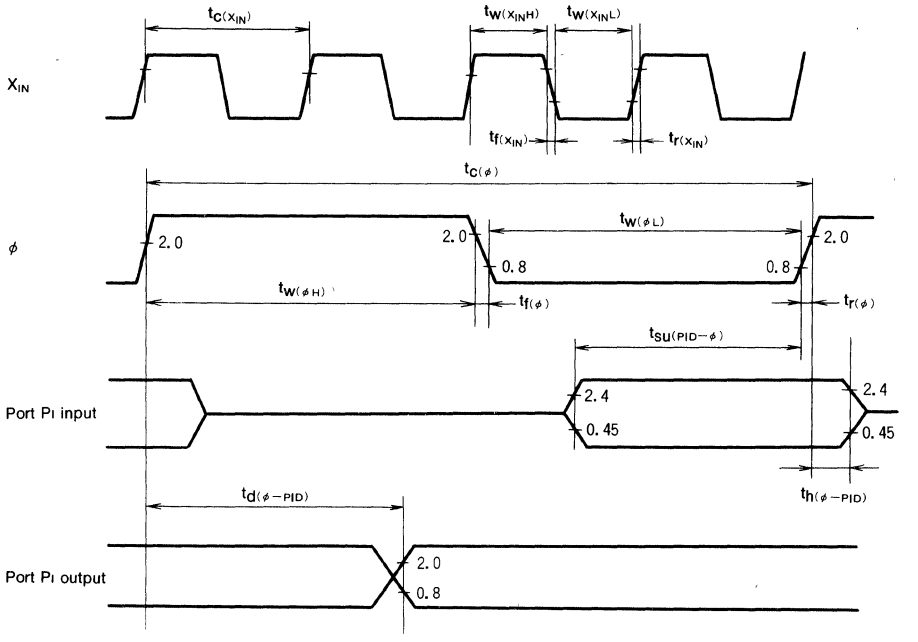


Fig. 45 I_{CC} (at stop mode) test condition

TIMING DIAGRAM

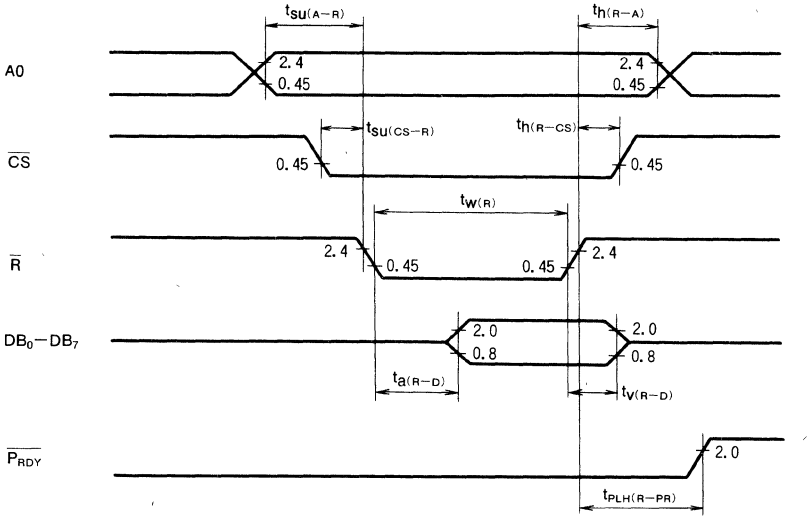
Port/single-chip mode timing diagram



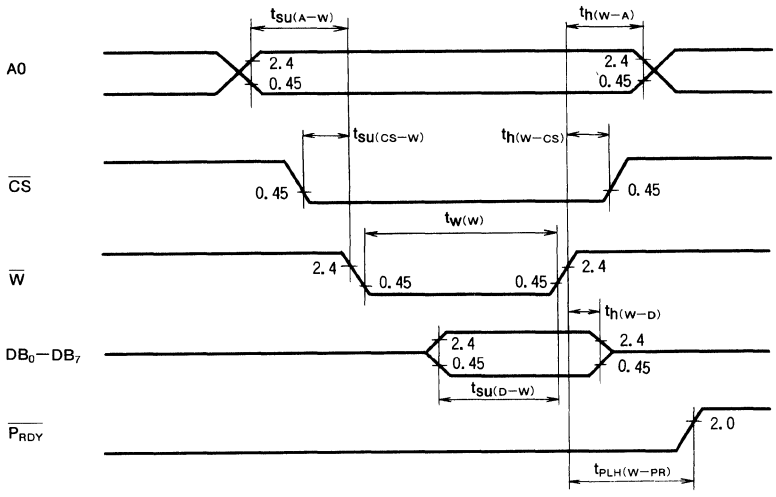
Note : V_{IH}=0.8V_{CC}, V_{IL}=0.16V_{CC} of X_{IN}

Master CPU bus interface/ $\overline{R}$ and $\overline{W}$ separation type timing diagram

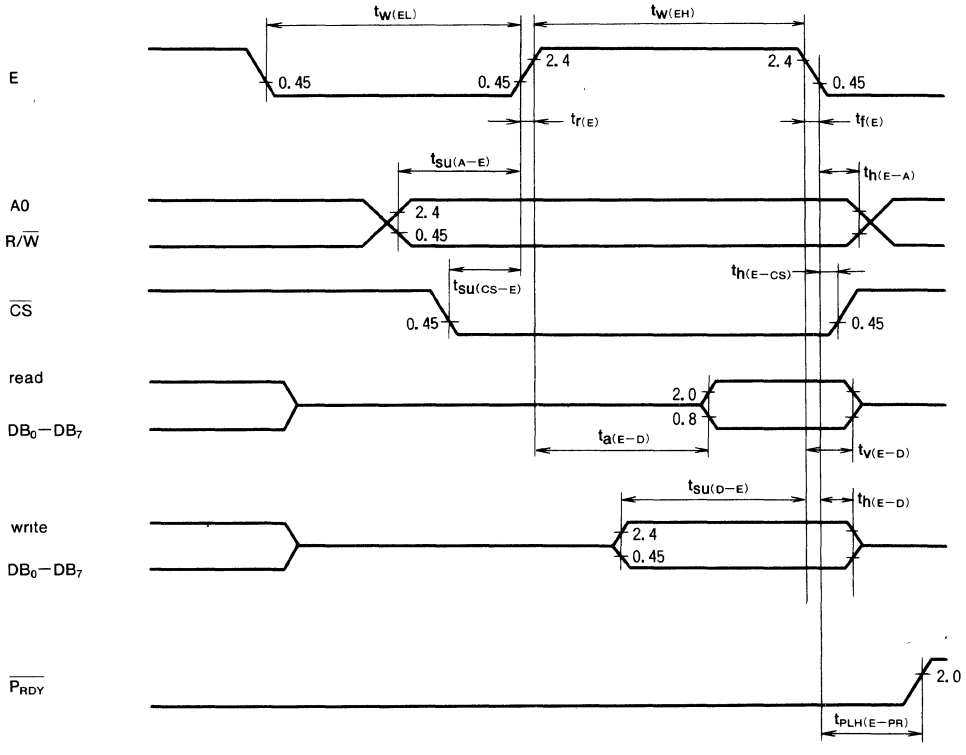
Read



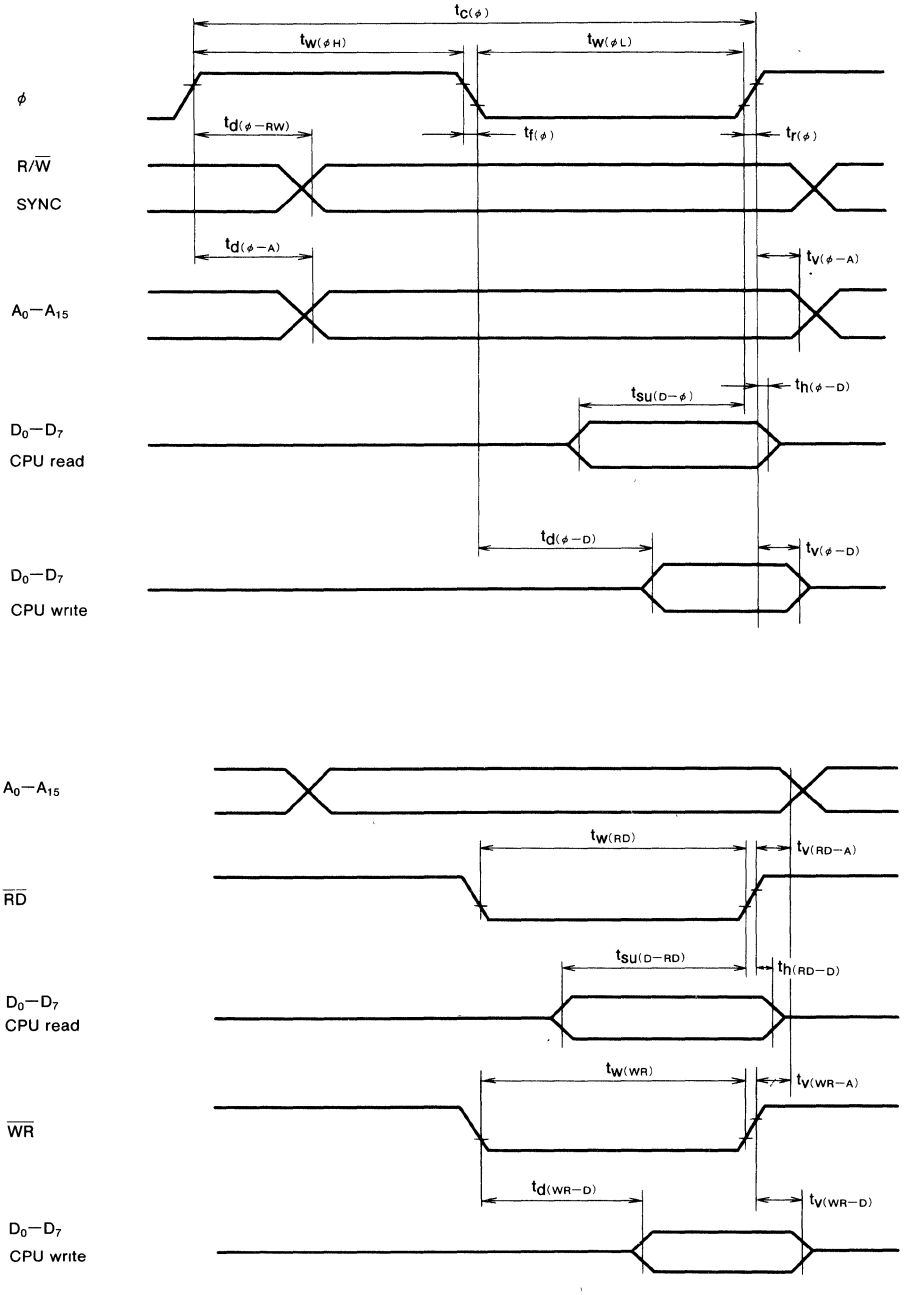
Write



Master CPU interface/ R/$\overline{W}$ type timing diagram



Local bus timing diagram



Serial I/O timing diagram