M37451SSP/FP/GP

8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37451SSP/FP/GP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP or a 0.8mm pitch or 0.65mm pitch 80-pin plastic molded QFP. In addition to its simple instruction sets, the ROM, RAM and I/O addresses are placed on the same memory map to enable easy programming. It is suited for office automation equipment and control devices. The low power consumption made possible by the use of a CMOS process makes it especially suitable for battery powered devices requiring low power consumption. It also has a unique feature that enables it to be used as a slave microcomputer.

M37451SSP/FP/GP has basically the same functions as M37451M4-XXXSP/FP/GP except the RAM size and the fact that these three need external ROM area.

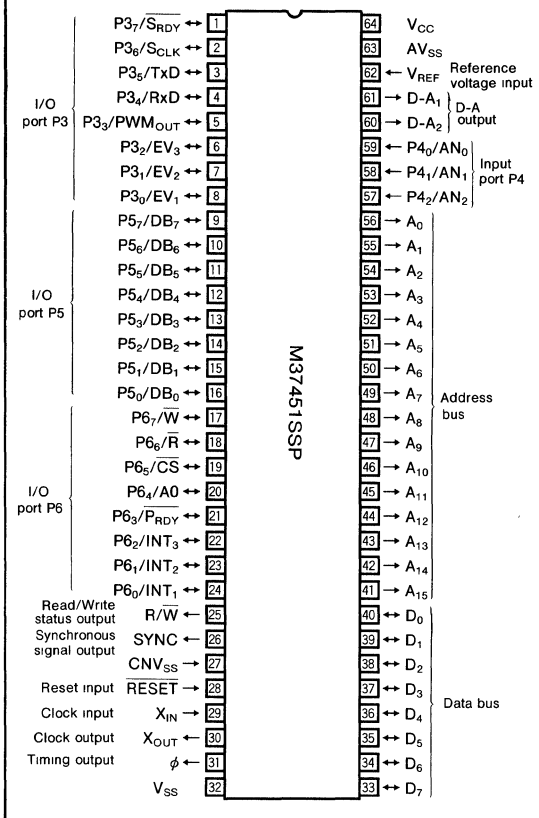
FEATURES

- Number of basic instructions 71
  69 MELPS 740 basic instructions + 2 multiply/divide instructions
- Memory size ROM ..... None
  RAM ..... 1024 bytes
- Instruction execution time
  (minimum instructions at 12.5 MHz frequency) 0.64 μs
- Single power supply ..... 5V $\pm$ 10%
- Power dissipation normal operation mode
  (at 12.5MHz frequency) 40mW
- Subroutine nesting ..... 128 levels max.
- Interrupt ..... 15 events
- Master CPU bus interface ..... 1 byte
- 16-bit timer 3
- 8-bit timer (Serial I/O use) 1
- Serial I/O (UART or clock synchronous) 1
- A-D converter (8-bit resolution) ..... 3 channels (DIP)
  8 channels (QFP)
- D-A converter (8-bit resolution) ..... 2 channels
- PWM output with 8-bit prescaler
  (Either resolution 8-bit or 16-bit is software selectable) 1
- Programmable I/O
  (Ports P3, P5, P6) 24
- Input (Port P4) ..... 3 (DIP), 8 (QFP)
- Output (Port D-A_1, D-A_2) 2

APPLICATION

Slave controller for PPCs, facsimiles and page printers
HDD, optical disk, inverter and industrial motor controllers
Industrial robots and machines

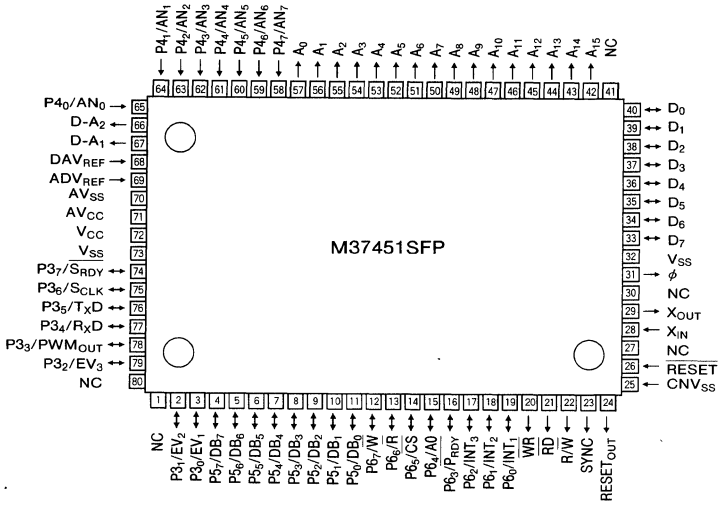
PIN CONFIGURATION (TOP VIEW)



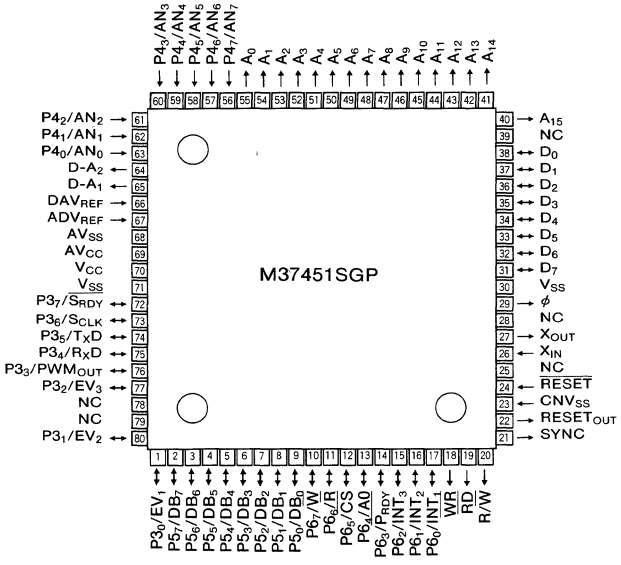
Outline 64P4B

MITSUBISHI ELECTRIC

PIN CONFIGURATION (TOP VIEW)



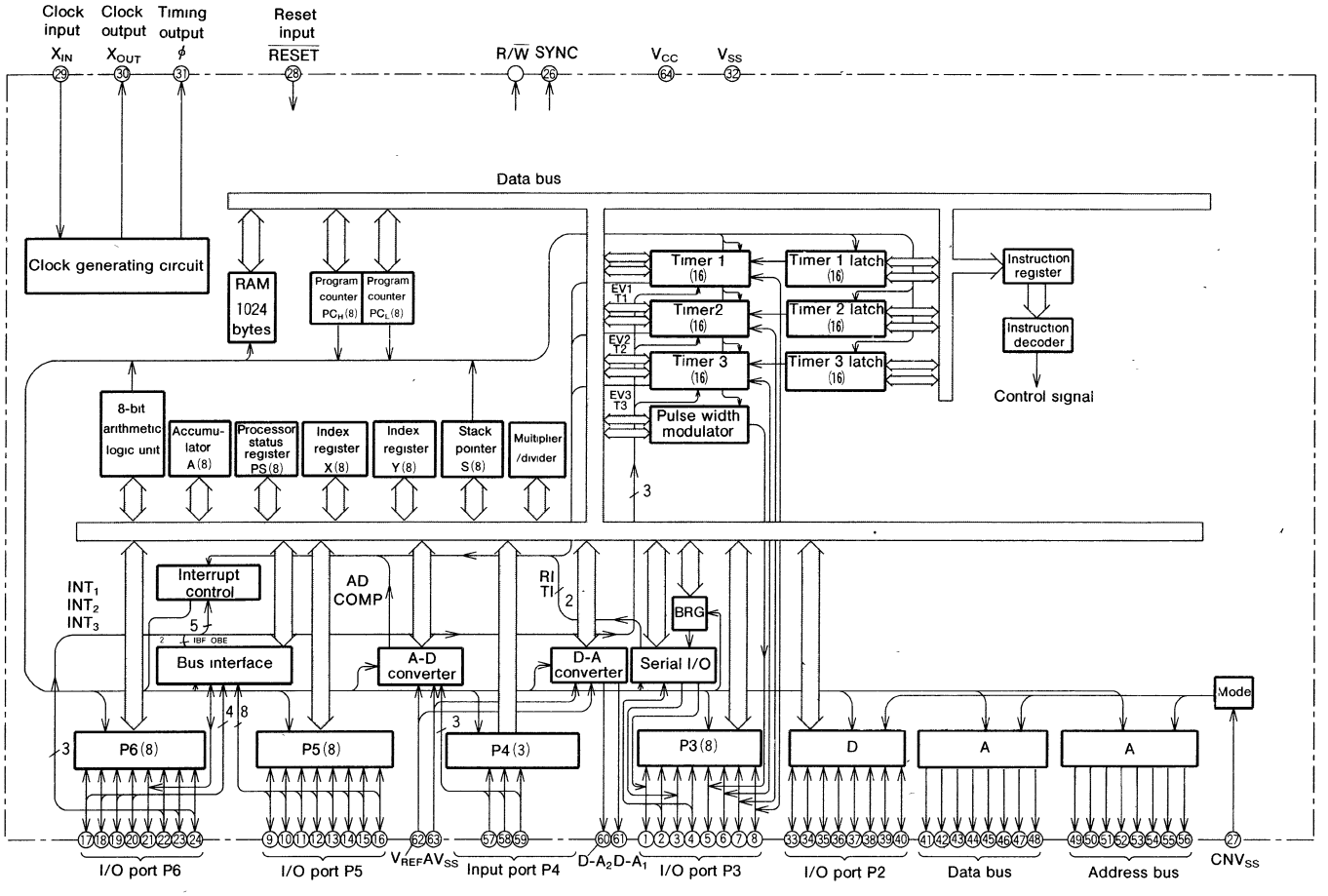
Outline 80P6N



Outline 80P6S

NC : No connection

M37451SSP BLOCK DIAGRAM



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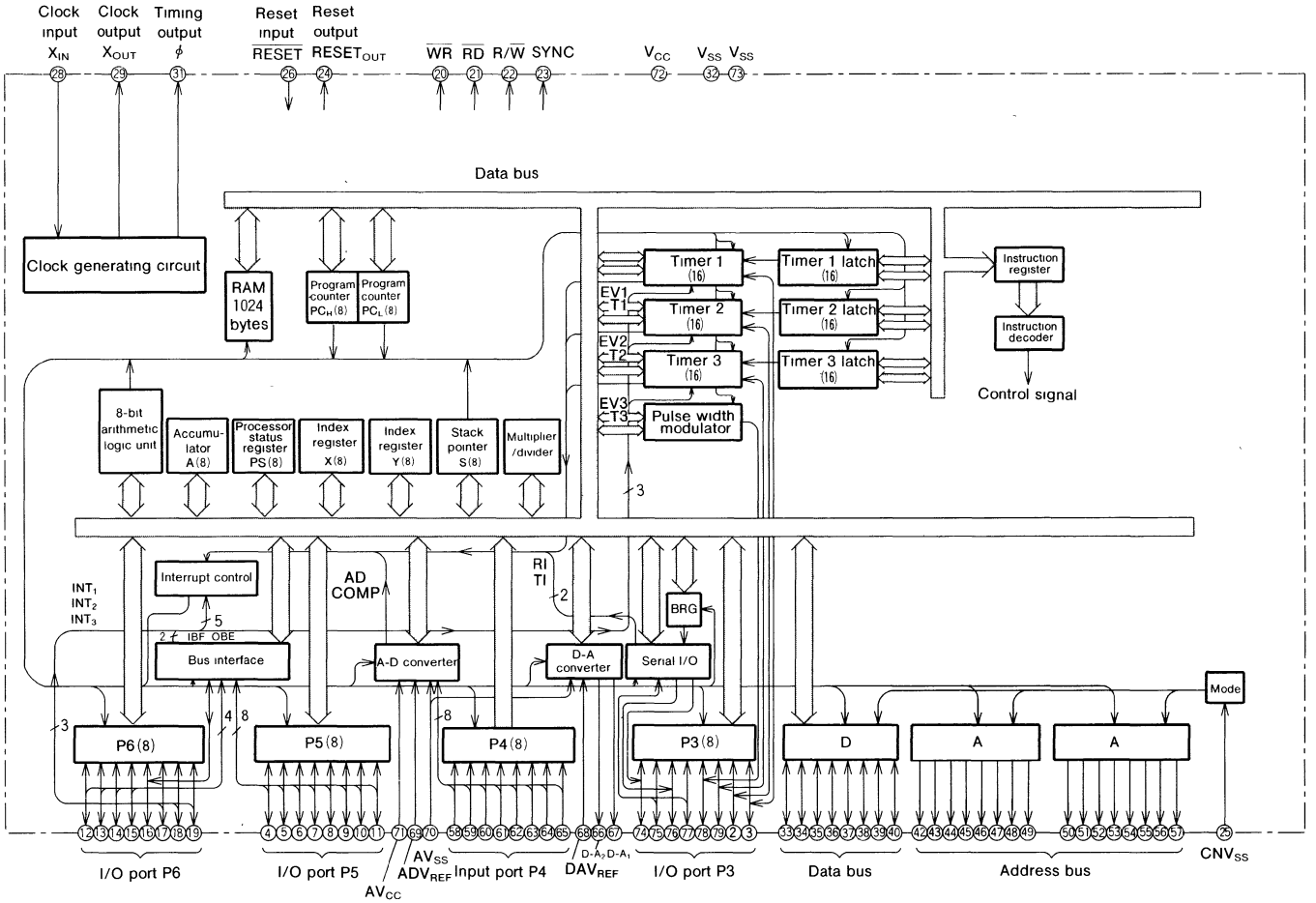
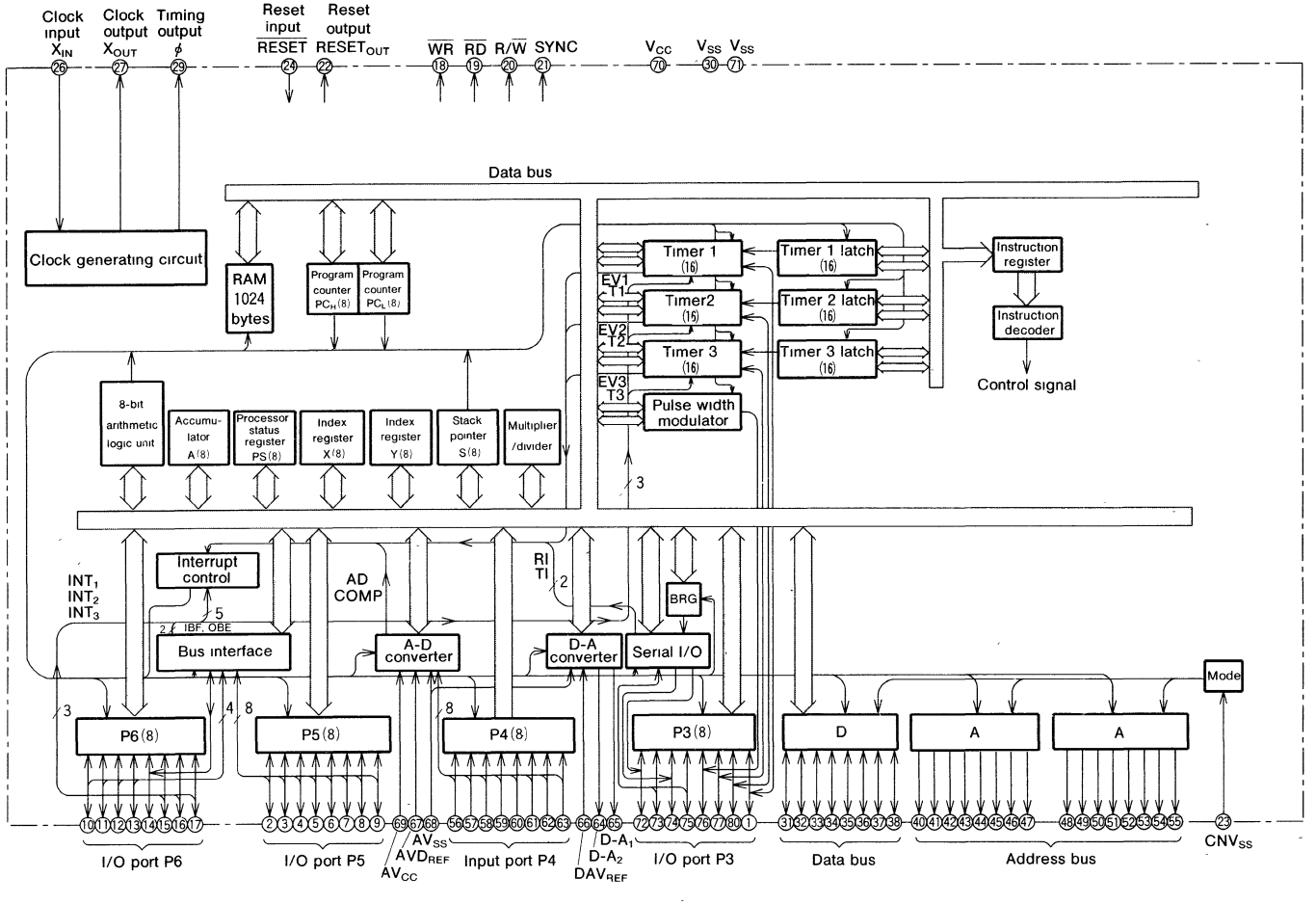
M37451SFP BLOCK DIAGRAM



M37451SGP BLOCK DIAGRAM



MITSUBISHI ELECTRIC

FUNCTIONS OF M37451SSP/FP/GP

Parameter			Functions
Number of basic instructions			71(69 MELPS 740 basic instructions+2)
Instruction execution time			0.64μs(minimum instructions, at 12.5MHz frequency)
Clock frequency			12.5MHz(max.)
RAM size	M37451SSP/FP/GP		1024 bytes
Input/Output port	P3, P5, P6	I/O	8-bit×3
	P4	Input	3-bit×1(8-bit×1 for 80-pin model)
	D-A	Output	2-bit×1
Serial I/O			UART or clock synchronous
Timers			16-bit timer×3, 8-bit timer(serial I/O baud rate generator)×1
A-D converter			8-bit×3 channels(8 channels for 80-pin model)
D-A converter			8-bit×2 channels
Pulse width modulator(with 8-bit prescaler)			8-bit or 16-bit×1
Data bus buffer			1-byte input and output each
Subroutine nesting			128-levels (max.)
Interrupt			6 external interrupts, 8 internal interrupts, 1 software interrupt
Clock generating circuit			Built-in(ceramic or quarts crystal oscillator)
Supply voltage			5V±10%
Power dissipation			40mW(at 12.5MHz frequency)
Input/Output characters	Input/Output voltage		5V
	Output current		±5mA(max.)
Operating temperature range			−20 to 85℃
Device structure			CMOS silicon gate
Package	M37451SSP		64-pin shrink plastic molded DIP
	M37451SFP		80-pin plastic molded QFP(0.8mm pitch)
	M37451SGP		80-pin plastic molded QFP(0.65mm pitch)

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Supply voltage		Power supply inputs 5V±10% to V_{CC}, and 0V to V_{SS}
CNV_{SS}	CNV_{SS}	Input	This is connected to V_{CC}
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 8 clock cycles(under normal V_{CC} conditions) If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X_{IN} and X_{OUT} pins If an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open
X_{OUT}	Clock output	Output	
ϕ	Timing output	Output	Normally outputs signal consisting of oscillating frequency divided by four
SYNC	Synchronous signal output	Output	This signal is output "H" during operation code fetch and is used to control single stepping of programs
R/$\overline{W}$	Read/Write status output	Output	This signal determines the direction of the data bus It is "H" during read and "L" during write
A_0-A_{15}	Address bus	Output	This is 16-bit address bus
D_0-D_7	Data bus	I/O	This is 8-bit data bus
$P3_0$-$P3_7$	Input/Output port P3	I/O	Port P3 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programed as input or output The output structure is CMOS output Serial I/O, PWM output, or even I/O function can be selected with a program
$P4_0$-$P4_2$ ($P4_0$-$P4_7$)	Input port P4	Input	Analog input pin for the A-D converter The 64-pin model has three pins and the 80-pin model has eight pins They may also be used as digital input pins
$P5_0$-$P5_7$	Input/Output port P5	I/O	An 8-bit input/output port with the same function as P3 This port functions as an 8-bit data bus for the master CPU when slave mode is selected with a program
$P6_0$-$P6_7$	Input/Output port P6	I/O	An 8-bit input/output port with the same function as P3 Pins $P6_3$-$P6_7$ change to a control bus for the master CPU when slave mode is selected with a program Pins $P6_0$-$P6_2$ may be programmed as external interrupt input pins
D-A_1, D-A_2	D-A output	Output	Analog signal from D-A converter is output
V_{REF}	Reference voltage input	Input	Reference voltage input pin for A-D and D-A converter This pin is for 64-pin model only
ADV_{REF}	A-D reference voltage input	Input	Reference voltage input pin for A-D converter This pin is for 80-pin model only
DAV_{REF}	D-A reference voltage input	Input	Reference voltage input pin for D-A converter This pin is for 80-pin model only
AV_{SS}	Analog power supply		Ground level input pin for A-D and D-A converter Same voltage as V_{SS} is applied
AV_{CC}	Analog power supply		Power supply input pin for A-D converter This pin is for 80-pin model only Same voltage as V_{CC} is applied In the case of the 64-pin model AV_{CC} is connected to V_{CC} internally
$\overline{RD}$	Read signal output	Output	Control signal output as active "L" when valid data is read from data bus This pin is for 80-pin model only
$\overline{WR}$	Write signal output	Output	Control signal output as active "L" when writing data from data bus to external component This pin is for 80-pin model only
$RESET_{OUT}$	Reset output	Output	Control signal output as active "H" during reset It is used as a reset output signal for peripheral components This pin is for 80-pin model only

BASIC FUNCTION BLOCKS

The differences between M37451M4-XXXSP/FP/GP and M37451SSP/FP/GP are noted below. Other functions are the same as M37451M4-XXXSP/FP/GP in microprocessor mode.

MEMORY

• Special Function Register (SFR) Area

The special function register (SFR) area contains the registers relating to functions such as I/O ports and timers.

• RAM

RAM is used for data storage as well as a stack area.

• Interrupt Vector Area

The interrupt vector area is for storing jump destination addresses used at reset or when an interrupt is generated. (This area must be located in ROM area)

• Zero Page

Zero page addressing mode is useful because it enables access to this area with only 2 bytes,

• Special Page

Special page addressing mode is useful because it enables access to this area with only 2 bytes.

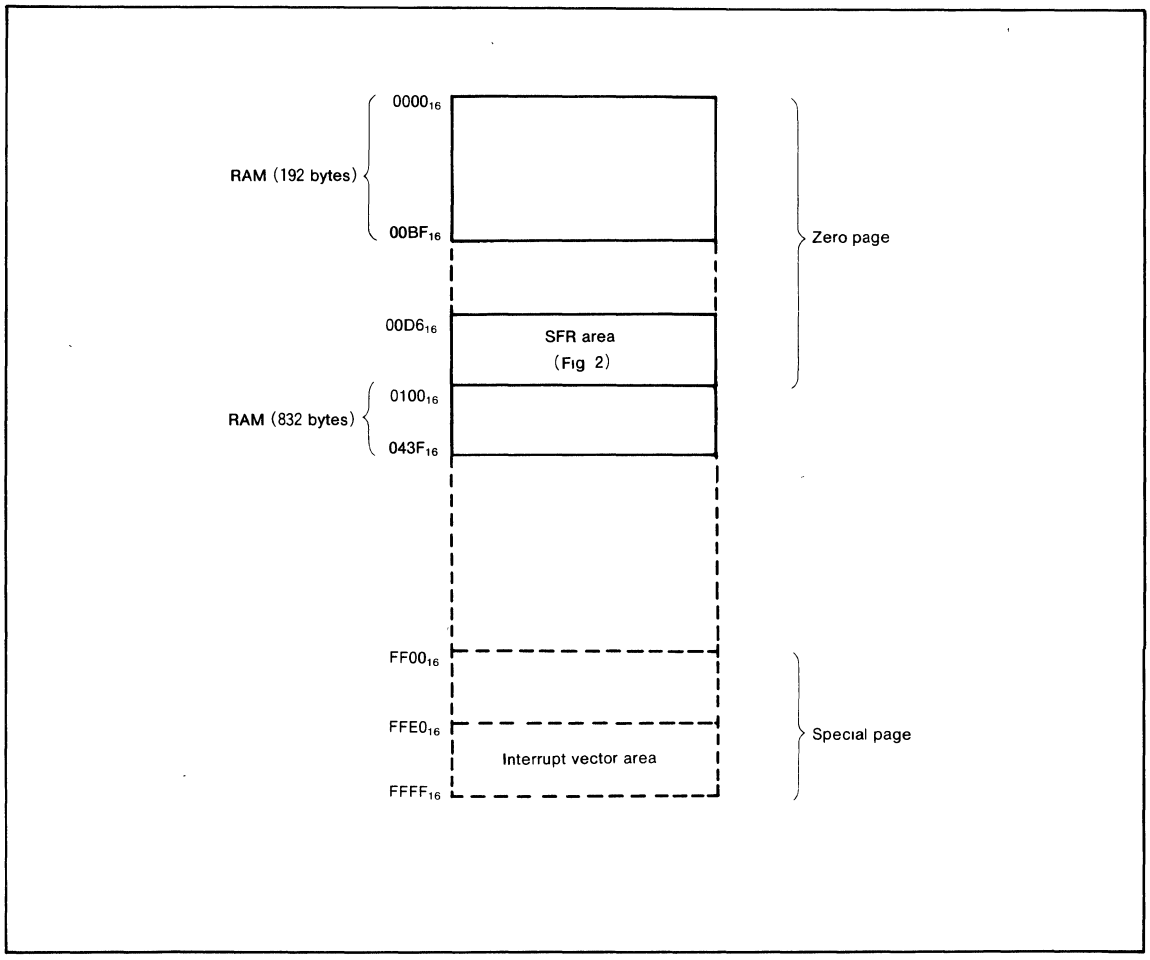


Fig. 1 Memory map

$00D6_{16}$	P3 register	$00EB_{16}$	PWM register (low-order)
$00D7_{16}$	P3 directional register	$00EC_{16}$	PWM register (high-order)
$00D8_{16}$	P4 register/PWM prescaler latch	$00ED_{16}$	Timer 1 control register
$00D9_{16}$	Additional function register	$00EE_{16}$	Timer 2 control register
$00DA_{16}$	P5 register	$00EF_{16}$	Timer 3 control register
$00DB_{16}$	P5 directional register	$00F0_{16}$	Timer 1 register (low-order)
$00DC_{16}$	P6 register	$00F1_{16}$	Timer 1 register (high-order)
$00DD_{16}$	P6 directional register	$00F2_{16}$	Timer 1 latch (low-order)
$00DE_{16}$	MISRG1	$00F3_{16}$	Timer 1 latch (high-order)
$00DF_{16}$	MISRG2	$00F4_{16}$	Timer 2 register (low-order)
$00E0_{16}$	D-A1 register	$00F5_{16}$	Timer 2 register (high-order)
$00E1_{16}$	D-A2 register	$00F6_{16}$	Timer 2 latch (low-order)
$00E2_{16}$	A-D register	$00F7_{16}$	Timer 2 latch (high-order)
$00E3_{16}$	A-D control register	$00F8_{16}$	Timer 3 register (low-order)
$00E4_{16}$	Data bus buffer register	$00F9_{16}$	Timer 3 register (high-order)
$00E5_{16}$	Data bus buffer status register	$00FA_{16}$	Timer 3 latch (low-order)
$00E6_{16}$	Receive/transmit buffer register	$00FB_{16}$	Timer 3 latch (high-order)
$00E7_{16}$	Serial I/O status register	$00FC_{16}$	Interrupt request register 1
$00E8_{16}$	Serial I/O control register	$00FD_{16}$	Interrupt request register 2
$00E9_{16}$	UART control register	$00FE_{16}$	Interrupt control register 1
$00EA_{16}$	Baud rate generator	$00FF_{16}$	Interrupt control register 2

Fig. 2 SFR (Special Function Register) memory map

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state	−0.3 to 7	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		−0.3 to 7	V
V_I	Input voltage D_0-D_7, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, ADV_{REF}, DAV_{REF}, V_{REF}, AV_{CC}		−0.3 to V_{CC}+0.3	V
V_I	Input voltage CNV_{SS}		−0.3 to 13	V
V_O	Output voltage A_0-A_{15}, D_0-D_7, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, X_{OUT}, ϕ, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, $RESET_{OUT}$, SYNC		−0.3 to V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000 (Note 1)	mW
Topr	Operating temperature		−20 to 85	℃
Tstg	Storage temperature		−40 to 125	℃

Note 1 : 500mW for QFP type

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=5V±10%, Ta=−20 to 85℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	"H" input voltage $\overline{RESET}$, X_{IN}, CNV_{SS} (Note 1)	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage D_0-D_7, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (except Note 1)	2.0		V_{CC}	V
V_{IL}	"L" input voltage CNV_{SS} (Note 1)	0		0.2V_{CC}	V
V_{IL}	"L" input voltage D_0-D_7, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (except Note 1)	0		0.8	V
V_{IL}	"L" input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OL(peak)}$	"L" peak output current A_0-A_{15}, D_0-D_7, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			10	mA
$I_{OL(avg)}$	"L" average output current A_0-A_{15}, D_0-D_7, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note 2)			5	mA
$I_{OH(peak)}$	"H" peak output current A_0-A_{15}, D_0-D_7, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$			−10	mA
$I_{OH(avg)}$	"H" average output current A_0-A_{15}, D_0-D_7, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$ (Note 2)			−5	mA
$f(X_{IN})$	Clock oscillating frequency	1		12.5	MHz

Note 1 : Ports operate as INT_1-INT_3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_xD($P3_4$) and S_{CLK}($P3_6$)
2 : The average output current $I_{OH(avg)}$ and $I_{OL(avg)}$ are the average value during a 100ms
3 : The total of "L" output current $I_{OL(peak)}$ of port P3, P5, P6, R/$\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is less than 40mA
The total of "H" output current $I_{OH(peak)}$ of port P3, P5, P6, R/$\overline{W}$, SYNC, $RESET_{OUT}$, $\overline{RD}$, $\overline{WR}$ and ϕ is less than 40mA

ELECTRICAL CHARACTERISTICS (V_{CC} = 5V±10%, V_{SS} = 0V, T_a = −20 to 85℃, f(X_{IN}) = 12.5MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ.	Max	
V_{OH}	"H" output voltage $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	I_{OH}=−2mA	V_{CC}−1			V
V_{OH}	"H" output voltage A_0-A_{15}, D_0-D_7, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	I_{OH}=−5mA	V_{CC}−1			V
V_{OL}	"L" output voltage A_0-A_{15}, D_0-D_7, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ	I_{OL}=2mA			0.45	V
V_{OL}	"L" output voltage A_0-A_{15}, D_0-D_7, $P3_0$-$P3_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$	I_{OL}=5mA			1	V
$V_{T+}-V_{T-}$	Hysterisis INT_1-INT_3($P6_0$-$P6_2$), EV_1-EV_3($P3_0$-$P3_2$), R_XD($P3_4$), S_{CLK}($P3_6$)	Function input level	0.3		1	V
$V_{T+}-V_{T-}$	Hysterisis $\overline{RESET}$				0.7	V
$V_{T+}-V_{T-}$	Hysterisis X_{IN}		0.1		0.5	V
I_{IL}	"L" input current D_0-D_7, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	V_I=V_{SS}	−5		5	μA
I_{IH}	"H" input current D_0-D_7, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $\overline{RESET}$, X_{IN}	V_I=V_{CC}	−5		5	μA
V_{RAM}	RAM retention voltage	At stop mode	2			V
I_{CC}	Supply current	At system operation f(X_{IN})=12.5MHz		8	15	mA
		At stop mode (Note 1)		1	10	μA

Note 1 : The terminals $\overline{RD}$, $\overline{WR}$, R/$\overline{W}$, SYNC, $RESET_{OUT}$, ϕ, D-A_1 and D-A_2 are all open The other ports, which are in the input mode, are connected to V_{SS} A-D converter is in the A-D completion state The current through ADV_{REF} and DAV_{REF} is not included(Fig.7)

A-D CONVERTER CHARACTERISTICS

(V_{CC} = AV_{CC} = 5V ± 10%, V_{SS} = AV_{SS} = 0V, T_a = −20 to 85℃, f(X_{IN})=12.5MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=AV_{CC}=ADV_{REF}=5V±10%		±1.5	±3	LSB
t_{CONV}	Conversion time				49	$t_C(\phi)$
V_{IA}	Analog input voltage		AV_{SS}		AV_{CC}	V
V_{ADVREF}	Reference input voltage		2		V_{CC}	V
R_{LADDER}	Ladder resistance value	ADV_{REF}=5V	20	35	50	kΩ
$I_{IADVREF}$	Reference input current	ADV_{REF}=5V	0.1	0.14	0.25	mA
V_{AVCC}	Analog power supply input voltage			V_{CC}		V
V_{AVSS}	Analog power supply input voltage			0		V

D-A CONVERTER CHARACTERISTICS (V_{CC} = 5V ±10%, V_{SS} = AV_{SS} = 0V, T_a = −20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ	Max	
—	Resolution				8	Bits
—	Absolute accuracy	V_{CC}=DAV_{REF}=5V±10%			1.0	%
t_{SU}	Setup time				3	μs
R_O	Output resistance		1	2	4	kΩ
V_{AVSS}	Analog power supply input voltage			0		V
V_{DAVREF}	Reference input voltage		4		V_{CC}	V
I_{DAVREF}	Reference power input current		0	5	10	mA

TIMING REQUIREMENTS

Port (V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{su(P3D-\phi)}$	Port P3 input setup time	Fig 3	160			ns
$t_{su(P4D-\phi)}$	Port P4 input setup time		160			ns
$t_{su(P5D-\phi)}$	Port P5 input setup time		160			ns
$t_{su(P6D-\phi)}$	Port P6 input setup time		160			ns
$t_{h(\phi-P3D)}$	Port P3 input hold time		40			ns
$t_{h(\phi-P4D)}$	Port P4 input hold time		40			ns
$t_{h(\phi-P5D)}$	Port P5 input hold time		40			ns
$t_{h(\phi-P6D)}$	Port P6 input hold time		40			ns
$t_C(X_{IN})$	External clock input cycle time		80		1000	ns
$t_W(X_{IN}L)$	External clock input "L" pulse width		20			ns
$t_W(X_{IN}H)$	External clock input "H" pulse width		20			ns
$t_r(X_{IN})$	External clock rising edge time				20	ns
$t_f(X_{IN})$	External clock falling edge time				20	ns

Master CPU bus interface timing ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{su(CS-R)}$	$\overline{CS}$ setup time	Fig 4	0			ns
$t_{su(CS-W)}$	$\overline{CS}$ setup time		0			ns
$t_{h(R-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{h(W-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-R)}$	A0 setup time		10			ns
$t_{su(A-W)}$	A0 setup time		10			ns
$t_{h(R-A)}$	A0 hold time		0			ns
$t_{h(W-A)}$	A0 hold time		0			ns
$t_{W(R)}$	Read pulse width		120			ns
$t_{W(W)}$	Write pulse width		120			ns
$t_{su(D-W)}$	Date input setup time before write		50			ns
$t_{h(W-D)}$	Date input hold time after write		0			ns

Master CPU bus interface timing (R/$\overline{W}$ type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{su(CS-E)}$	$\overline{CS}$ setup time	Fig 4	0			ns
$t_{h(E-CS)}$	$\overline{CS}$ hold time		0			ns
$t_{su(A-E)}$	A0 setup time		10			ns
$t_{h(E-A)}$	A0 hold time		0			ns
$t_{su(RW-E)}$	R/$\overline{W}$ setup time		0			ns
$t_{h(E-RW)}$	R/$\overline{W}$ hold time		0			ns
$t_{W(EL)}$	Enable clock "L" pulse width		120			ns
$t_{W(EH)}$	Enable clock "H" pulse width		120			ns
$t_{r(E)}$	Enable clock rising edge time				25	ns
$t_{f(E)}$	Enable clock falling edge time				25	ns
$t_{su(D-E)}$	Data input setup time before write		50			ns
$t_{h(E-D)}$	Data input hold time after write		0			ns

Local bus/Memory expansion mode, Microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{SU(D-\phi)}$	Data input setup time	Fig 5	60			ns
$t_{h(\phi-D)}$	Data input hold time		0			ns
$t_{SU(D-RD)}$	Data input setup time		60			ns
$t_{h(RD-D)}$	Data input hold time		0			ns

Clock synchronous serial I/O (V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{SU(RxD-SCLK)}$	Serial input setup time	Fig 6	160			ns
$t_{h(SCLK-RxD)}$	Serial input hold time		80			ns
$t_{r(RxD)}$	Serial input rising edge time				30	ns
$t_{f(RxD)}$	Serial input falling edge time				30	ns
$t_{r(SCLK)}$	Serial input clock rising edge time				30	ns
$t_{f(SCLK)}$	Serial input clock falling edge time				30	ns
$t_{C(SCLK)}$	Serial input clock period		640			ns
$t_{W(SCLKL)}$	Serial input clock "L" pulse width		290			ns
$t_{W(SCLKH)}$	Serial input clock "H" pulse width		290			ns

SWITCHING CHARACTERISTICS

Port (V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{d(\phi-P3Q)}$	Port P3 data output delay time	Fig 3			200	ns
$t_{d(\phi-P5Q)}$	Port P5 data output delay time				200	ns
$t_{d(\phi-P6Q)}$	Port P6 data output delay time				200	ns
$t_{C(\phi)}$	Cycle time		320		4000	ns
$t_{W(\phi H)}$	ϕ clock pulse width ("H" level)		150			ns
$t_{W(\phi L)}$	ϕ clock pulse width ("L" level)		130			ns
$t_{r(\phi)}$	ϕ clock rising edge time				20	ns
$t_{f(\phi)}$	ϕ clock falling edge time				20	ns

Master CPU bus interface ($\overline{R}$ and $\overline{W}$ separation type mode)

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{a(R-D)}$	Data output enable time after read	Fig 4			80	ns
$t_{v(R-D)}$	Data output disable time after read		0		30	ns
$t_{PLH(R-PR)}$	$\overline{P_{RDY}}$ output transmission time after read				150	ns
$t_{PLH(W-PR)}$	$\overline{P_{RDY}}$ output transmission time after write				150	ns

Master CPU bus interface (R/$\overline{W}$ type mode) (V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{a(E-D)}$	Data output enable time after read	Fig 4			80	ns
$t_{v(E-D)}$	Data output disable time after read		0		30	ns
$t_{PLH(E-PR)}$	$\overline{P_{RDY}}$ output transmission time after E clock				150	ns

Local bus/Memory expansion mode, microprocessor mode

(V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{d(\phi-A)}$	Address delay time after ϕ	Fig 5			80	ns
$t_{v(\phi-A)}$	Address effective time after ϕ		10			ns
$t_{v(RD-A)}$	Address effective time after $\overline{RD}$		10			ns
$t_{v(WR-A)}$	Address effective time after $\overline{WR}$		10			ns
$t_{d(\phi-D)}$	Data output delay time after ϕ				80	ns
$t_{d(WR-D)}$	Data output delay time after $\overline{WR}$				80	ns
$t_{v(\phi-D)}$	Data output effective time after ϕ		20			ns
$t_{v(WR-D)}$	Data output effective time after $\overline{WR}$		20			ns
$t_{d(\phi-RW)}$	R/$\overline{W}$ delay time after ϕ				80	ns
$t_{d(\phi-SYNC)}$	SYNC delay time after ϕ				80	ns
$t_{w(RD)}$	$\overline{RD}$ pulse width		130			ns
$t_{w(WR)}$	$\overline{WR}$ pulse width		130			ns

Clock synchronous serial I/O (V_{CC}=5V±10%, V_{SS}=0V, T_a=−20 to 85℃, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{d(S_{CLK}-T_{XD})}$	Serial output delay time	Fig 6			100	ns
$t_{r(S_{CLK})}$	Serial output clock rising edge time				30	ns
$t_{f(S_{CLK})}$	Serial output clock falling edge time				30	ns
$t_{c(S_{CLK})}$	Serial output clock period		640			ns
$t_{w(S_{CLK}L)}$	Serial output clock "L" pulse width		290			ns
$t_{w(S_{CLK}H)}$	Serial output clock "H" pulse width		290			ns

TEST CONDITION

Input voltage level : V_{IH} 2.4V
V_{IL} 0.45V
Output test level : V_{OH} 2.0V
V_{OL} 0.8V

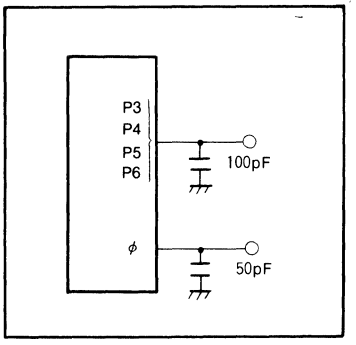


Fig. 3 Port test circuit

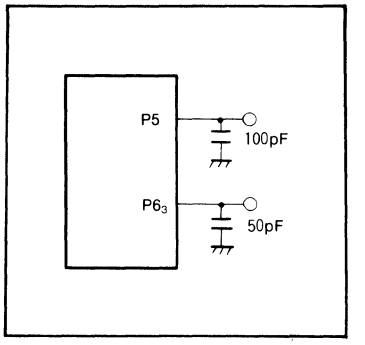


Fig. 4 Master CPU bus interface test circuit

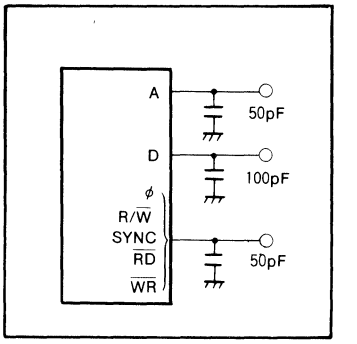


Fig. 5 Local bus test circuit

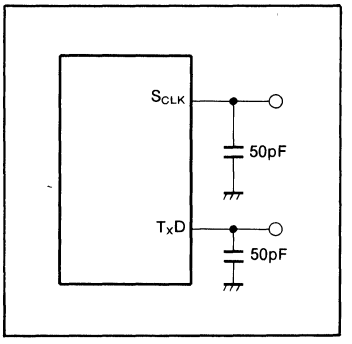


Fig. 6 Serial I/O test circuit

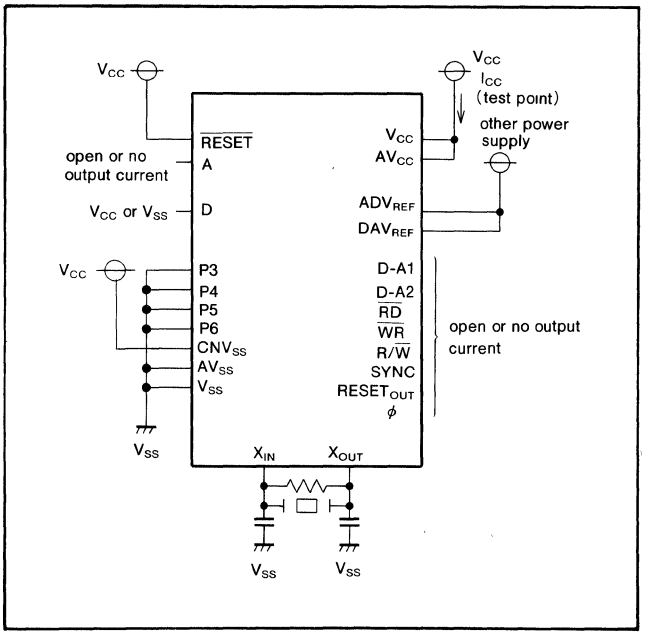


Fig. 7 I_{CC} (at stop mode) test condition

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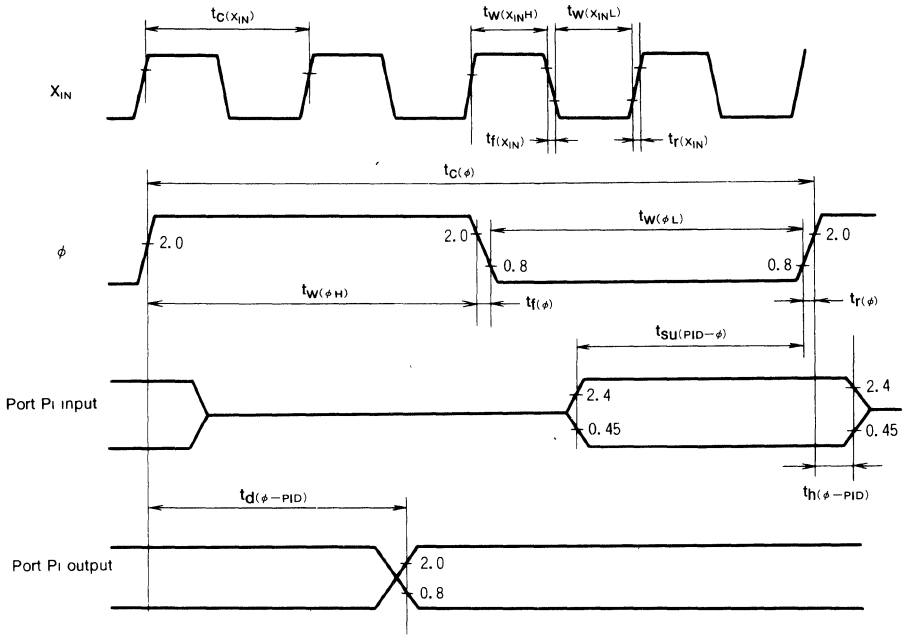
TIMING DIAGRAM

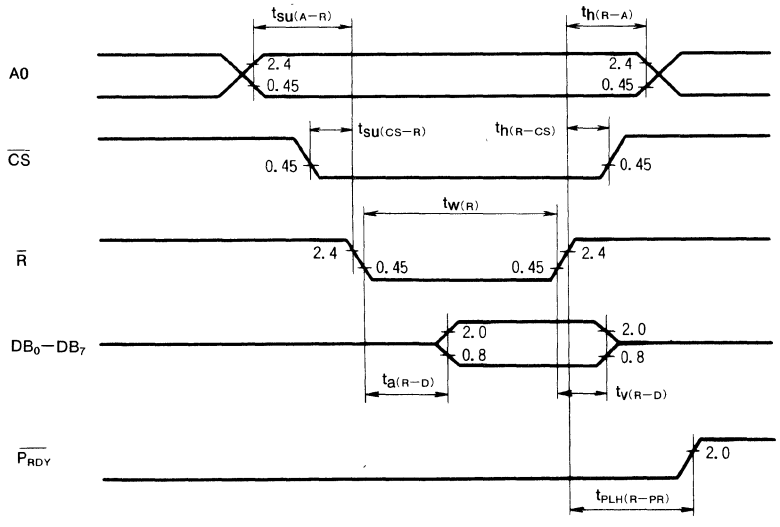
Port/single-chip mode timing diagram



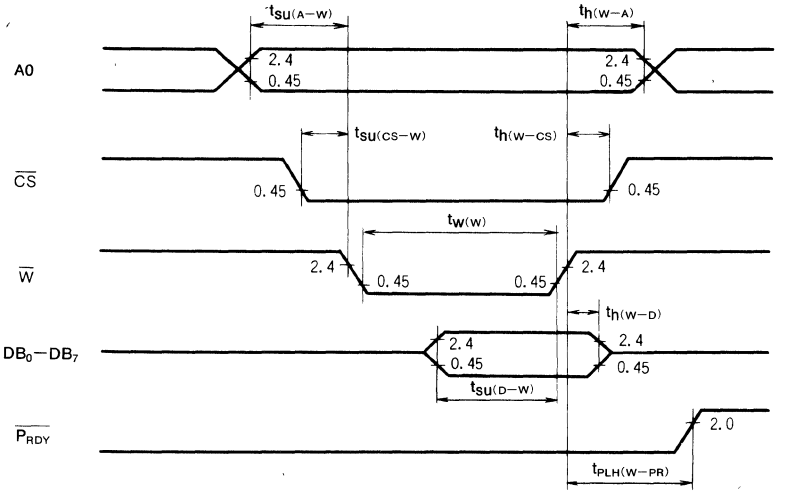
Note : $V_{IH}=0.8V_{CC}$, $V_{IL}=0.16V_{CC}$ of X_{IN}

Master CPU bus interface/ $\overline{R}$ and $\overline{W}$ separation type timing diagram

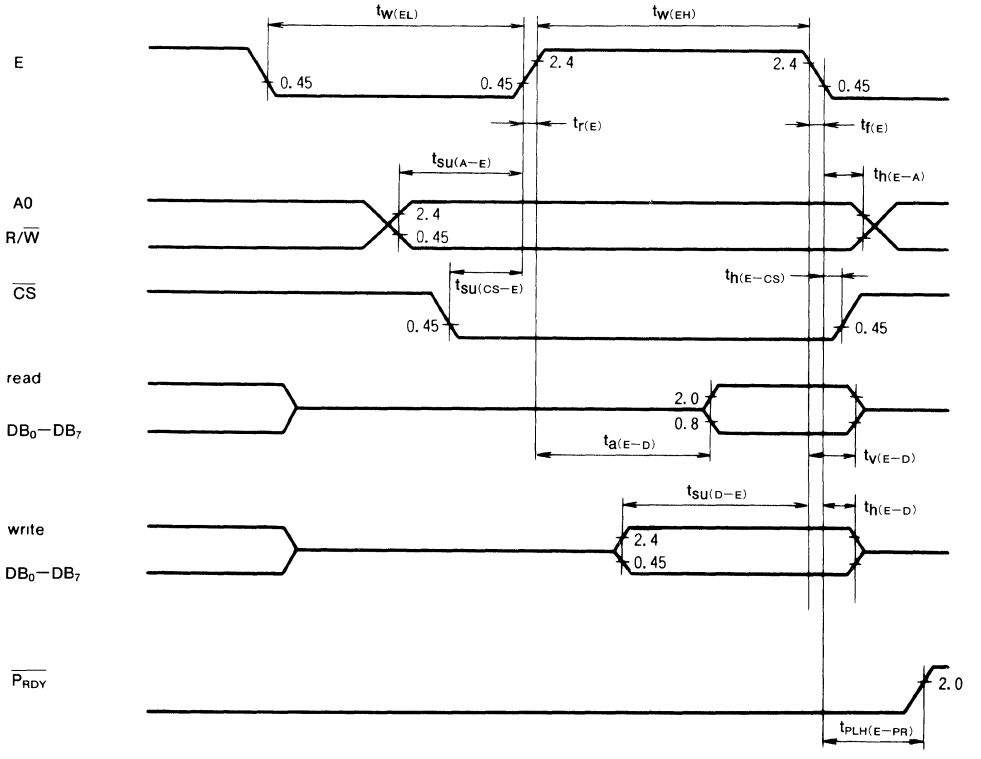
Read



Write



Master CPU interface/ R/$\overline{W}$ type timing diagram



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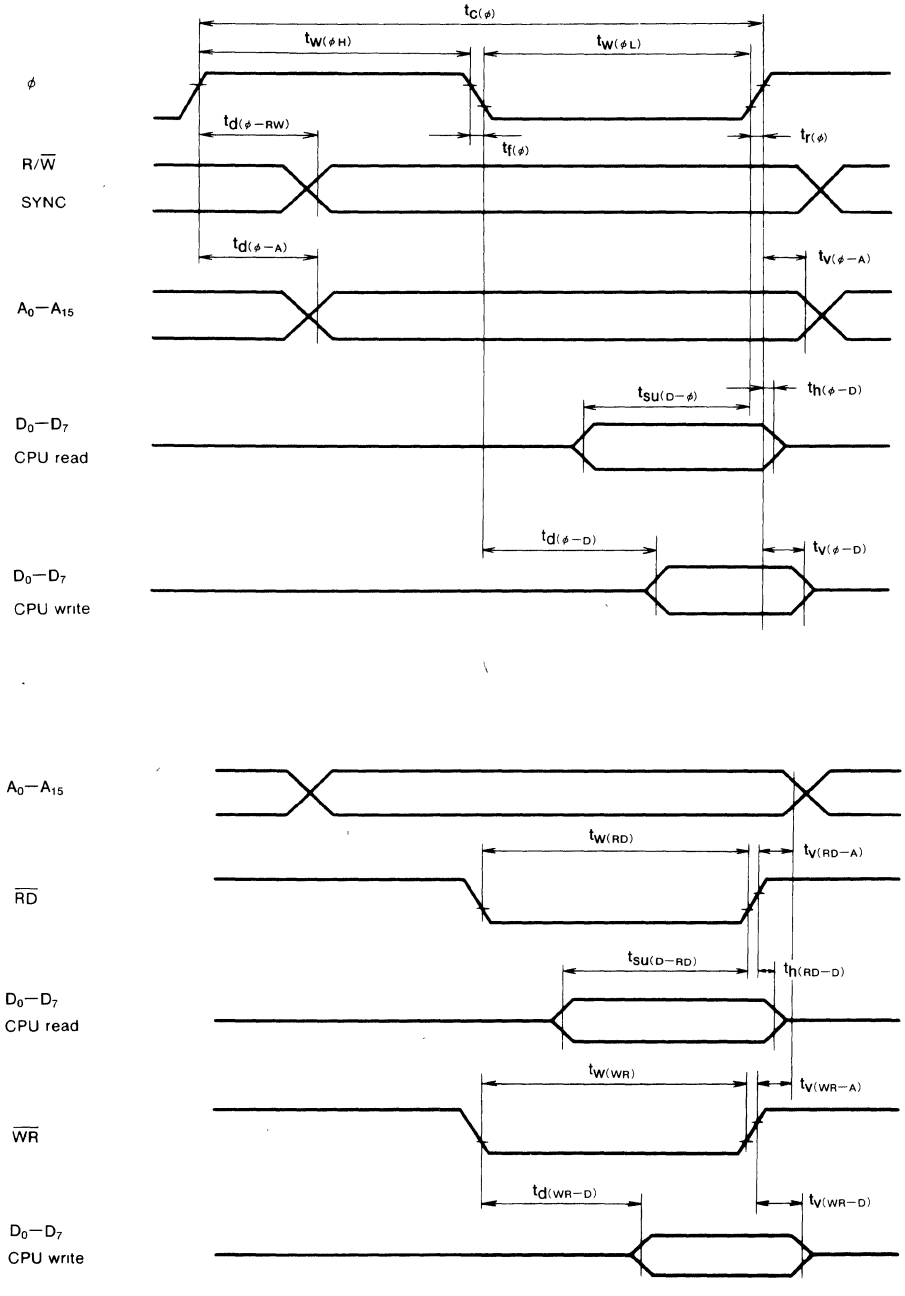
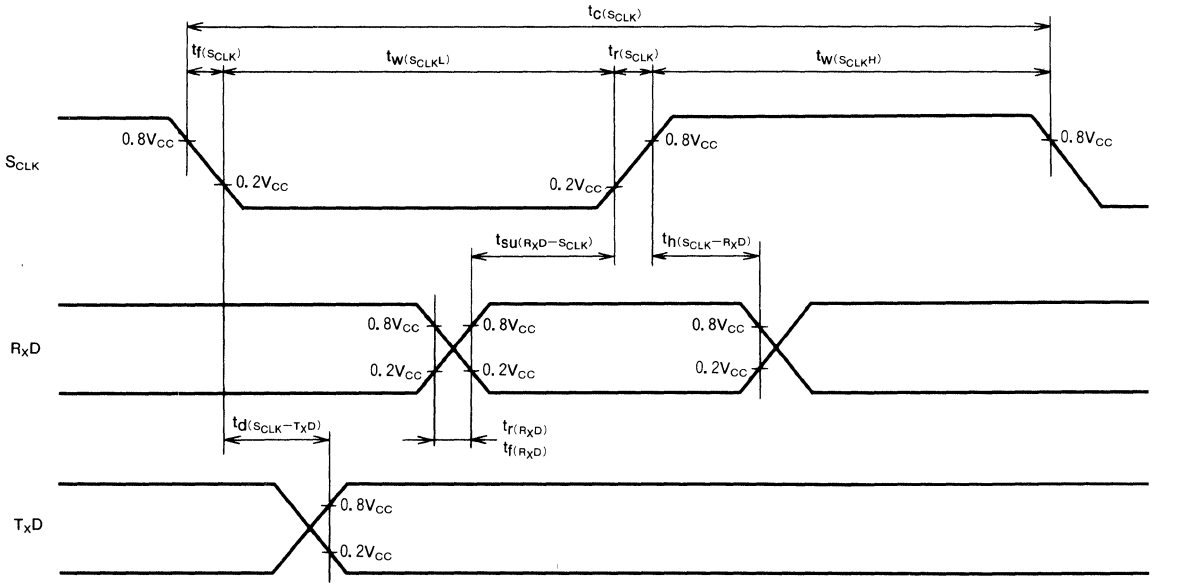
Local bus timing diagram



Clock synchronous serial I/O timing diagram



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