M37471E4-XXXSP/FP
M37471E8-XXXSP/FP,M37471E8SS

PROM VERSION of M37471M4-XXXSP/FP,M37471M8-XXXSP/FP

DESCRIPTION

The M37471E4-XXXSP/FP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 42-pin shrink plastic molded DIP or a 56-pin plastic molded QFP. The features of this chip are similar to those of the M37471M4-XXXSP/FP except that this chip has a 8192 bytes PROM built-in. This single-chip microcomputer is useful for home electrical appliances and consumer appliance controllers.

In addition to its simple instruction sets, the PROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming. Since general purpose PROM writers can be used for the built-in PROM, this chip is suitable for small quantity production runs.

The differences between the M37471E4-XXXSP/FP and the M37471E8-XXXSP/FP are noted below. The M37471E8SS are the window type. The following explanations apply to the M37471E4-XXXSP/FP.

Specification variations for other chips are noted accordingly.

Type name	ROM size	RAM size
M37471E4-XXXSP/FP	8192 bytes	192 bytes
M37471E8-XXXSP/FP M37471E8SS	16384 bytes	384 bytes

The differences between the M37471E4-XXXSP and the M37471E4-XXXFP are the package outline and the power dissipation ability (absolute maximum ratings).

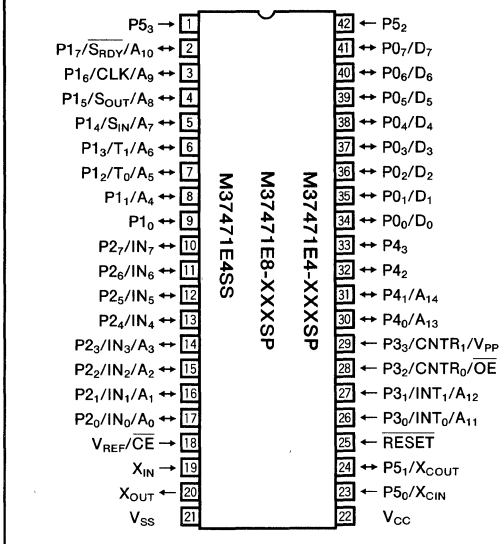
FEATURES

- Number of basic instructions 69
- Memory size PROM ..... 8192 bytes (M37471E4)
  16384 bytes (M37471E8)
  RAM ..... 192 bytes (M37471E4)
  384 bytes (M37471E8)
- Instruction execution time
  ..... 1μs (minimum instructions at 4MHz frequency)
- Single power supply ..... 2.7~5.5V
- Power dissipation
  normal operation mode (at 4MHz frequency) 17.5mW
- Subroutine nesting ..... 96 levels max. (M37471E4)
- Interrupt ..... 12 types, 10 vectors
- 8-bit timer 4
- Serial I/O ..... 8-bit×1
- Programmable I/O ports (Ports P0, P1, P2, P4) 28
- Input ports (Port P3, P5) 8
- A-D converter 8-bit, 8-channel
- Two clock generator circuits
  (One is for main clock, the other is for clock function)
- PROM (equivalent to the M5L27256)
  program voltage 12.5V

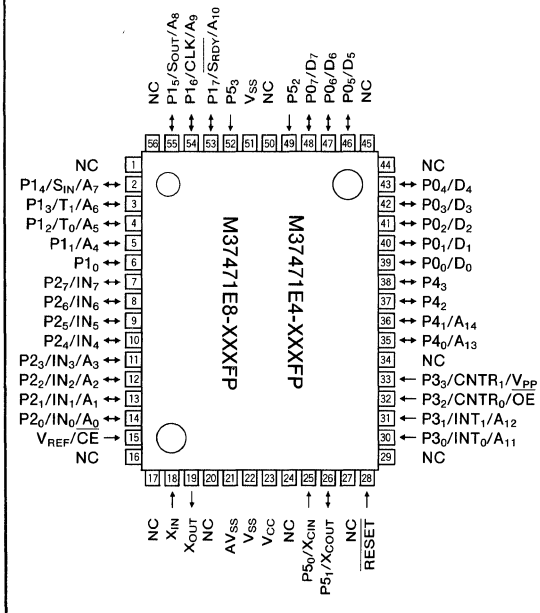
APPLICATION

Office automation equipment, VCR, Tuner, Audio-visual equipment

PIN CONFIGURATION (TOP VIEW)



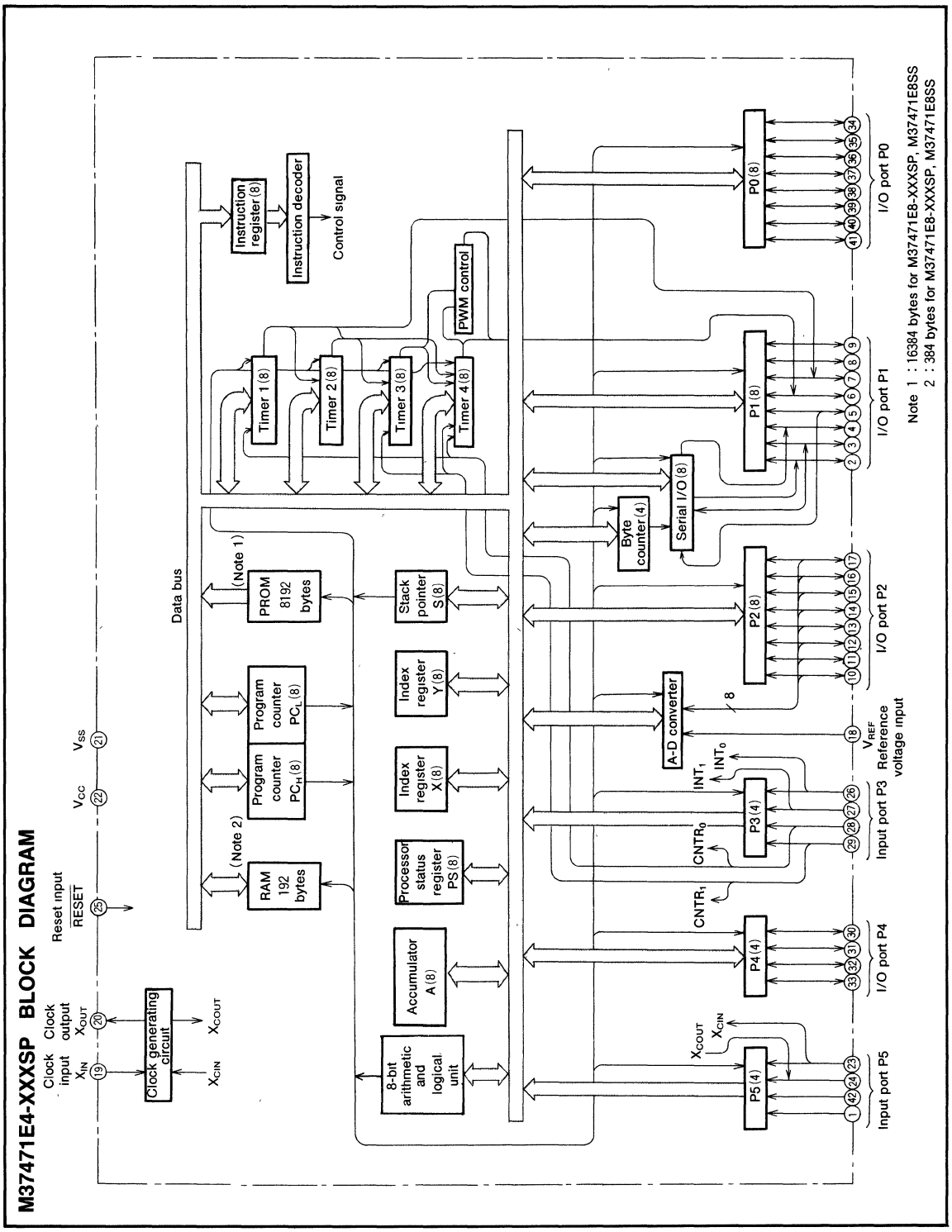
Outline 42P4B (OTP)
42S1B (Window)



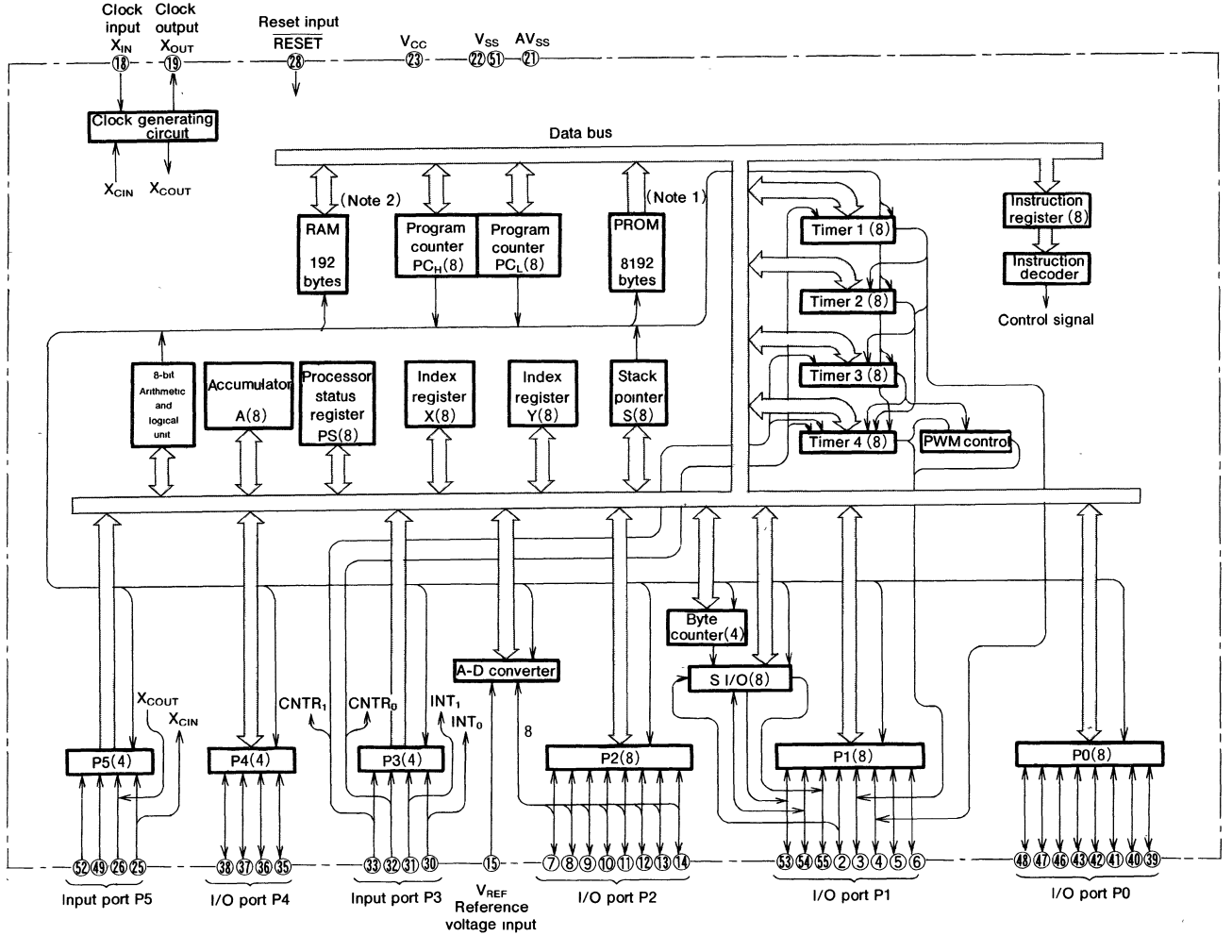
Outline 56P6N

NC : No connection

M37471E4-XXXSP BLOCK DIAGRAM



M37471E4-XXXFP BLOCK DIAGRAM



Note 1 : 16384 bytes for M37471E8-XXXFP
2 : 384 bytes for M37471E8-XXXFP

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FUNCTIONS OF M37471E4-XXXSP/FP, M37471E8-XXXSP/FP, M37471E8SS

Parameter			Functions
Number of basic instructions			69
Instruction execution time			1μs (minimum instructions, at 4MHz frequency)
Clock frequency			4MHz (main clock input), 32kHz (for clock function).
Memory size	M37471E4-XXXSP/FP	PROM	8192 bytes (Note 1)
		RAM	192 bytes
	M37471E8-XXXSP/FP	PROM	16384 bytes (Note 1)
	M37471E8SS	RAM	384 bytes
Input/Output port	P0, P1, P2	I/O	8-bit×3
	P3, P5	Input	4-bit×2
	P4	I/O	4-bit×1
Serial I/O			8-bit×1
Timers			8-bit timer×4
A-D converter			8-bit×1 (8channel)
Subroutine nesting	M37471E4-XXXSP/FP		96 levels (max.)
	M37471E8-XXXSP/FP, M37471E8SS		192 levels (max.)
Interrupt			Five external interrupts, six internal interrupts, one software interrupt
Clock generating circuit			Two built-in circuits with internal feedback resistor (ceramic or quartz crystal oscillator)
Supply voltage			2.7~5.5V
Power dissipation	At high-speed operation		17.5mW (at $f(X_{IN})$=4MHz)
	At low-speed operation		0.15mW (at $f(X_{CIN})$=32kHz)
	At stop mode		0.5μW (at clock stop)
Input/Output characteristics	Input/Output voltage		5V
	Output current		−5~10mA (ports P0, P1, P2, P4 CMOS tri-state output)
Operating temperature range			−20~85°C
Device structure			CMOS Silicon gate
Package	M37471E4-XXXSP		42-pin shrink plastic molded DIP
	M37471E8-XXXSP		
	M37471E4-XXXFP		56-pin plastic molded QFP
	M37471E8-XXXFP		
	M37471E8SS		42-pin shrink ceramic DIP

Note 1 : The PROM programming voltage is 12.5V (equivalent to the M5L27256)

PIN DESCRIPTION

Pin	Mode	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Single-chip /EPROM	Supply voltage		Power supply inputs 2 7~5 5V to V_{CC} and 0V to V_{SS}
AV_{SS}	Single-chip /EPROM	Analog power supply		Ground level input pin for A-D converter Same voltage as V_{SS} is applied This pin is for 56-pin model only
$\overline{RESET}$	Single-chip	RESET input	Input	To reset, keep this input terminal low for more than 2μs (min) under normal V_{CC} conditions
	EPROM	RESET input		Connect to V_{SS}
X_{IN}	Single-chip /EPROM	Clock input	Input	Connect a ceramic or a quartz crystal oscillator between X_{IN} and X_{OUT} for clock oscillation If an external clock input is used, connect the clock input to the X_{IN} pin and open the X_{OUT} pin Feedback resistor is connected between the X_{IN} and X_{OUT} pins
X_{OUT}		Clock output	Output	
$P0_0$~$P0_7$	Single-chip	I/O port P0	I/O	Port P0 is an 8-bit I/O port The output structure is CMOS output When this port is selected for input, pull-up transistor can be connected in units of 1-bit and a key on wake up function is provided
	EPROM	Data input/output D_0~D_7	I/O	Port P0 works as an 8-bit data bus (D_0~D_7)
$P1_0$~$P1_7$	Single-chip	I/O port P1	I/O	Port P1 is an 8-bit I/O port The output structure is CMOS output When this port is selected for input, pull-up transistor can be connected in units of 4-bit $P1_2$, $P1_3$ are in common with timer output pins T_0, T_1 $P1_4$, $P1_5$, $P1_6$, $P1_7$ are in common with serial I/O pins S_{IN}, S_{OUT}, CLK, $\overline{S_{RDY}}$, respectively The output structure of S_{OUT} and $\overline{S_{RDY}}$ can be changed to N-channel open drain output
	EPROM	Address input A_4~A_{10}	Input	$P1_1$~$P1_7$ works as the 7-bit address input (A_4~A_{10}) $P1_0$ must be opened
$P2_0$~$P2_7$	Single-chip	I/O port P2	I/O	Port P2 is an 8-bit I/O port The output structure is CMOS output When this port is selected for input, pull-up transistor can be connected in units of 4-bit This port is in common with analog input pins IN_0~IN_7.
	EPROM	Address input A_0~A_3	Input	$P2_0$~$P2_3$ works as the lower 4-bit address input (A_0~A_3) $P2_4$~$P2_7$ must be opened.
$P3_0$~$P3_3$	Single-chip	Input port P3	Input	Port P3 is an 4-bit input port $P3_0$, $P3_1$ are in common with external interrupt input pins INT_0, INT_1 and $P3_2$, $P3_3$ are in common with timer input pins $CNTR_0$, $CNTR_1$
	EPROM	Address input A_{11}, A_{12} Select mode V_{PP} input	Input	$P3_0$, $P3_1$ works as the 2-bit address input (A_{11}, A_{12}) $P3_2$ works as $\overline{OE}$ input Connect to $P3_3$ to V_{PP} when programming or verifing
$P4_0$~$P4_3$	Single-chip	I/O port P4	I/O	Port P4 is an 4-bit I/O port The output structure is CMOS output When this port is selected for input, pull-up transistor can be connected in units of 4-bit
	EPROM	Address input A_{13}, A_{14}	Input	$P4_0$, $P4_1$ works as the higher 2-bit address input (A_{13}, A_{14}) $P4_2$, $P4_3$ must be opened
$P5_0$~$P5_3$	Single-chip	Input port P5	Input	Port P5 is an 4-bit input port and pull-up transistor can be connected in units of 4-bit $P5_0$, $P5_1$ are in common with input/output pins of clock for clock function X_{CIN}, X_{COUT}. When $P5_0$, $P5_1$ are used as X_{CIN}, X_{COUT}, connect a ceramic or a quartz crystal oscillator between X_{CIN} and X_{COUT} If an external clock input is used, connect the clock input to the X_{CIN} pin and open the X_{COUT} pin Feedback resistor is connected between X_{CIN} and X_{COUT} pins
	EPROM			Open
V_{REF}	Single-chip	Reference voltage input	Input	This is the reference voltage input pin for the A-D converter
	EPROM	Select mode	Input	V_{REF} works as $\overline{CE}$ input

EPROM MODE

The M37471E4-XXXSP/FP, M37471E8-XXXSP/FP, M37471E8SS feature an EPROM mode in addition to its normal modes. When the $\overline{RESET}$ signal level is low ("L"), the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 1, 2 gives the pin connection in the EPROM mode. When in the EPROM mode, ports P0, $P1_1 \sim P1_7$, $P2_0 \sim P2_3$, P3, $P4_0$, $P4_1$, V_{REF} are used for the PROM (equivalent to the M5L27256). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5L27256. The oscillator should be connected to the X_{IN} and X_{OUT} pins, or external clock should be connected to the X_{IN} pin.

Table 1. Pin function in EPROM mode

	M37471E4-XXXSP/FP, M37471E8-XXXSP/FP, M37471E8SS	M5L27256
V_{CC}	V_{CC}	V_{CC}
V_{PP}	$P3_3$	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports $P1_1 \sim P1_7$, $P2_0 \sim P2_3$ $P3_0$, $P3_1$, $P4_0$, $P4_1$	$A_0 \sim A_{14}$
Data I/O	Port P0	$D_0 \sim D_7$
$\overline{CE}$	V_{REF}	$\overline{CE}$
$\overline{OE}$	$P3_2$	$\overline{OE}$

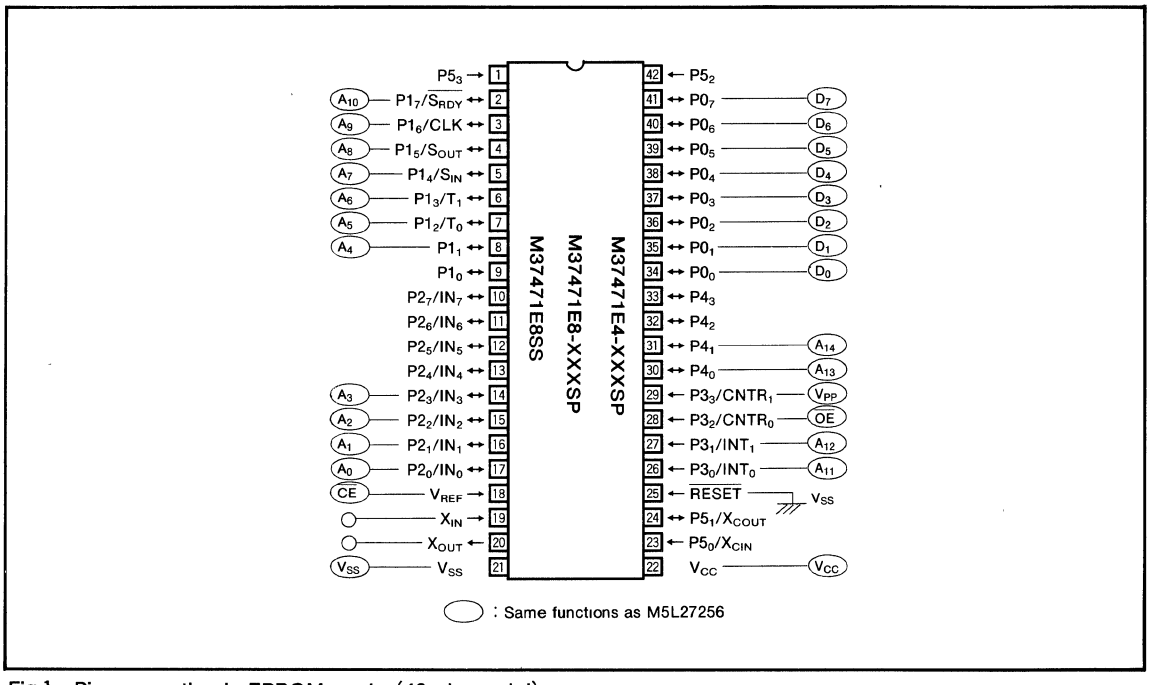


Fig.1 Pin connection in EPROM mode (42-pin model)

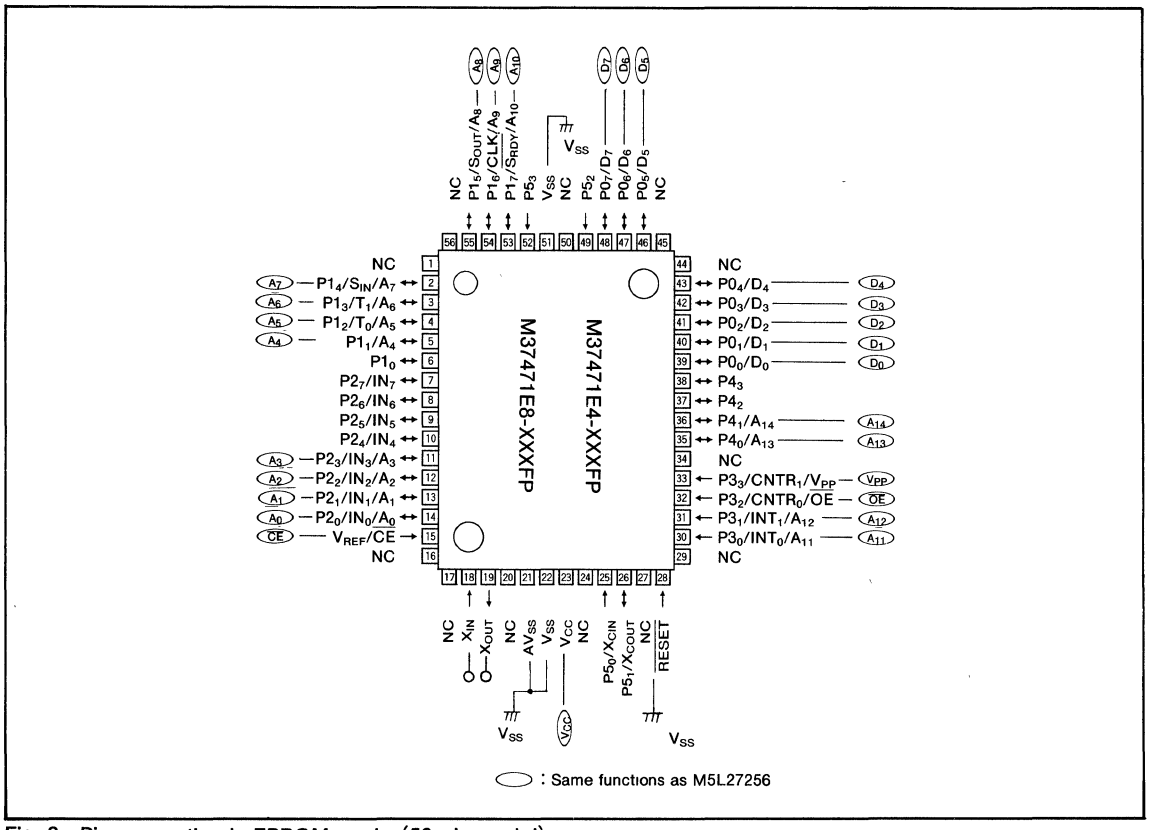


Fig. 2 Pin connection in EPROM mode (56-pin model)

PROM READING AND WRITING

Reading

To read the PROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level. Input the address of the data ($A_0 \sim A_{14}$) to be read and the data will be output to the I/O pins $D_0 \sim D_7$. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pin is in the "H" state.

Writing

To write to the PROM, set the $\overline{OE}$ pin to a "H" level. The CPU will enter the program mode when V_{PP} is applied to the V_{PP} pin. The address to be written to is selected with pins $A_0 \sim A_{14}$, and the data to be written is input to pins $D_0 \sim D_7$. Set the $\overline{CE}$ pin to a "L" level to begin writing.

Notes on Writing

● M37471E4-XXXSP/FP

When using a PROM writer, the address range should be between 6000_{16} and $7FFF_{16}$. Read/write operations on addresses 0000_{16} to $5FFF_{16}$ cannot be performed correctly.

● M37471E8-XXXSP/FP, M37471E8SS

When using a PROM writer, the address range should be between 4000_{16} and $7FFF_{16}$. When data is written between addresses 0000_{16} and $7FFF_{16}$, fill addresses 0000_{16} to $3FFF_{16}$ with FF_{16}.

Erasing

Data can only erased on the M37471E8SS ceramic package, which includes a window. To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power necessary for erasing is 15W · s/cm^2.

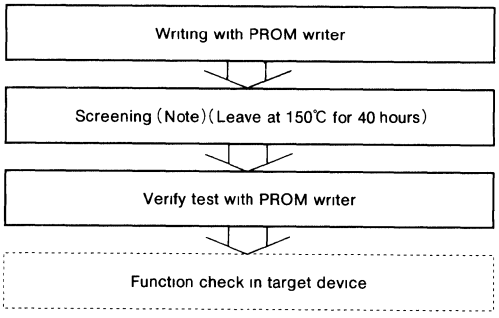
NOTES ON HANDLING

(1) Sunlight and fluorescent light contain wave lengths capable of erasing data. For ceramic package types, cover the transparent window with a seal (provided) when this chip is in use. However, this seal must not contact the lead pins.

(2) Before erasing, the glass should be cleaned and stains such as finger prints should be removed thoroughly. If these stains are not removed, complete erasure of the data could be prevented.

(3) Since a high voltage (12.5V) is used to write data, care should be taken when turning on the PROM writer's power.

(4) For the programmable microcomputer (shipped in blank or OTP type), Mitsubishi does not perform PROM write test and screening in the assembly process and following processes. To improve reliability after write, performing write and test according to the flow below before use is recommended.



Note : Since the screening temperature is higher than storage temperature, never expose to 150℃ exceeding 100 hours.

Table 2. I/O signal in each mode

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{CC}	Data I/O
Read-out	V_{IL}	V_{IL}	V_{CC}	V_{CC}	Output
Output disable	V_{IL}	V_{IH}	V_{CC}	V_{CC}	Floating
Programming	V_{IL}	V_{IH}	V_{PP}	V_{CC}	Input
Programming verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	Output
Program disable	V_{IH}	V_{IH}	V_{PP}	V_{CC}	Floating

Note 1 : V_{IL} and V_{IH} indicate a "L" and "H" input voltage, respectively

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to V_{SS} Output transistors are at "OFF" state	−0.3∼7	V
V_I	Input voltage X_{IN}		−0.3∼V_{CC}+0.3	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_3$, $P4_0$∼$P4_3$, $P5_0$∼$P5_3$, V_{REF}, $\overline{RESET}$		−0.3∼V_{CC}+0.3 (Note 1)	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P4_0$∼$P4_3$, X_{OUT}		−0.3∼V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25℃	1000 (Note 2)	mW
Topr	Operating temperature		−20∼85	℃
Tstg	Storage temperature		−40∼150	℃

Note 1 : In EPROM programming mode, $P3_3$ is 13V
2 : 500mW for QFP type

RECOMMENDED OPERATING CONDITIONS

(V_{CC}=2.7∼5.5V, V_{SS}=AV_{SS}=0V, Ta=−20∼85℃ unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ'	Max	
V_{CC}	Supply voltage	2.7	5	5.5	V
V_{SS}	Supply voltage		0		V
AV_{SS}	Analog supply voltage		0		V
V_{IH}	"H" Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$∼$P3_3$, $\overline{RESET}$, X_{IN}	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" Input voltage $P2_0$∼$P2_7$, $P4_0$∼$P4_3$, $P5_0$∼$P5_3$ (Note 1)	0.7V_{CC}		V_{CC}	V
V_{IL}	"L" Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P3_0$∼$P3_3$	0		0.2V_{CC}	V
V_{IL}	"L" Input voltage $P2_0$∼$P2_7$, $P4_0$∼$P4_3$, $P5_0$∼$P5_3$ (Note 1)	0		0.25V_{CC}	V
V_{IL}	"L" Input voltage $\overline{RESET}$	0		0.12V_{CC}	V
V_{IL}	"L" Input voltage X_{IN}	0		0.16V_{CC}	V
$I_{OH(sum)}$	"H" sum output current $P0_0$∼$P0_7$, $P4_0$∼$P4_3$			−30	mA
$I_{OH(sum)}$	"H" sum output current $P1_0$∼$P1_7$, $P2_0$∼$P2_7$			−30	mA
$I_{OL(sum)}$	"L" sum output current $P0_0$∼$P0_7$, $P4_0$∼$P4_3$			60	mA
$I_{OL(sum)}$	"L" sum output current $P1_0$∼$P1_7$, $P2_0$∼$P2_7$			60	mA
$I_{OL(peak)}$	"L" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P4_0$∼$P4_3$			20	mA
$I_{OL(avg)}$	"L" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P4_0$∼$P4_3$ (Note 4)			10	mA
$I_{OH(peak)}$	"H" peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P4_0$∼$P4_3$			−10	mA
$I_{OH(avg)}$	"H" average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P4_0$∼$P4_3$ (Note 4)			−5	mA
$f_{(CNTR)}$	Timer input frequency $CNTR_0$ ($P3_2$), $CNTR_1$ ($P3_3$) (Note 2)			1	MHz
$f_{(CLK)}$	Serial I/O clock input frequency CLK ($P1_6$) (Note 2)			1	MHz
$f(X_{IN})$	Clock oscillating frequency (Note 2)			4	MHz
$f(X_{CIN})$	Clock oscillating frequency for clock function (Note 2, 3)		32	50	kHz

Note 1 : It is except to use $P5_0$ as X_{CIN}
2 : Oscillation frequency is at 50% duty cycle
3 : When used in the low-speed mode, the clock oscillating frequency for clock function should be $f(X_{CIN}) < f(X_{IN})/3$
4 : The average output current $I_{OH(avg)}$ and $I_{OL(avg)}$ are the average value during a 100ms

ELECTRICAL CHARACTERISTICS (V_{CC}=2.7~5.5V, V_{SS}=0V, T_a=−20~85℃, unless otherwise noted)

Symbol	Parameter	Test Conditions		Limits			Unit
				Min	Typ	Max	
V_{OH}	"H" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_3$, $P4_0$~$P4_3$	V_{CC}=5V, I_{OH}=−5mA		3			V
		V_{CC}=3V, I_{OH}=−1.5mA		2			
V_{OL}	"L" output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_3$, $P4_0$~$P4_3$	V_{CC}=5V, I_{OL}=10mA				2	V
		V_{CC}=3V, I_{OL}=3mA				1	
V_{T+}−V_{T-}	Hysteresis $P0_0$~$P0_7$, $P3_0$~$P3_3$	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.3		
V_{T+}−V_{T-}	Hysteresis $\overline{RESET}$	V_{CC}=5V			0.5		V
		V_{CC}=3V			0.3		
V_{T+}−V_{T-}	Hysteresis $P1_6$/CLK	use as CLK input	V_{CC}=5V		0.5		V
			V_{CC}=3V		0.3		
I_{IL}	"L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P3_0$~$P3_2$, $P4_0$~$P4_3$, $P5_0$~$P5_3$	V_I=0V, not use pull-up transistor	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
		V_I=0V, use pull-up transistor	V_{CC}=5V	−0.25	−0.5	−1.0	mA
			V_{CC}=3V	−0.08	−0.18	−0.35	
I_{IL}	"L" input current $P3_3$	V_I=0V	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
I_{IL}	"L" input current $P2_0$~$P2_7$	V_I=0V, not use as analog input, not use pull-up transistor	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
		V_I=0V, not use as analog input, use pull-up transistor	V_{CC}=5V	−0.25	−0.5	−1.0	mA
			V_{CC}=3V	−0.08	−0.18	−0.35	
I_{IL}	"L" input current $\overline{RESET}$, X_{IN}	V_I=0V (X_{IN} is at stop mode)	V_{CC}=5V			−5	μA
			V_{CC}=3V			−3	
I_{IH}	"H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P3_0$~$P3_2$, $P4_0$~$P4_3$, $P5_0$~$P5_3$	V_I=V_{CC}, not use pull-up transistor	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{IH}	"H" input current $P3_3$	V_I=V_{CC}	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{IH}	"H" input current $P2_0$~$P2_7$	V_I=V_{CC}, not use as analog input, not use pull-up transistor	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{IH}	"H" input current $\overline{RESET}$, X_{IN}	V_I=V_{CC}, (X_{IN} is at stop mode)	V_{CC}=5V			5	μA
			V_{CC}=3V			3	
I_{CC}	Supply current	At normal operation, A-D conversion is not executed X_{IN}=4MHz	V_{CC}=5V		3.5	7	mA
			V_{CC}=3V		1.8	3.6	
		At normal operation, A-D conversion is not executed X_{IN}=4MHz	V_{CC}=5V		4	8	
			V_{CC}=3V		2	4	
		At low-speed mode, X_{COUT} is low-power mode, A-D conversion is not executed X_{IN}=0Hz, X_{CIN}=32kHz, T_a=25℃	V_{CC}=5V		30	80	μA
			V_{CC}=3V		15	40	
		At wait mode, X_{IN}=4MHz	V_{CC}=5V		1	2	mA
			V_{CC}=3V		0.5	1	
		At wait mode, X_{IN}=0Hz, X_{CIN}=32kHz, X_{COUT} is low-power mode, T_a=25℃	V_{CC}=5V		3	12	μA
			V_{CC}=3V		2	8	
		Stop all oscillation V_{CC}=5V	T_a=25℃		0.1	1	
			T_a=85℃		1	10	
V_{RAM}	RAM retention voltage	Stop all oscillation		2			V

A-D CONVERTER CHARACTERISTICS (V_{CC}=2.7~5.5V, V_{SS}=0V, T_a=−20~85℃, f(X_{IN})=4MHz, unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min	Typ.	Max	
—	Resolution				8	bits
—	Non-linearity error				±2	LSB
—	Differential non-linearity error				±0.9	LSB
V_{OT}	Zero transition error	V_{CC}=V_{REF}=5.12V, $I_{OL(sum)}$=0mA			2	LSB
		V_{CC}=V_{REF}=3.072V, $I_{OL(sum)}$=0mA			3	
V_{FST}	Full-scale transition error	V_{CC}=V_{REF}=5.12V			4	LSB
		V_{CC}=V_{REF}=3.072V			7	
t_{CONV}	Conversion time				25	μs
V_{VREF}	Reference input voltage		0.5V_{CC}		V_{CC}	V
R_{LADDER}	Ladder resistance value		2	5	10	kΩ
V_{IA}	Analog input voltage		0		V_{REF}	V