

**PRELIMINARY**  
 Notice: This is not a final specification.  
 Some parametric limits are subject to  
 change.

**MITSUBISHI MICROCOMPUTERS**  
**M37516F8HP**

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

**DESCRIPTION**

The M37516F8HP is the 8-bit microcomputer based on the 740 family core technology.

The M37516F8HP is designed for household products and office automation equipment and includes serial I/O functions, 8-bit timer, A-D converter, and I<sup>2</sup>C-BUS interface.

**FEATURES**

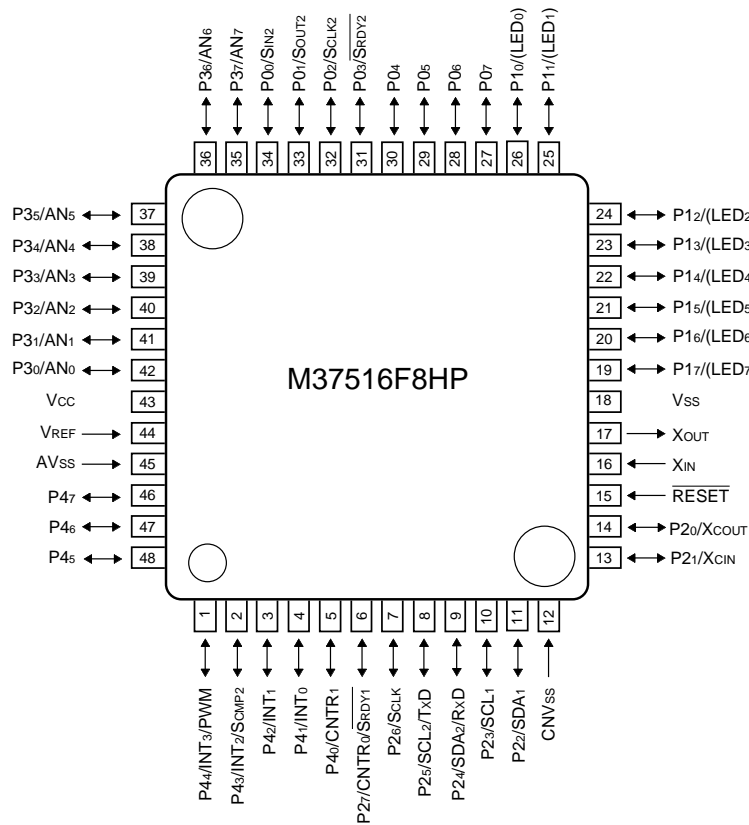
- Basic machine-language instructions ..... 71
- Minimum instruction execution time ..... 0.5 μs  
 (at 8 MHz oscillation frequency)
- Memory size  
 Flash memory ..... 32 Kbytes  
 RAM ..... 1 Kbytes
- Programmable input/output ports ..... 40
- Interrupts ..... 17 sources, 16 vectors
- Timers ..... 8-bit X 4
- Serial I/O1 ..... 8-bit X 1 (UART or Clock-synchronized)
- Serial I/O2 ..... 8-bit X 1 (Clock-synchronized)
- Multi-master I<sup>2</sup>C-BUS interface (option) ..... 1 channel
- PWM ..... 8-bit X 1
- A-D converter ..... 10-bit X 8 channels
- Watchdog timer ..... 16-bit X 1

- Clock generating circuit ..... Built-in 2 circuits  
 (connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage  
 In high-speed mode ..... 4.0 to 5.5 V  
 (at 8 MHz oscillation frequency)  
 In high-speed mode ..... 2.7 to 5.5 V  
 (at 4 MHz oscillation frequency)  
 In middle-speed mode ..... 2.7 to 5.5 V  
 (at 8 MHz oscillation frequency)  
 In low-speed mode ..... 2.7 to 5.5 V  
 (at 32 kHz oscillation frequency)
- Power dissipation  
 In high-speed mode ..... 34 mW  
 (at 8 MHz oscillation frequency, at 5 V power source voltage)  
 In low-speed mode ..... T.B.D.  
 (at 32 kHz oscillation frequency, at 3 V power source voltage)
- Operating temperature range ..... -20 to 85°C

**APPLICATION**

Office automation equipment, FA equipment, Household products, Consumer electronics, etc.

**PIN CONFIGURATION (TOP VIEW)**



Package type : 48P6Q-A

Fig. 1 M37516F8HP pin configuration

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**FUNCTIONAL BLOCK**

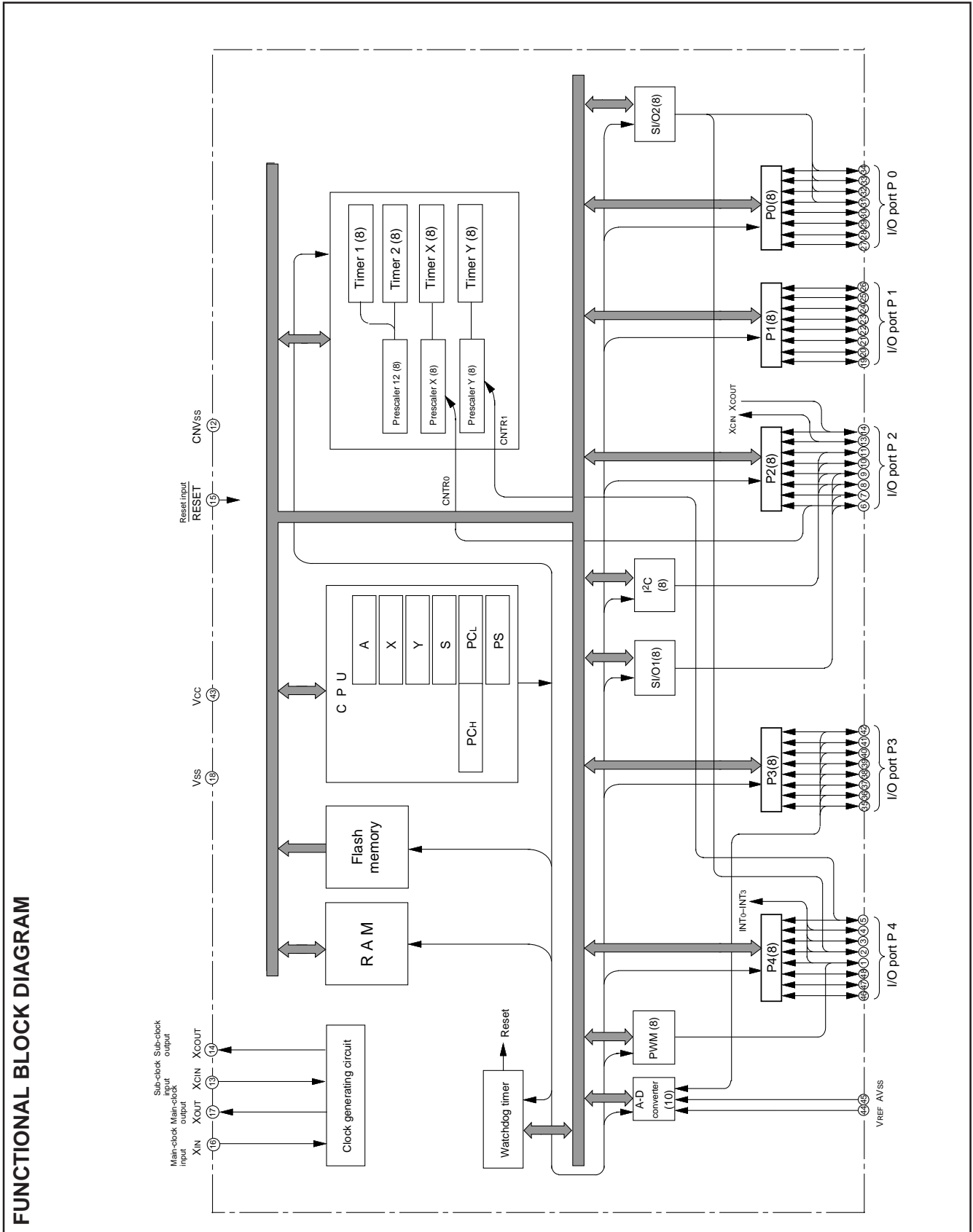


Fig. 2 Functional block diagram

**PIN DESCRIPTION**

**Table 1 Pin description**

Pin	Name	Functions	
			Function except a port function
VCC, VSS	Power source	•Apply voltage of 2.7 V – 5.5 V to Vcc, and 0 V to Vss.	
CNVSS	CNVSS input	•This pin controls the operation mode of the chip. •Normally connected to VSS.	
RESET	Reset input	•Reset input pin for active “L.”	
XIN	Clock input	•Input and output pins for the clock generating circuit. •Connect a ceramic resonator or quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency.	
XOUT	Clock output	•When an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open.	
P00/SIN2 P01/SOUT2 P02/SCLK2 P03/SRDY2 P04–P07	I/O port P0	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •CMOS 3-state output structure.	• Serial I/O2 function pin
P10–P17	I/O port P1	•P10 to P17 (8 bits) are enabled to output large current for LED drive.	
P20/XCOU P21/XCIN	I/O port P2	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level.	• Sub-clock generating circuit I/O pins (connect a resonator) • I <sup>2</sup> C-BUS interface function pins
P22/SDA1 P23/SCL1		•P22 to P25 can be switched between CMOS compatible input level or SMBUS input level in the I <sup>2</sup> C-BUS interface function.	• I <sup>2</sup> C-BUS interface function pin/ Serial I/O1 function pins
P24/SDA2/RxD P25/SCL2/TxD		•P20, P21, P24 to P27: CMOS3-state output structure. •P24, P25: N-channel open-drain structure in the I <sup>2</sup> C-BUS interface function. •P22, P23: N-channel open-drain structure.	• Serial I/O1 function pin
P26/SCLK			• Serial I/O1 function pin/ Timer X function pin
P27/CNTR0/ SRDY1			
P30/AN0– P37/AN7	I/O port P3	•8-bit CMOS I/O port with the same function as port P0. •CMOS compatible input level. •CMOS 3-state output structure.	• A-D converter input pin
P40/CNTR1	I/O port P4	•8-bit CMOS I/O port with the same function as port P0. •CMOS compatible input level. •CMOS 3-state output structure.	• Timer Y function pin • Interrupt input pins
P41/INT0 P42/INT1			
P43/INT2/SCMP2			• Interrupt input pin/SCMP2 output pin
P44/INT3/PWM			• Interrupt input pin/PWM output pin
P45–P47			

**FUNCTIONAL DESCRIPTION**  
**CENTRAL PROCESSING UNIT (CPU)**

The M37516F8HP uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

- The FST and SLW instructions cannot be used.
- The STP, WIT, MUL, and DIV instructions can be used.

**[CPU Mode Register (CPUM)] 003B16**

The CPU mode register contains the stack page selection bit, etc. The CPU mode register is allocated at address 003B16.

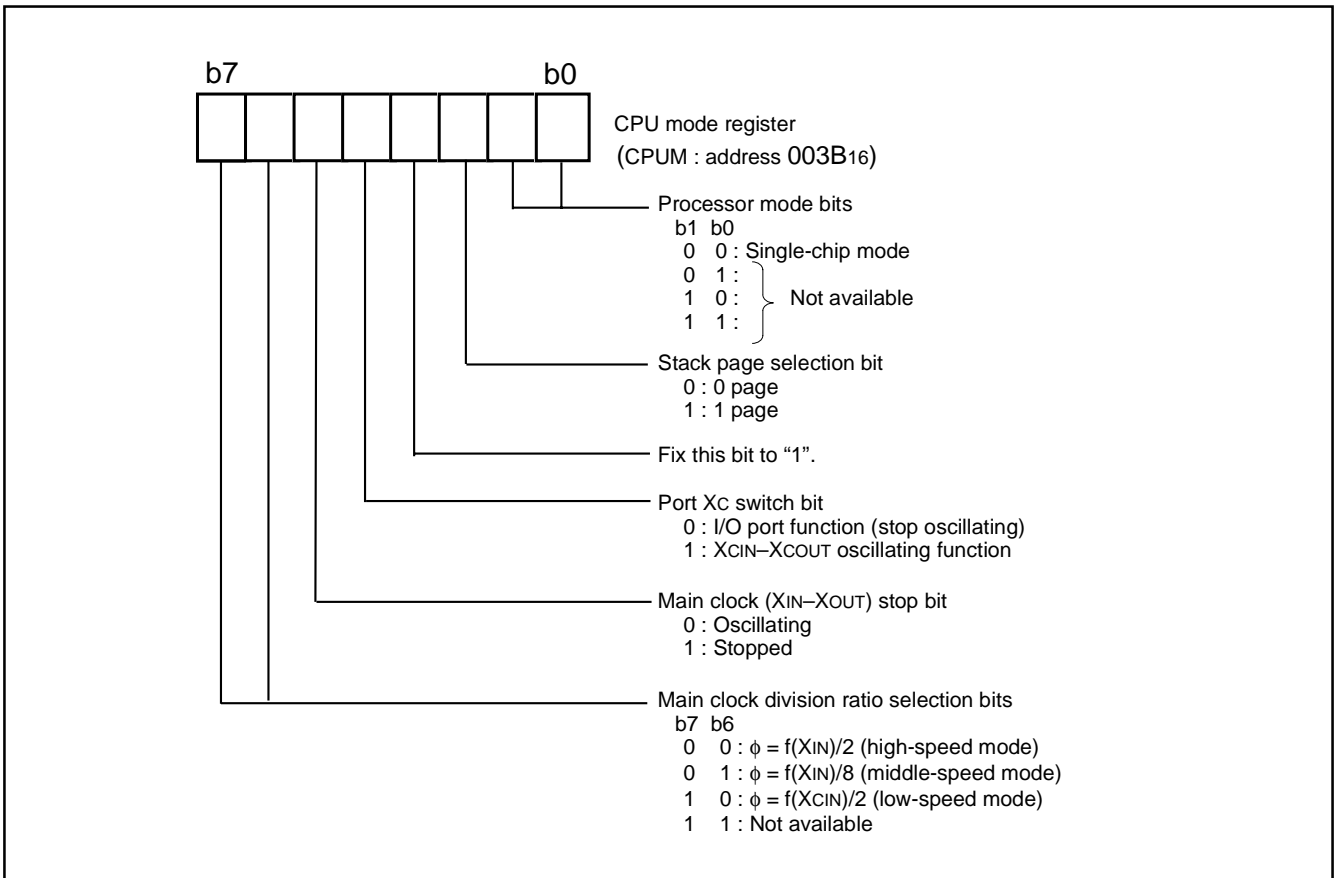


Fig. 3 Structure of CPU mode register

**MEMORY**

**Special Function Register (SFR) Area**

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

**RAM**

RAM is used for data storage and for stack area of subroutine calls and interrupts.

**Flash Memory**

The first 128 bytes and the last 2 bytes of flash memory are reserved for device testing and the rest is user area for storing programs.

**Interrupt Vector Area**

The interrupt vector area contains reset and interrupt vectors.

**Zero Page**

Access to this area with only 2 bytes is possible in the zero page addressing mode.

**Special Page**

Access to this area with only 2 bytes is possible in the special page addressing mode.

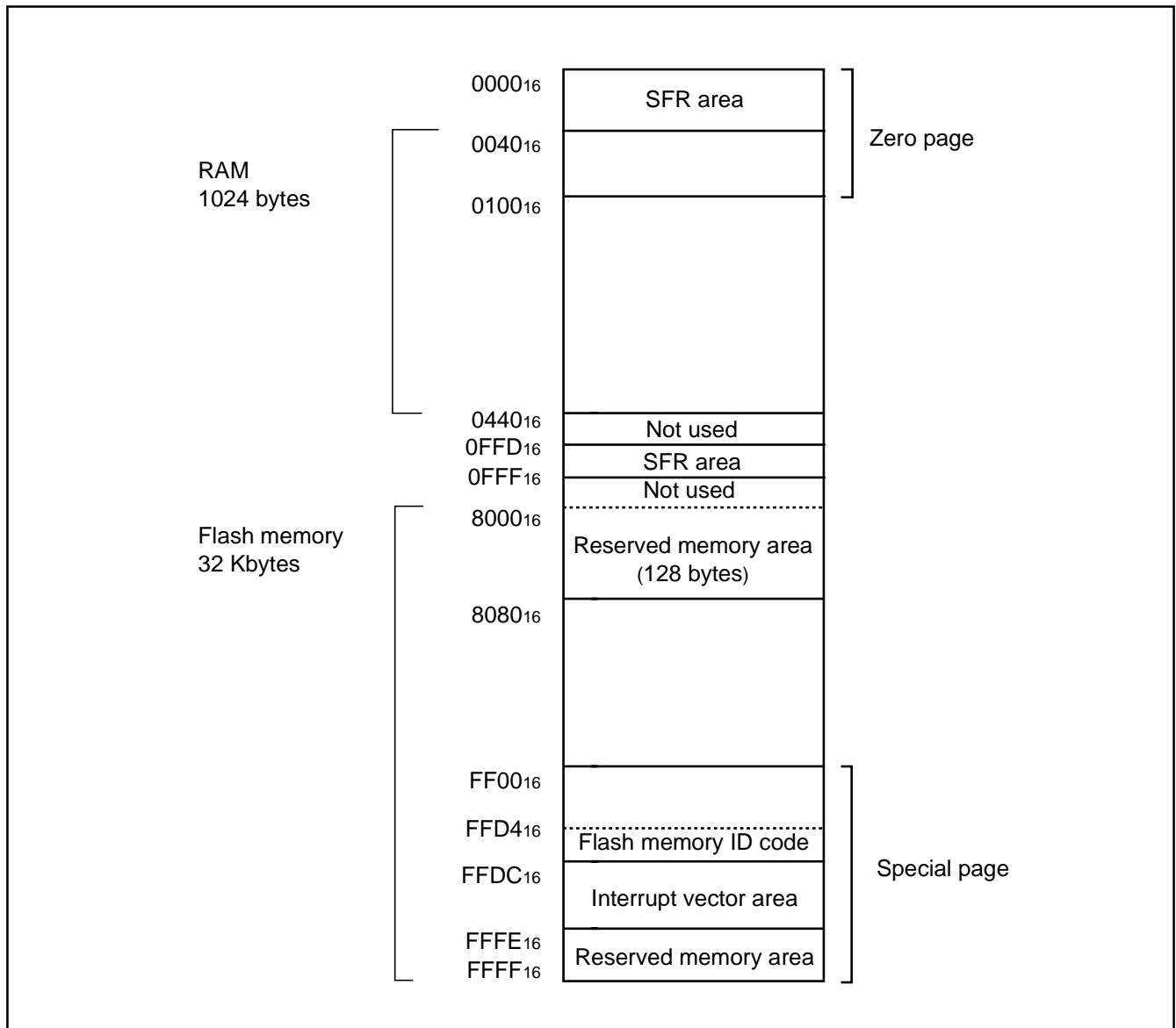


Fig. 4 Memory map diagram

0000 <sub>16</sub>	Port P0 (P0)	0020 <sub>16</sub>	Prescaler 12 (PRE12)
0001 <sub>16</sub>	Port P0 direction register (P0D)	0021 <sub>16</sub>	Timer 1 (T1)
0002 <sub>16</sub>	Port P1 (P1)	0022 <sub>16</sub>	Timer 2 (T2)
0003 <sub>16</sub>	Port P1 direction register (P1D)	0023 <sub>16</sub>	Timer XY mode register (TM)
0004 <sub>16</sub>	Port P2 (P2)	0024 <sub>16</sub>	Prescaler X (PREX)
0005 <sub>16</sub>	Port P2 direction register (P2D)	0025 <sub>16</sub>	Timer X (TX)
0006 <sub>16</sub>	Port P3 (P3)	0026 <sub>16</sub>	Prescaler Y (PREY)
0007 <sub>16</sub>	Port P3 direction register (P3D)	0027 <sub>16</sub>	Timer Y (TY)
0008 <sub>16</sub>	Port P4 (P4)	0028 <sub>16</sub>	Timer count source selection register (TCSS)
0009 <sub>16</sub>	Port P4 direction register (P4D)	0029 <sub>16</sub>	
000A <sub>16</sub>		002A <sub>16</sub>	
000B <sub>16</sub>		002B <sub>16</sub>	I <sup>2</sup> C data shift register (S0)
000C <sub>16</sub>		002C <sub>16</sub>	I <sup>2</sup> C address register (S0D)
000D <sub>16</sub>		002D <sub>16</sub>	I <sup>2</sup> C status register (S1)
000E <sub>16</sub>		002E <sub>16</sub>	I <sup>2</sup> C control register (S1D)
000F <sub>16</sub>		002F <sub>16</sub>	I <sup>2</sup> C clock control register (S2)
0010 <sub>16</sub>		0030 <sub>16</sub>	I <sup>2</sup> C start/stop condition control register (S2D)
0011 <sub>16</sub>		0031 <sub>16</sub>	Reserved *
0012 <sub>16</sub>	Reserved *	0032 <sub>16</sub>	
0013 <sub>16</sub>	Reserved *	0033 <sub>16</sub>	
0014 <sub>16</sub>	Reserved *	0034 <sub>16</sub>	A-D control register (ADCON)
0015 <sub>16</sub>	Serial I/O2 control register 1 (SIO2CON1)	0035 <sub>16</sub>	A-D conversion low-order register (ADL)
0016 <sub>16</sub>	Serial I/O2 control register 2 (SIO2CON2)	0036 <sub>16</sub>	A-D conversion high-order register (ADH)
0017 <sub>16</sub>	Serial I/O2 register (SIO2)	0037 <sub>16</sub>	Reserved *
0018 <sub>16</sub>	Transmit/Receive buffer register (TB/RB)	0038 <sub>16</sub>	MISRG
0019 <sub>16</sub>	Serial I/O1 status register (SIOSTS)	0039 <sub>16</sub>	Watchdog timer control register (WDTCN)
001A <sub>16</sub>	Serial I/O1 control register (SIOCON)	003A <sub>16</sub>	Interrupt edge selection register (INTEDGE)
001B <sub>16</sub>	UART control register (UARTCON)	003B <sub>16</sub>	CPU mode register (CPUM)
001C <sub>16</sub>	Baud rate generator (BRG)	003C <sub>16</sub>	Interrupt request register 1 (IREQ1)
001D <sub>16</sub>	PWM control register (PWMCON)	003D <sub>16</sub>	Interrupt request register 2 (IREQ2)
001E <sub>16</sub>	PWM prescaler (PREPWM)	003E <sub>16</sub>	Interrupt control register 1 (ICON1)
001F <sub>16</sub>	PWM register (PWM)	003F <sub>16</sub>	Interrupt control register 2 (ICON2)
		0FFD <sub>16</sub>	Reserved *
		0FFE <sub>16</sub>	Flash memory control register (FCON)
		0FFF <sub>16</sub>	Reserved *

\* Reserved : Do not write any data to the reserved area.

Fig. 5 Memory map of special function register (SFR)

## I/O PORTS

The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

**Table 2 I/O port function**

Pin	Name	Input/Output	I/O Structure	Non-Port Function	Related SFRs	Ref.No.
P00/SIN2 P01/SOUT2 P02/SCLK2 P03/SRDY2	Port P0	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Serial I/O2 function I/O	Serial I/O2 control register	(1)
P04-P07						(2)
P10-P17	Port P1					(3)
P20/XCOUT P21/XCIN	Port P2			Sub-clock generating circuit	CPU mode register	(4)
P22/SDA1 P23/SCL1						(5)
P24/SDA2/RxD P25/SCL2/TxD			CMOS compatible input level CMOS/SMBUS input level (when selecting I <sup>2</sup> C-BUS interface function) N-channel open-drain output	I <sup>2</sup> C-BUS interface func- tion I/O	I <sup>2</sup> C control register	(6)
P26/SCLK			CMOS compatible input level CMOS/SMBUS input level (when selecting I <sup>2</sup> C-BUS interface function) CMOS 3-state output N-channel open-drain output (when selecting I <sup>2</sup> C-BUS interface function)	I <sup>2</sup> C-BUS interface func- tion I/O Serial I/O1 function I/O	I <sup>2</sup> C control register Serial I/O1 control register	(7)
P27/CNTR0/ SRDY1			CMOS compatible input level CMOS 3-state output	Serial I/O1 function I/O Timer X function I/O	Serial I/O1 control register Timer XY mode register	(8)
P30/AN0- P37/AN7	Port P3			A-D conversion input	A-D control register	(9)
P40/CNTR1	Port P4			Timer Y function I/O	Timer XY mode register	(10)
P41/INT0 P42/INT1		External interrupt input	Interrupt edge selection register	(11)		
P43/INT2/SCMP2		External interrupt input SCMP2 output	Interrupt edge selection register Serial I/O2 control register	(12)		
P44/INT3/PWM		External interrupt input PWM output	Interrupt edge selection register PWM control register	(13)		
P45-P47						(5)

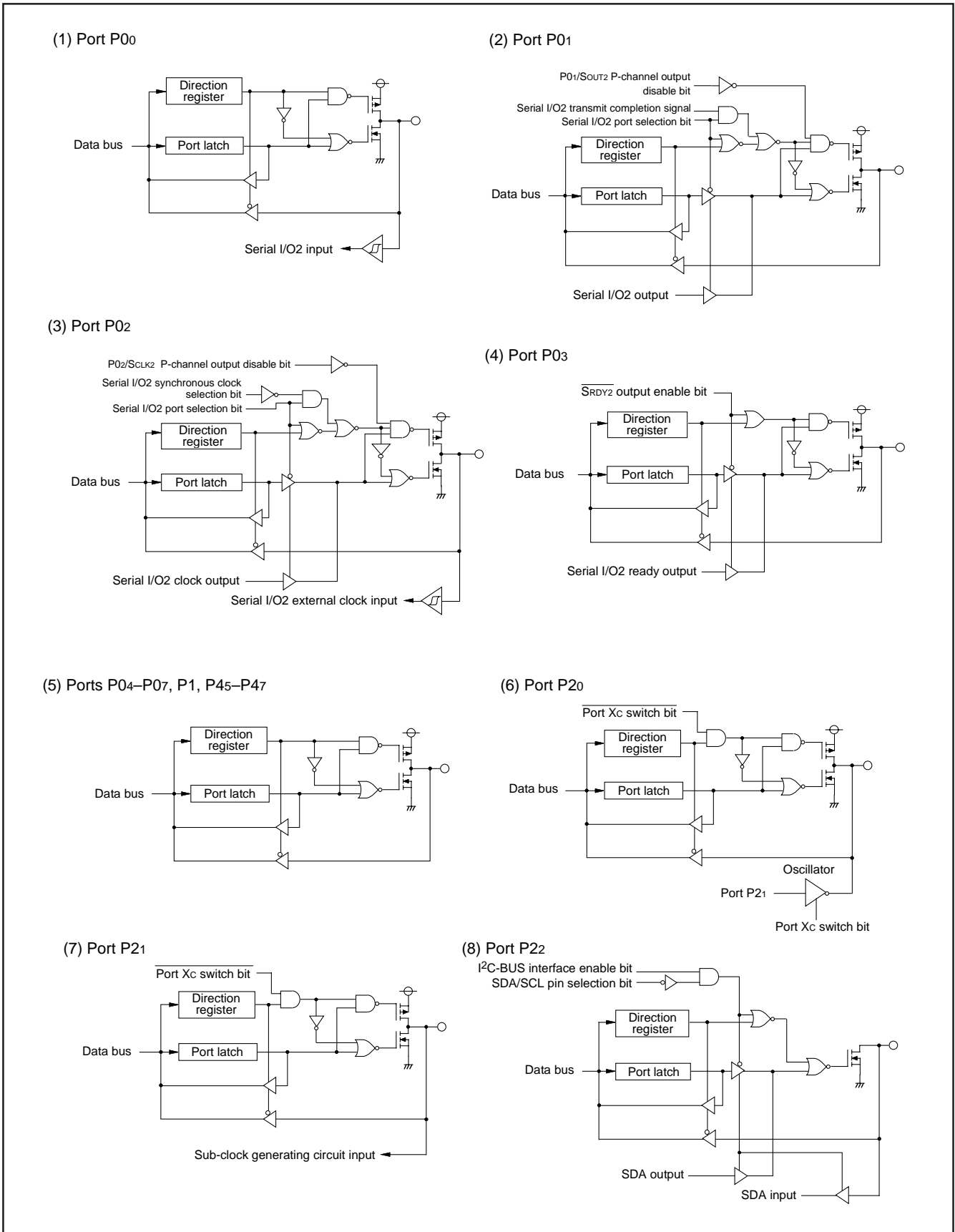


Fig. 6 Port block diagram (1)



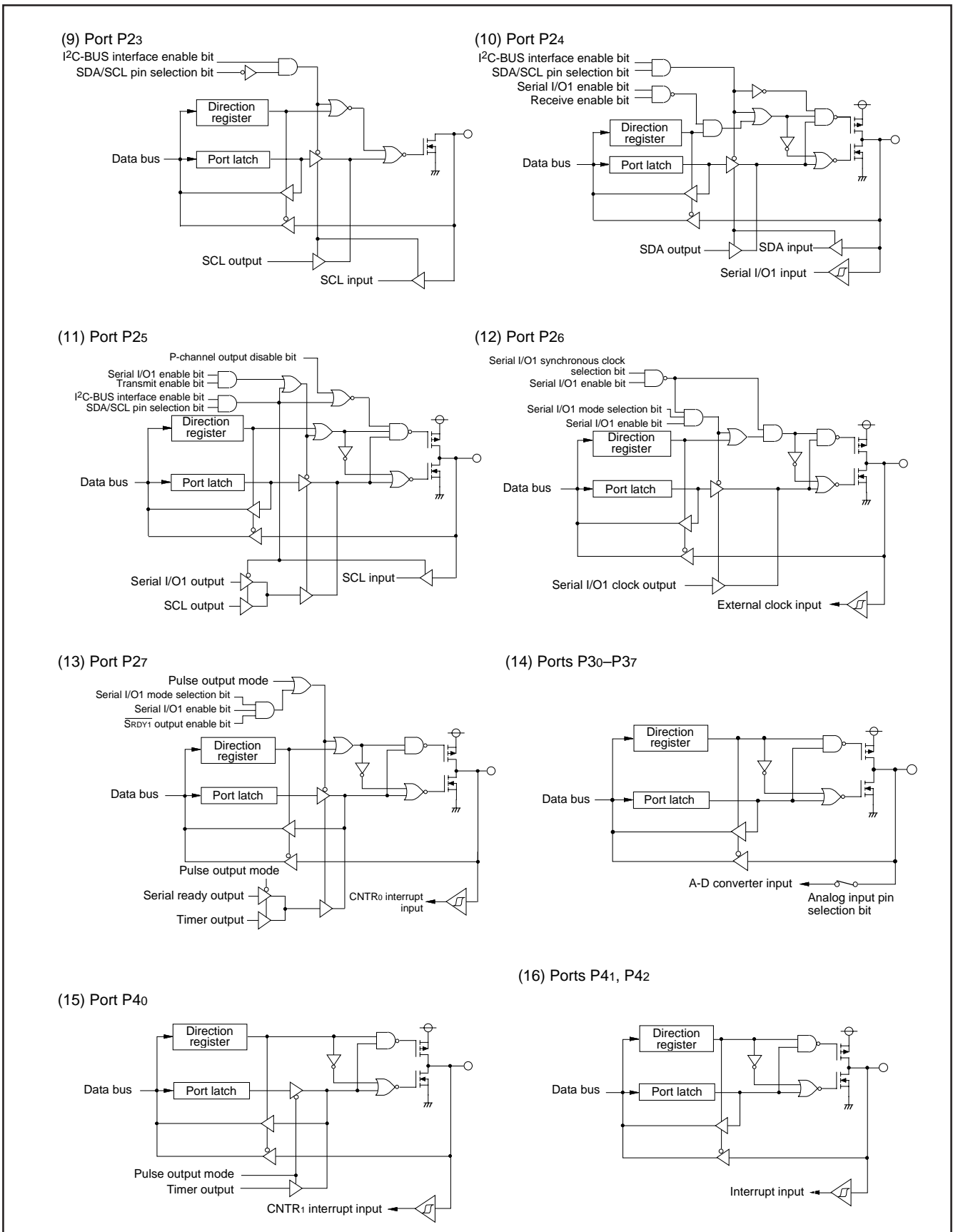


Fig. 7 Port block diagram (2)

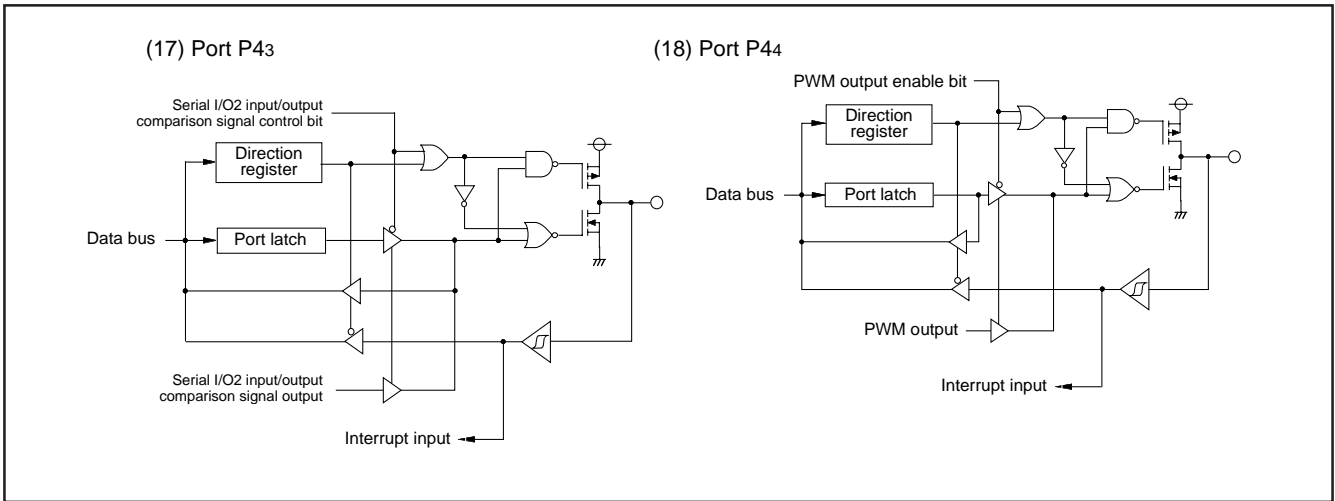


Fig. 8 Port block diagram (3)

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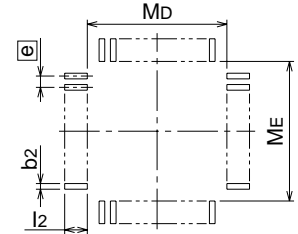
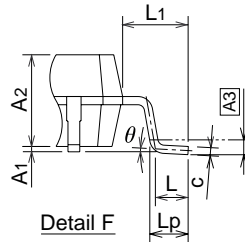
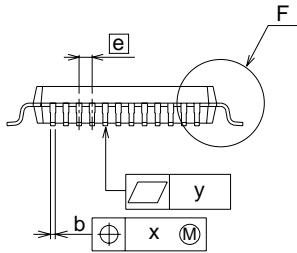
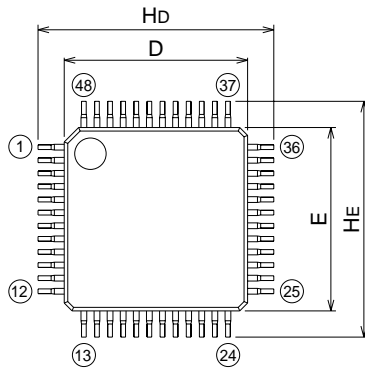
SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

**PACKAGE OUTLINE**

**48P6Q-A**

**Plastic 48pin 7X7mm body LQFP**

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP48-P-77-0.50	-	-	Cu Alloy



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	-	-	1.7
A1	0	0.1	0.2
A2	-	1.4	-
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
e	-	0.5	-
Hd	8.8	9.0	9.2
HE	8.8	9.0	9.2
L	0.35	0.5	0.65
L1	-	1.0	-
Lp	0.45	0.6	0.75
A3	-	0.25	-
x	-	-	0.08
y	-	-	0.1
θ	0°	-	8°
b2	-	0.225	-
l2	1.0	-	-
MD	-	7.4	-
ME	-	7.4	-

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REVISION HISTORY

M37516F8HP DATA SHEET

Rev. No.	Revision Description	Rev. date
0.1	First Edition	2/3/00