M37702M2LXXXGP, M37702S1LGP
M37702M2LXXXHP, M37702S1LHP

SINGLE-CHIP 16-BIT CMOS MICROCOMPUTER

DESCRIPTION

The M37702M2LXXXGP is a single-chip 16-bit microcomputer designed with high-performance CMOS silicon gate technology. This is housed in a small 80-pin plastic molded QFP. This single-chip microcomputer has a large 16 M bytes address space, three instruction queue buffers, and two data buffers for high-speed instruction execution. The CPU is a 16-bit parallel processor that can also be switched to perform 8-bit parallel processing. This microcomputer is suitable for communication, office, business and industrial equipment controller that require high-speed processing of large data.

The strong points of the M37702M2LXXXGP, M37702S1LGP, M37702M2LXXXHP and M37702S1LHP are the low supply voltage and small package.

The differences between M37702M2LXXXGP, M37702S1LGP, M37702M2LXXXHP and M37702S1LHP are the ROM size and the package as shown below. Therefore, the following descriptions will be for the M37702M2LXXXGP unless otherwise noted.

Type name	ROM size	Package
M37702M2LXXXGP	16 K bytes	80-pin plastic molded QFP (80P6S-A)
M37702S1LGP	External	80-pin plastic molded QFP (80P6S-A)
M37702M2LXXXHP	16 K bytes	80-pin plastic molded fine-pitch QFP (80P6D-A)
M37702S1LHP	External	80-pin plastic molded fine-pitch QFP (80P6D-A)

FEATURES

- Number of basic instructions 103
- Memory size ROM ..... 16 K bytes
  RAM ..... 512 bytes
- Instruction execution time
  The fastest instruction at 8 MHz frequency ..... 500 ns
- Single low supply voltage ..... 2.7 – 5.5 V
- Low power dissipation
  (At 3 V supply voltage, 8 MHz frequency) ..... 12 mW (Typ.)
  (At 5 V supply voltage, 8 MHz frequency) ..... 30 mW (Typ.)
- Wide operating temperature range ..... –40 – 80°C
- Interrupts ..... 19 types 7 levels
- Multiple function 16-bit timer ..... 5 + 3
- UART (may also be synchronous) 2
- 8-bit A-D converter ..... 8-channel inputs
- 12-bit watchdog timer
- Programmable input/output
  (ports P0, P1, P2, P3, P4, P5, P6, P7, P8) 68
- Small package
  M37702M2LXXXGP, M37702S1LGP
  ..... 80-pin QFP (0.65 mm lead pitch)
  M37702M2LXXXHP, M37702S1LHP
  ..... 80-pin fine-pitch QFP (0.5 mm lead pitch)

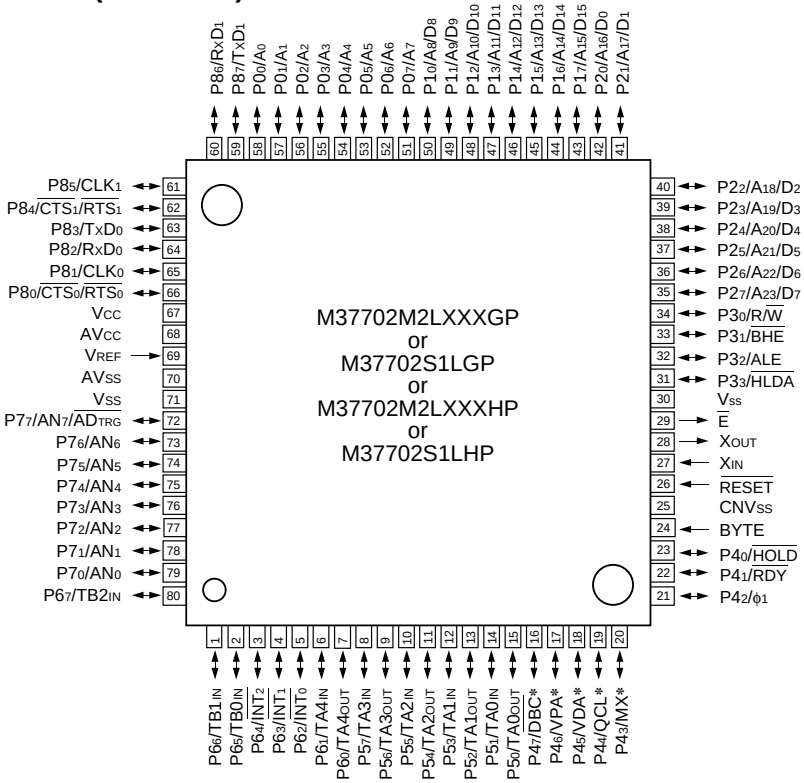
APPLICATION

Control devices for communication equipment such as cellular radio telephones, cordless telephones, and radio communications
Control devices for office equipment such as copiers, printers, typewriters, facsimiles, word processors, and personal computers
Control devices for industrial equipments such as ME, NC, and measuring instruments

NOTE

Refer to “Chapter 5 PRECAUTIONS” when using this microcomputer.

PIN CONFIGURATION (TOP VIEW)

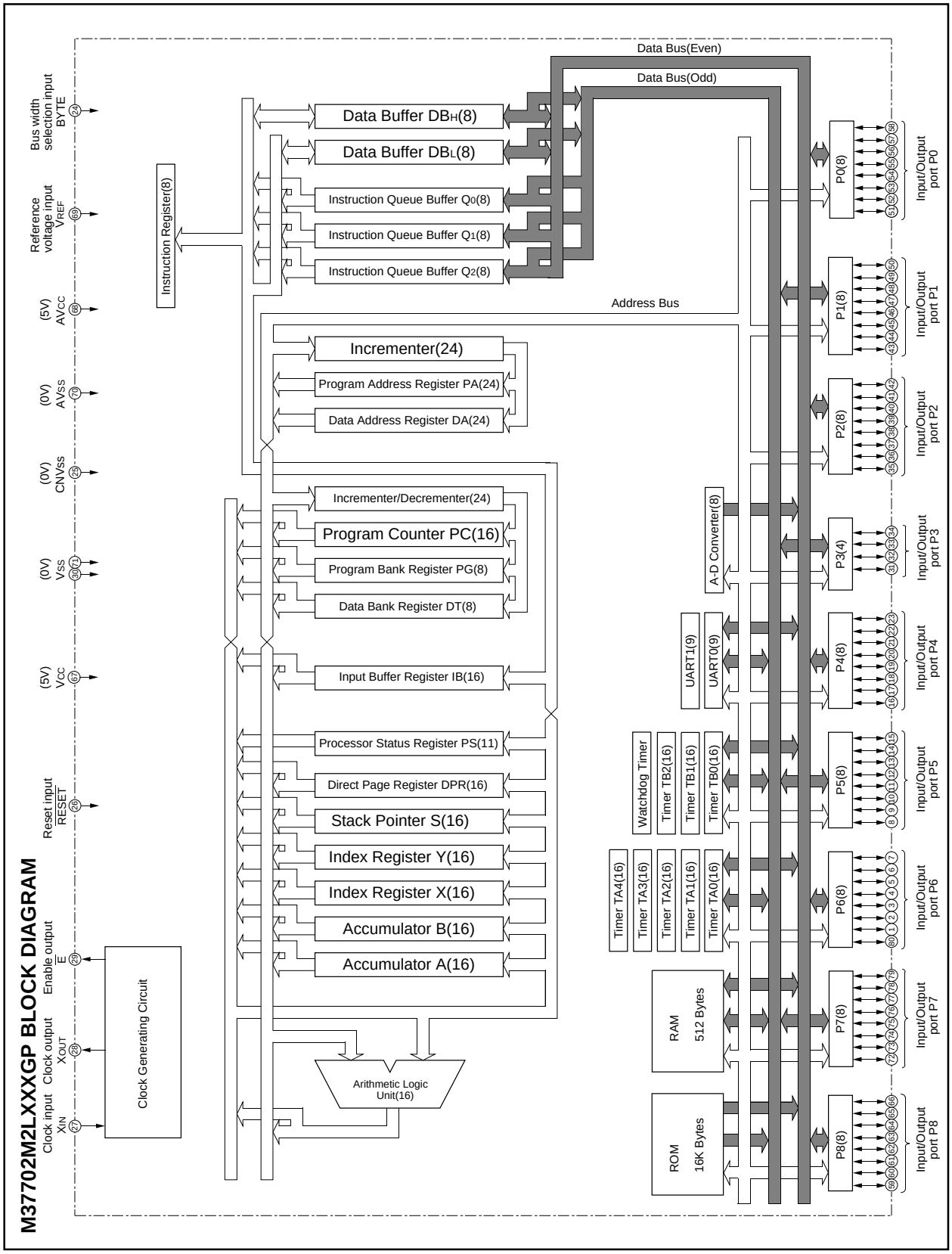


Outline

M37702M2LXXXGP, M37702S1LGP••••••80P6S-A

M37702M2LXXXHP, M37702S1LHP••••••80P6D-A

✻ : Used in the evaluation chip mode only


M37702M2LXXXGP BLOCK DIAGRAM
Data Bus(Even)
Data Bus(Odd)
Data Buffer DBH(8)
Data Buffer DBL(8)
Instruction Queue Buffer Q0(8)
Instruction Queue Buffer Q1(8)
Instruction Queue Buffer Q2(8)
Instruction Register(8)
Address Bus
Incrementer(24)
Program Address Register PA(24)
Data Address Register DA(24)
Incrementer/Decrementer(24)
Program Counter PC(16)
Program Bank Register PG(8)
Data Bank Register DT(8)
Input Buffer Register IB(16)
Processor Status Register PS(11)
Direct Page Register DPR(16)
Stack Pointer S(16)
Index Register Y(16)
Index Register X(16)
Accumulator B(16)
Accumulator A(16)
Arithmetic Logic Unit(16)
Clock Generating Circuit
A-D Converter(8)
UART1(9)
UART0(9)
Watchdog Timer
Timer TB2(16)
Timer TB1(16)
Timer TB0(16)
Timer TA4(16)
Timer TA3(16)
Timer TA2(16)
Timer TA1(16)
Timer TA0(16)
RAM 512 Bytes
ROM 16K Bytes
Bus width selection input BYTE
Reference voltage input VREF
(5V) AVCC
(0V) AVSS
(0V) CNVSS
(0V) VSS
(5V) VCC
Reset input RESET
Enable output E
Clock output XOUT
Clock input XIN
P0(8)
P1(8)
P2(8)
P3(4)
P4(8)
P5(8)
P6(8)
P7(8)
P8(8)
Input/Output port P0
Input/Output port P1
Input/Output port P2
Input/Output port P3
Input/Output port P4
Input/Output port P5
Input/Output port P6
Input/Output port P7
Input/Output port P8

FUNCTIONS OF M37702M2LXXXGP

Parameter		Functions
Number of basic instructions		103
Instruction execution time		500 ns (the fastest instruction at external clock 8 MHz frequency)
Memory size	ROM	16 K bytes
	RAM	512 bytes
Input/Output ports	P0 – P2, P4 – P8	8-bit × 8
	P3	4-bit × 1
Multi-function timers	TA0, TA1, TA2, TA3, TA4	16-bit × 5
	TB0, TB1, TB2	16-bit × 3
Serial I/O		(UART or clock synchronous serial I/O) × 2
A-D converter		8-bit × 1 (8 channels)
Watchdog timer		12-bit × 1
Interrupts		3 external types, 16 internal types (Each interrupt can be set the priority levels to 0 – 7.)
Clock generating circuit		Built-in (externally connected to a ceramic resonator or quartz crystal resonator)
Supply voltage		2.7 – 5.5 V
Power dissipation		12 mW (at 3 V supply voltage, external clock 8 MHz frequency)
		30 mW (at 5 V supply voltage, external clock 8 MHz frequency)
Input/Output characteristic	Input/Output voltage	5 V
	Output current	5 mA
Memory expansion		Maximum 16 M bytes
Operating temperature range		–40 – 85°C
Device structure		CMOS high-performance silicon gate process
Package	M37702M2LXXXGP, M37702S1LGP	80-pin plastic molded QFP (80P6S-A: 0.65 mm lead pitch)
	M37702M2LXXXHP, M37702S1LHP	80-pin plastic molded fine-pitch QFP (80P6D-A: 0.5 mm lead pitch)

PIN DESCRIPTION

Pin	Name	Input/Output	Functions
V_{CC}, V_{SS}	Power supply		Supply 2.7 – 5.5 V to V_{CC} and 0 V to V_{SS}.
CNV_{SS}	CNV_{SS} input	Input	This pin controls the processor mode. Connect to V_{SS} for single-chip mode, and to V_{CC} for external ROM types.
$\overline{RESET}$	Reset input	Input	To enter the reset state, this pin must be kept at a "L" condition which should be maintained for the required time.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit. Connect a ceramic or quartz crystal resonator between X_{IN} and X_{OUT}. When an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
$\overline{E}$	Enable output	Output	Data or instruction read and data write are performed when output from this pin is "L".
BYTE	Bus width selection input	Input	In memory expansion mode or microprocessor mode, this pin determines whether the external data bus is 8-bit width or 16-bit width. The width is 16 bits when "L" signal inputs and 8 bits when "H" signal inputs.
AV_{CC}, AV_{SS}	Analog supply input		Power supply for the A-D converter. Connect AV_{CC} to V_{CC} and AV_{SS} to V_{SS} externally.
V_{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D converter.
$P0_0$ – $P0_7$	I/O port P0	I/O	In single-chip mode, port P0 becomes an 8-bit I/O port. An I/O direction register is available so that each pin can be programmed for input or output. These ports are in input mode when reset. Address (A_7 – A_0) is output in memory expansion mode or microprocessor mode.
$P1_0$ – $P1_7$	I/O port P1	I/O	In single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to "L" in memory expansion mode or microprocessor mode and external data bus is 16-bit width, high-order data (D_{15} – D_8) is input or output when $\overline{E}$ output is "L" and an address (A_{15} – A_8) is output when $\overline{E}$ output is "H". If the BYTE pin is "H" that is an external data bus is 8-bit width, only address (A_{15} – A_8) is output.
$P2_0$ – $P2_7$	I/O port P2	I/O	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode low-order data (D_7 – D_0) is input or output when $\overline{E}$ output is "L" and an address (A_{23} – A_{16}) is output when $\overline{E}$ output is "H".
$P3_0$ – $P3_3$	I/O port P3	I/O	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, R/$\overline{W}$, $\overline{BHE}$, ALE and $\overline{HLDA}$ signals are output.
$P4_0$ – $P4_7$	I/O port P4	I/O	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, $P4_0$ and $P4_1$ become $\overline{HOLD}$ and $\overline{RDY}$ input pin respectively. Functions of other pins are the same as in single-chip mode. In single-chip mode or memory expansion mode, port $P4_2$ can be programmed for ϕ_1 output pin divided the clock to X_{IN} pin by 2. In microprocessor mode. $P4_2$ always has the function as ϕ_1 output pin.
$P5_0$ – $P5_7$	I/O port P5	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as I/O pins for timer A0, timer A1, timer A2 and timer A3.
$P6_0$ – $P6_7$	I/O port P6	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as I/O pins for timer A4, external interrupt input $\overline{INT_0}$, $\overline{INT_1}$ and $\overline{INT_2}$ pins, and input pins for timer B0, timer B1 and timer B2.
$P7_0$ – $P7_7$	I/O port P7	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as analog input AN_0 – AN_7 input pins. $P7_7$ also has an A-D conversion trigger input function.
$P8_0$ – $P8_7$	I/O port P8	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as RxD, TxD, CLK, $\overline{CTS}$/$\overline{RTS}$ pins for UART 0 and UART 1.

BASIC FUNCTION BLOCKS

The M37702M2LXXXGP has the same functions as the M37702M2BXXXFP except for the reset circuit.
Refer to the section on the M37702M2BXXXFP.

RESET CIRCUIT

Reset occurs when the $\overline{\text{RESET}}$ pin is returned to "H" level after holding it at "L" level when the power voltage is at 2.7 – 5.5 V. Program execution starts at the address formed by setting the address pins A_{23} – A_{16} to 00_{16}, A_{15} – A_8 to the contents of address $FFFF_{16}$, and A_7 – A_0 to the contents of address $FFFE_{16}$.

Figure 1 shows the status of the internal registers when a reset occurs.
Figure 2 shows an example of a reset circuit. The reset input voltage must be held 0.55 V or lower when the power voltage reaches 2.7 V.

	Address	
(1) Port P0 data direction register	(04_{16})•••	00_{16}
(2) Port P1 data direction register	(05_{16})•••	00_{16}
(3) Port P2 data direction register	(08_{16})•••	00_{16}
(4) Port P3 data direction register	(09_{16})•••	X X X X 0 0 0 0
(5) Port P4 data direction register	($0C_{16}$)•••	00_{16}
(6) Port P5 data direction register	($0D_{16}$)•••	00_{16}
(7) Port P6 data direction register	(10_{16})•••	00_{16}
(8) Port P7 data direction register	(11_{16})•••	00_{16}
(9) Port P8 data direction register	(14_{16})•••	00_{16}
(10) A-D control register	($1E_{16}$)•••	0 0 0 0 0 ? ? ?
(11) A-D sweep pin selection register	($1F_{16}$)•••	X X X X X X 1 1
(12) UART 0 transmit/receive mode register	(30_{16})•••	00_{16}
(13) UART 1 transmit/receive mode register	(38_{16})•••	00_{16}
(14) UART 0 transmit/receive control register 0	(34_{16})•••	X X X X 1 0 0 0
(15) UART 1 transmit/receive control register 0	($3C_{16}$)•••	X X X X 1 0 0 0
(16) UART 0 transmit/receive control register 1	(35_{16})•••	0 0 0 0 0 0 1 0
(17) UART 1 transmit/receive control register 1	($3D_{16}$)•••	0 0 0 0 0 0 1 0
(18) Count start flag	(40_{16})•••	00_{16}
(19) One- shot start flag	(42_{16})•••	X X X 0 0 0 0 0
(20) Up-down flag	(44_{16})•••	00_{16}
(21) Timer A0 mode register	(56_{16})•••	00_{16}
(22) Timer A1 mode register	(57_{16})•••	00_{16}
(23) Timer A2 mode register	(58_{16})•••	00_{16}
(24) Timer A3 mode register	(59_{16})•••	00_{16}
(25) Timer A4 mode register	($5A_{16}$)•••	00_{16}
(26) Timer B0 mode register	($5B_{16}$)•••	0 0 1 X 0 0 0 0
(27) Timer B1 mode register	($5C_{16}$)•••	0 0 1 X 0 0 0 0
(28) Timer B2 mode register	($5D_{16}$)•••	0 0 1 X 0 0 0 0

	Address	
(29) Processor mode register	($5E_{16}$)•••	00_{16}
(30) Watchdog timer	(60_{16})•••	FFF_{16}
(31) Watchdog timer frequency selection flag	(61_{16})•••	X X X X X X 0
(32) A-D conversion interrupt control register	(70_{16})•••	X X X 0 0 0 0
(33) UART 0 transmission interrupt control register	(71_{16})•••	X X X 0 0 0 0
(34) UART 0 receive interrupt control register	(72_{16})•••	X X X 0 0 0 0
(35) UART 1 transmission interrupt control register	(73_{16})•••	X X X 0 0 0 0
(36) UART 1 receive interrupt control register	(74_{16})•••	X X X 0 0 0 0
(37) Timer A0 interrupt control register	(75_{16})•••	X X X 0 0 0 0
(38) Timer A1 interrupt control register	(76_{16})•••	X X X 0 0 0 0
(39) Timer A2 interrupt control register	(77_{16})•••	X X X 0 0 0 0
(40) Timer A3 interrupt control register	(78_{16})•••	X X X 0 0 0 0
(41) Timer A4 interrupt control register	(79_{16})•••	X X X 0 0 0 0
(42) Timer B0 interrupt control register	($7A_{16}$)•••	X X X 0 0 0 0
(43) Timer B1 interrupt control register	($7B_{16}$)•••	X X X 0 0 0 0
(44) Timer B2 interrupt control register	($7C_{16}$)•••	X X X 0 0 0 0
(45) $\overline{\text{INT}_0}$ interrupt control register	($7D_{16}$)•••	X X 0 0 0 0 0
(46) $\overline{\text{INT}_1}$ interrupt control register	($7E_{16}$)•••	X X 0 0 0 0 0
(47) $\overline{\text{INT}_2}$ interrupt control register	($7F_{16}$)•••	X X 0 0 0 0 0
(48) Processor status register PS		0 0 0 ? ? 0 0 0 1 ? ?
(49) Program bank register PG		00_{16}
(50) Program counter PC_H		Content of $FFFF_{16}$
(51) Program counter PC_L		Content of $FFFE_{16}$
(52) Direct page register DPR		0000_{16}
(53) Data bank register DT		00_{16}

Contents of other registers and RAM are not initialized and should be initialized by software.

Fig. 1 Microcomputer internal status during reset

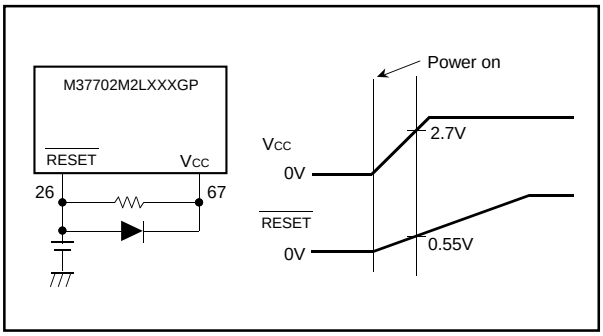


Fig. 2 Example of a reset circuit (perform careful evaluation at the system design level before using)

MEMORY

The memory map is shown in Figure 3.

ADDRESSING MODES

The M37702M2LXXXGP has 28 powerful addressing modes. Refer to the 7700 Family addressing mode description for the details of each addressing mode.

MACHINE INSTRUCTION LIST

The M37702M2LXXXGP has 103 machine instructions. Refer to the 7700 Family machine instruction list for details.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

M37702M2LXXXGP;

(1) M37702M2LXXXGP mask ROM order confirmation form
(2) 80P6S mark specification form
(3) ROM data (EPROM 3 sets)

M37702M2LXXXHP;

(1) M37702M2LXXXHP mask ROM order confirmation form
(2) 80P6D mark specification form
(3) ROM data (EPROM 3 sets)

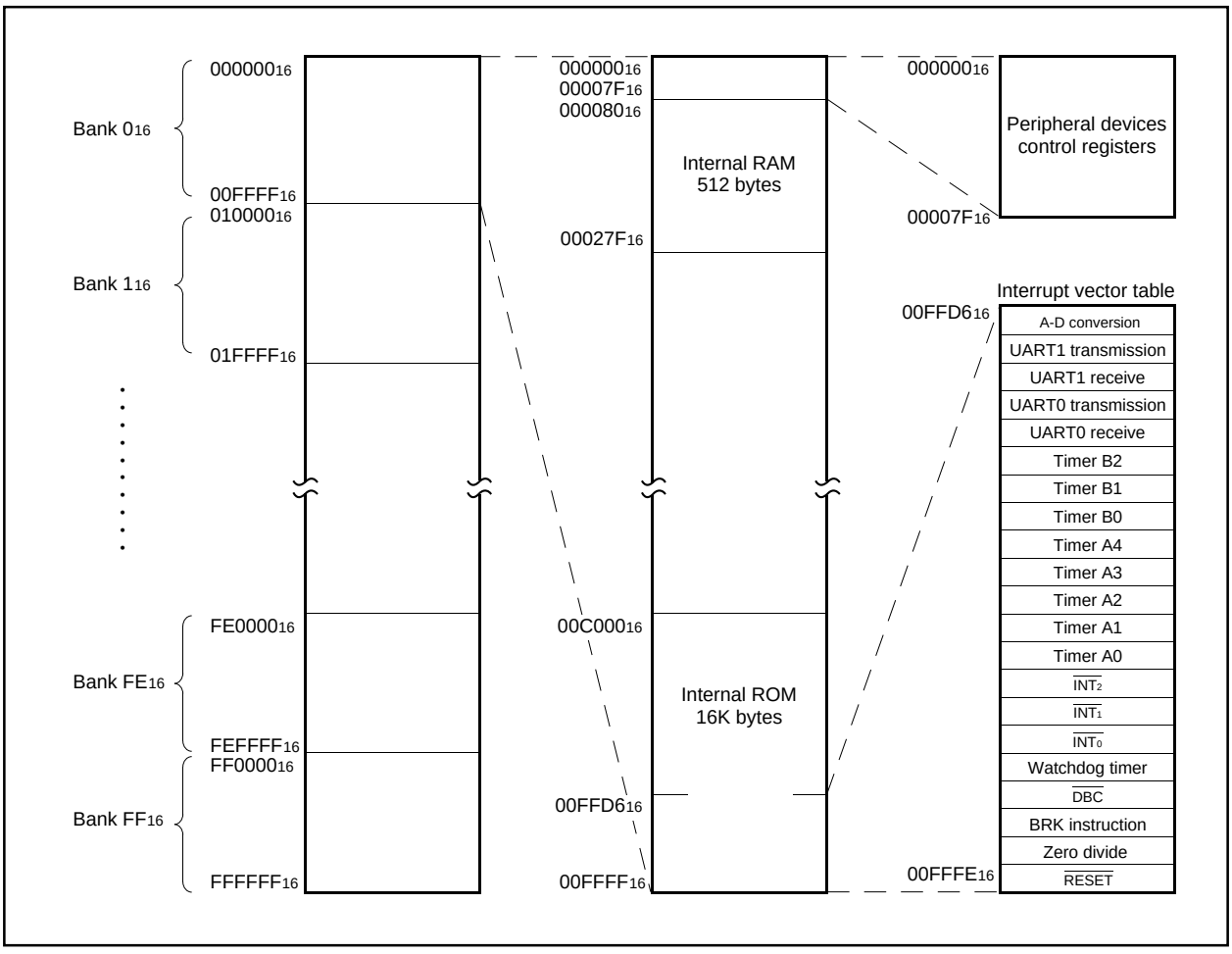


Fig. 3 Memory map

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		–0.3 to 7	V
AV_{CC}	Analog supply voltage		–0.3 to 7	V
V_I	Input voltage $\overline{RESET}$, CNV_{SS}, BYTE		–0.3 to 12	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, V_{REF}, X_{IN}		–0.3 to V_{CC}+0.3	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, X_{OUT}, $\overline{E}$		–0.3 to V_{CC}+0.3	V
P_d	Power dissipation	T_a = 25 °C	300 (Note 1)	mW
T_{opr}	Operating temperature		–40 to 85	°C
T_{stg}	Storage temperature		–65 to 150	°C

Note 1. In the case of M37702M2LXXXHP and M37702S1LHP, the rating of power dissipation is 200 mW.

RECOMMENDED OPERATING CONDITIONS (V_{CC} = 2.7 to 5.5 V, T_a = –40 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage		2.7		5.5	V
AV_{CC}	Analog supply voltage			V_{CC}		V
V_{SS}	Supply voltage			0		V
AV_{SS}	Analog supply voltage			0		V
V_{IH}	High-level input voltage	$P0_0$–$P0_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0.8V_{CC}		V_{CC}	V
V_{IH}	High-level input voltage	$P1_0$–$P1_7$, $P2_0$–$P2_7$ (in single-chip mode)	0.8V_{CC}		V_{CC}	V
V_{IH}	High-level input voltage	$P1_0$–$P1_7$, $P2_0$–$P2_7$ (in memory expansion mode and micro-processor mode)	0.5V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage	$P0_0$–$P0_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0		0.2V_{CC}	V
V_{IL}	Low-level input voltage	$P1_0$–$P1_7$, $P2_0$–$P2_7$ (in single-chip mode)	0		0.2V_{CC}	V
V_{IL}	Low-level input voltage	$P1_0$–$P1_7$, $P2_0$–$P2_7$ (in memory expansion mode and micro-processor mode)	0		0.16V_{CC}	V
$I_{OH(peak)}$	High-level peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$			–10	mA
$I_{OH(avg)}$	High-level average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$			–5	mA
$I_{OL(peak)}$	Low-level peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$			10	mA
$I_{OL(avg)}$	Low-level average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$			5	mA
f(X_{IN})	External clock frequency input				8	MHz

Note 2. Average output current is the average value of a 100 ms interval.

3. The sum of $I_{OL(peak)}$ for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of $I_{OH(peak)}$ for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of $I_{OL(peak)}$ for ports P4, P5, P6, and P7 must be 80 mA or less, and the sum of $I_{OH(peak)}$ for ports P4, P5, P6, and P7 must be 80 mA or less.

ELECTRICAL CHARACTERISTICS (V_{CC} = 5 V, V_{SS} = 0 V, T_a = 25 °C, f(X_{IN}) = 8 MHz, unless otherwise noted)

Symbol	Parameter	Test conditions			Limits			Unit
					Min.	Typ.	Max.	
V_{OH}	High-level output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$, $P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	V_{CC} = 5 V, I_{OH} = –10 mA			3			V
		V_{CC} = 3 V, I_{OH} = –1 mA			2.5			
V_{OH}	High-level output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$, $P3_3$	V_{CC} = 5 V, I_{OH} = –400 µA			4.7			V
V_{OH}	High-level output voltage $P3_2$	V_{CC} = 5 V, I_{OH} = –10 mA			3.1			V
		V_{CC} = 5 V, I_{OH} = –400 µA			4.8			
		V_{CC} = 3 V, I_{OH} = –1 mA			2.6			
V_{OH}	High-level output voltage $\overline{E}$	V_{CC} = 5 V, I_{OH} = –10 mA			3.4			V
		V_{CC} = 5 V, I_{OH} = –400 µA			4.8			
		V_{CC} = 3 V, I_{OH} = –1 mA			2.6			
V_{OL}	Low-level output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$, $P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	V_{CC} = 5 V, I_{OL} = 10 mA					2	V
		V_{CC} = 3 V, I_{OL} = 1 mA					0.5	
V_{OL}	Low-level output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$, $P3_1$, $P3_3$	V_{CC} = 5 V, I_{OL} = 2 mA					0.45	V
V_{OL}	Low-level output voltage $P3_2$	V_{CC} = 5 V, I_{OL} = 10 mA					1.9	V
		V_{CC} = 5 V, I_{OL} = 2 mA					0.43	
		V_{CC} = 3 V, I_{OL} = 1 mA					0.4	
V_{OL}	Low-level output voltage $\overline{E}$	V_{CC} = 5 V, I_{OL} = 10 mA					1.6	V
		V_{CC} = 5 V, I_{OL} = 2 mA					0.4	
		V_{CC} = 3 V, I_{OL} = 1 mA					0.4	
V_{T+} — V_{T-}	Hysteresis $\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$–$TA4_{IN}$, $TB0_{IN}$–$TB2_{IN}$, $\overline{INT0}$–$\overline{INT2}$, AD_{TRG}, $\overline{CTS0}$, $\overline{CTS1}$, $CLK0$, $CLK1$	V_{CC} = 5 V			0.4		1	V
		V_{CC} = 3 V			0.1		0.7	
V_{T+} — V_{T-}	Hysteresis $\overline{RESET}$	V_{CC} = 5 V			0.2		0.5	V
		V_{CC} = 3 V			0.1		0.4	
V_{T+} — V_{T-}	Hysteresis X_{IN}	V_{CC} = 5 V			0.1		0.3	V
		V_{CC} = 3 V			0.06		0.2	
I_{IH}	High-level input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_{CC} = 5 V, V_I = 5 V					5	µA
		V_{CC} = 3 V, V_I = 3 V					4	
I_{IL}	Low-level input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_3$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_{CC} = 5 V, V_I = 0 V					–5	µA
		V_{CC} = 3 V, V_I = 0 V					–4	
V_{RAM}	RAM hold voltage	When clock is stopped.			2			V
I_{CC}	Power supply current	In single-chip mode output only pin is open and other pins are V_{SS} during reset.	f(X_{IN}) = 8 MHz, square waveform	V_{CC} = 5 V		6	12	mA
				V_{CC} = 3 V		4	8	
			T_a = 25 °C when clock is stopped.				1	µA
			T_a = 85 °C when clock is stopped.				20	

A-D CONVERTER CHARACTERISTICS (V_{CC} = 5 V, V_{SS} = 0 V, T_a = 25 °C, f(X_{IN}) = 8 MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	V_{REF} = V_{CC}			8	Bits
—	Absolute accuracy	V_{REF} = V_{CC}			±3	LSB
R_{LADDER}	Ladder resistance	V_{REF} = V_{CC}	2		10	kΩ
t_{CONV}	Conversion time		28.5			µs
V_{REF}	Reference voltage		2.7		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

TIMING REQUIREMENTS (V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = 25 °C, f(X_{IN}) = 8 MHz, unless otherwise noted)

External clock input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_C	External clock input cycle time	125		ns
$t_{W(H)}$	External clock input high-level pulse width	50		ns
$t_{W(L)}$	External clock input low-level pulse width	50		ns
t_r	External clock rise time		20	ns
t_f	External clock fall time		20	ns

Single-chip mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(P0D–E)}$	Port P0 input setup time	300		ns
$t_{su(P1D–E)}$	Port P1 input setup time	300		ns
$t_{su(P2D–E)}$	Port P2 input setup time	300		ns
$t_{su(P3D–E)}$	Port P3 input setup time	300		ns
$t_{su(P4D–E)}$	Port P4 input setup time	300		ns
$t_{su(P5D–E)}$	Port P5 input setup time	300		ns
$t_{su(P6D–E)}$	Port P6 input setup time	300		ns
$t_{su(P7D–E)}$	Port P7 input setup time	300		ns
$t_{su(P8D–E)}$	Port P8 input setup time	300		ns
$t_{h(E–P0D)}$	Port P0 input hold time	0		ns
$t_{h(E–P1D)}$	Port P1 input hold time	0		ns
$t_{h(E–P2D)}$	Port P2 input hold time	0		ns
$t_{h(E–P3D)}$	Port P3 input hold time	0		ns
$t_{h(E–P4D)}$	Port P4 input hold time	0		ns
$t_{h(E–P5D)}$	Port P5 input hold time	0		ns
$t_{h(E–P6D)}$	Port P6 input hold time	0		ns
$t_{h(E–P7D)}$	Port P7 input hold time	0		ns
$t_{h(E–P8D)}$	Port P8 input hold time	0		ns

Memory expansion mode and microprocessor mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(P1D–E)}$	Port P1 input setup time	80		ns
$t_{su(P2D–E)}$	Port P2 input setup time	80		ns
$t_{su(RDY–\phi1)}$	$\overline{RDY}$ input setup time	90		ns
$t_{su(HOLD–\phi1)}$	$\overline{HOLD}$ input setup time	90		ns
$t_{h(E–P1D)}$	Port P1 input hold time	0		ns
$t_{h(E–P2D)}$	Port P2 input hold time	0		ns
$t_{h(\phi1–RDY)}$	$\overline{RDY}$ input hold time	0		ns
$t_{h(\phi1–HOLD)}$	$\overline{HOLD}$ input hold time	0		ns

Timer A input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN input cycle time	250		ns
$t_{W(TAH)}$	TAiIN input high-level pulse width	125		ns
$t_{W(TAL)}$	TAiIN input low-level pulse width	125		ns

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN input cycle time	1000		ns
$t_{W(TAH)}$	TAiIN input high-level pulse width	500		ns
$t_{W(TAL)}$	TAiIN input low-level pulse width	500		ns

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN input cycle time	500		ns
$t_{W(TAH)}$	TAiIN input high-level pulse width	250		ns
$t_{W(TAL)}$	TAiIN input low-level pulse width	250		ns

Timer A input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{W(TAH)}$	TAiIN input high-level pulse width	250		ns
$t_{W(TAL)}$	TAiIN input low-level pulse width	250		ns

Timer A input (Up-down input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(UP)}$	TAiOUT input cycle time	5000		ns
$t_{W(UPH)}$	TAiOUT input high-level pulse width	2500		ns
$t_{W(UPL)}$	TAiOUT input low-level pulse width	2500		ns
$t_{su(UP-TIN)}$	TAiOUT input setup time	1000		ns
$t_{h(TIN-UP)}$	TAiOUT input hold time	1000		ns

Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(TB)}$	TBi_{IN} input cycle time (one edge count)	250		ns
$t_{W(TBH)}$	TBi_{IN} input high-level pulse width (one edge count)	125		ns
$t_{W(TBL)}$	TBi_{IN} input low-level pulse width (one edge count)	125		ns
$t_{C(TB)}$	TBi_{IN} input cycle time (both edges count)	500		ns
$t_{W(TBH)}$	TBi_{IN} input high-level pulse width (both edges count)	250		ns
$t_{W(TBL)}$	TBi_{IN} input low-level pulse width (both edges count)	250		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(TB)}$	TBi_{IN} input cycle time	1000		ns
$t_{W(TBH)}$	TBi_{IN} input high-level pulse width	500		ns
$t_{W(TBL)}$	TBi_{IN} input low-level pulse width	500		ns

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(TB)}$	TBi_{IN} input cycle time	1000		ns
$t_{W(TBH)}$	TBi_{IN} input high-level pulse width	500		ns
$t_{W(TBL)}$	TBi_{IN} input low-level pulse width	500		ns

A-D trigger input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(AD)}$	$\overline{ADTRG}$ input cycle time (minimum allowable trigger)	2000		ns
$t_{W(ADL)}$	$\overline{ADTRG}$ input low-level pulse width	250		ns

Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(CK)}$	CLK_i input cycle time	500		ns
$t_{W(CKH)}$	CLK_i input high-level pulse width	250		ns
$t_{W(CKL)}$	CLK_i input low-level pulse width	250		ns
$t_{d(C-Q)}$	TxD_i output delay time		170	ns
$t_{h(C-Q)}$	TxD_i hold time	0		ns
$t_{su(D-C)}$	RxD_i input setup time	80		ns
$t_{h(C-D)}$	RxD_i input hold time	100		ns

External interrupt $\overline{INT_i}$ input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT_i}$ input high-level pulse width	250		ns
$t_{W(INL)}$	$\overline{INT_i}$ input low-level pulse width	250		ns

SWITCHING CHARACTERISTICS (V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = 25 °C, f(X_{IN}) = 8 MHz, unless otherwise noted)

Single-chip mode

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
td(E–P0Q)	Port P0 data output delay time	Fig. 4		300	ns
td(E–P1Q)	Port P1 data output delay time			300	ns
td(E–P2Q)	Port P2 data output delay time			300	ns
td(E–P3Q)	Port P3 data output delay time			300	ns
td(E–P4Q)	Port P4 data output delay time			300	ns
td(E–P5Q)	Port P5 data output delay time			300	ns
td(E–P6Q)	Port P6 data output delay time			300	ns
td(E–P7Q)	Port P7 data output delay time			300	ns
td(E–P8Q)	Port P8 data output delay time			300	ns

Memory expansion mode and microprocessor mode (when wait bit = “0”, and external memory area is accessed)

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
td(P0A–E)	Port P0 address output delay time	Fig. 4	50		ns
td(E–P1Q)	Port P1 data output delay time (BYTE = “L”)			130	ns
tPXZ(E–P1Z)	Port P1 floating start delay time (BYTE = “L”)			10	ns
td(P1A–E)	Port P1 address output delay time		50		ns
td(P1A–ALE)	Port P1 address output delay time		40		ns
td(E–P2Q)	Port P2 data output delay time			130	ns
tPXZ(E–P2Z)	Port P2 floating start delay time			10	ns
td(P2A–E)	Port P2 address output delay time		50		ns
td(P2A–ALE)	Port P2 address output delay time		40		ns
td(φ1–HLDA)	$\overline{\text{HLDA}}$ output delay time			120	ns
td(ALE–E)	ALE output delay time		4		ns
tW(ALE)	ALE pulse width		60		ns
td(BHE–E)	$\overline{\text{BHE}}$ output delay time		50		ns
td(R/W–E)	R/$\overline{\text{W}}$ output delay time		50		ns
td(E–φ1)	φ1 output delay time		0	40	ns
th(E–P0A)	Port P0 address hold time		50		ns
th(ALE–P1A)	Port P1 address hold time (BYTE = “L”)		9		ns
th(E–P1Q)	Port P1 data hold time (BYTE = “L”)		50		ns
tPZX(E–P1Z)	Port P1 floating release delay time (BYTE = “L”)		95		ns
th(E–P1A)	Port P1 address hold time (BYTE = “H”)		50		ns
th(ALE–P2A)	Port P2 address hold time		9		ns
th(E–P2Q)	Port P2 data hold time		50		ns
tPZX(E–P2Z)	Port P2 floating release delay time		95		ns
th(E–BHE)	$\overline{\text{BHE}}$ hold time		18		ns
th(E–R/W)	R/$\overline{\text{W}}$ hold time		18		ns
tW(EL)	$\overline{\text{E}}$ pulse width		460		ns

Memory expansion mode and microprocessor mode (when wait bit = "1")

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
$t_{d(P0A-E)}$	Port P0 address output delay time	Fig. 4	50		ns
$t_{d(E-P1Q)}$	Port P1 data output delay time (BYTE = "L")			130	ns
$t_{PXZ(E-P1Z)}$	Port P1 floating start delay time (BYTE = "L")			10	ns
$t_{d(P1A-E)}$	Port P1 address output delay time		50		ns
$t_{d(P1A-ALE)}$	Port P1 address output delay time		40		ns
$t_{d(E-P2Q)}$	Port P2 data output delay time			130	ns
$t_{PXZ(E-P2Z)}$	Port P2 floating start delay time			10	ns
$t_{d(P2A-E)}$	Port P2 address output delay time		50		ns
$t_{d(P2A-ALE)}$	Port P2 address output delay time		40		ns
$t_{d(\phi1-HLDA)}$	$\overline{HLDA}$ output delay time			120	ns
$t_{d(ALE-E)}$	ALE output delay time		4		ns
$t_{W(ALE)}$	ALE pulse width		60		ns
$t_{d(BHE-E)}$	$\overline{BHE}$ output delay time		50		ns
$t_{d(R/W-E)}$	R/$\overline{W}$ output delay time		50		ns
$t_{d(E-\phi1)}$	$\phi1$ output delay time		0	40	ns
$t_{h(E-P0A)}$	Port P0 address hold time		50		ns
$t_{h(ALE-P1A)}$	Port P1 address hold time (BYTE = "L")		9		ns
$t_{h(E-P1Q)}$	Port P1 data hold time (BYTE = "L")		50		ns
$t_{PZX(E-P1Z)}$	Port P1 floating release delay time (BYTE = "L")		95		ns
$t_{h(E-P1A)}$	Port P1 address hold time (BYTE = "H")		50		ns
$t_{h(ALE-P2A)}$	Port P2 address hold time		9		ns
$t_{h(E-P2Q)}$	Port P2 data hold time		50		ns
$t_{PZX(E-P2Z)}$	Port P2 floating release delay time		95		ns
$t_{h(E-BHE)}$	$\overline{BHE}$ hold time		18		ns
$t_{h(E-R/W)}$	R/$\overline{W}$ hold time		18		ns
$t_{W(EL)}$	$\overline{E}$ pulse width		210		ns

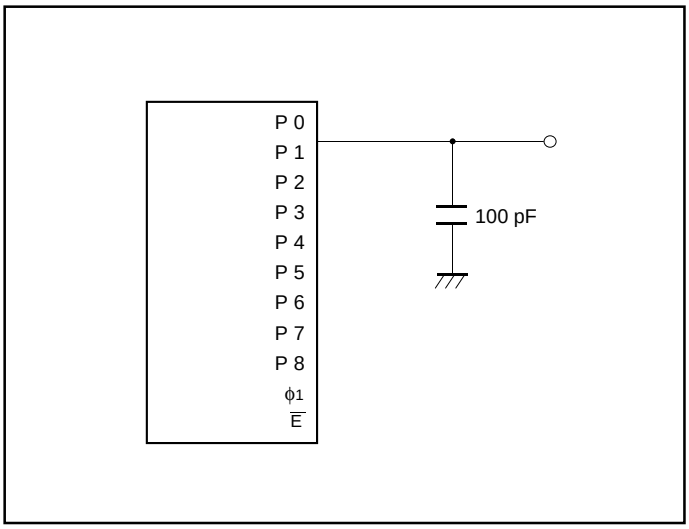
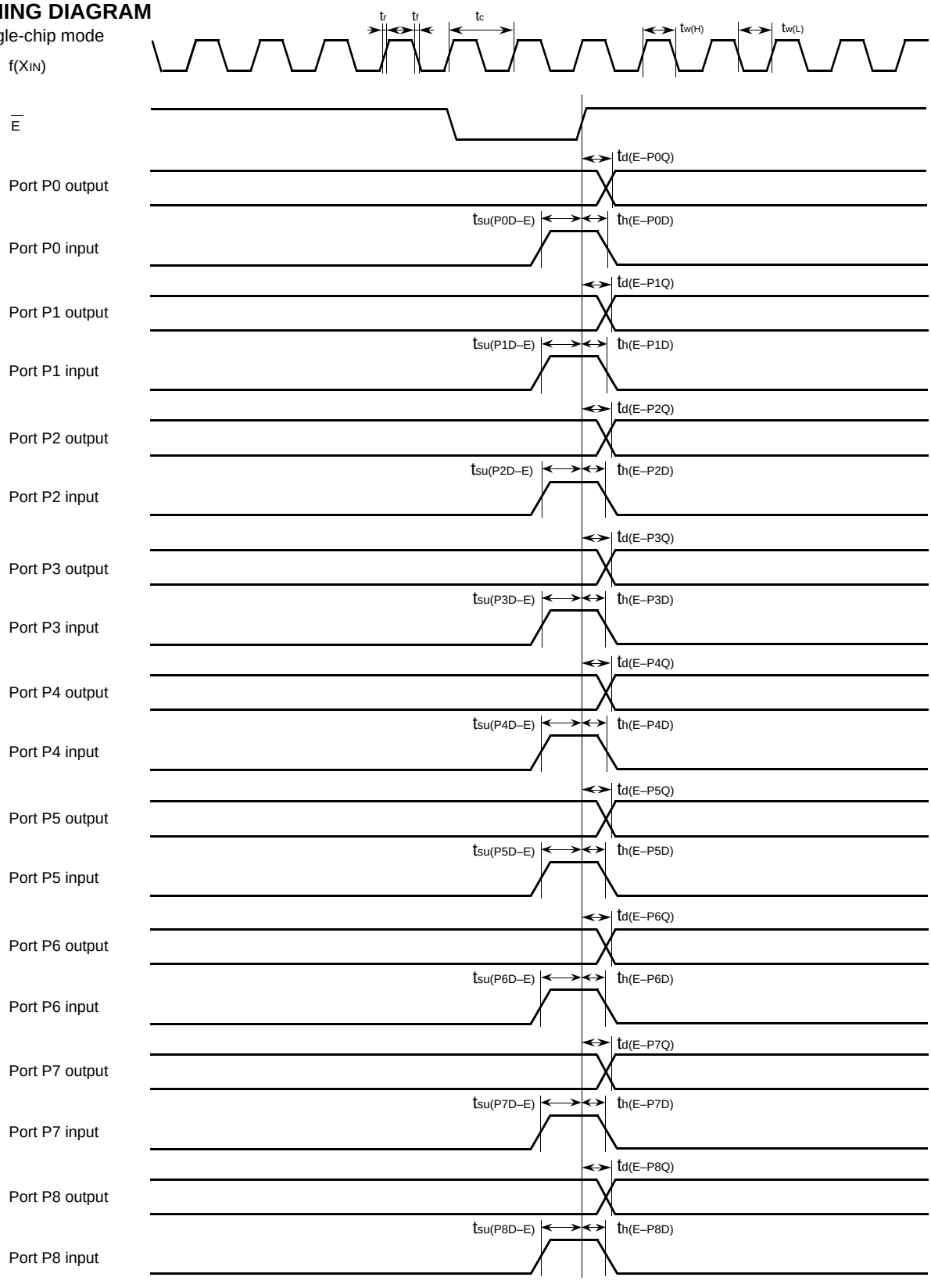
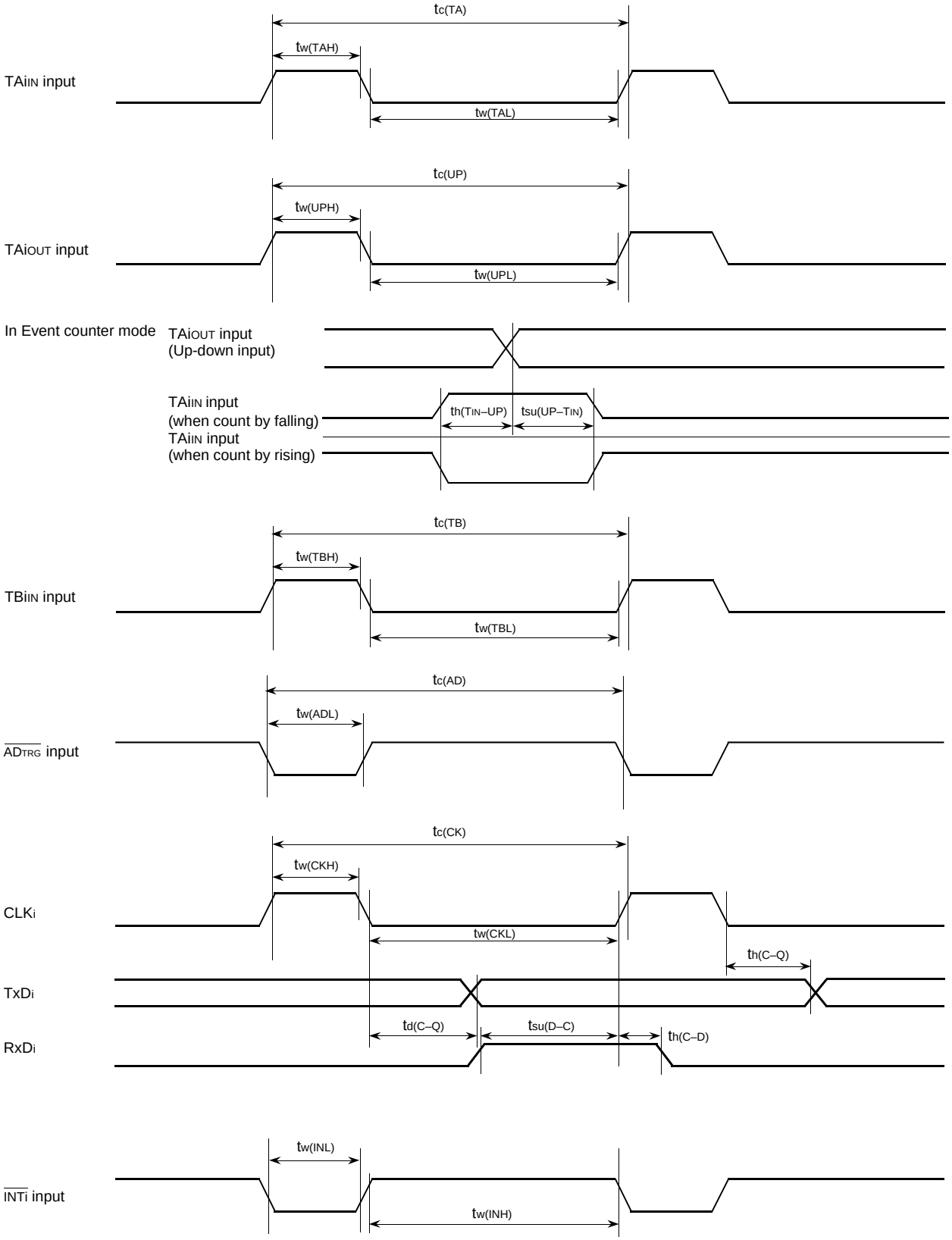


Fig. 4 Testing circuit for ports P0–P8, $\phi1$

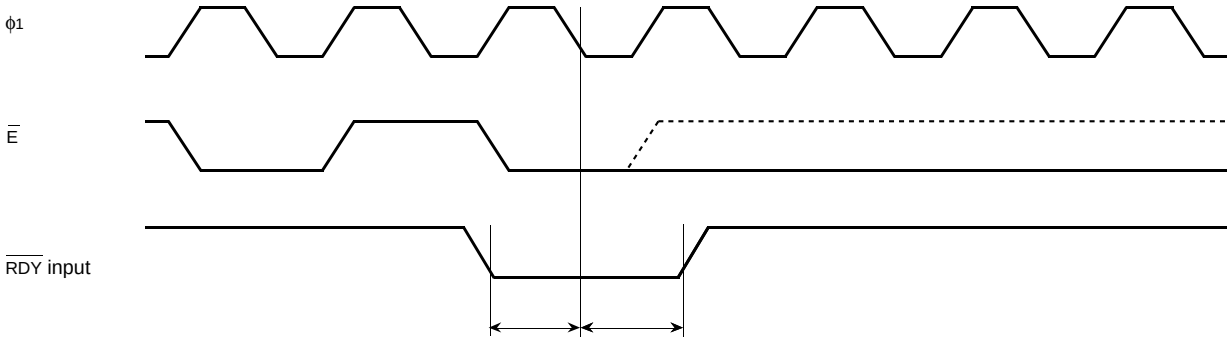
TIMING DIAGRAM

Single-chip mode

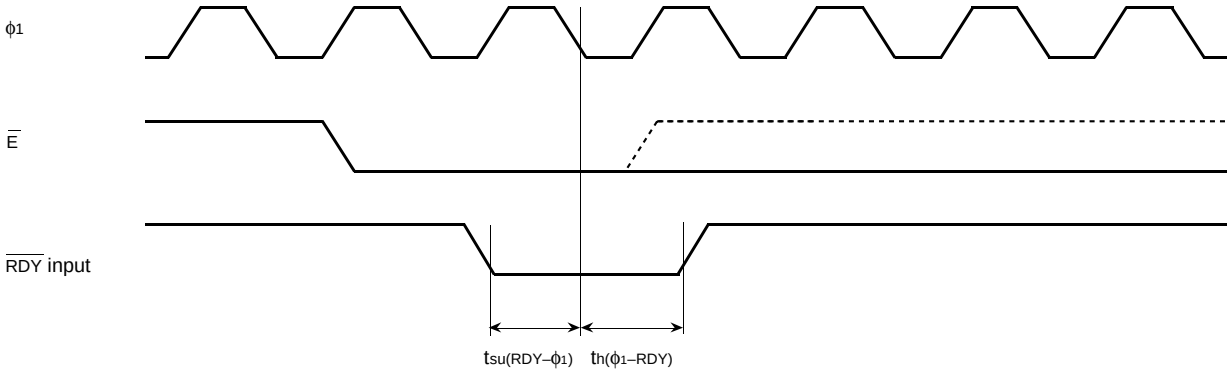



tc(TA)
tw(TAH)
TAiIN input
tw(TAL)
tc(UP)
tw(UPH)
TAiOUT input
tw(UPL)
In Event counter mode
TAiOUT input
(Up-down input)
TAiIN input
(when count by falling)
th(TIN–UP)
tsu(UP–TIN)
TAiIN input
(when count by rising)
tc(TB)
tw(TBH)
TBiIN input
tw(TBL)
tc(AD)
tw(ADL)
ADTRG input
tc(CK)
tw(CKH)
CLKi
tw(CKL)
th(C–Q)
TxDi
td(C–Q)
tsu(D–C)
th(C–D)
RxDi
tw(INL)
INTi input
tw(INH)

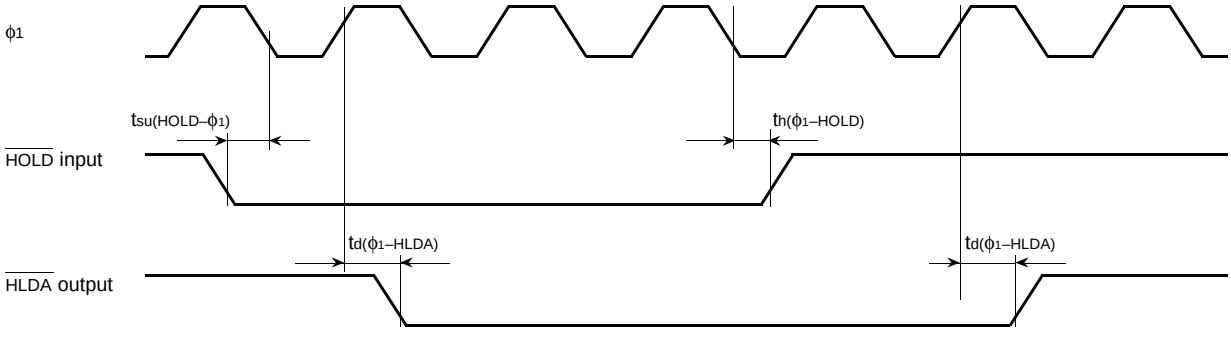
Memory expansion mode and microprocessor mode
(When wait bit = "1")



(When wait bit = "0")

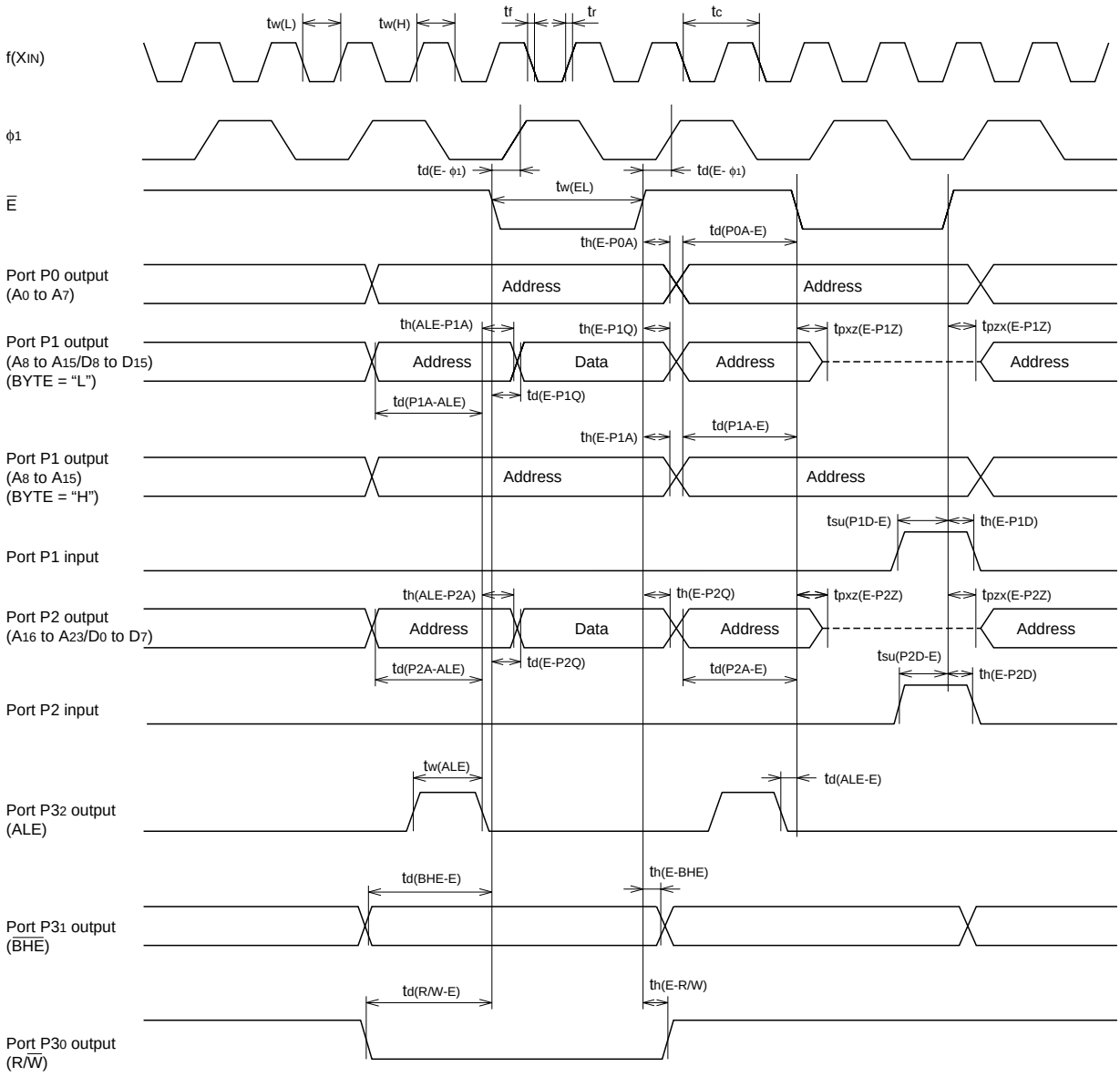


(When wait bit = "1" or "0" in common)



Test conditions
- V_{CC} = 2.7 to 5.5 V
- Input timing voltage : V_{IL} = 0.2 V_{CC}, V_{IH} = 0.8 V_{CC}
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

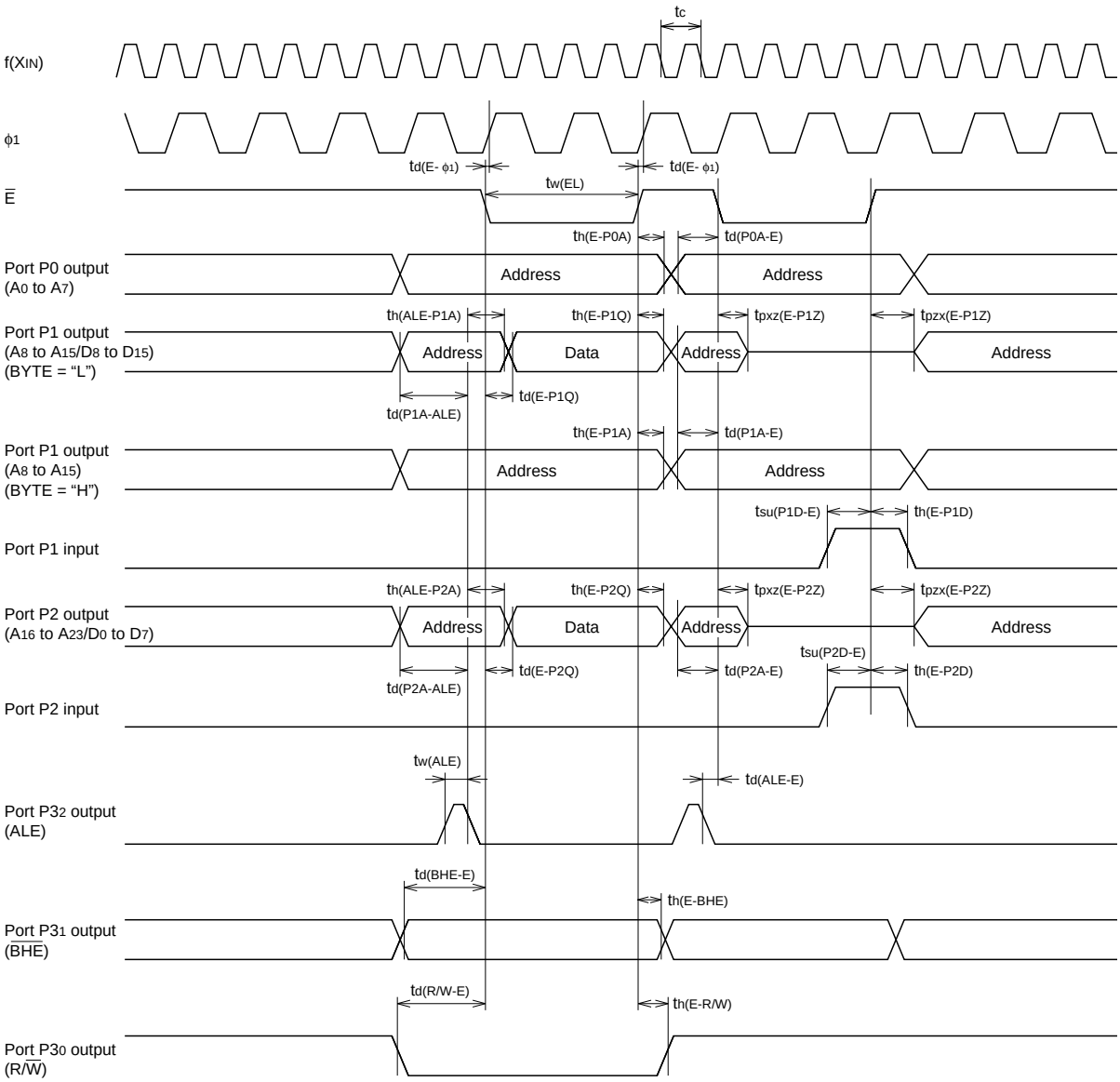
Memory expansion mode and microprocessor mode (When wait bit = “1”)



Test conditions

- V_{CC} = 2.7 to 5.5 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Ports P1, P2 input : V_{IL} = 0.16 V_{CC}, V_{IH} = 0.5 V_{CC}

Memory expansion mode and microprocessor mode (When wait bit = “0”, and external memory area is accessed)



Test conditions

- V_{CC} = 2.7 to 5.5 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Ports P1, P2 input : V_{IL} = 0.16 V_{CC}, V_{IH} = 0.5 V_{CC}

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