

# M37710E4LXXXFP

## PROM VERSION of M37710M4LXXXFP

### DESCRIPTION

The M37710E4LXXXFP is a built-in PROM single-chip microcomputer designed with high-performance CMOS silicon gate technology. This is housed in a small 80-pin plastic molded QFP. The features of this chip are similar to those of the M37710M4BXXXFP except that this chip has a 32K-byte PROM built in.

This single-chip microcomputer has a large 16M bytes address space, three instruction queue buffers, and two data buffers for high-speed instruction execution. The CPU is a 16-bit parallel processor that can also be switched to perform 8-bit parallel processing. This microcomputer is suitable for communication, office, business and industrial equipment controller that require high-speed processing of large data. Since general purpose PROM writers can be used for the built-in PROM, this chip is suitable for small quantity production runs.

### FEATURES

- Number of basic instructions.....103
- Memory size PROM(one time).....32K bytes  
RAM.....1024 bytes
- Instruction execution time  
The fastest instruction at 8MHz frequency.....500ns
- Single low supply voltage.....2.7~5.5V

- Low power dissipation  
(At 3V supply voltage, 8MHz frequency) ... 12mW (Typ.)  
(At 5V supply voltage, 8MHz frequency) ... 30mW (Typ.)
- Wide operating temperature range.....-40~85°C
- Interrupts .....19 types 7 levels
- Multiple function 16-bit timer .....5+3  
(Pulse motor drive waveform can be output)
- UART (may also be synchronous) .....2
- 10-bit A-D converter.....8-channel inputs
- 8-bit D-A converter .....2-channel outputs
- 12-bit watchdog timer
- Programmable input/output  
(ports P0, P1, P2, P3, P4, P5, P6, P7, P8) .....68

### APPLICATION

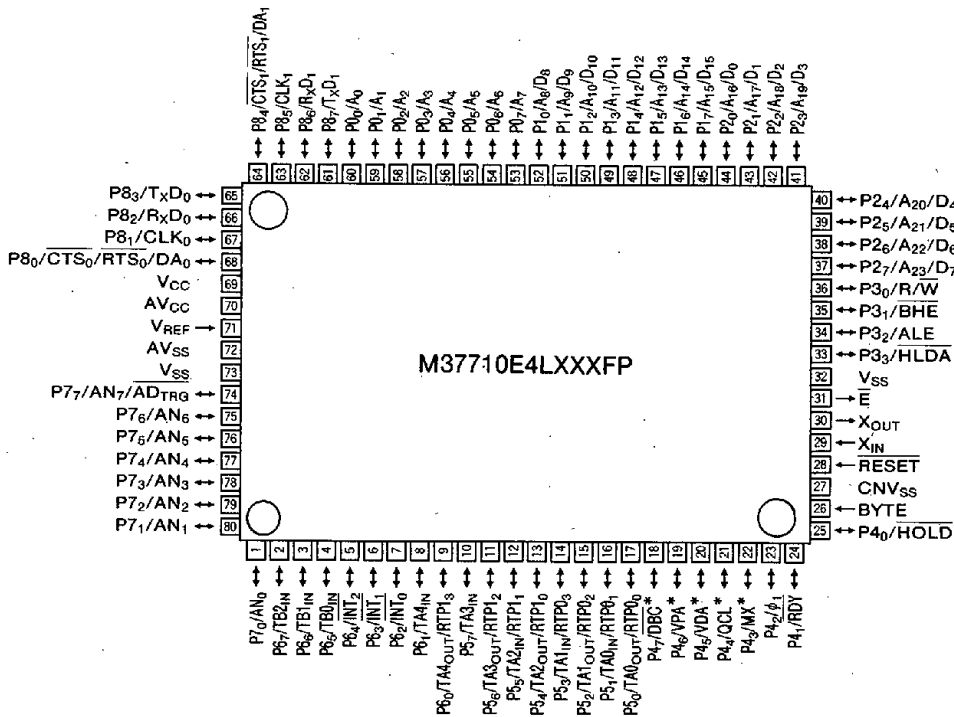
Control devices for office equipment such as copiers, printers, typewriters, facsimiles, word processors, and personal computers

Control devices for industrial equipment such as ME, NC, communication, portable equipment, and measuring instruments

### NOTE

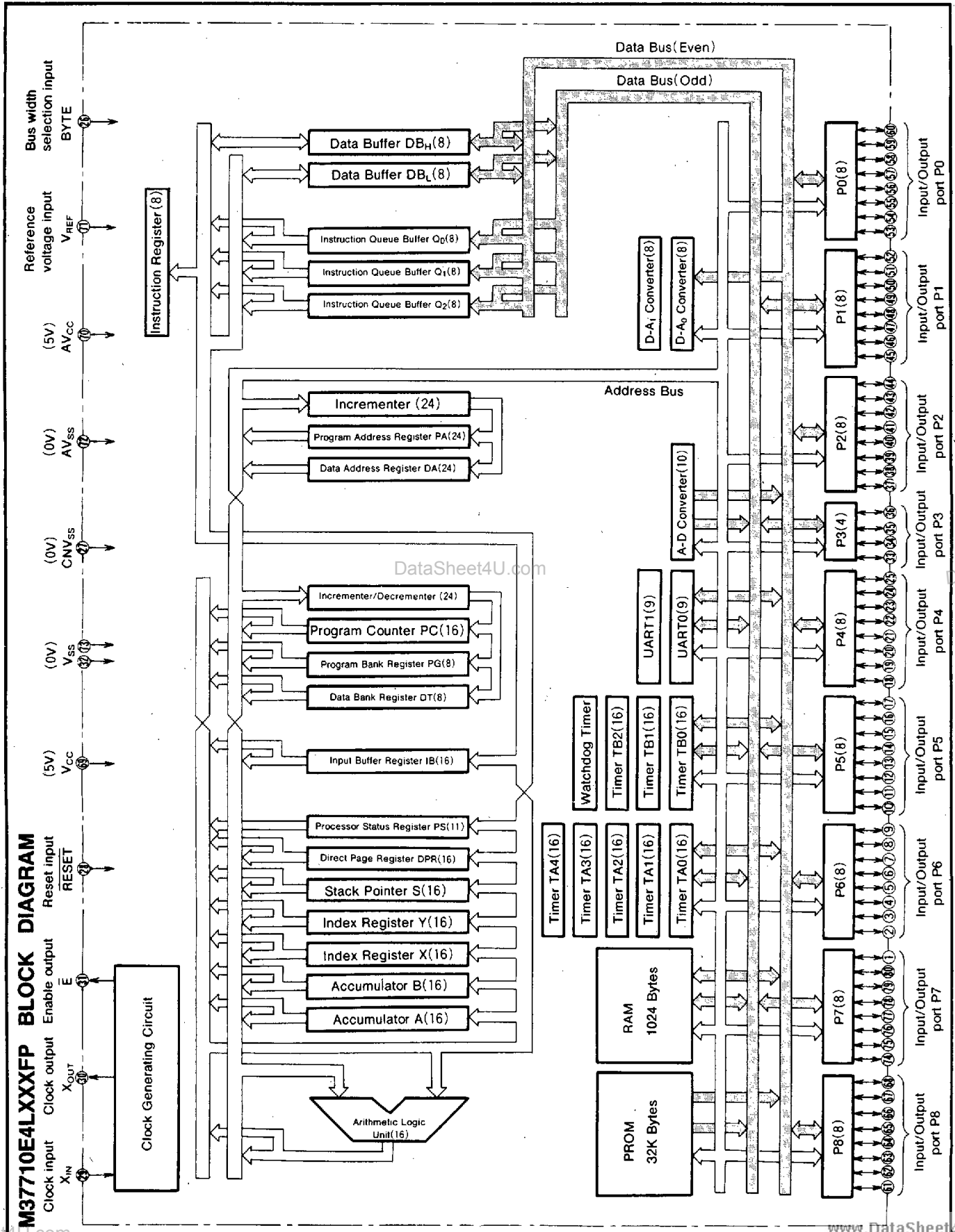
Refer to "Chapter 5 PRECAUTIONS" when using this microcomputer.

### PIN CONFIGURATION (TOP VIEW)



Outline 80P6N-A

\*: Used in the evaluation chip mode only



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**PROM VERSION of M37710M4LXXXFP****FUNCTIONS OF M37710E4LXXXFP**

Parameter		Functions
Number of basic instructions		103
Instruction execution time		500ns (the fastest instruction at external clock 8MHz frequency)
Memory size	PROM	32K bytes
	RAM	1024 bytes
Input/Output ports	P0~P2, P4~P8	8-bitX 8
	P3	4-bitX 1
Multi-function timers	TA0, TA1, TA2, TA3, TA4	16-bitX 5
	TB0, TB1, TB2	16-bitX 3
Serial I/O		(UART or clock synchronous serial I/O)X2
A-D converter		10-bitX 1 (8 channels)
D-A converter		8-bitX 2
Watchdog timer		12-bitX 1
Interrupts		3 external types, 16 internal types (Each interrupt can be set the priority levels to 0~7.)
Clock generating circuit		Built-in(externally connected to a ceramic resonator or quartz crystal resonator)
Supply voltage		2.7~5.5V
Power dissipation		12mW (At 3V supply voltage, external clock 8MHz frequency)
		30mW (At 5V supply voltage, external clock 8MHz frequency)
Input/Output characteristic	Input/Output voltage	5 V
	Output current	5 mA
Memory expansion		Maximum 16M bytes
Operating temperature range		-40~85°C
Device structure		CMOS high-performance silicon gate process
Package		80-pin plastic molded QFP

# MITSUBISHI MICROCOMPUTERS

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### PROM VERSION of M37710M4LXXXFP

#### PIN DESCRIPTION

Pin	Name	Input/Output	Functions
V <sub>CC</sub> , V <sub>SS</sub>	Power supply		Supply 2.7 to 5.5V to V <sub>CC</sub> and 0 V to V <sub>SS</sub> .
CNV <sub>SS</sub>	CNV <sub>SS</sub> input	Input	This pin controls the processor mode. Connect to V <sub>SS</sub> for single-chip mode, and to V <sub>CC</sub> for external ROM types.
$\overline{\text{RESET}}$	Reset input	Input	To enter the reset state, this pin must be kept at a "L" condition which should be maintained for the required time.
X <sub>IN</sub>	Clock input	Input	These are I/O pins of internal clock generating circuit. Connect a ceramic or quartz crystal resonator between X <sub>IN</sub> and X <sub>OUT</sub> . When an external clock is used, the clock source should be connected to the X <sub>IN</sub> pin and the X <sub>OUT</sub> pin should be left open.
X <sub>OUT</sub>	Clock output	Output	
$\overline{\text{E}}$	Enable output	Output	Data or instruction read and data write are performed when output from this pin is "L".
BYTE	Bus width selection input	Input	In memory expansion mode or microprocessor mode, this pin determines whether the external data bus is 8-bit width or 16-bit width. The width is 16 bits when "L" signal inputs and 8 bits when "H" signal inputs.
AV <sub>CC</sub> AV <sub>SS</sub>	Analog supply input		Power supply for the A-D converter. AV <sub>SS</sub> is also used for D-A converter. Connect AV <sub>CC</sub> to V <sub>CC</sub> and AV <sub>SS</sub> to V <sub>SS</sub> externally.
V <sub>REF</sub>	Reference voltage input	Input	This is reference voltage input pin for the A-D converter and the D-A converter.
P0 <sub>0</sub> ~P0 <sub>7</sub>	I/O port P0	I/O	In single-chip mode, port P0 becomes an 8-bit I/O port. An I/O direction register is available so that each pin can be programmed for input or output. These ports are in input mode when reset. Address(A <sub>7</sub> ~A <sub>0</sub> ) is output in memory expansion mode or microprocessor mode.
P1 <sub>0</sub> ~P1 <sub>7</sub>	I/O port P1	I/O	In single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to "L" in memory expansion mode or microprocessor mode and external data bus is 16-bit width, high-order data (D <sub>15</sub> ~D <sub>8</sub> ) is input or output when $\overline{\text{E}}$ output is "L" and an address (A <sub>15</sub> ~A <sub>8</sub> ) is output when $\overline{\text{E}}$ output is "H". If the BYTE pin is "H" that is an external data bus is 8-bit width, only address(A <sub>15</sub> ~A <sub>8</sub> ) is output.
P2 <sub>0</sub> ~P2 <sub>7</sub>	I/O port P2	I/O	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode low-order data(D <sub>7</sub> ~D <sub>0</sub> ) is input or output when $\overline{\text{E}}$ output is "L" and an address(A <sub>23</sub> ~A <sub>16</sub> ) is output when $\overline{\text{E}}$ output is "H".
P3 <sub>0</sub> ~P3 <sub>3</sub>	I/O port P3	I/O	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, R/W, BHE, ALE, and HLDA signals are output.
P4 <sub>0</sub> ~P4 <sub>7</sub>	I/O port P4	I/O	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, P4 <sub>0</sub> and P4 <sub>1</sub> become HOLD and RDY input pin respectively. Functions of other pins are the same as in single-chip mode. In single-chip mode or memory expansion mode, port P4 <sub>2</sub> can be programmed for $\phi_1$ output pin divided the clock to X <sub>IN</sub> pin by 2. In microprocessor mode, P4 <sub>2</sub> always has the function as $\phi_1$ output pin.
P5 <sub>0</sub> ~P5 <sub>7</sub>	I/O port P5	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as I/O pins for timer A0, timer A1, timer A2 and timer A3. P5 <sub>0</sub> ~P5 <sub>6</sub> also function as output pins for pulse motor drive waveform.
P6 <sub>0</sub> ~P6 <sub>7</sub>	I/O port P6	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as I/O pins for timer A4, external interrupt input $\overline{\text{INT}}_0$ , $\overline{\text{INT}}_1$ and $\overline{\text{INT}}_2$ pins, and input pins for timer B0, timer B1 and timer B2. P6 <sub>0</sub> also functions as an output pin for pulse motor drive waveform.
P7 <sub>0</sub> ~P7 <sub>7</sub>	I/O port P7	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as analog input AN <sub>0</sub> ~AN <sub>7</sub> input pins. P7 <sub>7</sub> also has an A-D conversion trigger input function.
P8 <sub>0</sub> ~P8 <sub>7</sub>	I/O port P8	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as RxD, TxD, CLK, CTS/RTS pins for UART 0 and UART 1, and output pins for D-A converter.

# MITSUBISHI MICROCOMPUTERS

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### PROM VERSION of M37710M4LXXXFP

#### PIN DESCRIPTION (EPROM MODE)

Pin	Name	Input/Output	Functions
$V_{CC}, V_{SS}$	Power supply		Supply $5V \pm 10\%$ to $V_{CC}$ and 0V to $V_{SS}$ .
CNV <sub>SS</sub>	V <sub>PP</sub> input	Input	Connect to V <sub>PP</sub> when programming or verifying.
BYTE	V <sub>PP</sub> input	Input	Connect to V <sub>PP</sub> when programming or verifying.
$\overline{RESET}$	Reset input	Input	Connect to $V_{SS}$ .
X <sub>IN</sub>	Clock input	Input	Connect a ceramic resonator between X <sub>IN</sub> and X <sub>OUT</sub> .
X <sub>OUT</sub>	Clock output	Output	
$\overline{E}$	Enable output	Output	Keep open.
AV <sub>CC</sub> , AV <sub>SS</sub>	Analog supply input		Connect AV <sub>CC</sub> to $V_{CC}$ and AV <sub>SS</sub> to $V_{SS}$ .
V <sub>REF</sub>	Reference voltage input	Input	Connect to $V_{SS}$ .
P0 <sub>0</sub> ~P0 <sub>7</sub>	Address input (A <sub>0</sub> ~A <sub>7</sub> )	Input	Port P0 functions as the lower 8 bits address input (A <sub>0</sub> ~A <sub>7</sub> ).
P1 <sub>0</sub> ~P1 <sub>7</sub>	Address input (A <sub>8</sub> ~A <sub>15</sub> )	Input	Port P1 <sub>0</sub> ~P1 <sub>7</sub> functions as the higher 8 bits address input (A <sub>8</sub> ~A <sub>15</sub> ). In 256K mode, connect P1 <sub>7</sub> to $V_{CC}$ .
P2 <sub>0</sub> ~P2 <sub>7</sub>	Data I/O (D <sub>0</sub> ~D <sub>7</sub> )	I/O	Port P2 functions as the 8 bits data bus (D <sub>0</sub> ~D <sub>7</sub> ).
P3 <sub>0</sub> ~P3 <sub>3</sub>	Input port P3	Input	Connect to $V_{SS}$ .
P4 <sub>0</sub> ~P4 <sub>7</sub>	Input port P4	Input	Connect to $V_{SS}$ .
P5 <sub>0</sub> ~P5 <sub>7</sub>	Control signal input	Input	P5 <sub>0</sub> *, P5 <sub>1</sub> and P5 <sub>2</sub> functions as $\overline{PGM}$ *, $\overline{OE}$ and $\overline{CE}$ input pin* respectively. Connect P5 <sub>3</sub> , P5 <sub>4</sub> and P5 <sub>5</sub> to $V_{CC}$ . Connect P5 <sub>6</sub> to $V_{SS}$ in 256K mode and to $V_{CC}$ in 1M mode. Connect P5 <sub>7</sub> to $V_{SS}$ .
P6 <sub>0</sub> ~P6 <sub>7</sub>	Input port P6	Input	Connect to $V_{SS}$ .
P7 <sub>0</sub> ~P7 <sub>7</sub>	Input port P7	Input	Connect to $V_{SS}$ .
P8 <sub>0</sub> ~P8 <sub>7</sub>	Input port P8	Input	Connect to $V_{SS}$ .

\* : It is available in 1M mode.

## BASIC FUNCTION BLOCKS

The M37710E4LXXXFP has the same functions as the M37710M4BXXXFP except for the following:

- (1) The external ROM is PROM.
- (2) The reset circuit is different.

Therefore, refer to the section on the M37710M4BXXXFP.

## MEMORY

The memory map is shown in Figure 1.

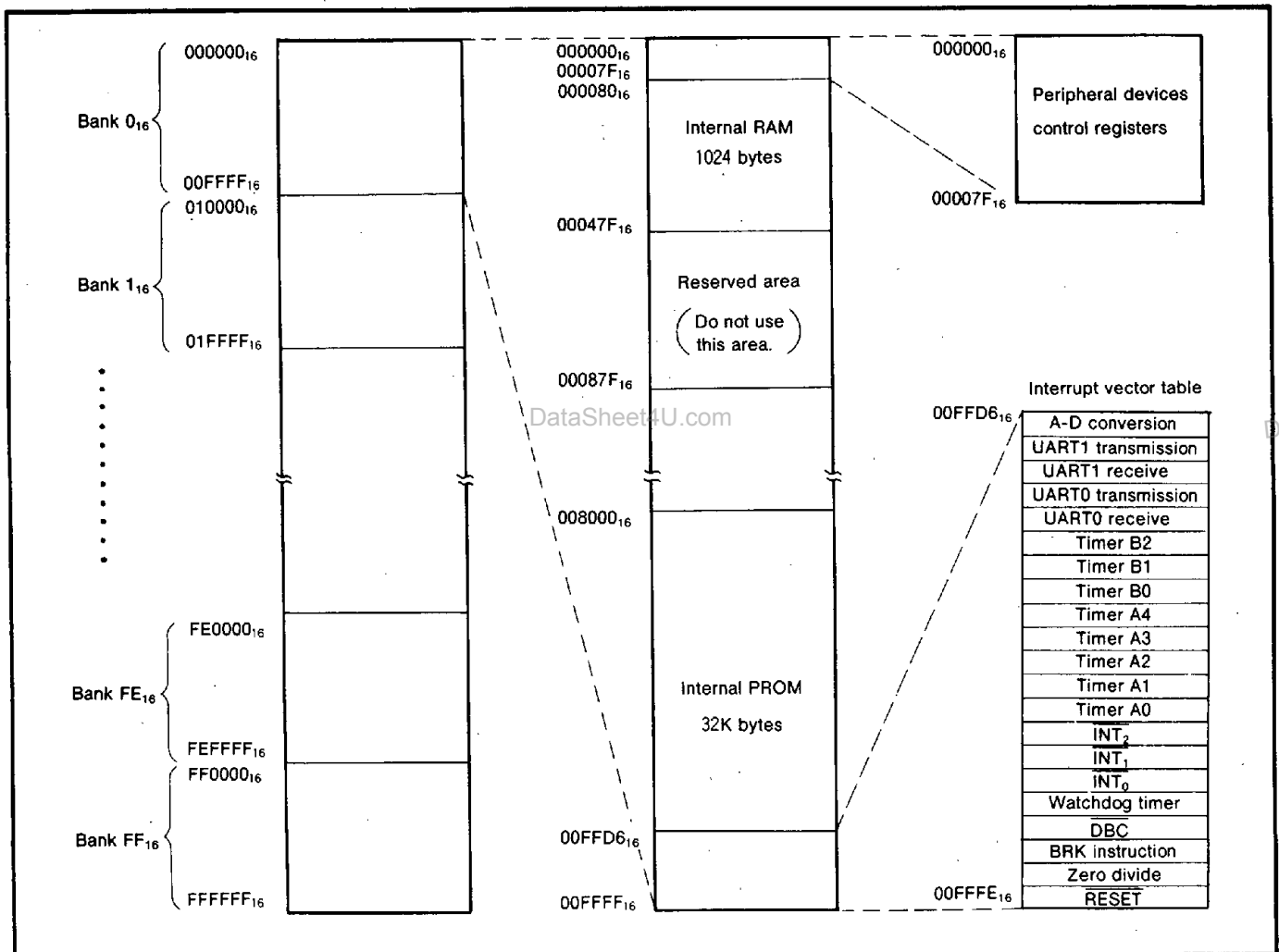


Fig. 1 Memory map

**RESET CIRCUIT**

Reset occurs when the RESET pin is returned to "H" level after holding it at "L" level when the power voltage is at 2.7 to 5.5V. Program execution starts at the address formed by setting the address pins A<sub>23</sub>~A<sub>16</sub> to 00<sub>16</sub>, A<sub>15</sub>~A<sub>8</sub> to the contents of address FFF<sub>16</sub>, and A<sub>7</sub>~A<sub>0</sub> to the contents of address FFE<sub>16</sub>.

Figure 2 shows the status of the internal registers when a reset occurs.

Figure 3 shows an example of a reset circuit. The reset input voltage must be held 0.55V or lower when the power voltage reaches 2.7V.

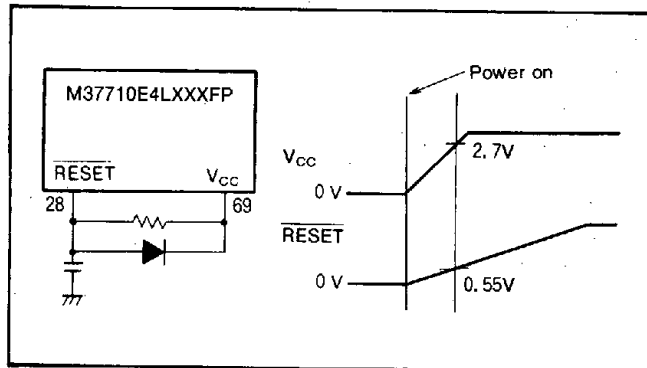


Fig. 3 Example of a reset circuit (perform careful evaluation at the system design level before using)

	Address	Contents		Address	Contents
(1) Port P0 data direction register	(04 <sub>16</sub> )...	00 <sub>16</sub>	(29) Processor mode register 0	(5E <sub>16</sub> )...	00 <sub>16</sub>
(2) Port P1 data direction register	(05 <sub>16</sub> )...	00 <sub>16</sub>	(30) Processor mode register 1	(5F <sub>16</sub> )...	XXXXXXXXXX0
(3) Port P2 data direction register	(08 <sub>16</sub> )...	00 <sub>16</sub>	(31) Watchdog timer	(60 <sub>16</sub> )...	FFF <sub>16</sub>
(4) Port P3 data direction register	(09 <sub>16</sub> )...	XXXXXXXXXX0000	(32) Watchdog timer frequency selection flag	(61 <sub>16</sub> )...	XXXXXXXXXX0
(5) Port P4 data direction register	(0C <sub>16</sub> )...	00 <sub>16</sub>	(33) Waveform output mode register	(62 <sub>16</sub> )...	00 <sub>16</sub>
(6) Port P5 data direction register	(0D <sub>16</sub> )...	00 <sub>16</sub>	(34) Reserved area (Do not write to this address)	(66 <sub>16</sub> )...	00 <sub>16</sub>
(7) Port P6 data direction register	(10 <sub>16</sub> )...	00 <sub>16</sub>	(35) A-D conversion interrupt control register	(70 <sub>16</sub> )...	XXXXXXXXXX0000
(8) Port P7 data direction register	(11 <sub>16</sub> )...	00 <sub>16</sub>	(36) UART 0 transmission interrupt control register	(71 <sub>16</sub> )...	XXXXXXXXXX0000
(9) Port P8 data direction register	(14 <sub>16</sub> )...	00 <sub>16</sub>	(37) UART 0 receive interrupt control register	(72 <sub>16</sub> )...	XXXXXXXXXX0000
(10) A-D control register 0	(1E <sub>16</sub> )...	000000???	(38) UART 1 transmission interrupt control register	(73 <sub>16</sub> )...	XXXXXXXXXX0000
(11) A-D control register 1	(1F <sub>16</sub> )...	00XXXX00011	(39) UART 1 receive interrupt control register	(74 <sub>16</sub> )...	XXXXXXXXXX0000
(12) UART 0 Transmit/Receive mode register	(30 <sub>16</sub> )...	00 <sub>16</sub>	(40) Timer A0 interrupt control register	(75 <sub>16</sub> )...	XXXXXXXXXX0000
(13) UART 1 Transmit/Receive mode register	(38 <sub>16</sub> )...	00 <sub>16</sub>	(41) Timer A1 interrupt control register	(76 <sub>16</sub> )...	XXXXXXXXXX0000
(14) UART 0 Transmit/Receive control register 0	(34 <sub>16</sub> )...	XXXXXXXXXX01000	(42) Timer A2 interrupt control register	(77 <sub>16</sub> )...	XXXXXXXXXX0000
(15) UART 1 Transmit/Receive control register 0	(3C <sub>16</sub> )...	XXXXXXXXXX01000	(43) Timer A3 interrupt control register	(78 <sub>16</sub> )...	XXXXXXXXXX0000
(16) UART 0 Transmit/Receive control register 1	(35 <sub>16</sub> )...	0000000010	(44) Timer A4 interrupt control register	(79 <sub>16</sub> )...	XXXXXXXXXX0000
(17) UART 1 Transmit/Receive control register 1	(3D <sub>16</sub> )...	0000000010	(45) Timer B0 interrupt control register	(7A <sub>16</sub> )...	XXXXXXXXXX0000
(18) Count start flag	(40 <sub>16</sub> )...	00 <sub>16</sub>	(46) Timer B1 interrupt control register	(7B <sub>16</sub> )...	XXXXXXXXXX0000
(19) One-shot start flag	(42 <sub>16</sub> )...	XXXXXXXXXX00000	(47) Timer B2 interrupt control register	(7C <sub>16</sub> )...	XXXXXXXXXX0000
(20) Up-down flag	(44 <sub>16</sub> )...	00 <sub>16</sub>	(48) INT <sub>0</sub> interrupt control register	(7D <sub>16</sub> )...	XXXX0000000
(21) Timer A0 mode register	(56 <sub>16</sub> )...	00 <sub>16</sub>	(49) INT <sub>1</sub> interrupt control register	(7E <sub>16</sub> )...	XXXX0000000
(22) Timer A1 mode register	(57 <sub>16</sub> )...	00 <sub>16</sub>	(50) INT <sub>2</sub> interrupt control register	(7F <sub>16</sub> )...	XXXX0000000
(23) Timer A2 mode register	(58 <sub>16</sub> )...	00 <sub>16</sub>	(51) Processor status register PS		0000??00001??
(24) Timer A3 mode register	(59 <sub>16</sub> )...	00 <sub>16</sub>	(52) Program bank register PG		00 <sub>16</sub>
(25) Timer A4 mode register	(5A <sub>16</sub> )...	00 <sub>16</sub>	(53) Program counter PC <sub>H</sub>		Content of FFF <sub>16</sub>
(26) Timer B0 mode register	(5B <sub>16</sub> )...	0001000000	(54) Program counter PC <sub>L</sub>		Content of FFE <sub>16</sub>
(27) Timer B1 mode register	(5C <sub>16</sub> )...	0001XXXX0000	(55) Direct page register DPR		0000 <sub>16</sub>
(28) Timer B2 mode register	(5D <sub>16</sub> )...	0001XXXX0000	(56) Data bank register DT		00 <sub>16</sub>

Contents of other registers and RAM are not initialized and should be initialized by software.

Fig. 2 Microcomputer internal status during reset

# M37710E4LXXXFP

## PROM VERSION of M37710M4LXXXFP

### EPROM MODE

The M37710E4LXXXFP features an EPROM mode in addition to its normal modes. When the RESET signal level is "L", the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 4 shows the pin connections in the EPROM mode.

There are two EPROM modes. One is the 256K mode for the EPROM that is equivalent to the M5M27C256K, and the other is the 1M mode for the EPROM that is equivalent to the M5M27C101K. 256K mode is selected when port P5<sub>6</sub> is set to "L" level, and 1M mode is selected when it is set to "H" level.

When in the EPROM mode, ports P0, P1, P2, P5<sub>0</sub>, P5<sub>1</sub>, P5<sub>2</sub>, CNV<sub>SS</sub> and BYTE are used for the EPROM (equivalent to the M5M27C256K or M5M27C101K). When in this mode,

the built-in PROM can be written to or read from using these pins in the same way as with the M5M27C256K or M5M27C101K.

This chip does not have Device Identifier Mode, so that set the corresponding program algorithm. The program area should specify address 0000<sub>16</sub>~7FFF<sub>16</sub> in 256K mode, and address 18000<sub>16</sub>~1FFFF<sub>16</sub> in 1M mode.

Connect the clock which is either ceramic resonator or external clock to X<sub>IN</sub> pin and X<sub>OUT</sub> pin.

For one time PROM version, 256K mode should be recommended to write more deeply.

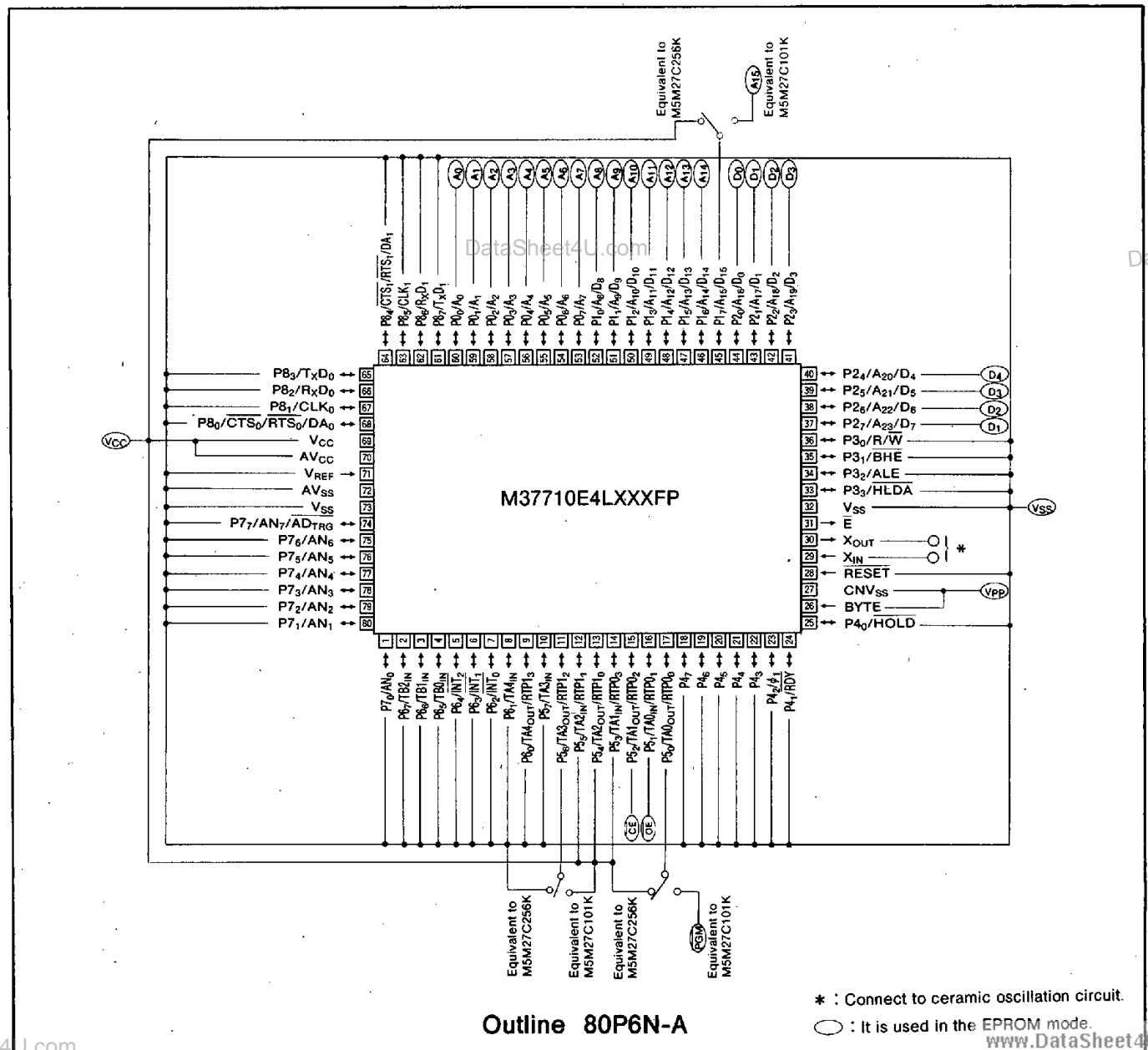


Fig. 4 Pin connection in EPROM mode



**MITSUBISHI MICROCOMPUTERS**  
**M37710E4LXXXFP**

**PROM VERSION of M37710M4LXXXFP**

**Table 1. Pin function in EPROM mode**

	M37710E4LXXXFP	M5M27C256K	M5M27C101K
$V_{CC}$	$V_{CC}$	$V_{CC}$	
$V_{PP}$	CNV <sub>SS</sub> , BYTE	$V_{PP}$	
$V_{SS}$	$V_{SS}$	$V_{SS}$	
Address input	Ports P0, P1 *	A <sub>0</sub> ~A <sub>14</sub>	A <sub>0</sub> ~A <sub>15</sub>
Data I/O	Port P2	D <sub>0</sub> ~D <sub>7</sub>	
$\overline{CE}$	P5 <sub>2</sub>	$\overline{CE}$	
$\overline{OE}$	P5 <sub>1</sub>	$\overline{OE}$	
$\overline{PGM}$	P5 <sub>0</sub> *	—	$\overline{PGM}$

\* : In 256K mode, connect P1<sub>7</sub> and P5<sub>0</sub> to  $V_{CC}$ .

# MITSUBISHI MICROCOMPUTERS

## M37710E4LXXXFP

### PROM VERSION of M37710M4LXXXFP

#### FUNCTION IN EPROM MODE

##### (1) 1M mode (equivalent to the M5M27C101K)

#### Reading

To read the EPROM, set the  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  pins to a "L" level. Input the address of the data ( $A_0 \sim A_{15}$ ) to be read, and the data will be output to the I/O pins  $D_0 \sim D_7$ . The data I/O pins will be floating when either the  $\overline{\text{CE}}$  or  $\overline{\text{OE}}$  pins are in the "H" state.

#### Writing

Writing must be performed in 8 bits by a byte program. To write to the EPROM, set the  $\overline{\text{CE}}$  pin to a "L" level and the  $\overline{\text{OE}}$  pin to a "H" level. The CPU will enter the program mode when 12.5V is applied to the  $V_{PP}$  pin. The address to be written to is selected with pins  $A_0 \sim A_{15}$ , and the data to be written is input to pins  $D_0 \sim D_7$ . Set the  $\overline{\text{PGM}}$  pin to a "L" level to being writing.

#### Writing operation

To program the M37710E4LXXXFP, first set  $V_{CC}=6V$ ,  $V_{PP}=12.5V$ , and set the address to  $18000_{16}$ . Apply a 0.2ms write pulse, check that the data can be read, and if it cannot be read OK, repeat the procedure, applying a 0.2ms write pulse and checking that the data can be read until it can be read OK. Record the accumulated number of pulse applied (X) before the data can be read OK, and then write the data again, applying a further once this number of pulses ( $0.2 \times X$  ms).

When this series of write operations is complete, increment the address, and continue to repeat the procedure above until the last address has been reached.

Finally, when all addresses have been written, read with  $V_{CC}=V_{PP}=5V$  (or  $V_{CC}=V_{PP}=5.5V$ ).

Table 2. I/O signal in each mode

Mode \ Pin	$\overline{\text{CE}}$	$\overline{\text{OE}}$	$\overline{\text{PGM}}$	$V_{PP}$	$V_{CC}$	Data I/O
Read-out	$V_{IL}$	$V_{IL}$	X	5 V	5 V	Output
Output	$V_{IL}$	$V_{IH}$	X	5 V	5 V	Floating
Disable	$V_{IH}$	X	X	5 V	5 V	Floating
Programming	$V_{IL}$	$V_{IH}$	$V_{IL}$	12.5V	6 V	Input
Programming Verify	$V_{IL}$	$V_{IL}$	$V_{IH}$	12.5V	6 V	Output
Program Disable	$V_{IH}$	$V_{IH}$	$V_{IH}$	12.5V	6 V	Floating

Note. An X indicates either  $V_{IL}$  or  $V_{IH}$ .

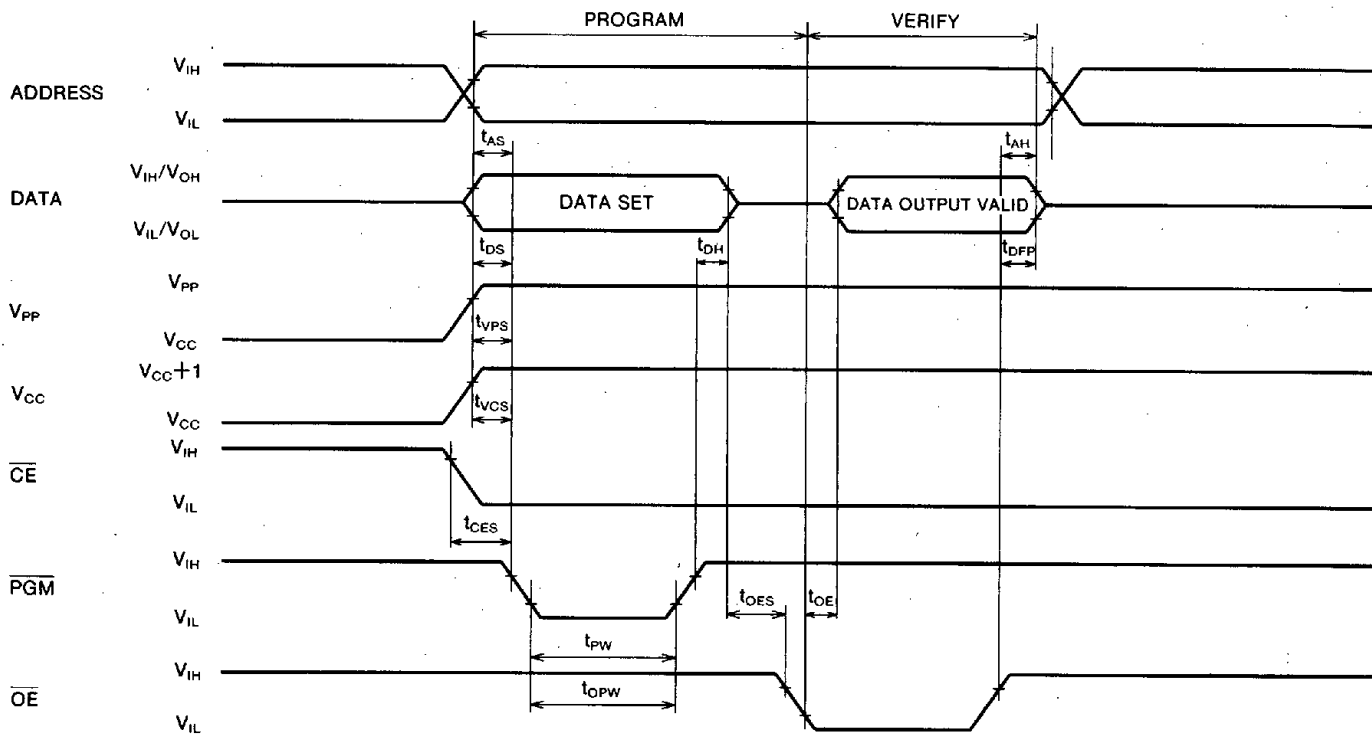
#### Program operation (equivalent to the M5M27C101K)

AC ELECTRICAL CHARACTERISTICS ( $T_a=25 \pm 5^\circ\text{C}$ ,  $V_{CC}=6V \pm 0.25V$ ,  $V_{PP}=12.5 \pm 0.3V$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{AS}$	Address setup time		2			$\mu\text{s}$
$t_{OES}$	$\overline{\text{OE}}$ setup time		2			$\mu\text{s}$
$t_{DS}$	Data setup time		2			$\mu\text{s}$
$t_{AH}$	Address hold time		0			$\mu\text{s}$
$t_{DH}$	Data hold time		2			$\mu\text{s}$
$t_{DFP}$	Output enable to output float delay		0		130	ns
$t_{VCS}$	$V_{CC}$ setup time		2			$\mu\text{s}$
$t_{VPS}$	$V_{PP}$ setup time		2			$\mu\text{s}$
$t_{PW}$	$\overline{\text{PGM}}$ pulse width		0.19	0.2	0.21	ms
$t_{OPW}$	$\overline{\text{PGM}}$ over program pulse width		0.19		5.25	ms
$t_{CES}$	$\overline{\text{CE}}$ setup time		2			$\mu\text{s}$
$t_{OE}$	Data valid from $\overline{\text{OE}}$				150	ns

PROM VERSION of M37710M4LXXFP

AC waveforms



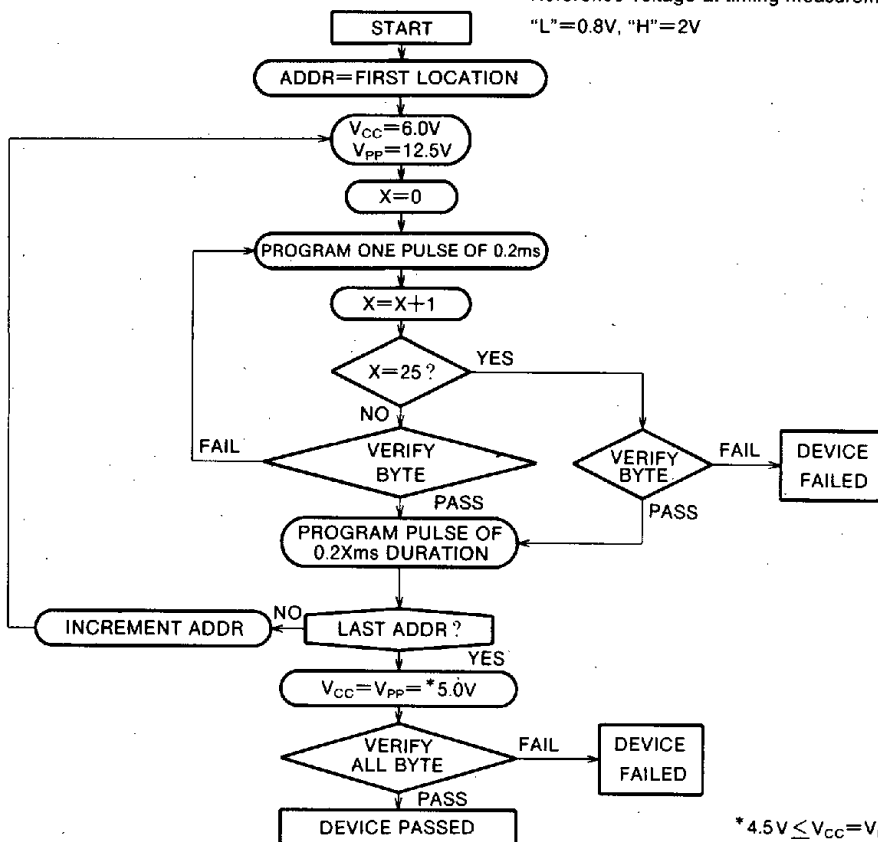
Test conditions for A.C. characteristics

Input voltage :  $V_{IL}=0.45V$ ,  $V_{IH}=2.4V$

Input rise and fall times (10%~90%) :  $\leq 20ns$

Reference voltage at timing measurement : Input, Output  
"L"=0.8V, "H"=2V

Programming algorithm flow chart



\*  $4.5V \leq V_{CC}=V_{PP} \leq 5.5V$

## M37710E4LXXXFP

## PROM VERSION of M37710M4LXXXFP

## (2) 256K mode (equivalent to the M5M27C256K)

## Reading

To read the EPROM, set the  $\overline{CE}$  and  $\overline{OE}$  pins to a "L" level. Input the address of the data ( $A_0 \sim A_{14}$ ) to be read, and the data will be output to the I/O pins  $D_0 \sim D_7$ . The data I/O pins will be floating when either the  $\overline{CE}$  or  $\overline{OE}$  pins are in the "H" state.

## Writing

To write to the EPROM, set the  $\overline{OE}$  pin to a "H" level. The CPU will enter the program mode when  $V_{PP}$  is applied to the  $V_{PP}$  pin. The address to be written to is selected with pins  $A_0 \sim A_{14}$ , and the data to be written is input to pins  $D_0 \sim D_7$ . Set the  $\overline{CE}$  pin to a "L" level to being writing.

## Writing operation

To program the M37710E4LXXXFP, first set  $V_{CC}=6V$ ,  $V_{PP}=12.5V$ , and set the address to "0". Apply a 1ms write pulse, check that the data can be read, and if it cannot be read OK, repeat the procedure, applying a 1ms write pulse and checking that the data can be read until it can be read OK. Record the accumulated number of pulse applied (X) before the data can be read OK, and then write the data again, applying a further three times this number of pulses ( $3 \times X$  ms).

When this series of write operations is complete, increment the address, and continue to repeat the procedure above until the last address has been reached.

Finally, when all addresses have been written, read with  $V_{CC}=V_{PP}=5V$  (or  $V_{CC}=V_{PP}=5.5V$ ).

Table 3. I/O signal in each mode

Mode	Pin				
	$\overline{CE}$	$\overline{OE}$	$V_{PP}$	$V_{CC}$	Data I/O
Read-out	$V_{IL}$	$V_{IL}$	5 V	5 V	Output
Output	$V_{IL}$	$V_{IH}$	5 V	5 V	Floating
Disable	$V_{IH}$	X	5 V	5 V	Floating
Programming	$V_{IL}$	$V_{IH}$	12.5V	6 V	Input
Programming Verify	$V_{IH}$	$V_{IL}$	12.5V	6 V	Output
Program Disable	$V_{IH}$	$V_{IH}$	12.5V	6 V	Floating

Note. An X indicates either  $V_{IL}$  or  $V_{IH}$ .

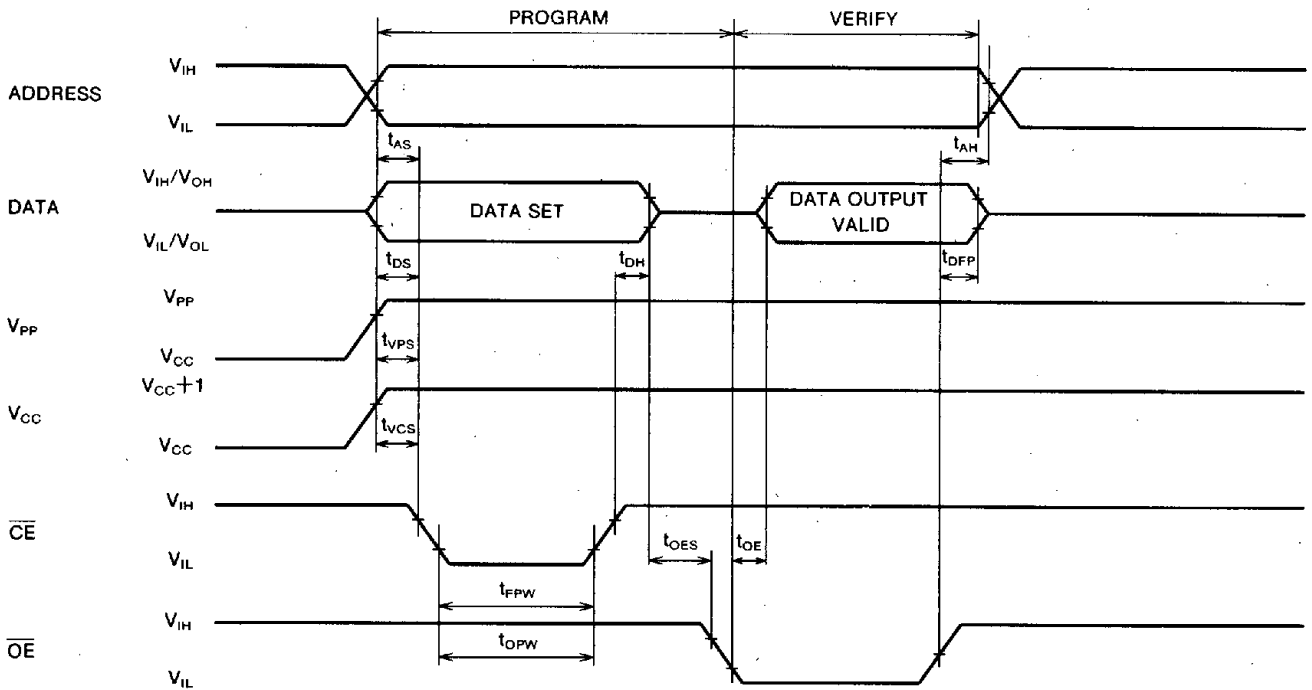
## Program operation (equivalent to the M5M27C256K)

AC ELECTRICAL CHARACTERISTICS ( $T_a=25 \pm 5^\circ C$ ,  $V_{CC}=6V \pm 0.25V$ ,  $V_{PP}=12.5 \pm 0.3V$ , unless otherwise noted)

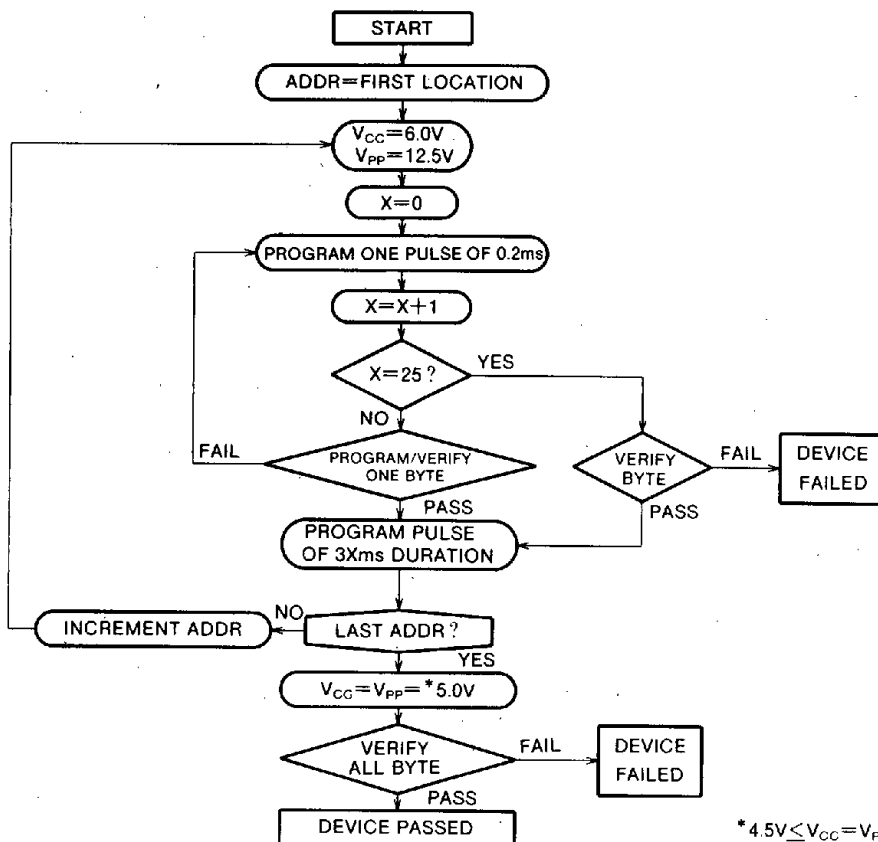
Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{AS}$	Address setup time		2			$\mu s$
$t_{OES}$	$\overline{OE}$ setup time		2			$\mu s$
$t_{DS}$	Data setup time		2			$\mu s$
$t_{AH}$	Address hold time		0			$\mu s$
$t_{DH}$	Data hold time		2			$\mu s$
$t_{DFP}$	Output enable to output float delay		0		130	ns
$t_{VCS}$	$V_{CC}$ setup time		2			$\mu s$
$t_{VPS}$	$V_{PP}$ setup time		2			$\mu s$
$t_{FPW}$	$\overline{CE}$ initial program pulse width		0.95	1	1.05	ms
$t_{OPW}$	$\overline{CE}$ over program pulse width		2.85		78.75	ms
$t_{OE}$	Data valid from $\overline{OE}$				150	ns

PROM VERSION of M37710M4LXXXFP

AC waveforms



Programming algorithm flow chart

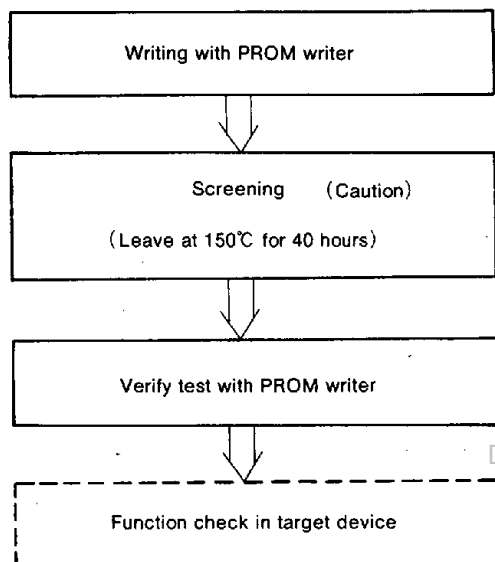


\*  $4.5V \leq V_{CC} = V_{PP} \leq 5.5V$

**PROM VERSION of M37710M4LXXXFP**
**SAFETY INSTRUCTIONS**

- (1) A high voltage is used for writing. Take care that over-voltage is not applied. Take care especially at power on.
- (2) The programmable M37710E4LFP that are shipped in blank is also provided.

For the M37710E4LFP, Mitsubishi Electric corp. does not perform PROM write test and screening following the assembly processes. To improve reliability after write, performing write and test according to the flow below before use is recommended.



Caution : Never expose to 150 °C exceeding 100 hours because the screening temperature is higher than the storage temperature.

**ADDRESSING MODES**

The M37710E4LXXXFP has 28 powerful addressing modes. Refer to the 7700 Family addressing mode description for the details of each addressing mode.

**MACHINE INSTRUCTION LIST**

The M37710E4LXXXFP has 103 machine instructions. Refer to the 7700 Family machine instruction list for details.

**DATA REQUIRED FOR PROM ORDERING**

Please send the following data for writing to PROM.

- (1) M37710E4LXXXFP writing to PROM order confirmation form
- (2) 80P6N mark specification form
- (3) ROM data (EPROM 3 sets)

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC}$	Supply voltage		-0.3~7	V
$AV_{CC}$	Analog supply voltage		-0.3~7	V
$V_I$	Input voltage RESET, CNV <sub>SS</sub> , BYTE		-0.3~12 (Note 1)	V
$V_I$	Input voltage P0 <sub>0</sub> ~P0 <sub>7</sub> , P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> , P3 <sub>0</sub> ~P3 <sub>3</sub> , P4 <sub>0</sub> ~P4 <sub>7</sub> , P5 <sub>0</sub> ~P5 <sub>7</sub> , P6 <sub>0</sub> ~P6 <sub>7</sub> , P7 <sub>0</sub> ~P7 <sub>7</sub> , P8 <sub>0</sub> ~P8 <sub>7</sub> , V <sub>REF</sub> , X <sub>IN</sub>		-0.3~ $V_{CC}+0.3$	V
$V_O$	Output voltage P0 <sub>0</sub> ~P0 <sub>7</sub> , P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> , P3 <sub>0</sub> ~P3 <sub>3</sub> , P4 <sub>0</sub> ~P4 <sub>7</sub> , P5 <sub>0</sub> ~P5 <sub>7</sub> , P6 <sub>0</sub> ~P6 <sub>7</sub> , P7 <sub>0</sub> ~P7 <sub>7</sub> , P8 <sub>0</sub> ~P8 <sub>7</sub> , X <sub>OUT</sub> , $\bar{E}$		-0.3~ $V_{CC}+0.3$	V
$P_d$	Power dissipation	T <sub>a</sub> =25°C	300	mW
T <sub>opr</sub>	Operating temperature		-40~85	°C
T <sub>stg</sub>	Storage temperature		-65~150	°C

Note 1. Input voltage for CNV<sub>SS</sub> and BYTE pins is 13V in writing to PROM.

RECOMMENDED OPERATING CONDITIONS (V<sub>CC</sub>=2.7~5.5V, T<sub>a</sub>=-40~85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$V_{CC}$	Supply voltage	2.7		5.5	V
$AV_{CC}$	Analog supply voltage		$V_{CC}$		V
$V_{SS}$	Supply voltage		0		V
$AV_{SS}$	Analog supply voltage		0		V
$V_{IH}$	High-level input voltage P0 <sub>0</sub> ~P0 <sub>7</sub> , P3 <sub>0</sub> ~P3 <sub>3</sub> , P4 <sub>0</sub> ~P4 <sub>7</sub> , P5 <sub>0</sub> ~P5 <sub>7</sub> , P6 <sub>0</sub> ~P6 <sub>7</sub> , P7 <sub>0</sub> ~P7 <sub>7</sub> , P8 <sub>0</sub> ~P8 <sub>7</sub> , X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , BYTE	0.8V <sub>CC</sub>		$V_{CC}$	V
$V_{IH}$	High-level input voltage P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> (in single-chip mode)	0.8V <sub>CC</sub>		$V_{CC}$	V
$V_{IH}$	High-level input voltage P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> (in memory expansion mode and microprocessor mode)	0.5V <sub>CC</sub>		$V_{CC}$	V
$V_{IL}$	Low-level input voltage P0 <sub>0</sub> ~P0 <sub>7</sub> , P3 <sub>0</sub> ~P3 <sub>3</sub> , P4 <sub>0</sub> ~P4 <sub>7</sub> , P5 <sub>0</sub> ~P5 <sub>7</sub> , P6 <sub>0</sub> ~P6 <sub>7</sub> , P7 <sub>0</sub> ~P7 <sub>7</sub> , P8 <sub>0</sub> ~P8 <sub>7</sub> , X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , BYTE	0		0.2V <sub>CC</sub>	V
$V_{IL}$	Low-level input voltage P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> (in single-chip mode)	0		0.2V <sub>CC</sub>	V
$V_{IL}$	Low-level input voltage P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> (in memory expansion mode and microprocessor mode)	0		0.16V <sub>CC</sub>	V
$I_{OH(peak)}$	High-level peak output current P0 <sub>0</sub> ~P0 <sub>7</sub> , P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> , P3 <sub>0</sub> ~P3 <sub>3</sub> , P4 <sub>0</sub> ~P4 <sub>7</sub> , P5 <sub>0</sub> ~P5 <sub>7</sub> , P6 <sub>0</sub> ~P6 <sub>7</sub> , P7 <sub>0</sub> ~P7 <sub>7</sub> , P8 <sub>0</sub> ~P8 <sub>7</sub>			-10	mA
$I_{OH(avg)}$	High-level average output current P0 <sub>0</sub> ~P0 <sub>7</sub> , P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> , P3 <sub>0</sub> ~P3 <sub>3</sub> , P4 <sub>0</sub> ~P4 <sub>7</sub> , P5 <sub>0</sub> ~P5 <sub>7</sub> , P6 <sub>0</sub> ~P6 <sub>7</sub> , P7 <sub>0</sub> ~P7 <sub>7</sub> , P8 <sub>0</sub> ~P8 <sub>7</sub>			-5	mA
$I_{OL(peak)}$	Low-level peak output current P0 <sub>0</sub> ~P0 <sub>7</sub> , P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> , P3 <sub>0</sub> ~P3 <sub>3</sub> , P4 <sub>0</sub> ~P4 <sub>7</sub> , P5 <sub>0</sub> ~P5 <sub>7</sub> , P6 <sub>0</sub> ~P6 <sub>7</sub> , P7 <sub>0</sub> ~P7 <sub>7</sub> , P8 <sub>0</sub> ~P8 <sub>7</sub>			10	mA
$I_{OL(avg)}$	Low-level average output current P0 <sub>0</sub> ~P0 <sub>7</sub> , P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> , P3 <sub>0</sub> ~P3 <sub>3</sub> , P4 <sub>0</sub> ~P4 <sub>7</sub> , P5 <sub>0</sub> ~P5 <sub>7</sub> , P6 <sub>0</sub> ~P6 <sub>7</sub> , P7 <sub>0</sub> ~P7 <sub>7</sub> , P8 <sub>0</sub> ~P8 <sub>7</sub>			5	mA
f(X <sub>IN</sub> )	External clock frequency input			8	MHz

Notes 2. Average output current is the average value of a 100ms interval.

3. The sum of  $I_{OL(peak)}$  for ports P0, P1, P2, P3, and P8 must be 80mA or less, the sum of  $I_{OH(peak)}$  for ports P0, P1, P2, P3, and P8 must be 80mA or less, the sum of  $I_{OL(peak)}$  for ports P4, P5, P6, and P7 must be 80mA or less, and the sum of  $I_{OH(peak)}$  for ports P4, P5, P6, and P7 must be 80mA or less.

**ELECTRICAL CHARACTERISTICS** ( $V_{CC}=5V$ ,  $V_{SS}=0V$ ,  $T_a=25^\circ C$ ,  $f(X_{IN})=8MHz$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit		
			Min.	Typ.	Max.			
$V_{OH}$	High-level output voltage P0 <sub>0</sub> ~P0 <sub>7</sub> , P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> , P3 <sub>0</sub> , P3 <sub>1</sub> , P3 <sub>3</sub> , P4 <sub>0</sub> ~P4 <sub>7</sub> , P5 <sub>0</sub> ~P5 <sub>7</sub> , P6 <sub>0</sub> ~P6 <sub>7</sub> , P7 <sub>0</sub> ~P7 <sub>7</sub> , P8 <sub>0</sub> ~P8 <sub>7</sub>	$V_{CC}=5V$ , $I_{OH}=-10mA$	3			V		
		$V_{CC}=3V$ , $I_{OH}=-1mA$	2.5					
$V_{OH}$	High-level output voltage P0 <sub>0</sub> ~P0 <sub>7</sub> , P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> , P3 <sub>0</sub> , P3 <sub>1</sub> , P3 <sub>3</sub>	$V_{CC}=5V$ , $I_{OH}=-400\mu A$	4.7			V		
$V_{OH}$	High-level output voltage P3 <sub>2</sub>	$V_{CC}=5V$ , $I_{OH}=-10mA$	3.1			V		
		$V_{CC}=5V$ , $I_{OH}=-400\mu A$	4.8					
		$V_{CC}=3V$ , $I_{OH}=-1mA$	2.6					
$V_{OH}$	High-level output voltage $\bar{E}$	$V_{CC}=5V$ , $I_{OH}=-10mA$	3.4			V		
		$V_{CC}=5V$ , $I_{OH}=-400\mu A$	4.8					
		$V_{CC}=3V$ , $I_{OH}=-1mA$	2.6					
$V_{OL}$	Low-level output voltage P0 <sub>0</sub> ~P0 <sub>7</sub> , P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> , P3 <sub>0</sub> , P3 <sub>1</sub> , P3 <sub>3</sub> , P4 <sub>0</sub> ~P4 <sub>7</sub> , P5 <sub>0</sub> ~P5 <sub>7</sub> , P6 <sub>0</sub> ~P6 <sub>7</sub> , P7 <sub>0</sub> ~P7 <sub>7</sub> , P8 <sub>0</sub> ~P8 <sub>7</sub>	$V_{CC}=5V$ , $I_{OL}=10mA$			2	V		
		$V_{CC}=3V$ , $I_{OL}=1mA$			0.5			
$V_{OL}$	Low-level output voltage P0 <sub>0</sub> ~P0 <sub>7</sub> , P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> , P3 <sub>0</sub> , P3 <sub>1</sub> , P3 <sub>3</sub>	$V_{CC}=5V$ , $I_{OL}=2mA$			0.45	V		
$V_{OL}$	Low-level output voltage P3 <sub>2</sub>	$V_{CC}=5V$ , $I_{OL}=10mA$			1.9	V		
		$V_{CC}=5V$ , $I_{OL}=2mA$			0.43			
		$V_{CC}=3V$ , $I_{OL}=1mA$			0.4			
$V_{OL}$	Low-level output voltage $\bar{E}$	$V_{CC}=5V$ , $I_{OL}=10mA$			1.6	V		
		$V_{CC}=5V$ , $I_{OL}=2mA$			0.4			
		$V_{CC}=3V$ , $I_{OL}=1mA$			0.4			
$V_{T+}-V_{T-}$	Hysteresis HOLD, RDY, TA0 <sub>IN</sub> ~TA4 <sub>IN</sub> , TB0 <sub>IN</sub> ~TB2 <sub>IN</sub> , INT0~INT2, AD <sub>TRG</sub> , CTS <sub>0</sub> , CTS <sub>1</sub> , CLK <sub>0</sub> , CLK <sub>1</sub>	$V_{CC}=5V$	0.4		1	V		
		$V_{CC}=3V$	0.1		0.7			
$V_{T+}-V_{T-}$	Hysteresis RESET	$V_{CC}=5V$	0.2		0.5	V		
		$V_{CC}=3V$	0.1		0.4			
$V_{T+}-V_{T-}$	Hysteresis X <sub>IN</sub>	$V_{CC}=5V$	0.1		0.3	V		
		$V_{CC}=3V$	0.06		0.2			
$I_{IH}$	High-level input current P0 <sub>0</sub> ~P0 <sub>7</sub> , P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> , P3 <sub>0</sub> ~P3 <sub>3</sub> , P4 <sub>0</sub> ~P4 <sub>7</sub> , P5 <sub>0</sub> ~P5 <sub>7</sub> , P6 <sub>0</sub> ~P6 <sub>7</sub> , P7 <sub>0</sub> ~P7 <sub>7</sub> , P8 <sub>0</sub> ~P8 <sub>7</sub> , X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , BYTE	$V_{CC}=5V$ , $V_I=5V$			5	$\mu A$		
		$V_{CC}=3V$ , $V_I=3V$			4			
$I_{IL}$	Low-level input current P0 <sub>0</sub> ~P0 <sub>7</sub> , P1 <sub>0</sub> ~P1 <sub>7</sub> , P2 <sub>0</sub> ~P2 <sub>7</sub> , P3 <sub>0</sub> ~P3 <sub>3</sub> , P4 <sub>0</sub> ~P4 <sub>7</sub> , P5 <sub>0</sub> ~P5 <sub>7</sub> , P6 <sub>0</sub> ~P6 <sub>7</sub> , P7 <sub>0</sub> ~P7 <sub>7</sub> , P8 <sub>0</sub> ~P8 <sub>7</sub> , X <sub>IN</sub> , RESET, CNV <sub>SS</sub> , BYTE	$V_{CC}=5V$ , $V_I=0V$			-5	$\mu A$		
		$V_{CC}=3V$ , $V_I=0V$			-4			
$V_{RAM}$	RAM hold voltage	When clock is stopped.	2			V		
$I_{CC}$	Power supply current	In single-chip mode output only pin is open and other pins are V <sub>SS</sub> during reset.	f(X <sub>IN</sub> )=8MHz, square waveform	$V_{CC}=5V$	6	12	mA	
				$V_{CC}=3V$	4	8		
				$T_a=25^\circ C$ when clock is stopped.			1	$\mu A$
				$T_a=85^\circ C$ when clock is stopped.			20	



# MITSUBISHI MICROCOMPUTERS

## M37710E4LXXXFP

### PROM VERSION of M37710M4LXXXFP

#### A-D CONVERTER CHARACTERISTICS ( $V_{CC}=AV_{CC}=5V$ , $V_{SS}=AV_{SS}=0V$ , $T_a=25^\circ C$ , $f(X_{IN})=8MHz$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	$V_{REF}=V_{CC}$			10	Bits
—	Absolute accuracy	$V_{REF}=V_{CC}$			$\pm 3$	LSB
$R_{LADDER}$	Ladder resistance	$V_{REF}=V_{CC}$	5		20	$k\Omega$
$t_{CONV}$	Conversion time		29.5			$\mu s$
$V_{REF}$	Reference voltage		2.7		$V_{CC}$	V
$V_{IA}$	Analog input voltage		0		$V_{REF}$	V

#### D-A CONVERTER CHARACTERISTICS ( $V_{CC}=5V$ , $V_{SS}=AV_{SS}=0V$ , $V_{REF}=5V$ , $T_a=25^\circ C$ , $f(X_{IN})=8MHz$ , unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy				1.0	%
$t_{su}$	Set time				3	$\mu s$
$R_O$	Output resistance		1	2.5	4	$k\Omega$
$I_{VREF}$	Reference power input current	(Note)			3.2	mA

Note. One D-A converter is used, and the value of D-A register for unused D-A converter is "00<sub>16</sub>".  
Current that flows to the ladder resistance of A-D converter is excluded.

# MITSUBISHI MICROCOMPUTERS

## M37710E4LXXXFP

### PROM VERSION of M37710M4LXXXFP

#### TIMING REQUIREMENTS ( $V_{CC}=2.7\sim 5.5V$ , $V_{SS}=0V$ , $T_a=25^\circ C$ , $f(X_{IN})=8MHz$ , unless otherwise noted)

##### External clock input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_C$	External clock input cycle time	125		ns
$t_{W(H)}$	External clock input high-level pulse width	50		ns
$t_{W(L)}$	External clock input low-level pulse width	50		ns
$t_r$	External clock rise time		20	ns
$t_f$	External clock fall time		20	ns

##### Single-chip mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{SU(P0D-E)}$	Port P0 input setup time	300		ns
$t_{SU(P1D-E)}$	Port P1 input setup time	300		ns
$t_{SU(P2D-E)}$	Port P2 input setup time	300		ns
$t_{SU(P3D-E)}$	Port P3 input setup time	300		ns
$t_{SU(P4D-E)}$	Port P4 input setup time	300		ns
$t_{SU(P5D-E)}$	Port P5 input setup time	300		ns
$t_{SU(P6D-E)}$	Port P6 input setup time	300		ns
$t_{SU(P7D-E)}$	Port P7 input setup time	300		ns
$t_{SU(P8D-E)}$	Port P8 input setup time	300		ns
$t_{H(E-P0D)}$	Port P0 input hold time	0		ns
$t_{H(E-P1D)}$	Port P1 input hold time	0		ns
$t_{H(E-P2D)}$	Port P2 input hold time	0		ns
$t_{H(E-P3D)}$	Port P3 input hold time	0		ns
$t_{H(E-P4D)}$	Port P4 input hold time	0		ns
$t_{H(E-P5D)}$	Port P5 input hold time	0		ns
$t_{H(E-P6D)}$	Port P6 input hold time	0		ns
$t_{H(E-P7D)}$	Port P7 input hold time	0		ns
$t_{H(E-P8D)}$	Port P8 input hold time	0		ns

##### Memory expansion mode and microprocessor mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{SU(P1D-E)}$	Port P1 input setup time	80		ns
$t_{SU(P2D-E)}$	Port P2 input setup time	80		ns
$t_{SU(RDY-\phi_1)}$	RDY input setup time	90		ns
$t_{SU(HOLD-\phi_1)}$	HOLD input setup time	90		ns
$t_{H(E-P1D)}$	Port P1 input hold time	0		ns
$t_{H(E-P2D)}$	Port P2 input hold time	0		ns
$t_{H(\phi_1-RDY)}$	RDY input hold time	0		ns
$t_{H(\phi_1-HOLD)}$	HOLD input hold time	0		ns

## PROM VERSION of M37710M4LXXXFP

**Timer A input** (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(TA)}$	TA <sub>IIN</sub> input cycle time	250		ns
$t_{W(TAH)}$	TA <sub>IIN</sub> input high-level pulse width	125		ns
$t_{W(TAL)}$	TA <sub>IIN</sub> input low-level pulse width	125		ns

**Timer A input** (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(TA)}$	TA <sub>IIN</sub> input cycle time	1000		ns
$t_{W(TAH)}$	TA <sub>IIN</sub> input high-level pulse width	500		ns
$t_{W(TAL)}$	TA <sub>IIN</sub> input low-level pulse width	500		ns

**Timer A input** (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(TA)}$	TA <sub>IIN</sub> input cycle time	500		ns
$t_{W(TAH)}$	TA <sub>IIN</sub> input high-level pulse width	250		ns
$t_{W(TAL)}$	TA <sub>IIN</sub> input low-level pulse width	250		ns

**Timer A input** (External trigger input in pulse width modulation mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{W(TAH)}$	TA <sub>IIN</sub> input high-level pulse width	250		ns
$t_{W(TAL)}$	TA <sub>IIN</sub> input low-level pulse width	250		ns

**Timer A input** (Up-down input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(UP)}$	TA <sub>IOUT</sub> input cycle time	5000		ns
$t_{W(UPH)}$	TA <sub>IOUT</sub> input high-level pulse width	2500		ns
$t_{W(UPL)}$	TA <sub>IOUT</sub> input low-level pulse width	2500		ns
$t_{SU(UP-TIN)}$	TA <sub>IOUT</sub> input setup time	1000		ns
$t_{H(TIN-UP)}$	TA <sub>IOUT</sub> input hold time	1000		ns

# MITSUBISHI MICROCOMPUTERS

## M37710E4LXXXFP

### PROM VERSION of M37710M4LXXXFP

#### Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(TB)}$	TB <sub>iIN</sub> input cycle time (one edge count)	250		ns
$t_{W(TBH)}$	TB <sub>iIN</sub> input high-level pulse width (one edge count)	125		ns
$t_{W(TBL)}$	TB <sub>iIN</sub> input low-level pulse width (one edge count)	125		ns
$t_{C(TB)}$	TB <sub>iIN</sub> input cycle time (both edges count)	500		ns
$t_{W(TBH)}$	TB <sub>iIN</sub> input high-level pulse width (both edges count)	250		ns
$t_{W(TBL)}$	TB <sub>iIN</sub> input low-level pulse width (both edges count)	250		ns

#### Timer B input (Pulse period measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(TB)}$	TB <sub>iIN</sub> input cycle time	1000		ns
$t_{W(TBH)}$	TB <sub>iIN</sub> input high-level pulse width	500		ns
$t_{W(TBL)}$	TB <sub>iIN</sub> input low-level pulse width	500		ns

#### Timer B input (Pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(TB)}$	TB <sub>iIN</sub> input cycle time	1000		ns
$t_{W(TBH)}$	TB <sub>iIN</sub> input high-level pulse width	500		ns
$t_{W(TBL)}$	TB <sub>iIN</sub> input low-level pulse width	500		ns

#### A-D trigger input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(AD)}$	AD <sub>TRG</sub> input cycle time (minimum allowable trigger)	2000		ns
$t_{W(ADL)}$	AD <sub>TRG</sub> input low-level pulse width	250		ns

#### Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(CLK)}$	CLK <sub>j</sub> input cycle time	500		ns
$t_{W(CLKH)}$	CLK <sub>j</sub> input high-level pulse width	250		ns
$t_{W(CLKL)}$	CLK <sub>j</sub> input low-level pulse width	250		ns
$t_{d(C-Q)}$	TxD <sub>j</sub> output delay time		170	ns
$t_{h(C-Q)}$	TxD <sub>j</sub> hold time	0		ns
$t_{SU(D-C)}$	RxD <sub>j</sub> input setup time	80		ns
$t_{h(C-D)}$	RxD <sub>j</sub> input hold time	100		ns

#### External interrupt INT<sub>j</sub> input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{W(INH)}$	INT <sub>j</sub> input high-level pulse width	250		ns
$t_{W(INL)}$	INT <sub>j</sub> input low-level pulse width	250		ns

**SWITCHING CHARACTERISTICS** ( $V_{CC}=2.7\sim 5.5V$ ,  $V_{SS}=0V$ ,  $T_a=25^\circ C$ ,  $f(X_{IN})=8MHz$ , unless otherwise noted)**Single-chip mode**

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
$t_{d(E-P0Q)}$	Port P0 data output delay time	Fig. 5		300	ns
$t_{d(E-P1Q)}$	Port P1 data output delay time			300	ns
$t_{d(E-P2Q)}$	Port P2 data output delay time			300	ns
$t_{d(E-P3Q)}$	Port P3 data output delay time			300	ns
$t_{d(E-P4Q)}$	Port P4 data output delay time			300	ns
$t_{d(E-P5Q)}$	Port P5 data output delay time			300	ns
$t_{d(E-P6Q)}$	Port P6 data output delay time			300	ns
$t_{d(E-P7Q)}$	Port P7 data output delay time			300	ns
$t_{d(E-P8Q)}$	Port P8 data output delay time			300	ns

**Memory expansion mode and microprocessor mode** (when wait bit = "1")

Symbol	Parameter	Test conditions	Limits		Unit	
			Min.	Max.		
$t_{d(P0A-E)}$	Port P0 address output delay time	Fig. 5	62		ns	
$t_{d(E-P1Q)}$	Port P1 data output delay time (BYTE="L")			130	ns	
$tp_{XZ(E-P1Z)}$	Port P1 floating start delay time (BYTE="L")			10	ns	
$t_{d(P1A-E)}$	Port P1 address output delay time			62	ns	
$t_{d(P1A-ALE)}$	Port P1 address output delay time			52	ns	
$t_{d(E-P2Q)}$	Port P2 data output delay time			130	ns	
$tp_{XZ(E-P2Z)}$	Port P2 floating start delay time			10	ns	
$t_{d(P2A-E)}$	Port P2 address output delay time			62	ns	
$t_{d(P2A-ALE)}$	Port P2 address output delay time			52	ns	
$t_{d(\phi_1-HLDA)}$	HLDA output delay time				120	ns
$t_{d(ALE-E)}$	ALE output delay time			4	ns	
$t_{W(ALE)}$	ALE pulse width			82	ns	
$t_{d(BHE-E)}$	BHE output delay time			62	ns	
$t_{d(R/W-E)}$	R/W output delay time			62	ns	
$t_{d(E-\phi_1)}$	$\phi_1$ output delay time			0	40	ns
$t_{h(E-P0A)}$	Port P0 address hold time			95	ns	
$t_{h(ALE-P1A)}$	Port P1 address hold time (BYTE="L")			9	ns	
$t_{h(E-P1Q)}$	Port P1 data hold time (BYTE="L")			95	ns	
$tp_{ZX(E-P1Z)}$	Port P1 floating release delay time (BYTE="L")			95	ns	
$t_{h(E-P1A)}$	Port P1 address hold time (BYTE="H")			95	ns	
$t_{h(ALE-P2A)}$	Port P2 address hold time			9	ns	
$t_{h(E-P2Q)}$	Port P2 data hold time			95	ns	
$tp_{ZX(E-P2Z)}$	Port P2 floating release delay time			95	ns	
$t_{h(E-BHE)}$	BHE hold time			18	ns	
$t_{h(E-R/W)}$	R/W hold time			18	ns	
$t_{W(EL)}$	E pulse width			220	ns	

# MITSUBISHI MICROCOMPUTERS

## M37710E4LXXFP

### PROM VERSION of M37710M4LXXFP

#### Memory expansion mode and microprocessor mode

(when wait bit = "0", wait selection bit = "1", and external memory area is accessed)

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
$t_{d(P0A-E)}$	Port P0 address output delay time	Fig. 5	62		ns
$t_{d(E-P1Q)}$	Port P1 data output delay time (BYTE="L")			130	ns
$tp_{XZ(E-P1Z)}$	Port P1 floating start delay time (BYTE="L")			10	ns
$t_{d(P1A-E)}$	Port P1 address output delay time		62		ns
$t_{d(P1A-ALE)}$	Port P1 address output delay time		52		ns
$t_{d(E-P2Q)}$	Port P2 data output delay time			130	ns
$tp_{XZ(E-P2Z)}$	Port P2 floating start delay time			10	ns
$t_{d(P2A-E)}$	Port P2 address output delay time		62		ns
$t_{d(P2A-ALE)}$	Port P2 address output delay time		52		ns
$t_{d(\phi_1-HLDA)}$	HLDA output delay time			120	ns
$t_{d(ALE-E)}$	ALE output delay time		4		ns
$t_{W(ALE)}$	ALE pulse width		82		ns
$t_{d(BHE-E)}$	BHE output delay time		62		ns
$t_{d(R/W-E)}$	R/W output delay time		62		ns
$t_{d(E-\phi_1)}$	$\phi_1$ output delay time		0	40	ns
$t_{h(E-P0A)}$	Port P0 address hold time		95		ns
$t_{h(ALE-P1A)}$	Port P1 address hold time (BYTE="L")		9		ns
$t_{h(E-P1Q)}$	Port P1 data hold time (BYTE="L")		95		ns
$tp_{ZX(E-P1Z)}$	Port P1 floating release delay time (BYTE="L")		95		ns
$t_{h(E-P1A)}$	Port P1 address hold time (BYTE="H")		95		ns
$t_{h(ALE-P2A)}$	Port P2 address hold time		9		ns
$t_{h(E-P2Q)}$	Port P2 data hold time		95		ns
$tp_{ZX(E-P2Z)}$	Port P2 floating release delay time		95		ns
$t_{h(E-BHE)}$	BHE hold time		18		ns
$t_{h(E-R/W)}$	R/W hold time		18		ns
$t_{W(EL)}$	$\bar{E}$ pulse width		470		ns

# MITSUBISHI MICROCOMPUTERS

## M37710E4LXXXFP

### PROM VERSION of M37710M4LXXXFP

#### Memory expansion mode and microprocessor mode

(when wait bit = "0", wait selection bit = "0", and external memory area is accessed)

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
$t_{d(P0A-E)}$	Port P0 address output delay time	Fig. 5	312		ns
$t_{d(E-P1Q)}$	Port P1 data output delay time (BYTE="L")			130	ns
$tp_{XZ(E-P1Z)}$	Port P1 floating start delay time (BYTE="L")			10	ns
$t_{d(P1A-E)}$	Port P1 address output delay time		312		ns
$t_{d(P1A-ALE)}$	Port P1 address output delay time		177		ns
$t_{d(E-P2Q)}$	Port P2 data output delay time			130	ns
$tp_{XZ(E-P2Z)}$	Port P2 floating start delay time			10	ns
$t_{d(P2A-E)}$	Port P2 address output delay time		312		ns
$t_{d(P2A-ALE)}$	Port P2 address output delay time		177		ns
$t_{d(\phi_1-HLDA)}$	HLDA output delay time			120	ns
$t_{d(ALE-E)}$	ALE output delay time		100		ns
$t_{W(ALE)}$	ALE pulse width		207		ns
$t_{d(BHE-E)}$	BHE output delay time		312		ns
$t_{d(R/W-E)}$	R/W output delay time		312		ns
$t_{d(E-\phi_1)}$	$\phi_1$ output delay time		0	40	ns
$t_{h(E-P0A)}$	Port P0 address hold time		95		ns
$t_{h(ALE-P1A)}$	Port P1 address hold time (BYTE="L")		105		ns
$t_{h(E-P1Q)}$	Port P1 data hold time (BYTE="L")		95		ns
$tp_{ZX(E-P1Z)}$	Port P1 floating release delay time (BYTE="L")		95		ns
$t_{h(E-P1A)}$	Port P1 address hold time (BYTE="H")		95		ns
$t_{h(ALE-P2A)}$	Port P2 address hold time		105		ns
$t_{h(E-P2Q)}$	Port P2 data hold time		95		ns
$tp_{ZX(E-P2Z)}$	Port P2 floating release delay time		95		ns
$t_{h(E-BHE)}$	BHE hold time		18		ns
$t_{h(E-R/W)}$	R/W hold time		18		ns
$t_{W(E)}$	$\bar{E}$ pulse width		470		ns

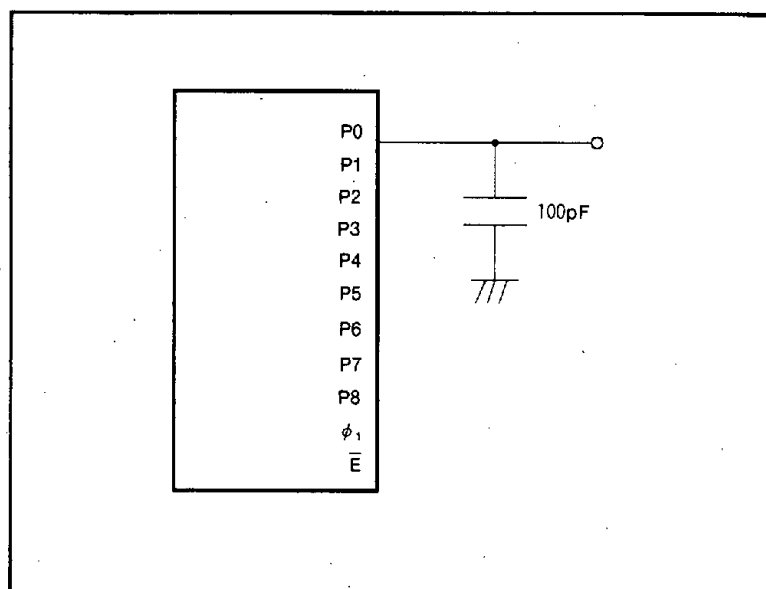
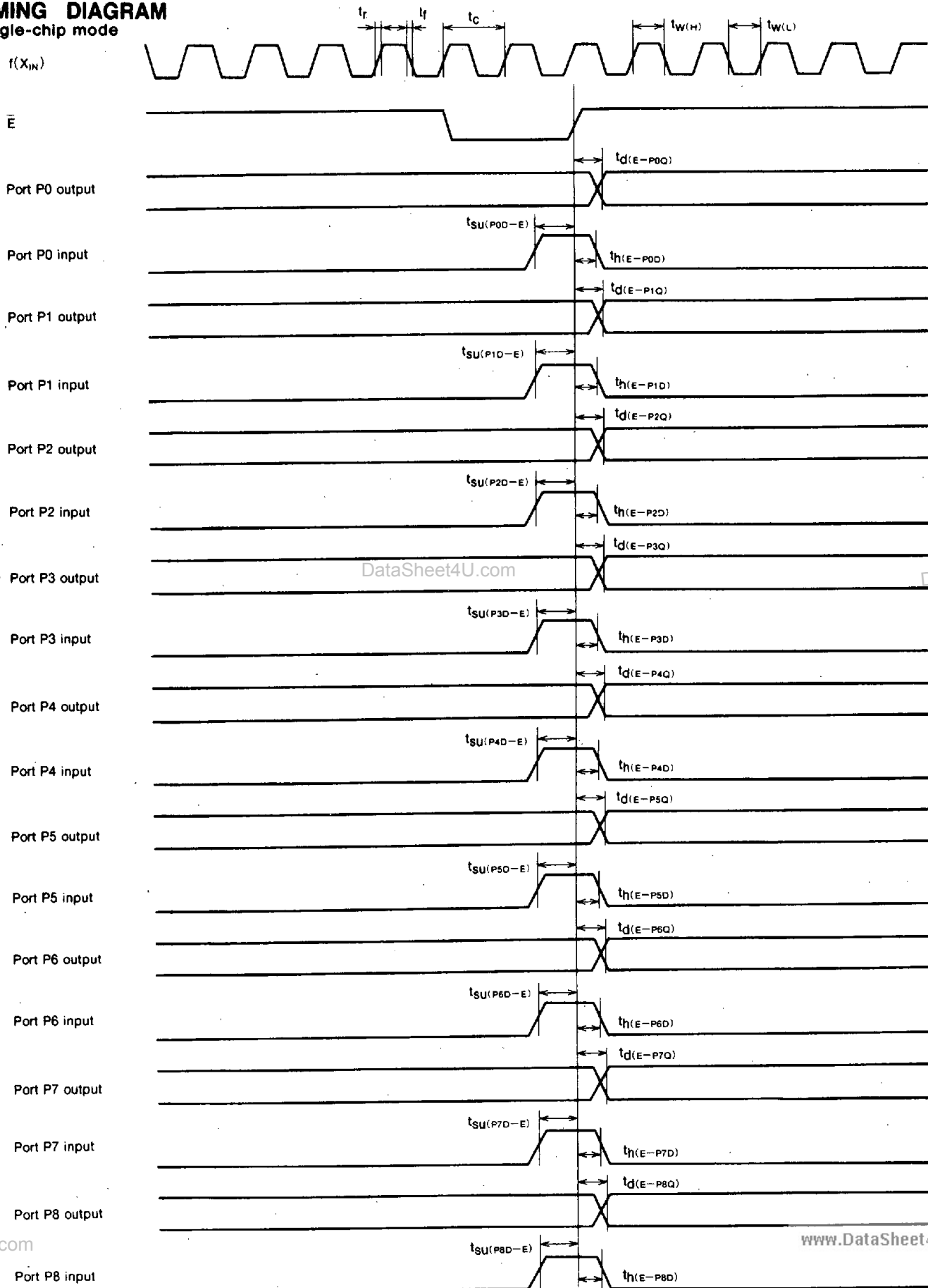


Fig. 5 Testing circuit for ports P0~P8,  $\phi_1$

### PROM VERSION of M37710M4LXXXFP

#### TIMING DIAGRAM

Single-chip mode



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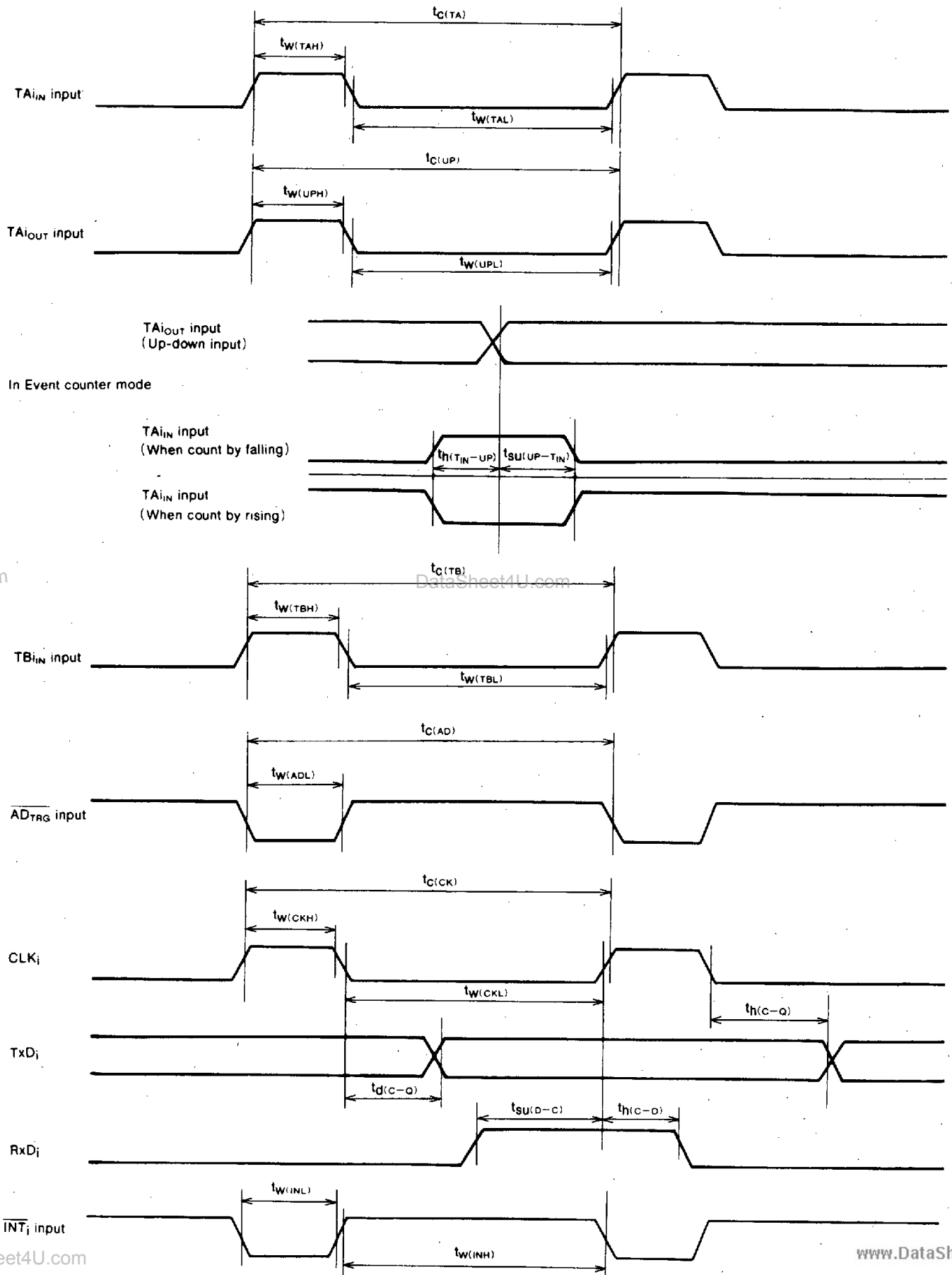
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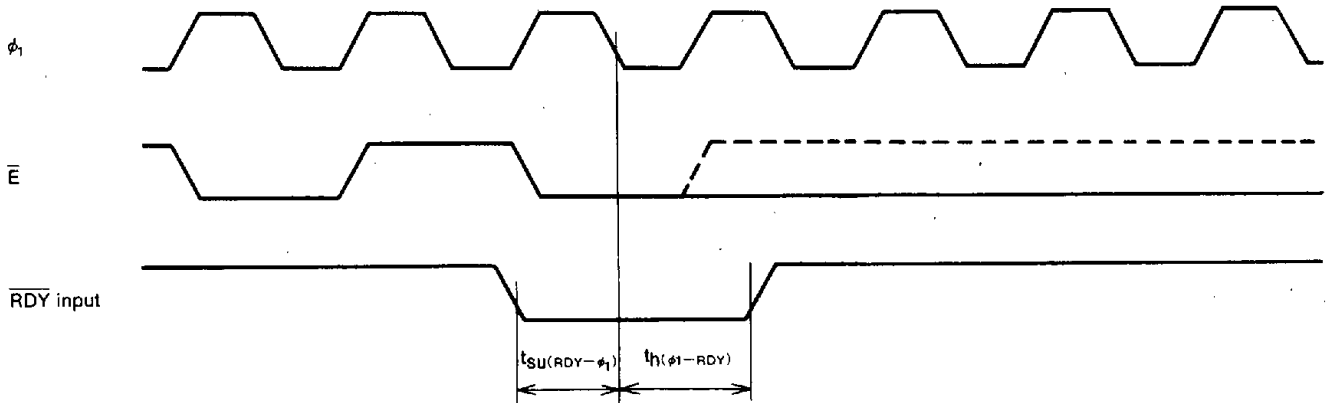
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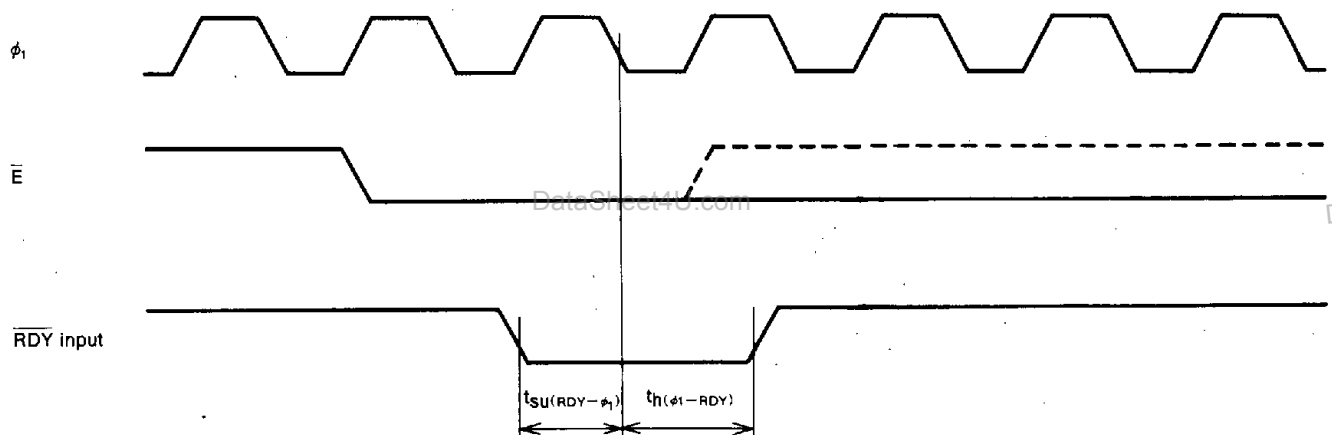
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**PROM VERSION of M37710M4LXXXFP**
**Memory expansion mode and microprocessor mode**

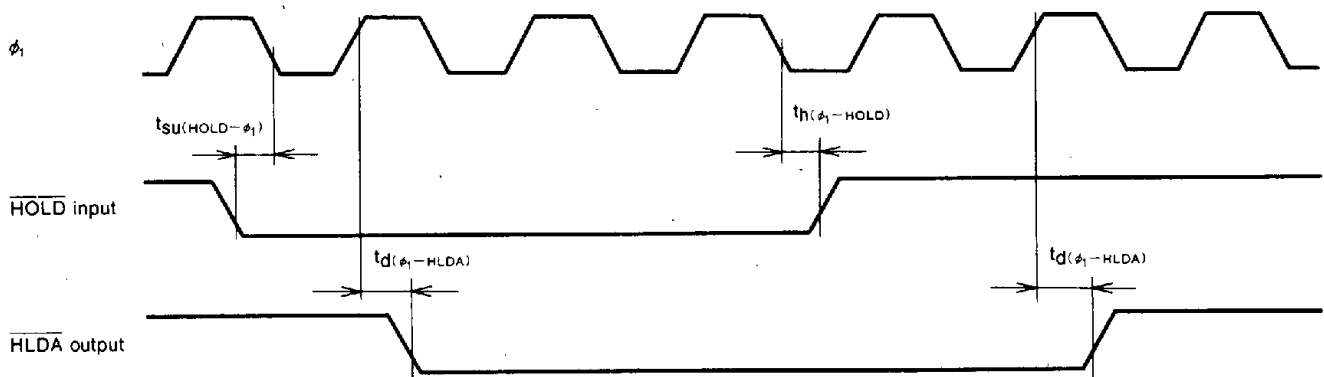
(When wait bit = "1")



(When wait bit = "0")

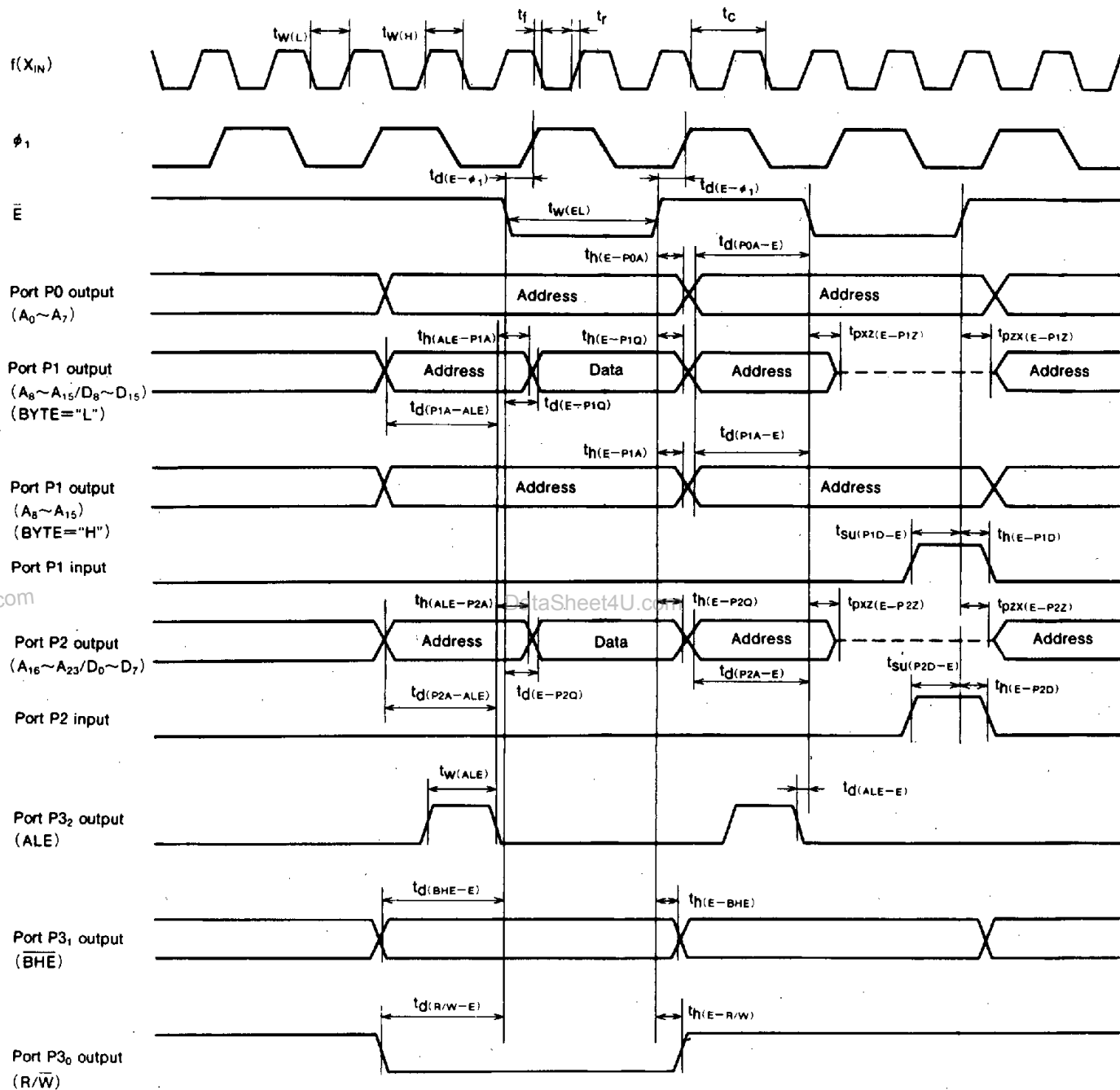


(When wait bit = "1" or "0" in common)


**Test conditions**

- $V_{CC} = 2.7 \sim 5.5V$
- Input timing voltage :  $V_{IL} = 0.2V_{CC}$ ,  $V_{IH} = 0.8V_{CC}$
- Output timing voltage :  $V_{OL} = 0.8V$ ,  $V_{OH} = 2.0V$

## Memory expansion mode and microprocessor mode (When wait bit="1")

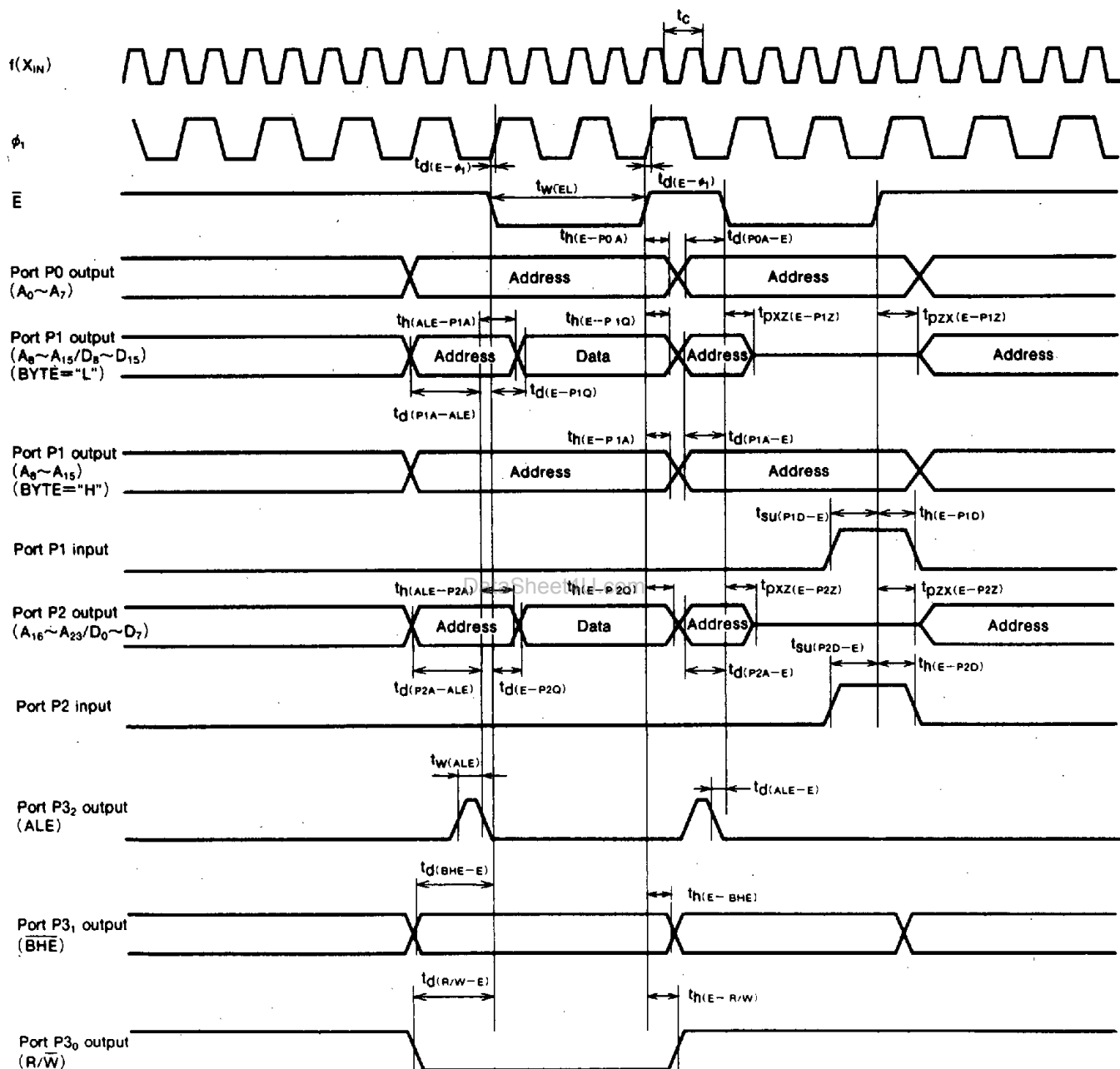


## Test conditions

- $V_{CC}=2.7\sim 5.5V$
- Output timing voltage :  $V_{OL}=0.8V$ ,  $V_{OH}=2.0V$
- Ports P1, P2 input :  $V_{IL}=0.16V_{CC}$ ,  $V_{IH}=0.5V_{CC}$

**PROM VERSION of M37710M4LXXXFP**
**Memory expansion mode and microprocessor mode**

(When wait bit = "0", wait selection bit = "1", and external memory area is accessed)

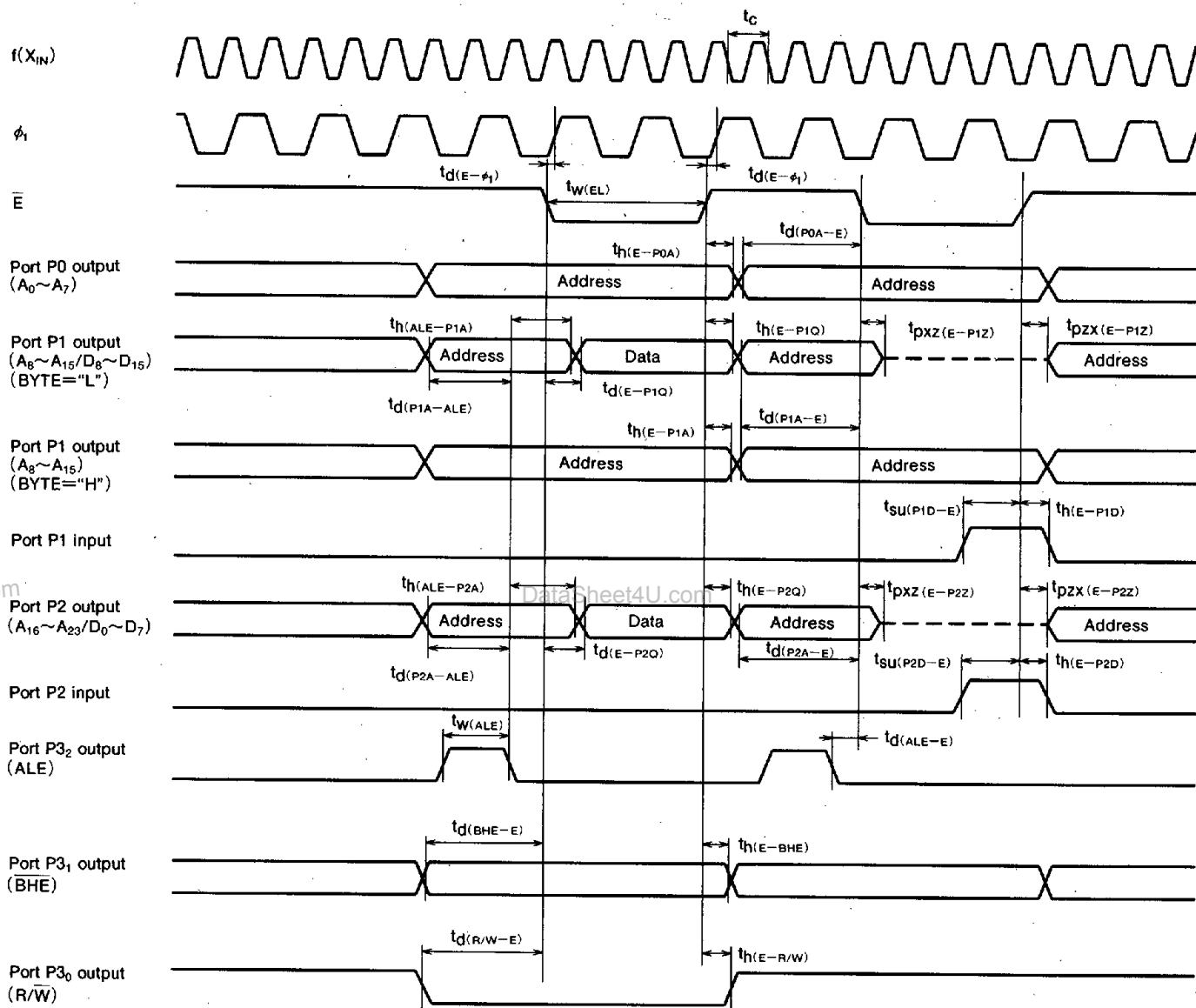

**Test conditions**

- $V_{CC}=2.7 \sim 5.5V$
- Output timing voltage :  $V_{OL}=0.8V, V_{OH}=2.0V$
- Ports P1, P2 input :  $V_{IL}=0.16V_{CC}, V_{IH}=0.5V_{CC}$

## PROM VERSION of M37710M4LXXXFP

## Memory expansion mode and microprocessor mode

(When wait bit = "0", wait selection bit = "0", and external memory area is accessed)



## Test conditions

- $V_{CC}=2.7\sim 5.5V$
- Output timing voltage :  $V_{OL}=0.8V, V_{OH}=2.0V$
- Ports P1, P2 input :  $V_{IL}=0.16V_{CC}, V_{IH}=0.5V_{CC}$

# 8/16-bit Data Bus Flash Memory Card

**MF84M1-G1EATXX**

Connector Type

**Two-piece 68-pin**

## DESCRIPTION

The MF84M1-G1EATXX is a flash memory card which uses sixteen two-megabit flash electrically erasable and programmable read only memory IC's.

## FEATURES

- 68 pin JEIDA/PCMCIA
- 8/16 controllable data bus width
- Buffered interface
- TTL interface level
- Program/erase operation by software command control
- Program/erase voltage 12V
- 10,000 program/erase cycles
- Write protect switch

## APPLICATIONS

- Note book computers
- Printers
- Industrial machines

## PRODUCT LIST

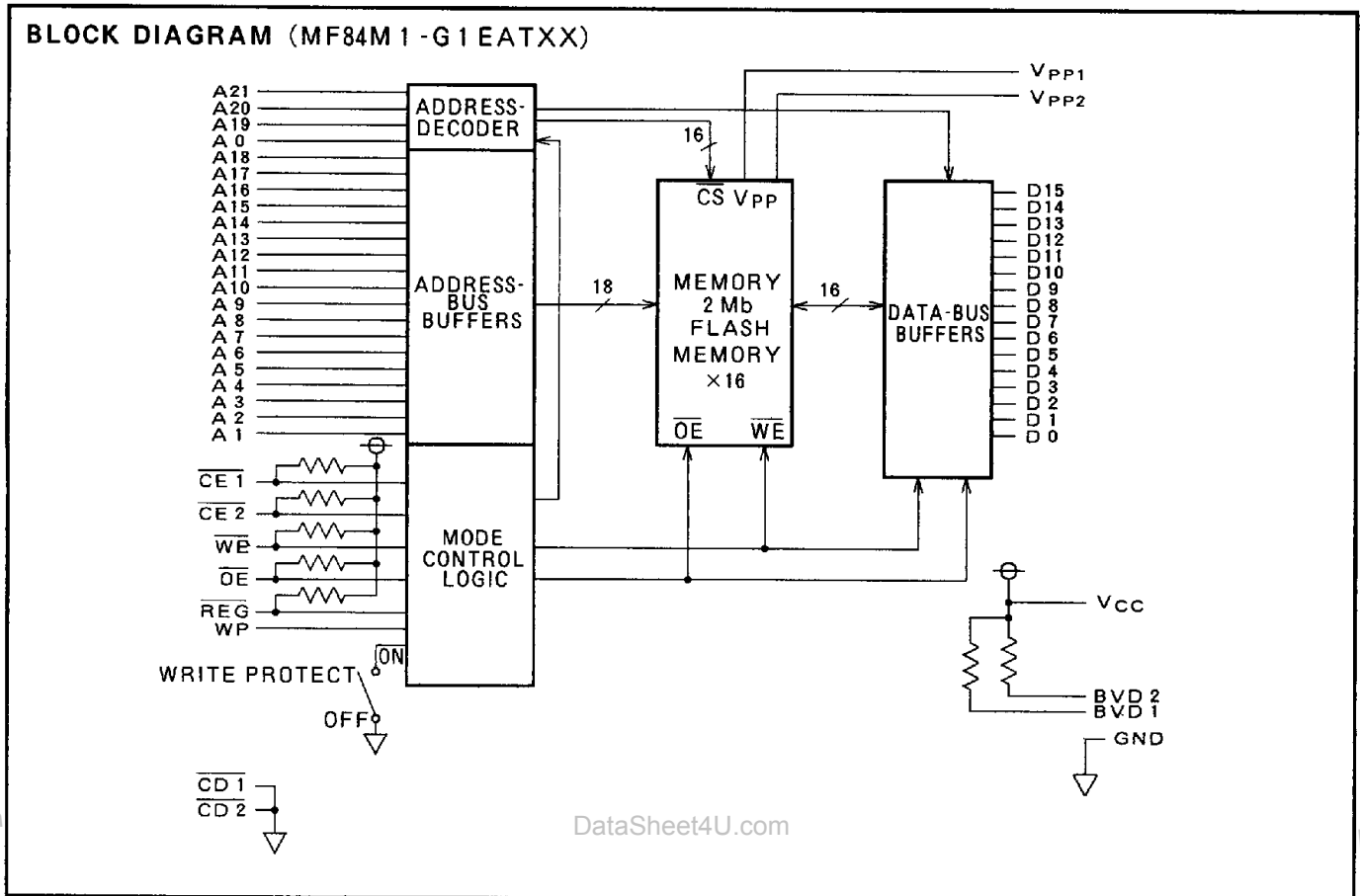
Type name	Item	Memory capacity	Data bus width (bits)	Access time (ns)	Connector type	Number of pins	Outline drawing
MF84M1-G1EATXX		4 MB	8/16	250	Two-piece	68	68P-002

## FLASH MEMORY CARDS

## PIN ASSIGNMENT

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground	35	GND	Ground
2	D 3	Data I/O	36	CD 1	Card detect 1
3	D 4		37	D11	Data I/O
4	D 5		38	D12	
5	D 6		39	D13	
6	D 7		40	D14	
7	CE 1		Card enable 1	41	D15
8	A10	Address input	42	CE 2	
9	OE	Output enable	43	NC	No connection
10	A11	Address input	44	NC	
11	A 9		45	NC	
12	A 8		46	A17	Address input
13	A13		47	A18	
14	A14	48	A19		
15	WE	Write enable	49	A20	Power supply voltage
16	NC	No connection	50	A21	
17	VCC	Power supply voltage	51	VCC	Power supply voltage
18	VPP 1	Programming supply voltage 1	52	VPP 2	Programming supply voltage 2
19	A16	Address input	53	NC	No connection
20	A15		54	NC	
21	A12		55	NC	
22	A 7		56	NC	
23	A 6		57	NC	
24	A 5		58	NC	
25	A 4		59	NC	
26	A 3		60	NC	
27	A 2		61	REG	Attribute memory select
28	A 1		62	BVD 2	Battery voltage detect 2
29	A 0	63	BVD 1	Battery voltage detect 1	
30	D 0	Data I/O	64	D 8	Data I/O
31	D 1		65	D 9	
32	D 2		66	D10	
33	WP		Write protect	67	CD 2
34	GND	Ground	68	GND	Ground

## FLASH MEMORY CARDS

**FUNCTIONAL DESCRIPTION**

The operating mode of the card is determined by five active low control signals ( $\overline{\text{REG}}$ ,  $\overline{\text{CE1}}$ ,  $\overline{\text{CE2}}$ ,  $\overline{\text{OE}}$ ,  $\overline{\text{WE}}$ ), three supply voltages ( $V_{\text{CC}}$ ,  $V_{\text{PP1}}$ ,  $V_{\text{PP2}}$ ) and control registers located in each memory IC.

**Common memory function**

When the  $\overline{\text{REG}}$  signal is set to a high level common memory is selected.

**Read only mode**

When the voltages applied to both  $V_{\text{PP1}}$  and  $V_{\text{PP2}}$  are less than the voltage applied to  $V_{\text{CC}}$  (i.e.  $V_{\text{PP}} = 0\text{V to } V_{\text{CC}}$ ), the control registers of each memory IC are set to read only mode.

Operation of the card then depends on the four possible combinations of  $\overline{\text{CE1}}$  and  $\overline{\text{CE2}}$  (note/ $\overline{\text{WE}}$  should be set to a high level when the device is in read only mode except during combination (4) where it's condition is unimportant):

(1) If  $\overline{\text{CE1}}$  is set to a low level and  $\overline{\text{CE2}}$  is set to a high level, the card will work as an eight bit data bus width card. Data can be accessed via the lower

half of the data bus (D0 to D7).

(2) If both  $\overline{\text{CE1}}$  and  $\overline{\text{CE2}}$  are set to a low level, data will be accessible via the full sixteen bit data bus width of the card. In this mode LSB of address bus (A0) is ignored.

(3) If  $\overline{\text{CE1}}$  is set to a high level and  $\overline{\text{CE2}}$  is set to a low level the odd bytes (only) can be accessed through upper half of the data bus (D8 to D15). This mode is useful when handling the odd (upper) bytes in a sixteen bit interface system. Note that A0 is also ignored in this operating condition.

(4) If  $\overline{\text{CE1}}$  and  $\overline{\text{CE2}}$  are set to a high level, the card will be in standby mode where it consumes low power. The data bus is kept high impedance.

When  $\overline{\text{OE}}$  is set to a low level data can be read from the card, depending on the address applied and the setting of  $\overline{\text{CE1}}$  and  $\overline{\text{CE2}}$  as mentioned above, except under combination (4).



## FLASH MEMORY CARDS

When  $\overline{OE}$  is set to a high level and  $\overline{WE}$  is set to a high level the card is in an output disable mode and the data bus will be in a high impedance state regardless of the condition of  $\overline{CE1}$  and  $\overline{CE2}$ .

**Read/write mode**

When a programming voltage ( $V_{PPH}$ ) is applied to either or both of  $V_{PP1}$  and  $V_{PP2}$ , read/write mode is enabled for the corresponding banks of memory IC's inside the card.  $V_{PP1}$  enables the Even Byte bank and  $V_{PP2}$  enables the Odd Byte bank.

By using the 4 combinations of  $\overline{CE1}$  and  $\overline{CE2}$  as descibed under Read only mode above the appropriate Data Out and Command/Data In bus selection can be made.

If  $\overline{OE}$  is set to a high level and  $\overline{WE}$  set to a low level, the control register will latch command data applied at the rising edge of the  $\overline{WE}$  signal. Note that more than one bus cycle may be required to latch the command and/or the related data – please refer to the Command Definition table.

If  $\overline{OE}$  is set to a low level and  $\overline{WE}$  is set to a high level the card data can be read from the card depending on the condition of the control register.

After latching the command data, the card will go into programming, erasure or other operation mode. For details please refer to the Command Definition table, each individual command's definition and the programming and erasure algorithms.

**Attribute memory**

When  $\overline{REG}$  is set to a low level attribute memory is selected.

The card then outputs FFh on the lower half of the data bus (D0 to D7) when the following conditions are applied :

- (1)  $\overline{CE1}$  : low level,  $\overline{CE2}$  : high level,  $\overline{OE}$  : low level,  $\overline{WE}$  : high level, A0 : low level
- (2)  $\overline{CE1}$  : low level,  $\overline{CE2}$  : low level,  $\overline{OE}$  : low level,  $\overline{WE}$  : high level.

**Write protect mode**

The card has a write protect switch on the opposite edge to the connector edge. When it is switched on, the card will be placed into a write protect mode, where data can be read from the card but it cannot be written to it. The WP output pin is set to a high level when the card is in write protect mode and  $V_{CC}$  is applied. When the card is not in write protect mode the WP output pin is set to a low level when  $V_{CC}$  is applied. By reading the state of the WP output the host system can easily check whether the card is in write protect mode or not.