M37735EHLXXXHP

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

DESCRIPTION

The M37735EHLXXXHP is a single-chip microcomputer using the 7700 Family core. This single-chip microcomputer has a CPU and a bus interface unit. The CPU is a 16-bit parallel processor that can be an 8-bit parallel processor, and the bus interface unit enhances the memory access efficiency to execute instructions fast. This microcomputer also includes a 32 kHz oscillation circuit, in addition to the PROM, RAM, multiple-function timers, serial I/O, A-D converter, and so on.

Its strong points are the low power dissipation, the low supply voltage and the small package.

The M37735EHLXXXHP has the same function as the M37735MHLXXXHP except that the built-in ROM is PROM. (Refer to the basic function blocks description.)

FEATURES

●Number of basic instructions 103
●Memory size   PROM .... 124 Kbytes
                   RAM .... 3968 bytes
●Instruction execution time
   The fastest instruction at 12 MHz frequency .... 333 ns

●Single power supply .... 2.7–5.5 V
●Low power dissipation (At 3 V supply voltage, 12 MHz frequency)
                                        9 mW (Typ.)
●Interrupts .... 19 types, 7 levels
●Multiple-function 16-bit timer .... 5 + 3
●Serial I/O (UART or clock synchronous) 3
●10-bit A-D converter .... 8-channel inputs
●Watchdog timer
●Programmable input/output
  (ports P0, P1, P2, P3, P4, P5, P6, P7, P8) 68
●Clock generating circuit .... 2 circuits built-in
●Small package .... 80-pin plastic molded fine-pitch QFP
                                              (0.5 mm lead pitch)

APPLICATION

Control devices for general commercial equipment such as office automation, office equipment, personal information equipment, and so on.

Control devices for general industrial equipment such as communication equipment, and so on.

PIN CONFIGURATION (TOP VIEW)

M37735EHLXXXHP

Outline   80P6D-A, 80P6Q-A

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M37735EHLXXXHP BLOCK DIAGRAM

External data bus width selection input BYTE

Reference voltage input V_{REF}

AV_{CC}

(0V) AV_{SS}

CNV_{SS}

(0V) V_{SS}

V_{CC}

Reset input RESET

Enable output $\overline{E}$

Clock output X_{OUT}

Clock input X_{IN}

X_{CIN} X_{COUT}

Clock Generating Circuit

Instruction Register(8)

Data Buffer $DB_H(8)$
Data Buffer $DB_L(8)$
Instruction Queue Buffer $Q_0(8)$
Instruction Queue Buffer $Q_1(8)$
Instruction Queue Buffer $Q_2(8)$

Incrementer(24)
Program Address Register PA(24)
Data Address Register DA(24)

Incrementer/Decrementer(24)
Program Counter PC(16)
Program Bank Register PG(8)
Data Bank Register DT(8)

Input Butter Register IB(16)

Processor Status Register PS(11)
Direct Page Register DPR(16)
Stack Pointer S(16)
Index Register Y(16)
Index Register X(16)
Accumulatcr B(16)
Accumulator A(16)

Arithmetic Logic Unit(16)

Data Bus(Even)
Data Bus(Odd)
Address Bus

A-D Converter(10)

UART2(9)
UART1(9)
UART0(9)

Watchdog Timer
Timer TB2(16)
Timer TB1(16)
Timer TB0(16)

Timer TA4(16)
Timer TA3(16)
Timer TA2(16)
Timer TA1(16)
Timer TA0(16)

RAM 3968 bytes

PROM 124 Kbytes

P0(8) — Input/Output port P0
P1(8) — Input/Output port P1
P2(8) — Input/Output port P2
P3(4) — Input/Output port P3
P4(8) — Input/Output port P4
P5(8) — Input/Output port P5
P6(8) — Input/Output port P6
P7(8) — Input/Output port P7
X_{COUT}→
X_{CIN}→
P8(8) — Input/Output port P8

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FUNCTIONS OF M37735EHLXXXHP

Parameter		Functions
Number of basic instructions		103
Instruction execution time		333 ns (the fastest instruction at external clock 12 MHz frequency)
Memory size	PROM	124 Kbytes
	RAM	3968 bytes
Input/Output ports	P0 – P2, P4 – P8	8-bit ✕ 8
	P3	4-bit ✕ 1
Multi-function timers	TA0, TA1, TA2, TA3, TA4	16-bit ✕ 5
	TB0, TB1, TB2	16-bit ✕ 3
Serial I/O		(UART or clock synchronous serial I/O) ✕ 3
A-D converter		10-bit ✕ 1 (8 channels)
Watchdog timer		12-bit ✕ 1
Interrupts		3 external types, 16 internal types Each interrupt can be set to the priority level (0 – 7.)
Clock generating circuit		2 circuits built-in (externally connected to a ceramic resonator or a quartz-crystal oscillator)
Supply voltage		2.7 – 5.5 V
Power dissipation		9 mW (at 3 V supply voltage, external clock 12 MHz frequency)
		22.5 mW (at 5 V supply voltage, external clock 12 MHz frequency)
Input/Output characteristic	Input/Output voltage	5 V
	Output current	5 mA
Memory expansion		Maximum 1 Mbytes
Operating temperature range		–40 to 85 °C
Device structure		CMOS high-performance silicon gate process
Package		80-pin plastic molded fine-pitch QFP (80P6D-A;0.5 mm lead pitch)

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PIN DESCRIPTION

Pin	Name	Input/Output	Functions
Vcc, Vss	Power source		Apply 2.7 – 5.5 V to Vcc and 0 V to Vss.
CNVss	CNVss input	Input	This pin controls the processor mode. Connect to Vss for the single-chip mode and the memory expansion mode, and to Vcc for the microprocessor mode.
$\overline{RESET}$	Reset input	Input	When "L" level is applied to this pin, the microcomputer enters the reset state.
X_{IN}	Clock input	Input	These are pins of main-clock generating circuit. Connect a ceramic resonator or a quartz-crystal oscillator between X_{IN} and X_{OUT}. When an external clock is used, the clock source should be connected to the X_{IN} pin, and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
$\overline{E}$	Enable output	Output	In the single-chip mode, this pin functions as the enable signal output pin which indicates the access status in the internal bus. In the memory expansion mode or the microprocessor mode, this pin functions as the $\overline{RDE}$ signal output pin.
BYTE	External data bus width selection input	Input	In the memory expansion mode or the microprocessor mode, this pin determines whether the external data bus has an 8-bit width or a 16-bit width. The data bus has a 16-bit width when "L" signal is input and an 8-bit width when "H" signal is input.
AVcc, AVss	Analog power source input		Power source input pin for the A-D converter. Externally connect AVcc to Vcc and AVss to Vss.
V_{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D converter.
$P0_0 – P0_7$	I/O port P0	I/O	In the single-chip mode, port P0 becomes an 8-bit I/O port. An I/O direction register is available so that each pin can be programmed for input or output. These ports are in the input mode when reset. In the memory expansion mode or the microprocessor mode, these pins output $\overline{CS_0} – \overline{CS_4}$, RSMP signals, and address (A_{16}, A_{17}).
$P1_0 – P1_7$	I/O port P1	I/O	In the single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to "L" in the memory expansion mode or the microprocessor mode and external data bus has a 16-bit width, high-order data ($D_8 – D_{15}$) is input/output or an address ($A_8 – A_{15}$) is output. When the BYTE pin is "H" and an external data bus has an 8-bit width, only address ($A_8 – A_{15}$) is output.
$P2_0 – P2_7$	I/O port P2	I/O	In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, low-order data ($D_0 – D_7$) is input/output or an address ($A_0 – A_7$) is output.
$P3_0 – P3_3$	I/O port P3	I/O	In the single-chip mode, these pins have the same function as port P0. In the memory expansion mode or the microprocessor mode, $\overline{WEL}$, $\overline{WEH}$, ALE, and $\overline{HLDA}$ signals are output.
$P4_0 – P4_7$	I/O port P4	I/O	In the single-chip mode, these pins have the same functions as port P0. In the memory expansion mode or the microprocessor mode, $P4_0$, $P4_1$, and $P4_2$ become $\overline{HOLD}$ and $\overline{RDY}$ input pins, and clock ϕ_1 output pin, respectively. Functions of the other pins are the same as in the single-chip mode. However, in the memory expansion mode, $P4_2$ also functions as an I/O port.
$P5_0 – P5_7$	I/O port P5	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timers A0 to A3 and input pins for key input interrupt input ($\overline{KI_0} – \overline{KI_3}$).
$P6_0 – P6_7$	I/O port P6	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for timer A4, input pins for external interrupt input ($\overline{INT_0} – \overline{INT_2}$) and input pins for timers B0 to B2. $P6_7$ also functions as sub-clock ϕ_{SUB} output pin.
$P7_0 – P7_7$	I/O port P7	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins function as input pins for A-D converter. $P7_2$ to $P7_5$ also function as I/O pins for UART2. Additionally, $P7_6$ and $P7_7$ have the function as the output pin (X_{COUT}) and the input pin (X_{CIN}) of the sub-clock (32 kHz) oscillation circuit, respectively. When $P7_6$ and $P7_7$ are used as the X_{COUT} and X_{CIN} pins, connect a resonator or an oscillator between the both.
$P8_0 – P8_7$	I/O port P8	I/O	In addition to having the same functions as port P0 in the single-chip mode, these pins also function as I/O pins for UART 0 and UART 1.

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PIN DESCRIPTION (EPROM MODE)

Pin	Name	Input/Output	Functions
V_{CC}, V_{SS}	Power supply		Supply 5V±10% to V_{CC} and 0V to V_{SS}.
$\overline{CNV_{SS}}$	V_{PP} input	Input	Connect to V_{PP} when programming or verifing.
BYTE	V_{PP} input	Input	Connect to V_{PP} when programming or verifing.
$\overline{RESET}$	Reset input	Input	Connect to V_{SS}.
X_{IN}	Clock input	Input	Connect a ceramic resonator between X_{IN} and X_{OUT}.
X_{OUT}	Clock output	Output	
$\overline{E}$	Enable output	Output	Keep open.
AV_{CC}, AV_{SS}	Analog supply input		Connect AV_{CC} to V_{CC} and AV_{SS} to V_{SS}.
V_{REF}	Reference voltage input	Input	Connect to V_{SS}.
$P0_0 - P0_7$	Address input ($A_0 - A_7$)	Input	Port P0 functions as the lower 8 bits address input ($A_0 - A_7$).
$P1_0 - P1_7$	Address input ($A_8 - A_{15}$)	Input	Port P1 functions as the higher 8 bits address input ($A_8 - A_{15}$).
$P2_0 - P2_7$	Data I/O ($D_0 - D_7$)	I/O	Port P2 functions as the 8 bits data bus($D_0 - D_7$).
$P3_0$	Address input (A_{16})	Input	$P3_0$ functions as the most significant bit address input (A_{16}).
$P3_1 - P3_3$	Input port P3	Input	Connect to V_{SS}.
$P4_0 - P4_7$	Input port P4	Input	Connect to V_{SS}.
$P5_0 - P5_7$	Control signal input	Input	$P5_0$, $P5_1$ and $P5_2$ function as $\overline{PGM}$, $\overline{OE}$ and $\overline{CE}$ input pins respectively. Connect $P5_3$, $P5_4$, $P5_5$ and $P5_6$ to V_{CC}. Connect $P5_7$ to V_{SS}.
$P6_0 - P6_7$	Input port P6	Input	Connect to V_{SS}.
$P7_0 - P7_7$	Input port P7	Input	Connect to V_{SS}.
$P8_0 - P8_7$	Input port P8	Input	Connect to V_{SS}.

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BASIC FUNCTION BLOCKS

The M37735EHLXXXHP has the same functions as the M37735MHBXXXFP except for the following :

(1) The built-in ROM is PROM.

(2) The status of bit 3 of the oscillation circuit control register 1 (address $6F_{16}$) at a reset is different.

(3) The usage condition of bit 3 of the oscillation circuit control register 1 is different.

(4) Part of the processor mode selection method is different.

Accordingly, refer to the basic function blocks description in the M37735MHBXXXFP except for Figure 1 (bit configuration of oscillation circuit control register 1), Figure 3 (microcomputer internal status during reset), and Table 1 (microprocessor mode selection method).

In the M37735EHLXXXHP, bit 3 of the oscillation circuit control register 1 must be "0". (Refer to Figure 1.) Bit 3 is "1" at a reset. Accordingly, write "0" to bit 3 in the single-chip mode after reset.

Figure 2 shows how to write data in oscillation circuit control register 1. In the M37735EHLXXXHP, the microprosessor mode cannot be selected by connecting the CNVss pin to Vcc. Connect the CNVss pin to Vss and start the microcomputer operating from the single-chip mode.

Table 1. Relationship between CNVss pin input level and processor modes

CNVss	Mode	Description
Vss	●Single-chip ●Memory expansion ●Microprocessor	Single-chip mode upon starting after reset. Each mode can be selected by changing the processor mode bits by software.
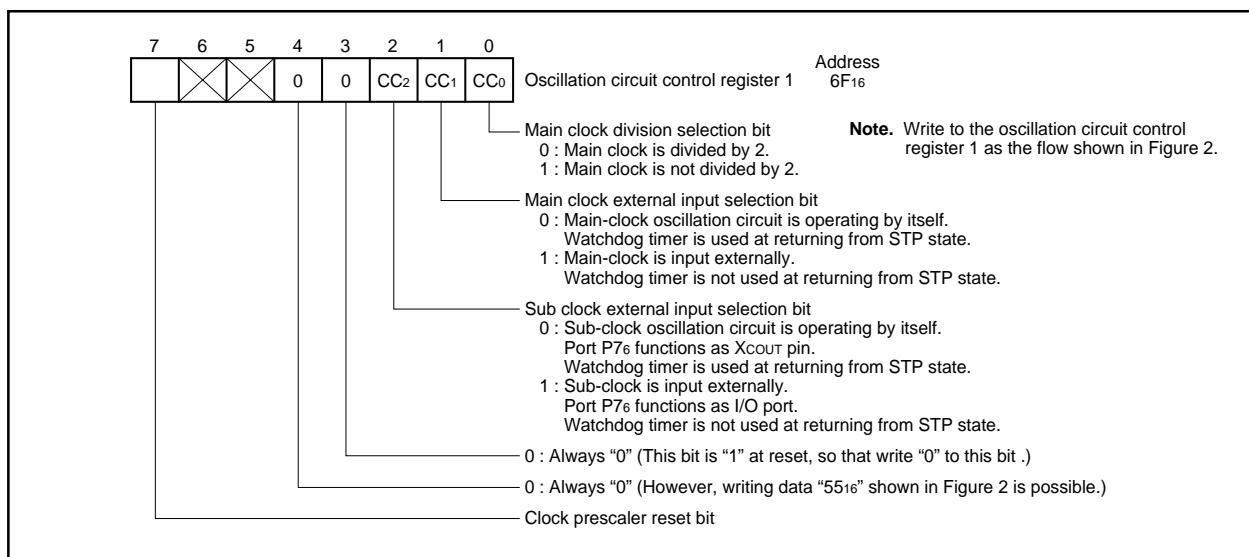
Fig. 1 Bit configuration of oscillation circuit control register 1 (corresponding to Figure 63 in data sheet "M37735MHBXXXFP")
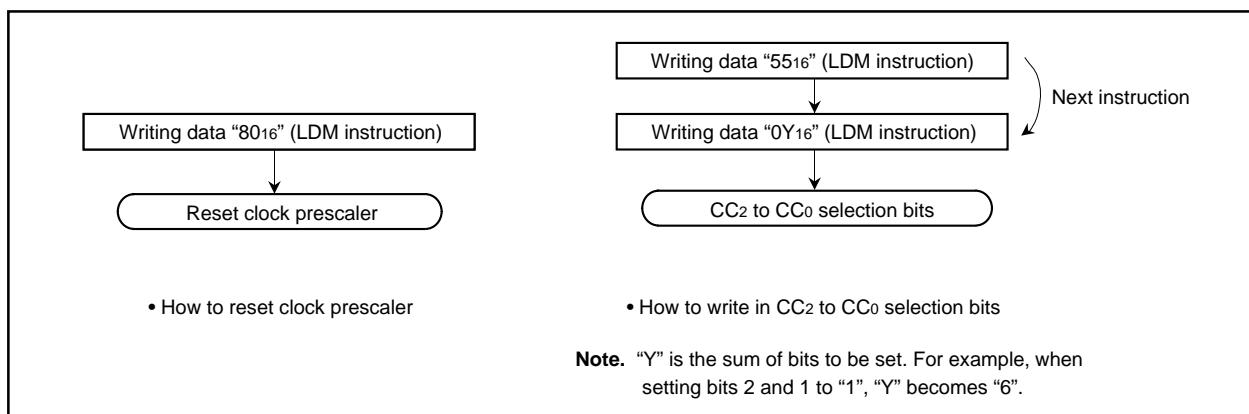
Fig. 2 How to write data in oscillation circuit control register 1 (identical with Figure 64 in data sheet "M37735MHBXXXFP")

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RESET CIRCUIT

The microcomputer is released from the reset state when the $\overline{\text{RESET}}$ pin is returned to "H" level after holding it at "L" level with the power source voltage at 2.7 – 5.5 V. Program execution starts at the address formed by setting address $A_{23} – A_{16}$ to 00_{16}, $A_{15} – A_8$ to the contents of address $FFFF_{16}$, and $A_7 – A_0$ to the contents of address $FFFE_{16}$. Figure 3 shows the microcomputer internal status during reset. Figure 4 shows an example of a reset circuit. When the stabilized clock is input from the external to the main-clock oscillation circuit, the reset input voltage must be 0.55 V or less when the power source voltage reaches 2.7 V. When a resonator/oscillator is connected to the main-clock oscillation circuit, change the reset input voltage from "L" to "H" after the main-clock oscillation is fully stabilized.

Note. In this case, stabilized clock is input from the external to the main-clock oscillation circuit. Perform careful evalvation at the system design level before using.
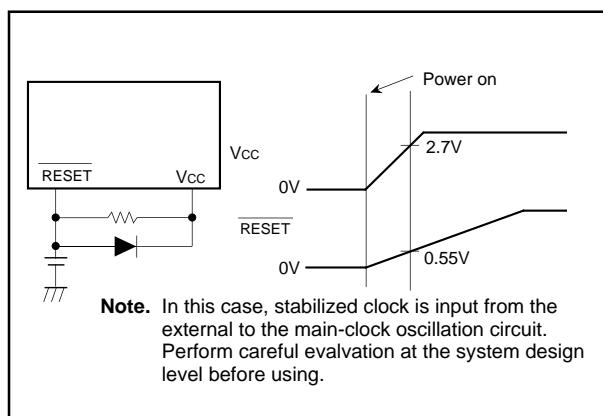
Fig. 4 Example of a reset circuit

Register	Address	Reset value
Port P0 direction register	(04_{16})	00_{16}
Port P1 direction register	(05_{16})	00_{16}
Port P2 direction register	(08_{16})	00_{16}
Port P3 direction register	(09_{16})	×××× 0 0 0 0
Port P4 direction register	$(0C_{16})$	00_{16}
Port P5 direction register	$(0D_{16})$	00_{16}
Port P6 direction register	(10_{16})	00_{16}
Port P7 direction register	(11_{16})	00_{16}
Port P8 direction register	(14_{16})	00_{16}
A-D control register 0	$(1E_{16})$	0 0 0 0 0 ? ? ?
A-D control register 1	$(1F_{16})$	× 0 0 0 × 1 1
UART 0 transmit/receive mode register	(30_{16})	00_{16}
UART 1 transmit/receive mode register	(38_{16})	00_{16}
UART 0 transmit/receive control register 0	(34_{16})	0 0 0 0 1 0 0 0
UART 1 transmit/receive control register 0	$(3C_{16})$	0 0 0 0 1 0 0 0
UART 0 transmit/receive control register 1	(35_{16})	0 0 0 0 0 0 1 0
UART 1 transmit/receive control register 1	$(3D_{16})$	0 0 0 0 0 0 1 0
Count start flag	(40_{16})	00_{16}
One-shot start flag	(42_{16})	××× 0 0 0 0 0
Up-down flag	(44_{16})	00_{16}
Timer A0 mode register	(56_{16})	00_{16}
Timer A1 mode register	(57_{16})	00_{16}
Timer A2 mode register	(58_{16})	00_{16}
Timer A3 mode register	(59_{16})	00_{16}
Timer A4 mode register	$(5A_{16})$	00_{16}
Timer B0 mode register	$(5B_{16})$	0 0 1 0 0 0 0 0
Timer B1 mode register	$(5C_{16})$	0 0 1 × 0 0 0 0
Timer B2 mode register	$(5D_{16})$	0 0 1 × 0 0 0 0
Processor mode register 0	$(5E_{16})$	00_{16}
Processor mode register 1	$(5F_{16})$	××××××× 0
Watchdog timer register	(60_{16})	FFF_{16}
Watchdog timer frequency selection flag	(61_{16})	××××××× 0
Memory allocation control register	(63_{16})	×× 0 0 0 0
UART2 transmit/receive mode register	(64_{16})	× 0 0 0 0 0 0
UART2 transmit/receive control register 0	(68_{16})	×××× 1 0 0 0
UART2 transmit/receive control register 1	(69_{16})	0 0 0 0 0 0 1 0
Oscillation circuit control register 0	$(6C_{16})$	0 0 0 0 0 × 1
Port function control register	$(6D_{16})$	00_{16}
Serial transmit control register	$(6E_{16})$	×× 0 0 ××××
Oscillation circuit control register 1	$(6F_{16})$	0 × 0 1 0 0 0
A-D/UART2 trans./rece. interrupt control register	(70_{16})	×××× 0 0 0 0
UART 0 transmission interrupt control register	(71_{16})	×××× 0 0 0 0
UART 0 receive interrupt control register	(72_{16})	×××× 0 0 0 0
UART 1 transmission interrupt control register	(73_{16})	×××× 0 0 0 0
UART 1 receive interrupt control register	(74_{16})	×××× 0 0 0 0
Timer A0 interrupt control register	(75_{16})	×××× 0 0 0 0
Timer A1 interrupt control register	(76_{16})	×××× 0 0 0 0
Timer A2 interrupt control register	(77_{16})	×××× 0 0 0 0
Timer A3 interrupt control register	(78_{16})	×××× 0 0 0 0
Timer A4 interrupt control register	(79_{16})	×××× 0 0 0 0
Timer B0 interrupt control register	$(7A_{16})$	×××× 0 0 0 0
Timer B1 interrupt control register	$(7B_{16})$	×××× 0 0 0 0
Timer B2 interrupt control register	$(7C_{16})$	×××× 0 0 0 0
$\overline{INT0}$ interrupt control register	$(7D_{16})$	×× 0 0 0 0 0
$\overline{INT1}$ interrupt control register	$(7E_{16})$	×× 0 0 0 0 0
$\overline{INT2}$/Key input interrupt control register	$(7F_{16})$	×× 0 0 0 0 0
Processor status register (PS)		0 0 0 ? ? 0 0 0 1 ? ?
Program bank register (PG)		00_{16}
Program counter (PCH)		Content of $FFFF_{16}$
Program counter (PCL)		Content of $FFFE_{16}$
Direct page register (DPR)		0000_{16}
Data bank register (DT)		00_{16}

Contents of other registers and RAM are undefined during reset. Initialize them by software.

Fig. 3 Microcomputer internal status during reset

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EPROM MODE

The M37735EHLXXXHP features an EPROM mode in addition to its normal modes. When the RESET signal level is "L", the chip automatically enters the EPROM mode. Table 2 lists the correspondence between pins and Figure 5 shows the pin connections in the EPROM mode.

The EPROM mode is the 1M mode for the EPROM that is equivalent to the M5M27C101K.

When in the EPROM mode, ports P0, P1, P2, $P3_0$, $P5_0$, $P5_1$, $P5_2$, CNVss and BYTE are used for the EPROM (equivalent to the M5M27C101K). When in this mode, the built-in PROM can be programmed or read from using these pins in the same way as with the M5M27C101K.

This chip does not have Device Identifier Mode, so that set the corresponding program algorithm. The program area should specify

address 0100_{16} – $1FFFF_{16}$.

Connect the clock which is either ceramic resonator or external clock to X_{IN} pin and X_{OUT} pin.

Table 2. Pin function in EPROM mode

	M37735EHLXXXHP	M5M27C101K
Vcc	Vcc	Vcc
Vpp	CNVss, BYTE	Vpp
Vss	Vss	Vss
Address input	Ports P0, P1, $P3_0$	$A_0 - A_{16}$
Data I/O	Port P2	$D_0 - D_7$
$\overline{CE}$	$P5_2$	$\overline{CE}$
$\overline{OE}$	$P5_1$	$\overline{OE}$
$\overline{PGM}$	$P5_0$	$\overline{PGM}$

Outline 80P6D-A, 80P6Q-A

∗ : Connect to ceramic oscillation circuit.
⬭ : It is used in the EPROM mode.
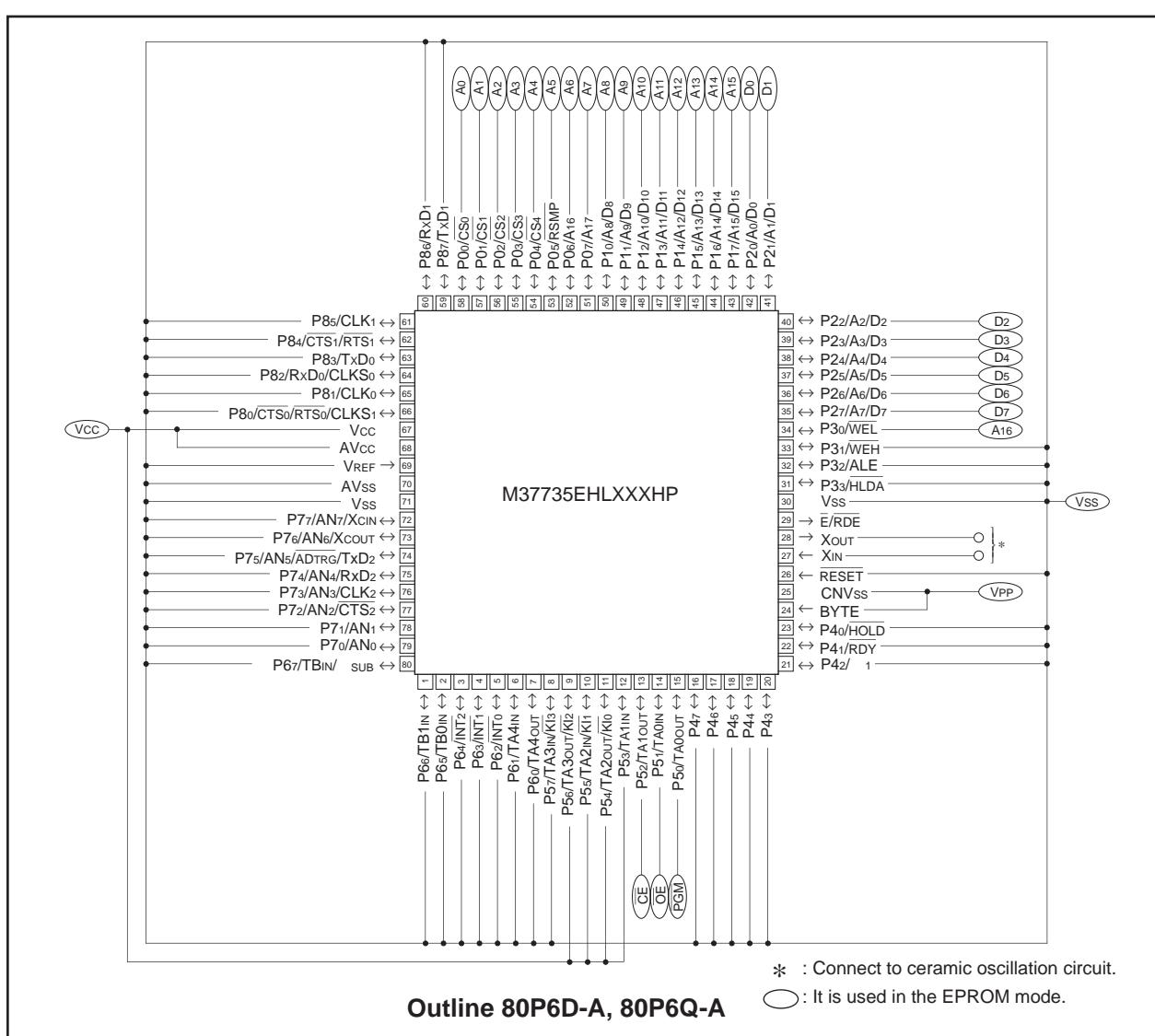
Fig. 5 Pin connection in EPROM mode

FUNCTION IN EPROM MODE
1M mode (equivalent to the M5M27C101K)

Reading

To read the EPROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level. Input the address of the data (A_0 – A_{16}) to be read, and the data will be output to the I/O pins D_0 – D_7. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pins are in the "H" state.

Programming

Programming must be performed in 8 bits by a byte program. To program to the EPROM, set the $\overline{CE}$ pin to a "L" level and the $\overline{OE}$ pin to a "H" level. The CPU will enter the programming mode when 12.5 V is applied to the V_{PP} pin. The address to be programmed to is selected with pins A_0 – A_{16}, and the data to be programmed is input to pins D_0 – D_7. Set the $\overline{PGM}$ pin to a "L" level to being programming.

Programming operation

To program the M37735EHLXXXHP, first set V_{CC} = 6 V, V_{PP} = 12.5 V, and set the address to 01000_{16}. Apply a 0.2 ms programming pulse, check that the data can be read, and if it cannot be read OK, repeat the procedure, applying a 0.2 ms programming pulse and checking that the data can be read until it can be read OK. Record the accumulated number of pulse applied (X) before the data can be read OK, and then write the data again, applying a further once this number of pulses (0.2 ✕ X ms).

When this series of programming operations is complete, increment the address, and continue to repeat the procedure above until the last address has been reached.

Finally, when all addresses have been programmed, read with V_{CC} = V_{PP} = 5 V (or V_{CC} = V_{PP} = 5.5 V).

Table 3. I/O signal in each mode

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Data I/O
Read-out	V_{IL}	V_{IL}	X	5 V	5 V	Output
Output	V_{IL}	V_{IH}	X	5 V	5 V	Floating
Disable	V_{IH}	X	X	5 V	5 V	Floating
Programming	V_{IL}	V_{IH}	V_{IL}	12.5 V	6 V	Input
Programming Verify	V_{IL}	V_{IL}	V_{IH}	12.5 V	6 V	Output
Program Disable	V_{IH}	V_{IH}	V_{IH}	12.5 V	6 V	Floating

Note 1 : An X indicates either V_{IL} or V_{IH}.

Programming operation (equivalent to the M5M27C101K)

AC ELECTRICAL CHARACTERISTICS (Ta = 25 ± 5 °C, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 ± 0.3 V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
t_{AS}	Address setup time		2			µs
t_{OES}	$\overline{OE}$ setup time		2			µs
t_{DS}	Data setup time		2			µs
t_{AH}	Address hold time		0			µs
t_{DH}	Data hold time		2			µs
t_{DFP}	Output enable to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			µs
t_{VPS}	V_{PP} setup time		2			µs
t_{PW}	$\overline{PGM}$ pulse width		0.19	0.2	0.21	ms
t_{OPW}	$\overline{PGM}$ over program pulse width		0.19		5.25	ms
t_{CES}	$\overline{CE}$ setup time		2			µs
t_{OE}	Data valid from $\overline{OE}$				150	ns

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AC waveforms
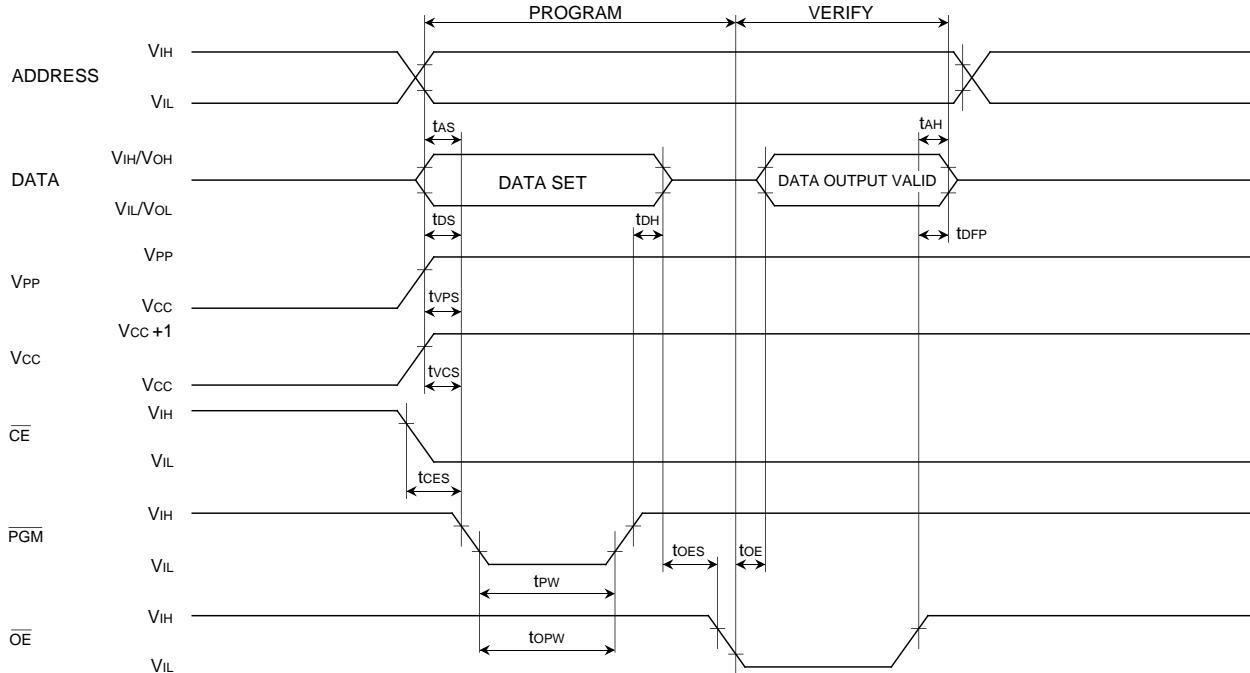
Test conditions for A.C. characteristics
Input voltage : V_{IL} = 0.45 V, V_{IH} = 2.4 V
Input rise and fall times (10 % – 90 %) : ≤ 20 ns
Reference voltage at timing measurement : Input, Output
"L" = 0.8 V, "H" = 2 V

Programming algorithm flow chart

*4.5 V ≤ V_{CC} = V_{PP} ≤ 5.5 V

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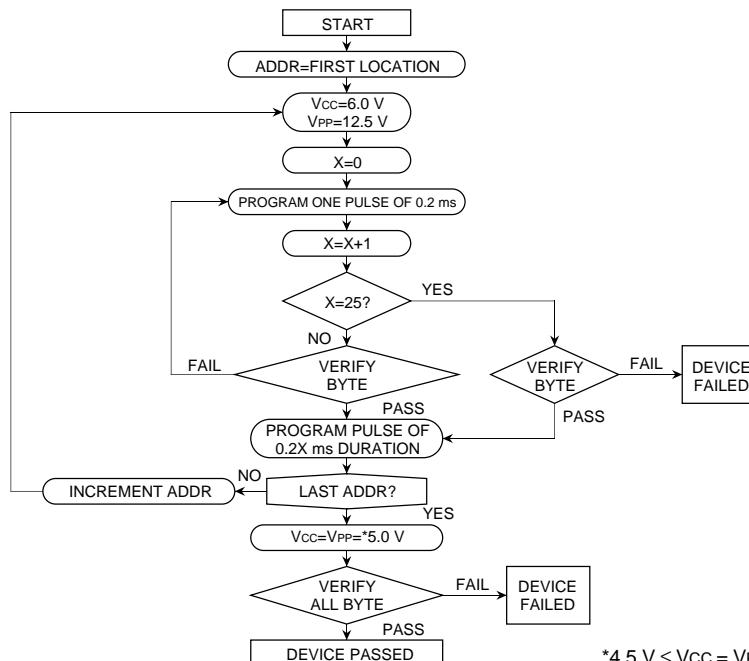
SAFETY INSTRUCTIONS

(1) A high voltage is used for programming. Take care that over-voltage is not applied. Take care especially at power on.

(2) The programmable M37735EHLHP that is shipped in blank is also provided. For the M37735EHLHP, Mitsubishi Electric corp. does not perform PROM programming test and screening following the assembly processes. To improve reliability after programming, performing programming and test according to the flow below before use is recommended.

```
┌─────────────────────────────────────┐
│  Programming with PROM programmer    │
└─────────────────────────────────────┘
                    ⇓
┌─────────────────────────────────────┐
│  Screening          (Caution)        │
│  (Leave at 150 °C for 40 hours)      │
└─────────────────────────────────────┘
                    ⇓
┌─────────────────────────────────────┐
│  Verify test with PROM programmer    │
└─────────────────────────────────────┘
                    ⇓
┌ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ┐
   Function check in target device
└ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ┘
```
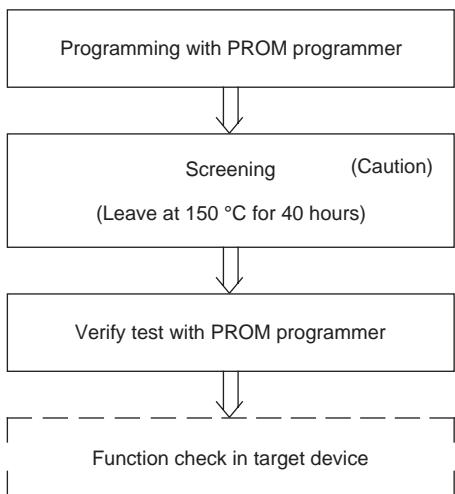
Caution : Never expose to 150 °C exceeding 100 hours.

ADDRESSING MODES

The M37735EHLXXXHP has 28 powerful addressing modes. Refer to the "7700 Family Software Manual" for the details.

MACHINE INSTRUCTION LIST

The M37735EHLXXXHP has 103 machine instructions. Refer to the "7700 Family Software Manual" for the details.

DATA REQUIRED FOR PROM ORDERING

Please send the following data for writing to PROM.
(1) M37735EHLXXXHP writing to PROM order confirmation form
(2) 80P6D, 80P6Q mark specification form
(3) ROM data (EPROM 3 sets)

MITSUBISHI ELECTRIC

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage		−0.3 to +7	V
AV_{CC}	Analog power source voltage		−0.3 to +7	V
V_I	Input voltage $\overline{RESET}$, CNVss, BYTE		−0.3 to +12 (Note)	V
V_I	Input voltage P0$_0$ – P0$_7$, P1$_0$ – P1$_7$, P2$_0$ – P2$_7$, P3$_0$ – P3$_3$, P4$_0$ – P4$_7$, P5$_0$ – P5$_7$, P6$_0$ – P6$_7$, P7$_0$ – P7$_7$, P8$_0$ – P8$_7$, V$_{REF}$, X$_{IN}$		−0.3 to Vcc + 0.3	V
V_O	Output voltage P0$_0$ – P0$_7$, P1$_0$ – P1$_7$, P2$_0$ – P2$_7$, P3$_0$ – P3$_3$, P4$_0$ – P4$_7$, P5$_0$ – P5$_7$, P6$_0$ – P6$_7$, P7$_0$ – P7$_7$, P8$_0$ – P8$_7$, X$_{OUT}$, $\overline{E}$		−0.3 to Vcc + 0.3	V
P_d	Power dissipation	Ta = 25 °C	200	mW
T_{opr}	Operating temperature		−40 to +85	°C
T_{stg}	Storage temperature		−65 to +150	°C

Note. When the EPROM is programmed, input voltage of pins CNVss and BYTE is 13 V respectively.

RECOMMENDED OPERATING CONDITIONS (Vcc = 2.7 – 5.5 V, Ta = −40 to +85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage	f(X$_{IN}$) : Operating	2.7		5.5	V
		f(X$_{IN}$) : Stopped, f(X$_{CIN}$) = 32.768 kHz	2.7		5.5	
AV_{CC}	Analog power source voltage			Vcc		V
V_{SS}	Power source voltage			0		V
AV_{SS}	Analog power source voltage			0		V
V_{IH}	High-level input voltage P0$_0$ – P0$_7$, P3$_0$ – P3$_3$, P4$_0$ – P4$_7$, P5$_0$ – P5$_7$, P6$_0$ – P6$_7$, P7$_0$ – P7$_7$, P8$_0$ – P8$_7$, X$_{IN}$, $\overline{RESET}$, CNVss, BYTE, X$_{CIN}$ (Note 3)		0.8 Vcc		Vcc	V
V_{IH}	High-level input voltage P1$_0$ – P1$_7$, P2$_0$ – P2$_7$ (in single-chip mode)		0.8 Vcc		Vcc	V
V_{IH}	High-level input voltage P1$_0$ – P1$_7$, P2$_0$ – P2$_7$ (in memory expansion mode and microprocessor mode)		0.5 Vcc		Vcc	V
V_{IL}	Low-level input voltage P0$_0$ – P0$_7$, P3$_0$ – P3$_3$, P4$_0$ – P4$_7$, P5$_0$ – P5$_7$, P6$_0$ – P6$_7$, P7$_0$ – P7$_7$, P8$_0$ – P8$_7$, X$_{IN}$, $\overline{RESET}$, CNVss, BYTE, X$_{CIN}$ (Note 3)		0		0.2Vcc	V
V_{IL}	Low-level input voltage P1$_0$ – P1$_7$, P2$_0$ – P2$_7$ (in single-chip mode)		0		0.2Vcc	V
V_{IL}	Low-level input voltage P1$_0$ – P1$_7$, P2$_0$ – P2$_7$ (in memory expansion mode and microprocessor mode)		0		0.16Vcc	V
$I_{OH(peak)}$	High-level peak output current P0$_0$ – P0$_7$, P1$_0$ – P1$_7$, P2$_0$ – P2$_7$, P3$_0$ – P3$_3$, P4$_0$ – P4$_7$, P5$_0$ – P5$_7$, P6$_0$ – P6$_7$, P7$_0$ – P7$_7$, P8$_0$ – P8$_7$				−10	mA
$I_{OH(avg)}$	High-level average output current P0$_0$ – P0$_7$, P1$_0$ – P1$_7$, P2$_0$ – P2$_7$, P3$_0$ – P3$_3$, P4$_0$ – P4$_7$, P5$_0$ – P5$_7$, P6$_0$ – P6$_7$, P7$_0$ – P7$_7$, P8$_0$ – P8$_7$				−5	mA
$I_{OL(peak)}$	Low-level peak output current P0$_0$ – P0$_7$, P1$_0$ – P1$_7$, P2$_0$ – P2$_7$, P3$_0$ – P3$_3$, P4$_0$ – P4$_3$, P5$_4$ – P5$_7$, P6$_0$ – P6$_7$, P7$_0$ – P7$_7$, P8$_0$ – P8$_7$				10	mA
$I_{OL(peak)}$	Low-level peak output current P4$_4$ – P4$_7$, P5$_0$ – P5$_3$				16	mA
$I_{OL(avg)}$	Low-level average output current P0$_0$ – P0$_7$, P1$_0$ – P1$_7$, P2$_0$ – P2$_7$, P3$_0$ – P3$_3$, P4$_0$ – P4$_3$, P5$_4$ – P5$_7$, P6$_0$ – P6$_7$, P7$_0$ – P7$_7$, P8$_0$ – P8$_7$				5	mA
$I_{OL(avg)}$	Low-level average output current P4$_4$ – P4$_7$, P5$_0$ – P5$_3$				12	mA
f(X$_{IN}$)	Main-clock oscillation frequency (Note 4)				12	MHz
f(X$_{CIN}$)	Sub-clock oscillation frequency			32.768	50	kHz

Notes 1. Average output current is the average value of a 100 ms interval.

2. The sum of I$_{OL(peak)}$ for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of I$_{OH(peak)}$ for ports P0, P1, P2, P3, and P8 must be 80 mA or less, the sum of I$_{OL(peak)}$ for ports P4, P5, P6, and P7 must be 100 mA or less, and the sum of I$_{OH(peak)}$ for ports P4, P5, P6, and P7 must be 80 mA or less.

3. Limits V$_{IH}$ and V$_{IL}$ for X$_{CIN}$ are applied when the sub clock external input selection bit = "1".

4. The maximum value of f(X$_{IN}$) = 6 MHz when the main clock division selection bit = "1".

ELECTRICAL CHARACTERISTICS (Vcc = 5 V, Vss = 0 V, Ta = –40 to +85 °C, f(X$_{IN}$) = 12 MHz, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
V$_{OH}$	High-level output voltage P0$_0$ – P0$_7$, P1$_0$ – P1$_7$, P2$_0$ – P2$_7$, P3$_3$, P4$_0$ – P4$_7$, P5$_0$ – P5$_7$, P6$_0$ – P6$_7$, P7$_0$ – P7$_7$, P8$_0$ – P8$_7$	V$_{CC}$ = 5 V, I$_{OH}$ = –10 mA		3			V
		V$_{CC}$ = 3 V, I$_{OH}$ = –1 mA		2.5			
V$_{OH}$	High-level output voltage P0$_0$ – P0$_7$, P1$_0$ – P1$_7$, P2$_0$ – P2$_7$, P3$_3$	V$_{CC}$ = 5 V, I$_{OH}$ = –400 µA		4.7			V
V$_{OH}$	High-level output voltage P3$_0$ – P3$_2$	V$_{CC}$ = 5 V, I$_{OH}$ = –10 mA		3.1			V
		V$_{CC}$ = 5 V, I$_{OH}$ = –400 µA		4.8			
		V$_{CC}$ = 3 V, I$_{OH}$ = –1 mA		2.6			
V$_{OH}$	High-level output voltage Ē	V$_{CC}$ = 5 V, I$_{OH}$ = –10 mA		3.4			V
		V$_{CC}$ = 5 V, I$_{OH}$ = –400 µA		4.8			
		V$_{CC}$ = 3 V, I$_{OH}$ = –1 mA		2.6			
V$_{OL}$	Low-level output voltage P0$_0$ – P0$_7$, P1$_0$ – P1$_7$, P2$_0$ – P2$_7$, P3$_3$, P4$_0$ – P4$_3$, P5$_4$ – P5$_7$, P6$_0$ – P6$_7$, P7$_0$ – P7$_7$, P8$_0$ – P8$_7$	V$_{CC}$ = 5 V, I$_{OL}$ = 10 mA				2	V
		V$_{CC}$ = 3 V, I$_{OL}$ = 1 mA				0.5	
V$_{OL}$	Low-level output voltage P4$_4$ – P4$_7$, P5$_0$ – P5$_3$	V$_{CC}$ = 5 V, I$_{OL}$ = 16 mA				1.8	V
		V$_{CC}$ = 3 V, I$_{OL}$ = 10 mA				1.5	
V$_{OL}$	Low-level output voltage P0$_0$ – P0$_7$, P1$_0$ – P1$_7$, P2$_0$ – P2$_7$, P3$_3$	V$_{CC}$ = 5 V, I$_{OL}$ = 2 mA				0.45	V
V$_{OL}$	Low-level output voltage P3$_0$ – P3$_2$	V$_{CC}$ = 5 V, I$_{OL}$ = 10 mA				1.9	V
		V$_{CC}$ = 5 V, I$_{OL}$ = 2 mA				0.43	
		V$_{CC}$ = 3 V, I$_{OL}$ = 1 mA				0.4	
V$_{OL}$	Low-level output voltage Ē	V$_{CC}$ = 5 V, I$_{OL}$ = 10 mA				1.6	V
		V$_{CC}$ = 5 V, I$_{OL}$ = 2 mA				0.4	
		V$_{CC}$ = 3 V, I$_{OL}$ = 1 mA				0.4	
V$_{T+}$ – V$_{T-}$	Hysteresis $\overline{HOLD}$, $\overline{RDY}$, TA0$_{IN}$ – TA4$_{IN}$, TB0$_{IN}$ – TB2$_{IN}$, $\overline{INT_0}$ – $\overline{INT_2}$, $\overline{AD_{TRG}}$, $\overline{CTS_0}$, CTS$_1$, CTS$_2$, CLK$_0$, CLK$_1$, CLK$_2$, $\overline{KI_0}$ – $\overline{KI_3}$	V$_{CC}$ = 5 V		0.4		1	V
		V$_{CC}$ = 3 V		0.1		0.7	
V$_{T+}$ – V$_{T-}$	Hysteresis $\overline{RESET}$	V$_{CC}$ = 5 V		0.2		0.5	V
		V$_{CC}$ = 3 V		0.1		0.4	
V$_{T+}$ – V$_{T-}$	Hysteresis X$_{IN}$	V$_{CC}$ = 5 V		0.1		0.4	V
		V$_{CC}$ = 3 V		0.06		0.26	
V$_{T+}$ – V$_{T-}$	Hysteresis X$_{CIN}$ (When external clock is input)	V$_{CC}$ = 5 V		0.1		0.4	V
		V$_{CC}$ = 3 V		0.06		0.26	
I$_{IH}$	High-level input current P0$_0$ – P0$_7$, P1$_0$ – P1$_7$, P2$_0$ – P2$_7$, P3$_0$ – P3$_3$, P4$_0$ – P4$_7$, P5$_0$ – P5$_7$, P6$_0$ – P6$_7$, P7$_0$ – P7$_7$, P8$_0$ – P8$_7$, X$_{IN}$, $\overline{RESET}$, CNV$_{SS}$, BYTE	V$_{CC}$ = 5 V, V$_I$ = 5 V				5	µA
		V$_{CC}$ = 3 V, V$_I$ = 3 V				4	
I$_{IL}$	Low-level input current P0$_0$ – P0$_7$, P1$_0$ – P1$_7$, P2$_0$ – P2$_7$, P3$_0$ – P3$_3$, P4$_0$ – P4$_7$, P5$_0$ – P5$_3$, P6$_0$, P6$_1$, P6$_5$ – P6$_7$, P7$_0$ – P7$_7$, P8$_0$ – P8$_7$, X$_{IN}$, $\overline{RESET}$, CNV$_{SS}$, BYTE	V$_{CC}$ = 5 V, V$_I$ = 0 V				–5	µA
		V$_{CC}$ = 3 V, V$_I$ = 0 V				–4	
I$_{IL}$	Low-level input current P5$_4$ – P5$_7$, P6$_2$ – P6$_4$	V$_I$ = 0 V, without a pull-up transistor	V$_{CC}$ = 5 V			–5	µA
			V$_{CC}$ = 3 V			–4	
		V$_I$ = 0 V, with a pull-up transistor	V$_{CC}$ = 5 V	–0.25	–0.5	–1.0	mA
			V$_{CC}$ = 3 V	–0.08	–0.18	–0.35	
V$_{RAM}$	RAM hold voltage	When clock is stopped.		2			V

MITSUBISHI ELECTRIC

ELECTRICAL CHARACTERISTICS (Vcc = 5 V, Vss = 0 V, Ta = −40 to +85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
Icc	Power source current	When single-chip mode, output pins are open, and other pins are Vss.	Vcc = 5 V, f(Xin) = 12 MHz (square waveform), (f(f2) = 6 MHz), f(Xcin) = 32.768 kHz, in operating (Note 1)		4.5	9	mA
			Vcc = 3 V, f(Xin) = 12 MHz (square waveform), (f(f2) = 6 MHz), f(Xcin) = 32.768 kHz, in operating (Note 1)		3	6	mA
			Vcc = 3 V, f(Xin) = 12 MHz (square waveform), (f(f2) = 0.75 MHz), f(Xcin) : Stopped, in operating		0.4	0.8	mA
			Vcc = 3 V, f(Xin) = 12 MHz (square waveform), f(Xcin) = 32.768 kHz, when a WIT instruction is executed (Note 2)		6	12	µA
			Vcc = 3 V, f(Xin) : Stopped, f(Xcin) = 32.768 kHz, in operating (Note 3)		30	60	µA
			Vcc = 3 V, f(Xin) : Stopped, f(Xcin) = 32.768 kHz, when a WIT instruction is executed (Note 4)		3	6	µA
			Ta = 25 °C, when clock is stopped			1	µA
			Ta = 85 °C, when clock is stopped			20	µA

Notes 1. This applies when the main clock external input selection bit = "1", the main clock division selection bit = "0", and the signal output stop bit = "1".

    2. This applies when the main clock external input selection bit = "1" and the system clock stop bit at wait state = "1".

    3. This applies when CPU and the clock timer are operating with the sub clock (32.768 kHz) selected as the system clock.

    4. This applies when the Xcout drivability selection bit = "0" and the system clock stop bit at wait state = "1".

A–D CONVERTER CHARACTERISTICS

(Vcc = AVcc = 5 V, Vss = AVss = 0 V, Ta = −40 to +85 °C, f(Xin) = 12 MHz, unless otherwise noted (Note))

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	Vref = Vcc			10	Bits
—	Absolute accuracy	Vref = Vcc			± 3	LSB
Rladder	Ladder resistance	Vref = Vcc	10		25	kΩ
tconv	Conversion time		19.6			µs
Vref	Reference voltage		2.7		Vcc	V
Via	Analog input voltage		0		Vref	V

Note. This applies when the main clock division selection bit = "0" and f(f2) = 6 MHz.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

TIMING REQUIREMENTS (V_{CC} = 2.7 – 5.5 V, V_{SS} = 0 V, Ta = –40 to +85 °C, f(X_{IN}) = 12 MHz, unless otherwise noted (Note 1))

Notes 1. This applies when the main clock division selection bit = "0" and f(f_2) = 6 MHz.

    2. Input signal's rise/fall time must be 100 ns or less, unless otherwise noted.

External clock input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_c	External clock input cycle time (Note 3)	83		ns
$t_{w(H)}$	External clock input high-level pulse width (Note 4)	33		ns
$t_{w(L)}$	External clock input low-level pulse width (Note 4)	33		ns
t_r	External clock rise time		15	ns
t_f	External clock fall time		15	ns

Notes 3. When the main clock division selection bit = "1", the minimum value of t_c = 166 ns.

    4. When the main clock division selection bit = "1", values of $t_{w(H)}$ / t_c and $t_{w(L)}$ / t_c must be set to values from 0.45 through 0.55.

Single-chip mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(P0D–E)}$	Port P0 input setup time	200		ns
$t_{su(P1D–E)}$	Port P1 input setup time	200		ns
$t_{su(P2D–E)}$	Port P2 input setup time	200		ns
$t_{su(P3D–E)}$	Port P3 input setup time	200		ns
$t_{su(P4D–E)}$	Port P4 input setup time	200		ns
$t_{su(P5D–E)}$	Port P5 input setup time	200		ns
$t_{su(P6D–E)}$	Port P6 input setup time	200		ns
$t_{su(P7D–E)}$	Port P7 input setup time	200		ns
$t_{su(P8D–E)}$	Port P8 input setup time	200		ns
$t_{h(E–P0D)}$	Port P0 input hold time	0		ns
$t_{h(E–P1D)}$	Port P1 input hold time	0		ns
$t_{h(E–P2D)}$	Port P2 input hold time	0		ns
$t_{h(E–P3D)}$	Port P3 input hold time	0		ns
$t_{h(E–P4D)}$	Port P4 input hold time	0		ns
$t_{h(E–P5D)}$	Port P5 input hold time	0		ns
$t_{h(E–P6D)}$	Port P6 input hold time	0		ns
$t_{h(E–P7D)}$	Port P7 input hold time	0		ns
$t_{h(E–P8D)}$	Port P8 input hold time	0		ns

Memory expansion mode and microprocessor mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{su(D–RDE)}$	Data input setup time	50		ns
$t_{su(RDY–\phi1)}$	RDY input setup time	80		ns
$t_{su(HOLD–\phi1)}$	HOLD input setup time	80		ns
$t_{h(RDE–D)}$	Data input hold time	0		ns
$t_{h(\phi1–RDY)}$	RDY input hold time	0		ns
$t_{h(\phi1–HOLD)}$	HOLD input hold time	0		ns

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PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Timer A input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time	250		ns
tw(TAH)	TAiIN input high-level pulse width	125		ns
tw(TAL)	TAiIN input low-level pulse width	125		ns

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time (Note)	666		ns
tw(TAH)	TAiIN input high-level pulse width (Note)	333		ns
tw(TAL)	TAiIN input low-level pulse width (Note)	333		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS" on page 19.

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tc(TA)	TAiIN input cycle time (Note)	666		ns
tw(TAH)	TAiIN input high-level pulse width	166		ns
tw(TAL)	TAiIN input low-level pulse width	166		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS" on page 19.

Timer A input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tw(TAH)	TAiIN input high-level pulse width	166		ns
tw(TAL)	TAiIN input low-level pulse width	166		ns

Timer A input (Up-down input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tc(UP)	TAiOUT input cycle time	3333		ns
tw(UPH)	TAiOUT input high-level pulse width	1666		ns
tw(UPL)	TAiOUT input low-level pulse width	1666		ns
tsu(UP–TiN)	TAiOUT input setup time	666		ns
th(TiN–UP)	TAiOUT input hold time	666		ns

Timer A input (Two-phase pulse input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tc(TA)	TAjIN input cycle time	2000		ns
tsu(TAjIN–TAjOUT)	TAjIN input setup time	500		ns
tsu(TAjOUT–TAjIN)	TAjOUT input setup time	500		ns

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Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_c(TB)$	TBiIN input cycle time (one edge count)	250		ns
$t_w(TBH)$	TBiIN input high-level pulse width (one edge count)	125		ns
$t_w(TBL)$	TBiIN input low-level pulse width (one edge count)	125		ns
$t_c(TB)$	TBiIN input cycle time (both edges count)	500		ns
$t_w(TBH)$	TBiIN input high-level pulse width (both edges count)	250		ns
$t_w(TBL)$	TBiIN input low-level pulse width (both edges count)	250		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_c(TB)$	TBiIN input cycle time (Note)	666		ns
$t_w(TBH)$	TBiIN input high-level pulse width (Note)	333		ns
$t_w(TBL)$	TBiIN input low-level pulse width (Note)	333		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS" on page 19.

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_c(TB)$	TBiIN input cycle time (Note)	666		ns
$t_w(TBH)$	TBiIN input high-level pulse width (Note)	333		ns
$t_w(TBL)$	TBiIN input low-level pulse width (Note)	333		ns

Note. Limits change depending on $f(X_{IN})$. Refer to "DATA FORMULAS" on page 19.

A-D trigger input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_c(AD)$	$\overline{AD}_{TRG}$ input cycle time (minimum allowable trigger)	1333		ns
$t_w(ADL)$	$\overline{AD}_{TRG}$ input low-level pulse width	166		ns

Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_c(CK)$	CLKi input cycle time	333		ns
$t_w(CKH)$	CLKi input high-level pulse width	166		ns
$t_w(CKL)$	CLKi input low-level pulse width	166		ns
$t_d(C–Q)$	TxDi output delay time		100	ns
$t_h(C–Q)$	TxDi hold time	0		ns
$t_{su}(D–C)$	RxDi input setup time	65		ns
$t_h(C–D)$	RxDi input hold time	75		ns

External interrupt $\overline{INT}$i input, key input interrupt $\overline{KI}$i input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_w(INH)$	$\overline{INT}$i input high-level pulse width	250		ns
$t_w(INL)$	$\overline{INT}$i input low-level pulse width	250		ns
$t_w(KIL)$	$\overline{KI}$i input low-level pulse width	250		ns

MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

DATA FORMULAS

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TA_{iIN} input cycle time	$\dfrac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TAH)}$	TA_{iIN} input high-level pulse width	$\dfrac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TAL)}$	TA_{iIN} input low-level pulse width	$\dfrac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TA)}$	TA_{iIN} input cycle time	$\dfrac{8 \times 10^9}{2 \cdot f(f_2)}$		ns

Timer B input (In pulse period measurement mode or pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{c(TB)}$	TB_{iIN} input cycle time	$\dfrac{8 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TBH)}$	TB_{iIN} input high-level pulse width	$\dfrac{4 \times 10^9}{2 \cdot f(f_2)}$		ns
$t_{w(TBL)}$	TB_{iIN} input low-level pulse width	$\dfrac{4 \times 10^9}{2 \cdot f(f_2)}$		ns

Note. $f(f_2)$ represents the clock f_2 frequency.
For the relation to the main clock and sub clock, refer to Table 10 in data sheet "M37735MHBXXXFP".

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

SWITCHING CHARACTERISTICS

(Vcc = 2.7 – 5.5 V, Vss = 0 V, Ta = −40 to +85°C, f(XiN) = 12 MHz, unless otherwise noted (Note))

Single-chip mode

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
td(E−P0Q)	Port P0 data output delay time			300	ns
td(E−P1Q)	Port P1 data output delay time			300	ns
td(E−P2Q)	Port P2 data output delay time			300	ns
td(E−P3Q)	Port P3 data output delay time			300	ns
td(E−P4Q)	Port P4 data output delay time	Fig. 6		300	ns
td(E−P5Q)	Port P5 data output delay time			300	ns
td(E−P6Q)	Port P6 data output delay time			300	ns
td(E−P7Q)	Port P7 data output delay time			300	ns
td(E−P8Q)	Port P8 data output delay time			300	ns

Note. This applies when the main clock division selection bit = "0" and f(f2) = 6 MHz.
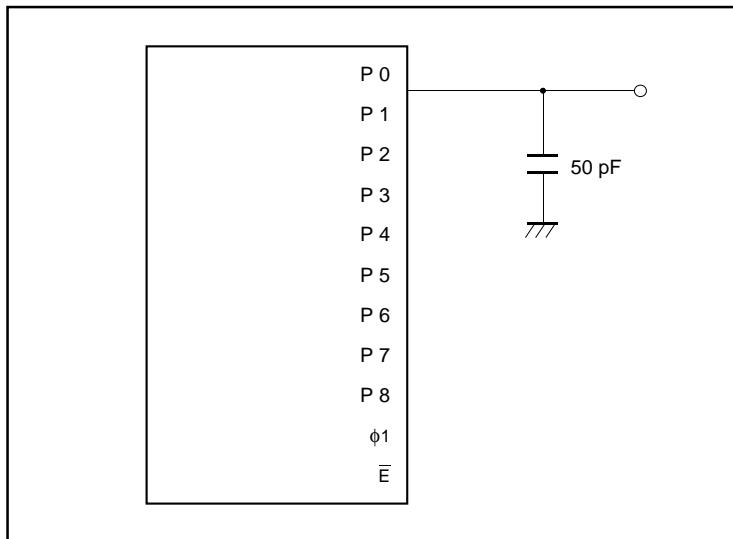
Fig. 6 Measuring circuit for ports P0 – P8 and φ1

MITSUBISHI ELECTRIC

Memory expansion mode and microprocessor mode

(Vcc = 2.7 – 5.5 V, Vss = 0 V, Ta = –40 to +85 °C, f(XIN) = 12 MHz, unless otherwise noted (Note 1))

Symbol	Parameter	(Note 2) Wait mode	Test conditions	Limits Min.	Limits Max.	Unit
td(CS–WE) td(CS–RDE)	Chip-select output delay time	No wait Wait 1		20		ns
		Wait 0		182		ns
th(WE–CS) th(RDE–CS)	Chip-select hold time			4		ns
td(An–WE) td(An–RDE)	Address output delay time	No wait Wait 1		20		ns
		Wait 0		182		ns
td(A–WE) td(A–RDE)	Address output delay time	No wait Wait 1		20		ns
		Wait 0		162		ns
th(WE–An) th(RDE–An)	Address hold time			40		ns
tw(ALE)	ALE pulse width	No wait Wait 1		40		ns
		Wait 0		123		ns
tsu(A–ALE)	Address output setup time	No wait Wait 1	Fig. 6	10		ns
		Wait 0		93		ns
th(ALE–A)	Address hold time	No wait Wait 1		9		ns
		Wait 0		40		ns
td(ALE–WE) td(ALE–RDE)	ALE output delay time	No wait Wait 1		4		ns
		Wait 0		40		ns
td(WE–DQ)	Data output delay time				90	ns
th(WE–DQ)	Data hold time			40		ns
tw(WE)	WEL/WEH pulse width	No wait		131		ns
		Wait 1 Wait 0		298		ns
tpxz(RDE–DZ)	Floating start delay time				10	ns
tpzx(RDE–DZ)	Floating release delay time			53		ns
tw(RDE)	RDE pulse width	No wait		128		ns
		Wait 1 Wait 0		295		ns
td(RSMP–WE) td(RSMP–RDE)	RSMP output delay time			25		ns
th(φ1–RSMP)	RSMP hold time			0		ns
td(WE–φ1) td(RDE–φ1)	φ1 output delay time			0	30	ns
td(φ1–HLDA)	HLDA output delay time				120	ns

Notes 1. This applies when the main clock division selection bit = "0" and f(f2) = 6 MHz.

　　2. No wait : Wait bit = "1".

　　　Wait 1 : The external memory area is accessed with wait bit = "0" and wait selection bit = "1".

　　　Wait 0 : The external memory area is accessed with wait bit = "0" and wait selection bit = "0".

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Bus timing data formulas (Vcc = 2.7 – 5.5V, Vss = 0 V, Ta = –40 to +85 °C, f(XIN) = 12 MHz (Max.), unless otherwise noted (Note1))

Symbol	Parameter	Wait mode	Min.	Max.	Unit
$t_{d(CS-WE)}$ $t_{d(CS-RDE)}$	Chip-select output delay time	No wait Wait 1	$\dfrac{1 \times 10^9}{2 \cdot f(f_2)} - 63$		ns
		Wait 0	$\dfrac{3 \times 10^9}{2 \cdot f(f_2)} - 68$		ns
$t_{h(WE-CS)}$ $t_{h(RDE-CS)}$	Chip-select hold time		4		ns
$t_{d(An-WE)}$ $t_{d(An-RDE)}$	Address output delay time	No wait Wait 1	$\dfrac{1 \times 10^9}{2 \cdot f(f_2)} - 63$		ns
		Wait 0	$\dfrac{3 \times 10^9}{2 \cdot f(f_2)} - 68$		ns
$t_{d(A-WE)}$ $t_{d(A-RDE)}$	Address output delay time	No wait Wait 1	$\dfrac{1 \times 10^9}{2 \cdot f(f_2)} - 63$		ns
		Wait 0	$\dfrac{3 \times 10^9}{2 \cdot f(f_2)} - 88$		ns
$t_{h(WE-An)}$ $t_{h(RDE-An)}$	Address hold time		$\dfrac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
$t_{w(ALE)}$	ALE pulse width	No wait Wait 1	$\dfrac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
		Wait 0	$\dfrac{2 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
$t_{su(A-ALE)}$	Address output setup time	No wait Wait 1	$\dfrac{1 \times 10^9}{2 \cdot f(f_2)} - 73$		ns
		Wait 0	$\dfrac{2 \times 10^9}{2 \cdot f(f_2)} - 73$		ns
$t_{h(ALE-A)}$	Address hold time	No wait Wait 1	9		ns
		Wait 0	$\dfrac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
$t_{d(ALE-WE)}$ $t_{d(ALE-RDE)}$	ALE output delay time	No wait Wait 1	4		ns
		Wait 0	$\dfrac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
$t_{d(WE-DQ)}$	Data output delay time			90	ns
$t_{h(WE-DQ)}$	Data hold time		$\dfrac{1 \times 10^9}{2 \cdot f(f_2)} - 43$		ns
$t_{w(WE)}$	$\overline{WEL}/\overline{WEH}$ pulse width	No wait	$\dfrac{2 \times 10^9}{2 \cdot f(f_2)} - 35$		ns
		Wait 1 Wait 0	$\dfrac{4 \times 10^9}{2 \cdot f(f_2)} - 35$		ns
$t_{pxz(RDE-DZ)}$	Floating start delay time			10	ns
$t_{pzx(RDE-DZ)}$	Floating release delay time		$\dfrac{1 \times 10^9}{2 \cdot f(f_2)} - 30$		ns
$t_{w(RDE)}$	$\overline{RDE}$ pulse width	No wait	$\dfrac{2 \times 10^9}{2 \cdot f(f_2)} - 38$		ns
		Wait 1 Wait 0	$\dfrac{4 \times 10^9}{2 \cdot f(f_2)} - 38$		ns
$t_{d(RSMP-WE)}$ $t_{d(RSMP-RDE)}$	$\overline{RSMP}$ output delay time		$\dfrac{1 \times 10^9}{2 \cdot f(f_2)} - 58$		ns
$t_{h(\phi_1-RSMP)}$	$\overline{RSMP}$ hold time		0		ns
$t_{d(WE-\phi_1)}$ $t_{d(RDE-\phi_1)}$	ϕ_1 output delay time		0	30	ns

Notes 1. This applies when the main clock division selection bit = "0".

    2. f(f₂) represents the clock f₂ frequency.

       For the relation to the main clock and sub clock, refer to Table 10 in data sheet "M37735MHBXXXFP".

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TIMING DIAGRAM

X_{IN}

$\overline{E}$

Port P0 output — $t_{d(E-P0Q)}$

Port P0 input — $t_{su(P0D-E)}$ $t_{h(E-P0D)}$

Port P1 output — $t_{d(E-P1Q)}$

Port P1 input — $t_{su(P1D-E)}$ $t_{h(E-P1D)}$

Port P2 output — $t_{d(E-P2Q)}$

Port P2 input — $t_{su(P2D-E)}$ $t_{h(E-P2D)}$

Port P3 output — $t_{d(E-P3Q)}$

Port P3 input — $t_{su(P3D-E)}$ $t_{h(E-P3D)}$

Port P4 output — $t_{d(E-P4Q)}$

Port P4 input — $t_{su(P4D-E)}$ $t_{h(E-P4D)}$

Port P5 output — $t_{d(E-P5Q)}$

Port P5 input — $t_{su(P5D-E)}$ $t_{h(E-P5D)}$

Port P6 output — $t_{d(E-P6Q)}$

Port P6 input — $t_{su(P6D-E)}$ $t_{h(E-P6D)}$

Port P7 output — $t_{d(E-P7Q)}$

Port P7 input — $t_{su(P7D-E)}$ $t_{h(E-P7D)}$

Port P8 output — $t_{d(E-P8Q)}$

Port P8 input — $t_{su(P8D-E)}$ $t_{h(E-P8D)}$

t_r t_f t_c $t_{w(H)}$ $t_{w(L)}$

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$\overline{AD_{TRG}}$ input

$t_{c(AD)}$

$t_{w(ADL)}$

CLK_i

$t_{c(CK)}$

$t_{w(CKH)}$

$t_{w(CKL)}$

$t_{h(C-Q)}$

TxD_i

$t_{d(C-Q)}$

$t_{su(D-C)}$

$t_{h(C-D)}$

RxD_i

$\overline{INT_i}$ input

$\overline{Kl_i}$ input

$t_{w(INL)}$

$t_{w(INH)}$

$t_{w(KNL)}$
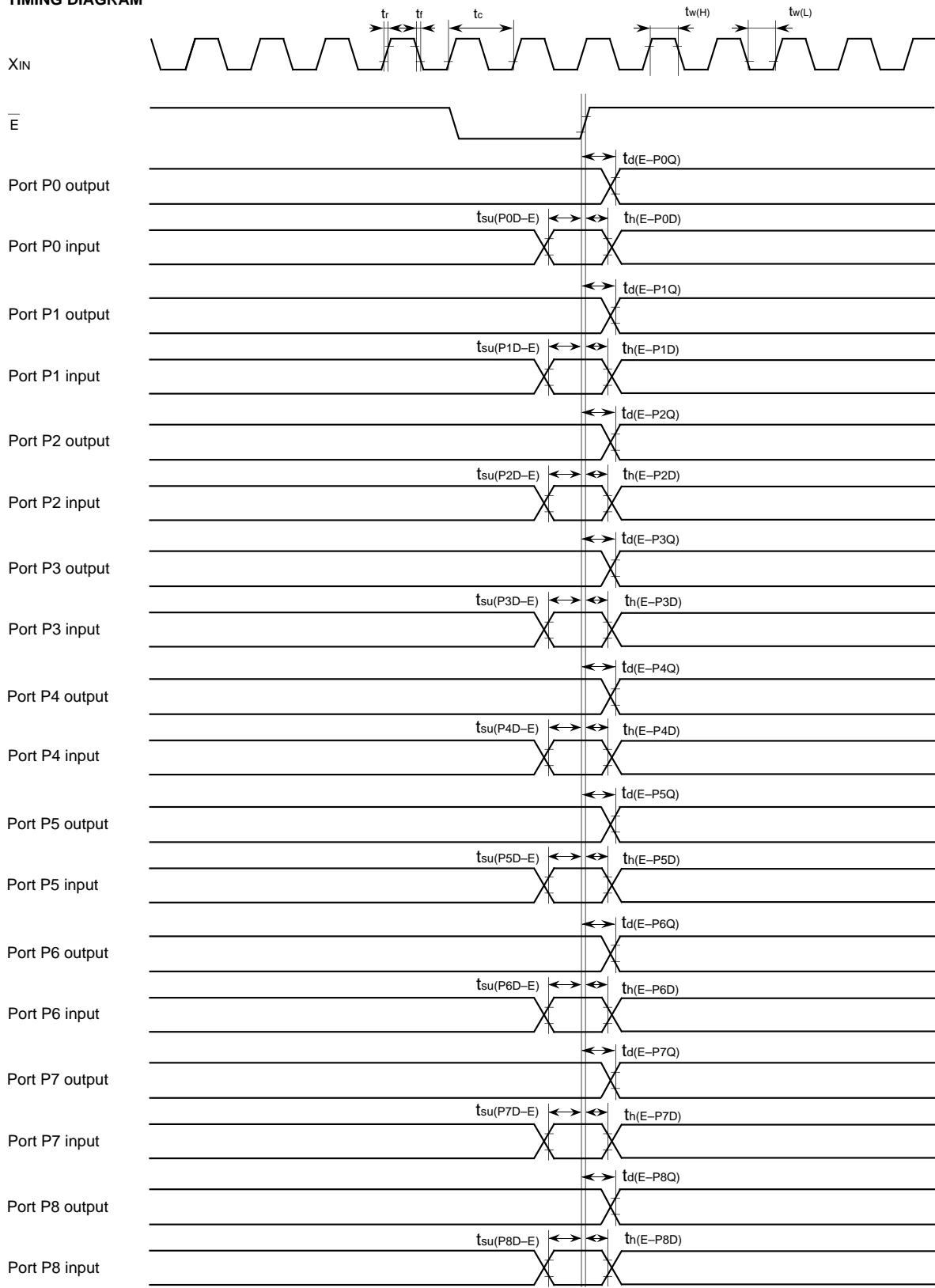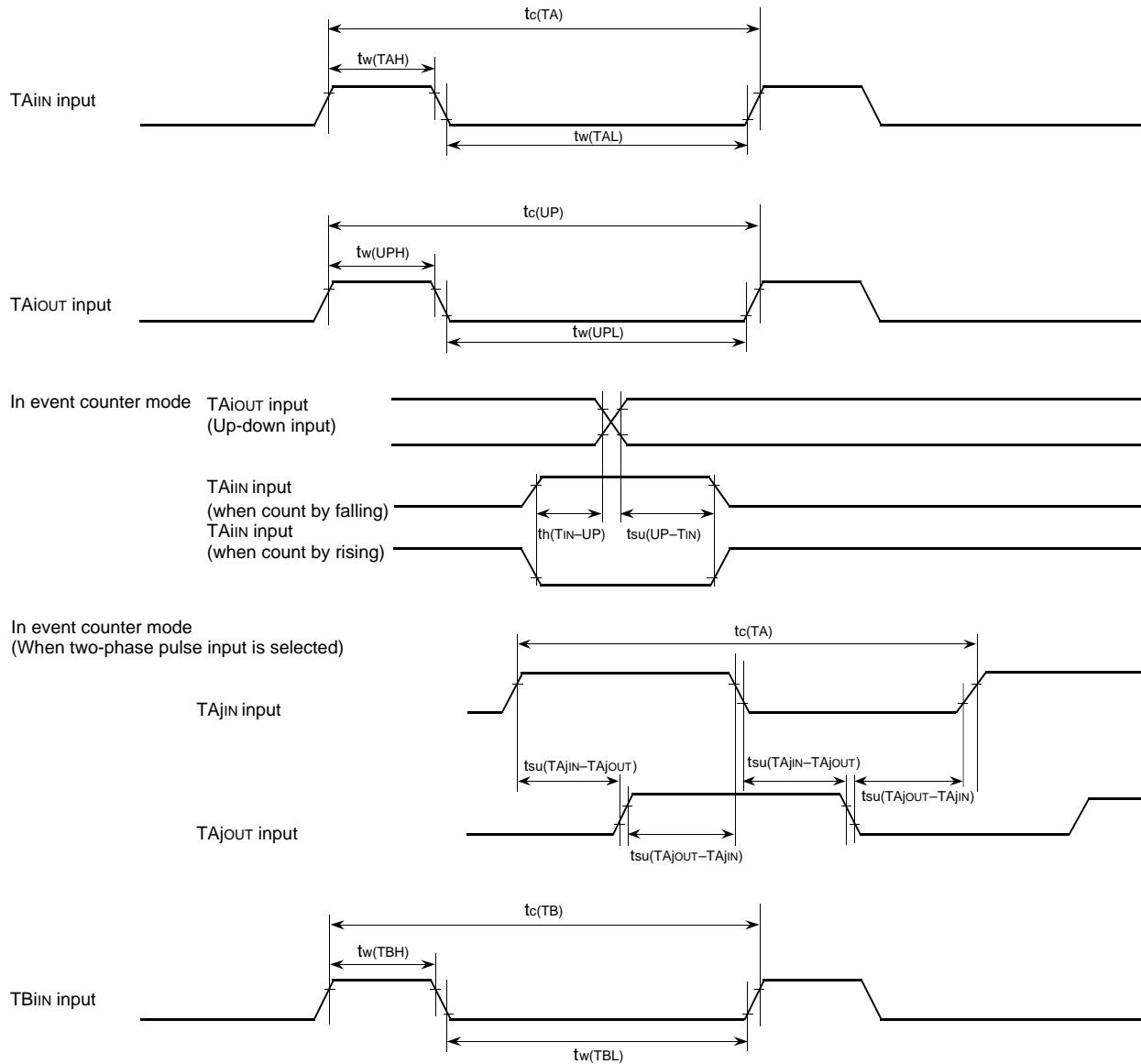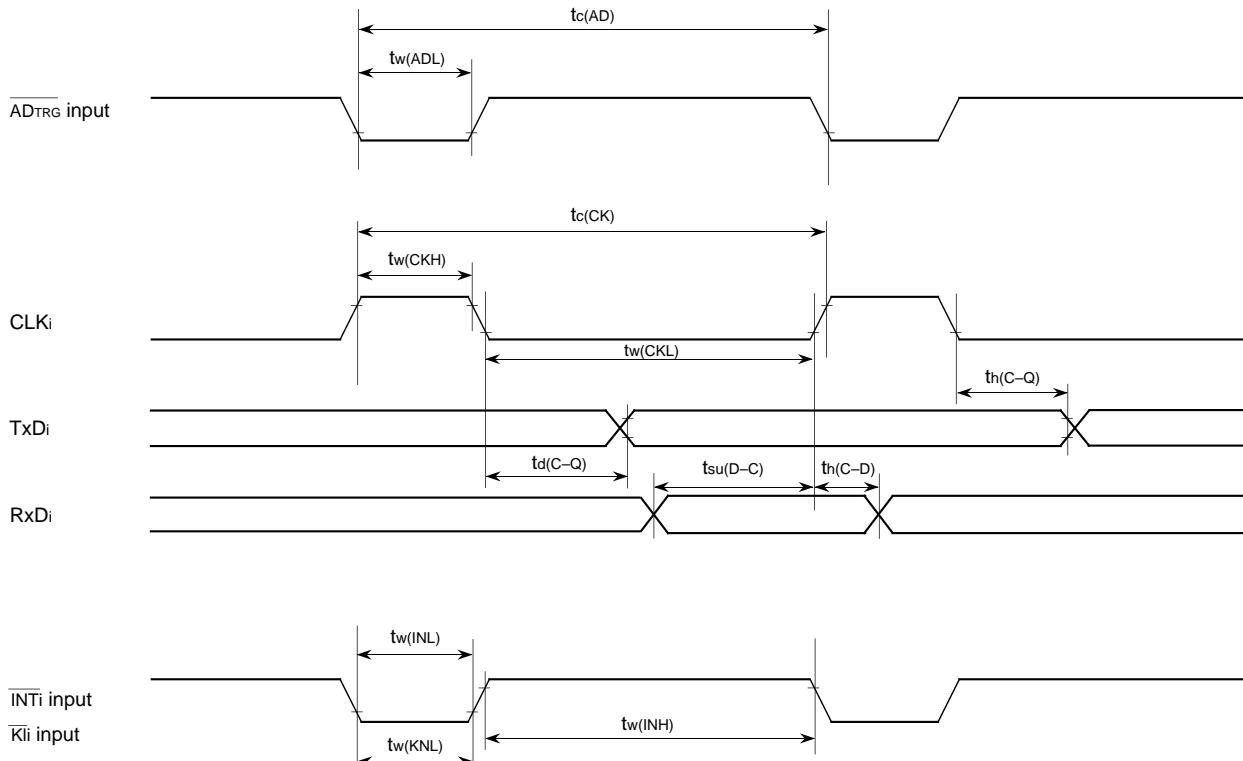
Memory expansion mode and microprocessor mode
(When wait bit = "1")

ϕ_1

$\overline{\text{WEL}}$
$\overline{\text{WEH}}$
$\overline{\text{RDE}}$

$\overline{\text{RDY}}$ input

$t_{su(RDY-\phi1)}$ $t_{h(\phi1-RDY)}$

(When wait bit = "0")

ϕ_1

$\overline{\text{WEL}}$
$\overline{\text{WEH}}$
$\overline{\text{RDE}}$

$\overline{\text{RDY}}$ input

$t_{su(RDY-\phi1)}$ $t_{h(\phi1-RDY)}$
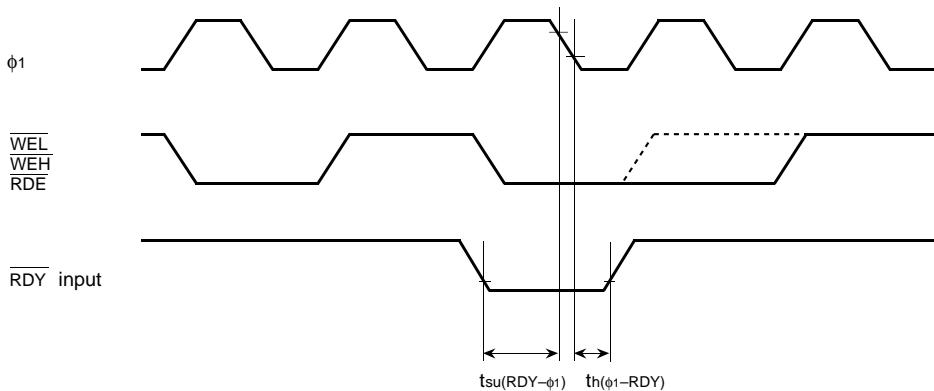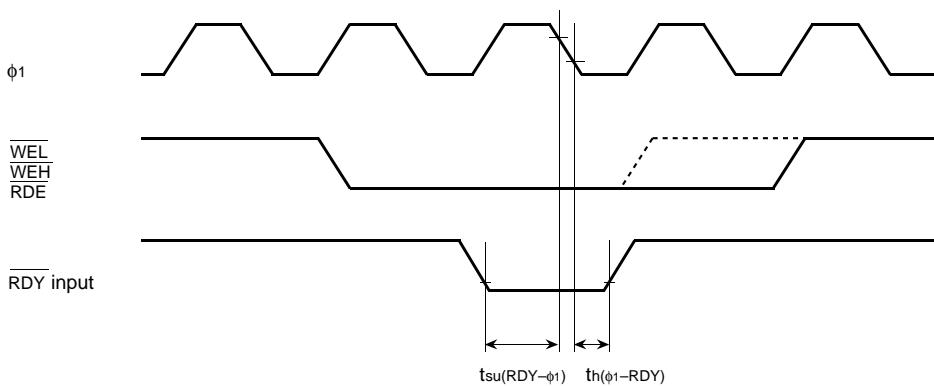
(When wait bit = "1" or "0" in common)

ϕ_1

$t_{su(HOLD-\phi1)}$ $t_{h(\phi1-HOLD)}$

$\overline{\text{HOLD}}$ input

$t_{d(\phi1-HLDA)}$ $t_{d(\phi1-HLDA)}$

$\overline{\text{HLDA}}$ output
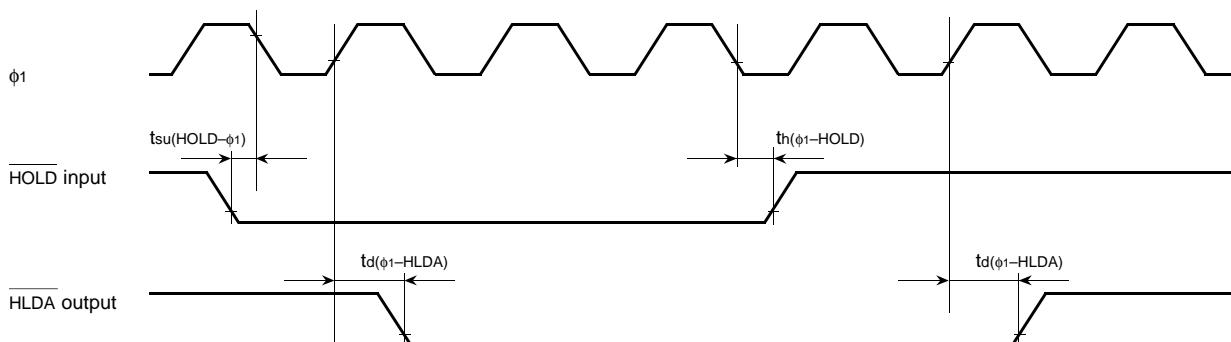
Test conditions
• V_{CC} = 2.7 – 5.5 V
• Input timing voltage : V_{IL} = 0.2V_{CC}, V_{IH} = 0.8V_{CC}
• Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V

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Memory expansion mode and microprocessor mode
(No wait : When wait bit = "1")
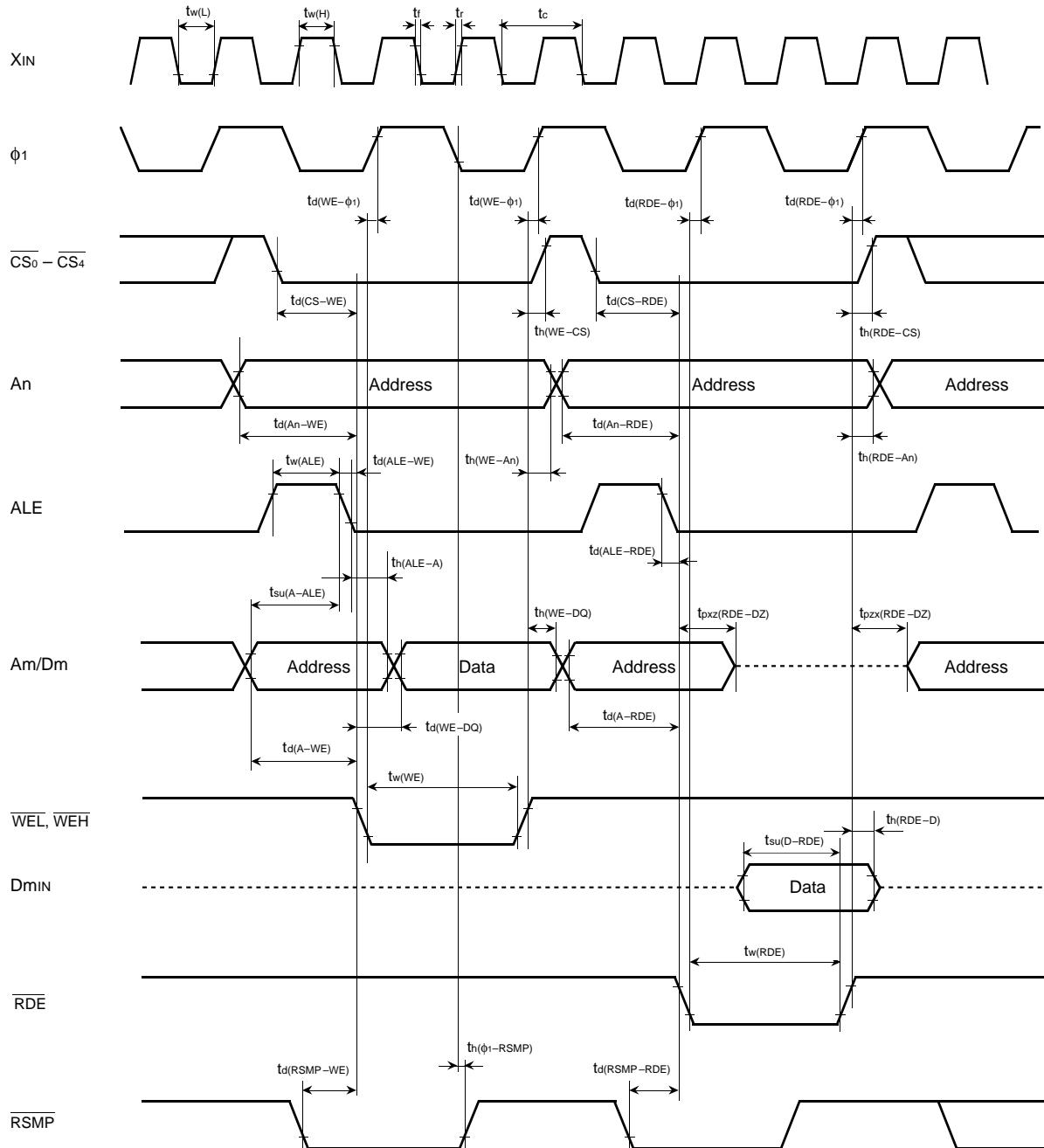
$t_{w(L)}$ $t_{w(H)}$ t_f t_r t_c

X_{IN}

ϕ_1

$t_{d(WE-\phi_1)}$ $t_{d(WE-\phi_1)}$ $t_{d(RDE-\phi_1)}$ $t_{d(RDE-\phi_1)}$

$\overline{CS_0} - \overline{CS_4}$

$t_{d(CS-WE)}$ $t_{d(CS-RDE)}$

$t_{h(WE-CS)}$ $t_{h(RDE-CS)}$

An | Address | Address | Address

$t_{d(An-WE)}$ $t_{d(An-RDE)}$

$t_{w(ALE)}$ $t_{d(ALE-WE)}$ $t_{h(WE-An)}$ $t_{h(RDE-An)}$

ALE

$t_{h(ALE-A)}$ $t_{d(ALE-RDE)}$

$t_{su(A-ALE)}$ $t_{h(WE-DQ)}$ $t_{pxz(RDE-DZ)}$ $t_{pzx(RDE-DZ)}$

Am/Dm | Address | Data | Address | Address

$t_{d(WE-DQ)}$ $t_{d(A-RDE)}$

$t_{d(A-WE)}$ $t_{w(WE)}$

$\overline{WEL}, \overline{WEH}$

$t_{h(RDE-D)}$ $t_{su(D-RDE)}$

Dm_{IN} | Data

$t_{w(RDE)}$

$\overline{RDE}$

$t_{d(RSMP-WE)}$ $t_{h(\phi_1-RSMP)}$ $t_{d(RSMP-RDE)}$

$\overline{RSMP}$

Test conditions
- Vcc = 2.7 – 5.5 V
- Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
- Data input Dm_{IN} : V_{IL} = 0.16 Vcc, V_{IH} = 0.5 Vcc

MITSUBISHI ELECTRIC

Memory expansion mode and microprocessor mode
(Wait 1 : The external memory area is accessed when wait bit = "0" and wait selection bit = "1".)
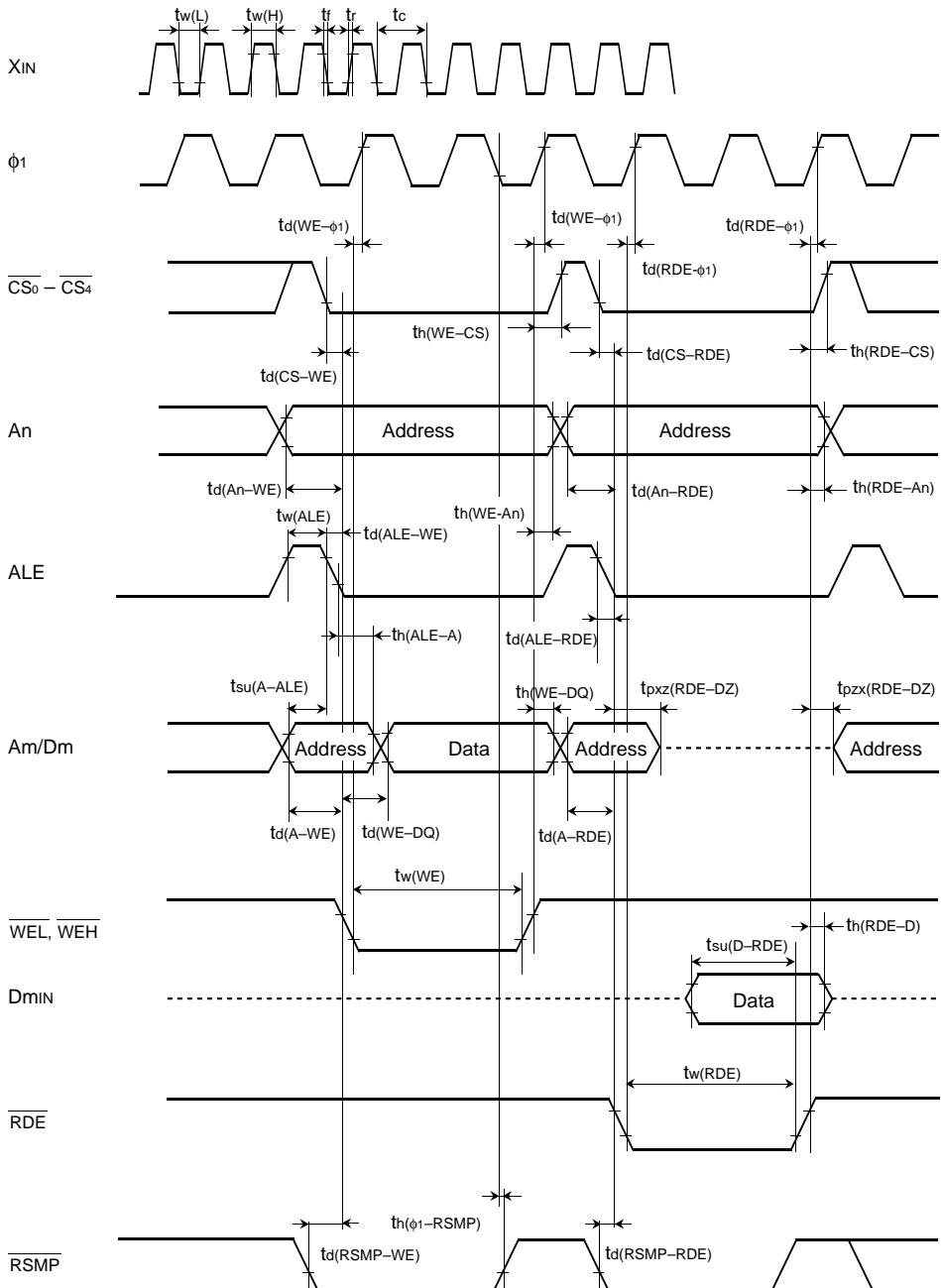
Test conditions
• Vcc = 2.7 – 5.5 V
• Output timing voltage : V_{OL} = 0.8 V, V_{OH} = 2.0 V
• Data input Dm_{IN} : V_{IL} = 0.16 V_{CC}, V_{IH} = 0.5 V_{CC}

MITSUBISHI ELECTRIC

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

Memory expansion mode and microprocessor mode
(Wait 0 : The external memory are is accessed when wait bit = "0" and wait selection bit = "0".)
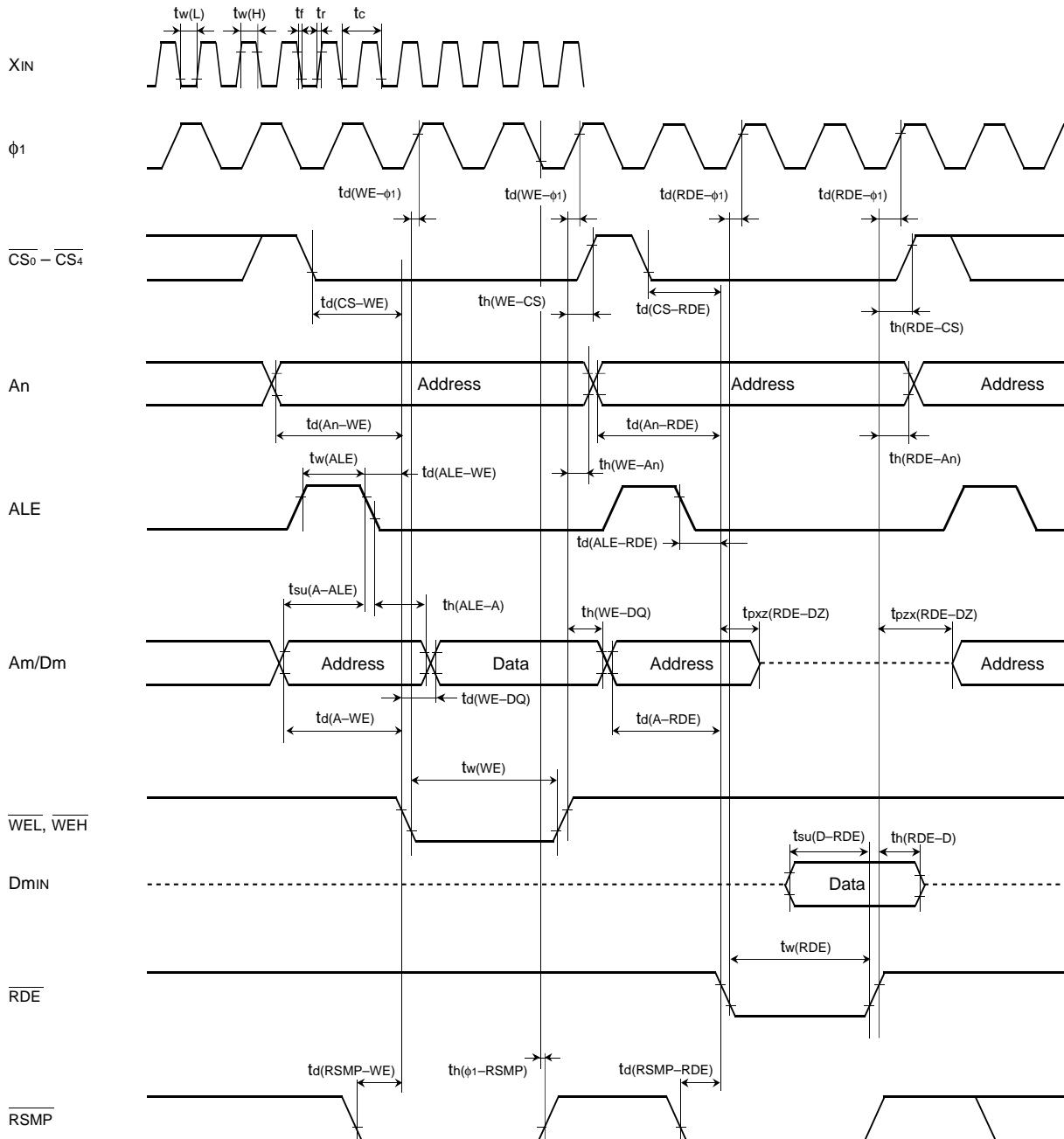
X_{IN} — $t_{w(L)}$ $t_{w(H)}$ t_f t_r t_c

ϕ_1

$\overline{CS_0} - \overline{CS_4}$ — $t_{d(WE-\phi_1)}$ $t_{d(WE-\phi_1)}$ $t_{d(RDE-\phi_1)}$ $t_{d(RDE-\phi_1)}$ $t_{d(CS-WE)}$ $t_{h(WE-CS)}$ $t_{d(CS-RDE)}$ $t_{h(RDE-CS)}$

An — Address Address Address $t_{d(An-WE)}$ $t_{d(An-RDE)}$ $t_{h(RDE-An)}$

ALE — $t_{w(ALE)}$ $t_{d(ALE-WE)}$ $t_{h(WE-An)}$ $t_{d(ALE-RDE)}$

Am/Dm — $t_{su(A-ALE)}$ $t_{h(ALE-A)}$ $t_{h(WE-DQ)}$ $t_{pxz(RDE-DZ)}$ $t_{pzx(RDE-DZ)}$ Address Data Address Address $t_{d(WE-DQ)}$ $t_{d(A-WE)}$ $t_{d(A-RDE)}$

$\overline{WEL}, \overline{WEH}$ — $t_{w(WE)}$

Dm_{IN} — $t_{su(D-RDE)}$ $t_{h(RDE-D)}$ Data

$\overline{RDE}$ — $t_{w(RDE)}$

$\overline{RSMP}$ — $t_{d(RSMP-WE)}$ $t_{h(\phi_1-RSMP)}$ $t_{d(RSMP-RDE)}$

Test conditions
• $V_{CC} = 2.7 - 5.5$ V
• Output timing voltage : $V_{OL} = 0.8$ V, $V_{OH} = 2.0$ V
• Data input Dm_{IN} : $V_{IL} = 0.16$ V_{CC}, $V_{IH} = 0.5$ V_{CC}

MITSUBISHI ELECTRIC

PACKAGE OUTLINE

80P6D−A

Plastic 80pin 12×12mm body LQFP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP80-P-1212-0.50	—	0.44	Alloy 42

Scale : 2.5/1
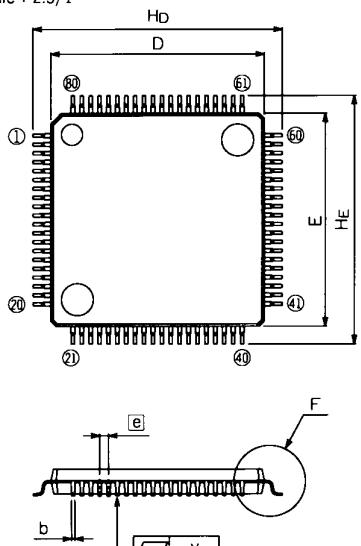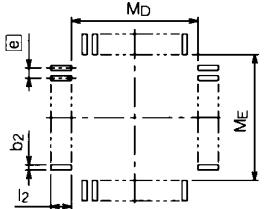
Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.7
A_1	0	0.1	0.2
A_2	—	1.4	—
b	0.13	0.18	0.28
c	0.105	0.125	0.175
D	11.9	12.0	12.1
E	11.9	12.0	12.1
e	—	0.5	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
L	0.3	0.5	0.7
L_1	—	1.0	—
y	—	—	0.1
θ	0°	—	10°
b_2	—	0.225	—
l_2	1.0	—	—
M_D	—	12.4	—
M_E	—	12.4	—
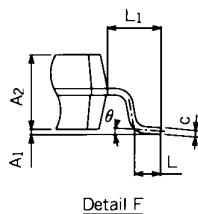
Detail F

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PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

GZZ–SH00–41B<68A0>

ROM number	

7700 FAMILY WRITING TO PROM ORDER CONFIRMATION FORM
SINGLE-CHIP 16-BIT MICROCOMPUTER
M37735EHLXXXHP
MITSUBISHI ELECTRIC

Receipt	Date:	
	Section head signature	Supervisor signature

Note : Please fill in all items marked ※

※	Customer	Company name	TEL ( )	Issuance signatures	Responsible officer	Supervisor
		Date issued	Date:			

※1. Confirmation

Specify the name of the product being ordered and the type of EPROMs submitted.

Three sets of EPROMs are required for each pattern.

If at least two of the three sets of EPROMs submitted contain the identical data, we will produce writing to PROM based on this data. We shall assume the responsibility for errors only if the written PROM data on the products we produce differ from this data. Thus, the customer must be especially careful in verifying the data contained in the EPROMs submitted.

Checksum code for entire EPROM areas [ ][ ][ ][ ] (hexadecimal notation)

EPROM Type :

27C201

```
          00000
///////    00010
          20000
DATA           ┐
          128K │
          3FFFF ┘
```
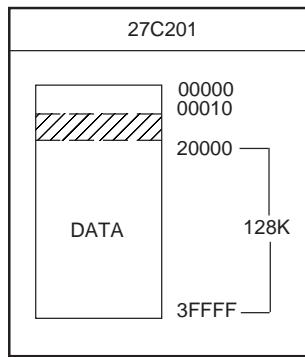
(1) Set "FF$_{16}$" in the shaded area.

(2) Address 0_{16} to $0F_{16}$ are the area for storing the data on model designation.This area must be written with the data shown below.

Address and data are written in hexadecimal notation.

Address			Address	
4D	0		4C	8
33	1		FF	9
37	2		FF	A
37	3		FF	B
33	4		FF	C
35	5		FF	D
45	6		FF	E
48	7		FF	F

※2. Mark specification

Mark specification must be submitted using the correct form for the type of package being ordered fill out the appropriate 80P6D Mark Specification Form (for M37735EHLXXXHP) and attach to the Writing to PROM Order Confirmation Form.

※3. Comments

80P6S (80-PIN QFP) MARK SPECIFICATION FORM
80P6D (80-PIN Fine-pitch QFP)

Mitsubishi IC catalog name [   ]

Please choose one of the marking types below (A, B, C), and enter the Mitsubishi IC catalog name and the special mark (if needed).

A. Standard Mitsubishi Mark

Mitsubishi IC catalog name

Mitsubishi IC catalog name

Mitsubishi product number
(6-digit, or 7-digit)
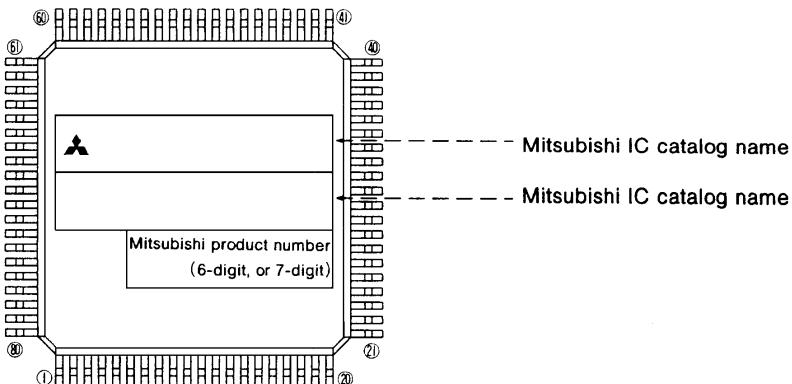
B. Customer's Parts Number + Mitsubishi IC Catalog Name

Customer's Parts Number
Note : The fonts and size of characters are standard Mitsubishi type.
Mitsubishi IC catalog name

Notes1 : The mark field should be written right aligned.
2 : The fonts and size of characters are standard Mitsubishi type.
3 : Customer's parts number can be up to 10 alphanumeric characters for capital letters, hyphens, commas, periods and so on.
4 : If the Mitsubishi logo ⟁ is not required, check the box below.

⟁Mitsubishi logo is not required

[ ]

5 : The allocation of Mitsubishi IC catalog name and Mitsubishi product number is different on the package owing to the number of Mitsubishi IC catalog name's characters, and the requiring Mitsubishi logo ⟁ or not.

C. Special Mark Required
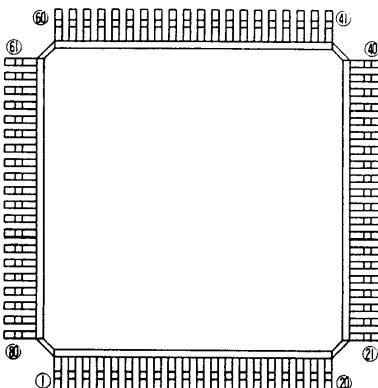
Notes1 : If special mark is to be printed, indicate the desired layout of the mark in the left figure. The layout will be duplicated technically as close as possible. Mitsubishi product number (6-digit, or 7-digit) and Mask ROM number (3-digit) are always marked for sorting the products.
2 : If special character fonts (e.g., customer's trade mark logo) must be used in Special Mark, check the box below.
For the new special character fonts a clean font original (ideally logo drawing) must be submitted.

Special character fonts required

[ ]

MITSUBISHI ELECTRIC

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Rev. No.	Revision Description	Rev. date
1.00	First Edition	970604
1.01	The following are added: • PROM ORDER CONFIRMATION FORM • MARK SPECIFICATION FORM	980421
2.00	The following are revised:	980731

Page	Previous Version	Revised Version
P1 PIN CON-FIGURATION (TOP VIEW) P9 Fig. 5	Outline 80P6D-A	Outline 80P6D-A, 80P6Q-A
P9 Left column Line 4	Table 2 list...	Table 2 lists...
P12 Right column Line 2	The M37735EHLXXXHP has 28 powerful addressing modes. Refer to the MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS for the details of each addressing mode. **MACHINE INSTRUCTION LIST** The M37735EHLXXXHP has 103 machine instructions. Refer to the MITSUBISHI SEMICONDUCTORS DATA BOOK SINGLE-CHIP 16-BIT MICROCOMPUTERS for details.	The M37735EHLXXXHP has 28 powerful addressing modes. Refer to the "7700 Family Software Manual" for the details. **MACHINE INSTRUCTION LIST** The M37735EHLXXXHP has 103 machine instructions. Refer to the "7700 Family Software Manual" for the details.
Line 10	(2) 80P6D mark specification form	(2) 80P6D, 80P6Q mark specification form

P16
Memory expansion mode and microprocessor mode

Previous Version

Symbol	Parameter	Limits Min.	Limits Max.	Unit
$t_{su(D-E)}$	Data input setup time	80		ns

Revised Version

Symbol	Parameter	Limits Min.	Limits Max.	Unit
$t_{su(D-E)}$	Data input setup time	50		ns